

## ASM330LHH: automotive inertial module digital 3-axis accelerometer and digital 3-axis gyroscope

### Introduction

This document provides usage information and application hints related to ST's [ASM330LHH](#) automotive inertial module.

The ASM330LHH is a 3-axis digital accelerometer and 3-axis digital gyroscope system-in-package with a digital I<sup>2</sup>C/SPI serial interface standard output, performing at 1.3 mA in combo high-performance mode. The accelerometer features smart sleep-to-wake-up (activity) and return-to-sleep (inactivity) functions that allow advanced power saving.

The device has a dynamic user-selectable full-scale acceleration range of  $\pm 2/\pm 4/\pm 8/\pm 16\text{ g}$  and an angular rate range of  $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000/\pm 4000\text{ dps}$ .

The ASM330LHH can be configured to generate interrupt signals by using hardware recognition of free-fall events, 6D orientation, activity or inactivity, and wake-up events.

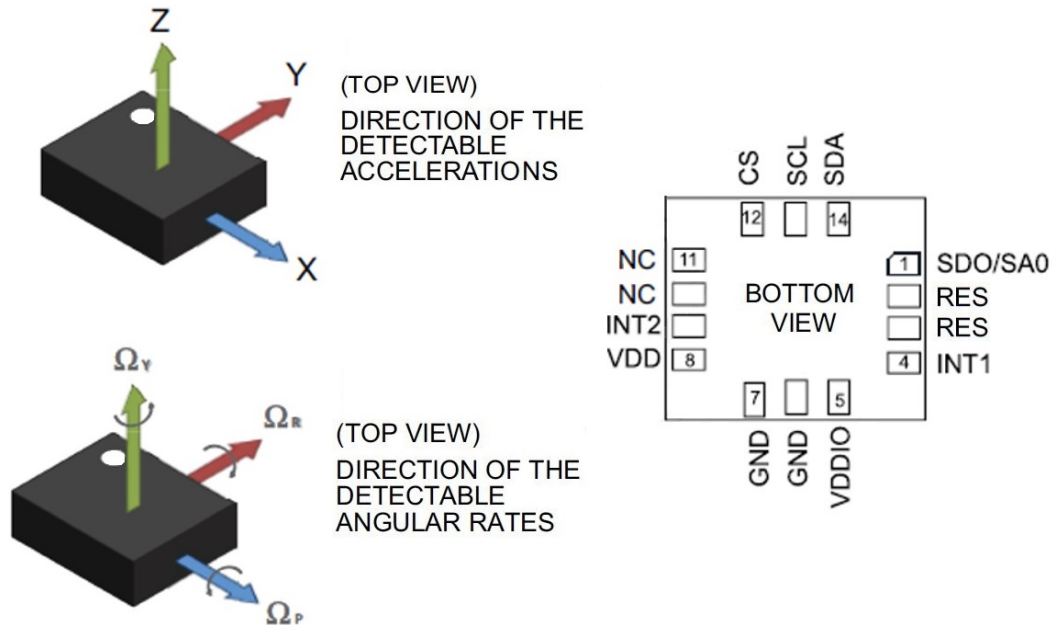
The ASM330LHH has an integrated smart first-in first-out (FIFO) buffer of up to 3 KB size, allowing dynamic batching of gyroscope data, accelerometer data, temperature data, and timestamp.

The ASM330LHH is available in a small plastic land grid array package (LGA-14L) and it is guaranteed to operate over an extended temperature range from  $-40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ .

All the design aspects of the ASM330LHH have been optimized to reach superior output stability, extremely low noise, and full data synchronization to the benefit of sensor-assisted applications like dead reckoning and sensor fusion.

## 1 Pin description

**Figure 1. Pin connections**



**Table 1. Internal pin status**

Pin #	Name	Function	Pin status
1	SDO	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up
	SA0	I <sup>2</sup> C least significant bit of the device address (SA0)	Pull-up is enabled if bit SDO_PU_EN = 1 in reg. 02h.
2	RES	Connect to VDDIO or GND	Default: input without pull-up
3	RES	Connect to VDDIO or GND	Default: input without pull-up
4	INT1 <sup>(1)</sup>	Programmable interrupt 1	Default: input with pull-down
5	VDDIO	Power supply for I/O pins	
6	GND	0 V supply	
7	GND	0 V supply	
8	VDD	Power supply	
9	INT2 <sup>(2)</sup>	Programmable interrupt 2 (INT2) / Data enabled (DEN)	Default: output forced to ground
10	NC	Leave unconnected	Default: input with pull-up
11	NC	Leave unconnected	Default: input with pull-up
12	CS	I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)	Default: input with pull-up Pull-up is disabled if bit I2C_disable = 1 in reg 13h and DEVICE_CONF = 1 in reg 18h.
13	SCL	I <sup>2</sup> C serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up
14	SDA	I <sup>2</sup> C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up

1. INT1 must be set to 0 or left unconnected during power-on. If no interrupt signal is needed on INT1, this pin can be left unconnected.

2. If no interrupt signal is needed on INT2, this pin can be left unconnected.

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on VDDIO.

*Note:*

*The procedure to correctly initialize the device is as follows:*

- 1. INT1 pin: leave unconnected or connect with external pull-down during power-on. Pull-up must be avoided on this pin.*
- 2. INT2 pin: recommended to not connect with external pull-up.*
- 3. Properly configure the device:*
  - a) SPI case: I2C\_disable = 1 in CTRL4\_C (13h) and DEVICE\_CONF = 1 in CTRL9\_XL (18h).*
  - b) I<sup>2</sup>C case: I2C\_disable = 0 (default) in CTRL4\_C (13h) and DEVICE\_CONF = 1 in CTRL9\_XL (18h).*

## 2

## Registers

Table 2. Registers

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIN_CTRL	02h	0	SDO_PU_EN	1	1	1	1	1	1
FIFO_CTRL1	07h	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0
FIFO_CTRL2	08h	STOP_ON_WTM	0	0	ODRCHG_EN	0	0	0	WTM8
FIFO_CTRL3	09h	BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0
FIFO_CTRL4	0Ah	DEC_TS_BATCH_1	DEC_TS_BATCH_0	ODR_T_BATCH_1	ODR_T_BATCH_0	0	FIFO_MODE2	FIFO_MODE1	FIFO_MODE0
COUNTER_BDR_REG1	0Bh	dataready_pulsed	RST_COUNTER_BDR	TRIG_COUNTER_BDR	0	0	0	CNT_BDR_TH_9	CNT_BDR_TH_8
COUNTER_BDR_REG2	0Ch	CNT_BDR_TH_7	CNT_BDR_TH_6	CNT_BDR_TH_5	CNT_BDR_TH_4	CNT_BDR_TH_3	CNT_BDR_TH_2	CNT_BDR_TH_1	CNT_BDR_TH_0
INT1_CTRL	0Dh	DEN_DRDY_flag	INT1_CNT_BDR	INT1_FIFO_FULL	INT1_FIFO_OVR	INT1_FIFO_TH	INT1_BOOT	INT1_DRDY_G	INT1_DRDY_XL
INT2_CTRL	0Eh	0	INT2_CNT_BDR	INT2_FIFO_FULL	INT2_FIFO_OVR	INT2_FIFO_TH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL
WHO_AM_I	0Fh	0	1	1	0	1	0	1	1
CTRL1_XL	10h	ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	LPF2_XL_EN	0
CTRL2_G	11h	ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS1_G	FS0_G	FS_125	FS_4000
CTRL3_C	12h	BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0	SW_RESET
CTRL4_C	13h	0	SLEEP_G	INT2_on_INT1	0	DRDY_MASK	I2C_disable	LPF1_SEL_G	0
CTRL5_C	14h	0	ROUNDING1	ROUNDING0	0	ST1_G	ST0_G	ST1_XL	ST0_XL
CTRL6_C	15h	TRIG_EN	LVL1_EN	LVL2_EN	0	USR_OFF_W	FTYPE_2	FTYPE_1	FTYPE_0
CTRL7_G	16h	0	HP_G_EN	HPM1_G	HPM0_G	0	0	USR_OFF_ON_OUT	0
CTRL8_XL	17h	HPCF_XL2	HPCF_XL1	HPCF_XL0	HP_REF_MODE_XL	FASTSETTL_MODE_XL	HP_SLOPE_XL_EN	0	LOW_PASS_ON_6D
CTRL9_XL	18h	DEN_X	DEN_Y	DEN_Z	DEN_XL_G	DEN_XL_EN	DEN_LH	DEVICE_CONF	0
CTRL10_C	19h	0	0	TIMESTAMP_EN	0	0	0	0	0
ALL_INT_SRC	1Ah	TIMESTAMP_ENDCOUNT	0	SLEEP_CHANGE_IA	D6D_IA	0	0	WU_IA	FF_IA
WAKE_UP_SRC	1Bh	0	SLEEP_CHANGE_IA	FF_IA	SLEEP_STATE	WU_IA	X_WU	Y_WU	Z_WU
D6D_SRC	1Dh	DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	XH	XL
STATUS_REG	1Eh	0	0	0	0	0	TDA	GDA	XLDA
OUT_TEMP_L	20h	Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
OUT_TEMP_H	21h	Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8
OUTX_L_G	22h	D7	D6	D5	D4	D3	D2	D1	D0
OUTX_H_G	23h	D15	D14	D13	D12	D11	D10	D9	D8
OUTY_L_G	24h	D7	D6	D5	D4	D3	D2	D1	D0



Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUTY_H_G	25h	D15	D14	D13	D12	D11	D10	D9	D8
OUTZ_L_G	26h	D7	D6	D5	D4	D3	D2	D1	D0
OUTZ_H_G	27h	D15	D14	D13	D12	D11	D10	D9	D8
OUTX_L_A	28h	D7	D6	D5	D4	D3	D2	D1	D0
OUTX_H_A	29h	D15	D14	D13	D12	D11	D10	D9	D8
OUTY_L_A	2Ah	D7	D6	D5	D4	D3	D2	D1	D0
OUTY_H_A	2Bh	D15	D14	D13	D12	D11	D10	D9	D8
OUTZ_L_A	2Ch	D7	D6	D5	D4	D3	D2	D1	D0
OUTZ_H_A	2Dh	D15	D14	D13	D12	D11	D10	D9	D8
FIFO_STATUS1	3Ah	DIFF_FIFO_7	DIFF_FIFO_6	DIFF_FIFO_5	DIFF_FIFO_4	DIFF_FIFO_3	DIFF_FIFO_2	DIFF_FIFO_1	DIFF_FIFO_0
FIFO_STATUS2	3Bh	FIFO_WTM_IA	FIFO_OVR_IA	FIFO_FULL_IA	COUNTER_BDR_IA	FIFO_OVR_LATCHED	0	DIFF_FIFO_9	DIFF_FIFO_8
TIMESTAMP0	40h	D7	D6	D5	D4	D3	D2	D1	D0
TIMESTAMP1	41h	D15	D14	D13	D12	D11	D10	D9	D8
TIMESTAMP2	42h	D23	D22	D21	D20	D19	D18	D17	D16
TIMESTAMP3	43h	D31	D30	D29	D28	D27	D26	D25	D24
INT_CFG0	56h	0	INT_CLR_ON_READ	SLEEP_STATUS_ON_INT	SLOPE_FDS	0	0	0	LIR
INT_CFG1	58h	INTERRUPTS_ENABLE	INACT_EN1	INACT_EN0	0	0	0	0	0
THS_6D	59h	D4D_EN	SIXD_THS1	SIXD_THS0	0	0	0	0	0
WAKE_UP_THS	5Bh	0	USR_OFF_ON_WU	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0
WAKE_UP_DUR	5Ch	FF_DUR5	WAKE_DUR1	WAKE_DUR0	WAKE_THS_W	SLEEP_DUR3	SLEEP_DUR2	SLEEP_DUR1	SLEEP_DUR0
FREE_FALL	5Dh	FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0
MD1_CFG	5Eh	INT1_SLEEP_CHANGE	0	INT1_WU	INT1_FF	0	INT1_6D	0	0
MD2_CFG	5Fh	INT2_SLEEP_CHANGE	0	INT2_WU	INT2_FF	0	INT2_6D	0	INT2_TIMESTAMP
INTERNAL_FREQ_FINE	63h	FREQ_FINE7	FREQ_FINE6	FREQ_FINE5	FREQ_FINE4	FREQ_FINE3	FREQ_FINE2	FREQ_FINE1	FREQ_FINE0
X_OFS_USR	73h	X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0
Y_OFS_USR	74h	Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0
Z_OFS_USR	75h	Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0
FIFO_DATA_OUT_TAG	78h	TAG_SENSOR_4	TAG_SENSOR_3	TAG_SENSOR_2	TAG_SENSOR_1	TAG_SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_PARITY
FIFO_DATA_OUT_X_L	79h	D7	D6	D5	D4	D3	D2	D1	D0
FIFO_DATA_OUT_X_H	7Ah	D15	D14	D13	D12	D11	D10	D9	D8
FIFO_DATA_OUT_Y_L	7Bh	D7	D6	D5	D4	D3	D2	D1	D0
FIFO_DATA_OUT_Y_H	7Ch	D15	D14	D13	D12	D11	D10	D9	D8



Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FIFO_DATA_OUT_Z_L	7Dh	D7	D6	D5	D4	D3	D2	D1	D0
FIFO_DATA_OUT_Z_H	7Eh	D15	D14	D13	D12	D11	D10	D9	D8

### 3 Operating modes

The ASM330LHH provides three possible operating configurations:

- Only accelerometer active and gyroscope in power-down or sleep mode
- Only gyroscope active and accelerometer in power-down
- Both accelerometer and gyroscope active with independent ODR

The device offers a wide VDD voltage range from 2.0 V to 3.6 V and a VDDIO range from 1.62 V to 3.6 V. The power-on sequence is not restricted: VDD/VDDIO pins can be either set to power supply level or to ground level (they must not be left floating) and no specific sequence is required for powering them on.

In order to avoid potential conflicts, during the power-on sequence it is recommended to set the lines (on the host side) connected to the device IO pins floating or connected to ground, until VDDIO is set. After VDDIO is set, the lines connected to the IO pins have to be configured according to their default status described in [Table 1. Internal pin status](#). In order to avoid an unexpected increase in current consumption, the input pins that are not pulled-up/pulled-down must be polarized by the host.

When the VDD power supply is applied, the device performs a 10 ms (maximum) boot procedure to load the trimming parameters. After the boot is completed, both the accelerometer and the gyroscope are automatically configured in power-down mode. To guarantee proper power-off of the device, it is recommended to maintain the duration of the VDD line to GND for at least 100  $\mu$ s.

The accelerometer and the gyroscope can be configured independently in power-down mode or high-performance mode. They are allowed to have different data rates without any limit. The gyroscope sensor can also be set to sleep mode to reduce its power consumption.

When both the accelerometer and gyroscope are on, the accelerometer is synchronized with the gyroscope, and the data rates of the two sensors are integer multiples of each other.

Referring to the datasheet, the output data rate (ODR\_XL) bits of the CTRL1\_XL register are used to select the output data rate of the accelerometer ([Table 3. Accelerometer ODR selection](#)).

**Note:**

*If the accelerometer is to be activated while the gyroscope is already running (that is, the gyroscope is not in power-down mode), proceed as follows:*

1. Set bit 4 to 1 in the CTRL6\_C (15h) register.
2. Write the CTRL1\_XL (10h) register to 50h.
3. Read the OUTZ\_H\_A (2Dh) register to clear the XLDA bit in the STATUS\_REG (1Eh) register.
4. Wait 1/ODR\_XL time period or wait until the XLDA bit in the STATUS\_REG (1Eh) register becomes equal to 1.
5. Set bit 4 to 0 in the CTRL6\_C (15h) register.
6. Write the CTRL1\_XL (10h) register to the desired value.

**Table 3. Accelerometer ODR selection**

ODR_XL [3:0]	ODR [Hz]
0000	Power-down
0001	12.5 Hz (high-performance)
0010	26 Hz (high-performance)
0011	52 Hz (high-performance)
0100	104 Hz (high-performance)
0101	208 Hz (high-performance)
0110	416 Hz (high-performance)
0111	833 Hz (high-performance)
1000	1.66 kHz (high-performance)
1001	3.33 kHz (high-performance)
1010	6.66 kHz (high-performance)

The output data rate (ODR\_G) bits of the CTRL2\_G register are used to select the output data rate of the gyroscope sensor (Table 4. Gyroscope ODR selection).

**Table 4. Gyroscope ODR selection**

ODR_G [3:0]	ODR [Hz]
0000	Power-down
0001	12.5 Hz (high-performance)
0010	26 Hz (high-performance)
0011	52 Hz (high-performance)
0100	104 Hz (high-performance)
0101	208 Hz (high-performance)
0110	416 Hz (high-performance)
0111	833 Hz (high-performance)
1000	1.66 kHz (high-performance)
1001	3.33 kHz (high-performance)
1010	6.66 kHz (high-performance)

Table 5. Power consumption at Vdd = 3.0 V (typical) shows the typical values of power consumption for the different operating modes.

**Table 5. Power consumption at Vdd = 3.0 V (typical)**

ODR [Hz]	Accelerometer only	Gyroscope only	Combo [accelerometer + gyroscope]
Power-down	-	-	3 $\mu$ A
Sleep	-	430 $\mu$ A	-
12.5 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
26 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
52 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
104 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
208 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
416 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
833 Hz (high-performance)	360 $\mu$ A	970 $\mu$ A	1.3 mA
1.66 kHz (high-performance)	361 $\mu$ A	970 $\mu$ A	1.3 mA
3.33 kHz (high-performance)	362 $\mu$ A	970 $\mu$ A	1.3 mA
6.66 kHz (high-performance)	363 $\mu$ A	970 $\mu$ A	1.3 mA

### 3.1 Power-down mode

When the accelerometer/gyroscope is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. Digital interfaces (I<sup>2</sup>C/SPI) are still active to allow communication with the device. The content of the configuration registers is preserved and the output data registers are not updated, keeping the last data sampled in memory before going into power-down mode.

### 3.2 High-performance mode

In high-performance mode, all accelerometer/gyroscope circuitry is always on and data are generated at the data rate selected through the ODR\_XL/ODR\_G bits.

Data interrupt generation is active.



### 3.3 Gyroscope sleep mode

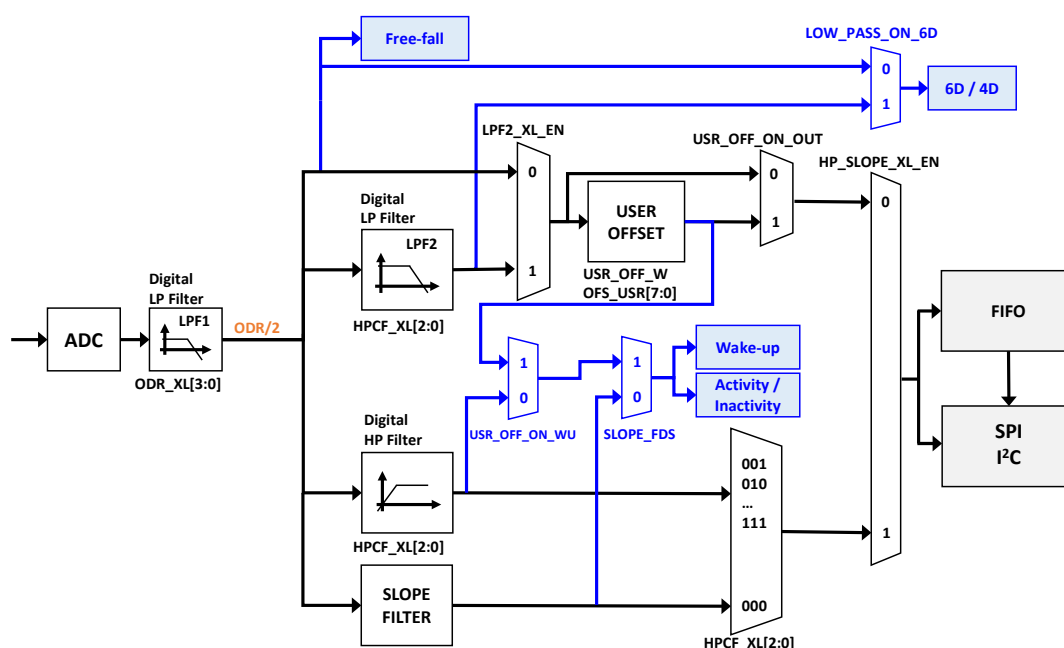
While the gyroscope is in sleep mode the circuitry that drives the oscillation of the gyroscope mass is kept active. Compared to gyroscope power-down, turn-on time from sleep mode to high-performance mode is drastically reduced.

If the gyroscope is not configured in power-down mode, it enters in sleep mode when the sleep mode enable (SLEEP\_G) bit of CTRL4\_C register is set to 1, regardless of the selected gyroscope ODR.

### 3.4 Accelerometer bandwidth

The accelerometer sampling chain is represented by a cascade of three main blocks: an ADC converter, a digital low-pass filter (LPF1), and the composite group of digital filters as shown in the following figure.

Figure 2. Accelerometer filtering chain



The signal converted by the ADC is filtered by a digital low-pass filter (LPF1) having a cutoff equal to  $ODR/2$ . Finally, the composite group of filters composed of a low-pass digital filter (LPF2), a high-pass digital filter, and a slope filter processes the digital signal.

The LPF2\_XL\_EN bit of the CTRL1\_XL register and the CTRL8\_XL register can be used to configure the composite filter group and the overall bandwidth of the accelerometer filtering chain, as shown in [Table 6. Accelerometer bandwidth selection](#). Referring to this table, on the low-pass path side, the bandwidth column refers to the LPF1 bandwidth if LPF2\_XL\_EN = 0. It refers to the LPF2 bandwidth if LPF2\_XL\_EN = 1. On the high-pass path side, the bandwidth column refers to the slope filter bandwidth if HPCF\_XL[2:0] = 000. It refers to the HP filter bandwidth for all the other configurations.

[Table 6. Accelerometer bandwidth selection](#) also provides the maximum (worst case) settling time in terms of samples to be discarded for the various configurations of the accelerometer filtering chain.

**Table 6. Accelerometer bandwidth selection**

HP_SLOPE_XL_EN	LPF2_XL_EN	HPCF_XL[2:0]	Bandwidth	Max overall settling time <sup>(1)</sup> (samples to be discarded)
0 (Low-pass path)	0	-	ODR / 2	See Table 8
	1	000	ODR / 4	See Table 8
		001	ODR / 10	10
		010	ODR / 20	19
		011	ODR / 45	38
		100	ODR / 100	75
		101	ODR / 200	150
		110	ODR / 400	296
		111	ODR / 800	595
1 (High-pass path)	-	000	ODR / 4 (slope filter)	See Table 8
		001	ODR / 10	14
		010	ODR / 20	19
		011	ODR / 45	38
		100	ODR / 100	75
		101	ODR / 200	150
		110	ODR / 400	296
		111	ODR / 800	595

1. Settling time @ 99% of the final value, taking into account all output data rates and all operating mode switches

Setting the HP\_SLOPE\_XL\_EN bit to 0, the low-pass path of the composite filter block is selected. If the LPF2\_XL\_EN bit is set to 0, no additional filter is applied. If the LPF2\_XL\_EN bit is set to 1, the LPF2 filter is applied in addition to LPF1, and the overall bandwidth of the accelerometer chain can be set by configuring the HPCF\_XL[2:0] field of the CTRL8\_XL register.

The LPF2 low-pass filter can also be used in the 6D/4D functionality by setting the LOW\_PASS\_ON\_6D bit of the CTRL8\_XL register to 1.

Setting the HP\_SLOPE\_XL\_EN bit to 1, the high-pass path of the composite filter block is selected. The HPCF\_XL[2:0] field is used in order to enable, in addition to the LPF1 filter, either the slope filter usage (when HPCF\_XL[2:0] = 000) or the digital high-pass filter (other HPCF\_XL[2:0] configurations). The HPCF\_XL[2:0] field is also used to select the cutoff frequencies of the HP filter.

The high-pass filter reference mode feature is available for the accelerometer sensor. When this feature is enabled, the current X, Y, Z accelerometer sample is internally stored and subtracted from all subsequent output values. In order to enable the reference mode, both the HP\_REF\_MODE\_XL bit and the HP\_SLOPE\_XL\_EN bit of the CTRL8\_XL register have to be set to 1, and the value of the HPCF\_XL[2:0] field has to be different than 000. When the reference mode feature is enabled, both the LPF2 filter and the HP filter are not available. The first accelerometer output data after enabling the reference mode has to be discarded.

The FASTSETTL\_MODE\_XL bit of the CTRL8\_XL register enables the accelerometer LPF2 or HPF fast-settling mode. The selected filter sets the second sample after writing this bit. This feature applies only upon device exit from power-down mode.

### 3.4.1 Accelerometer slope filter

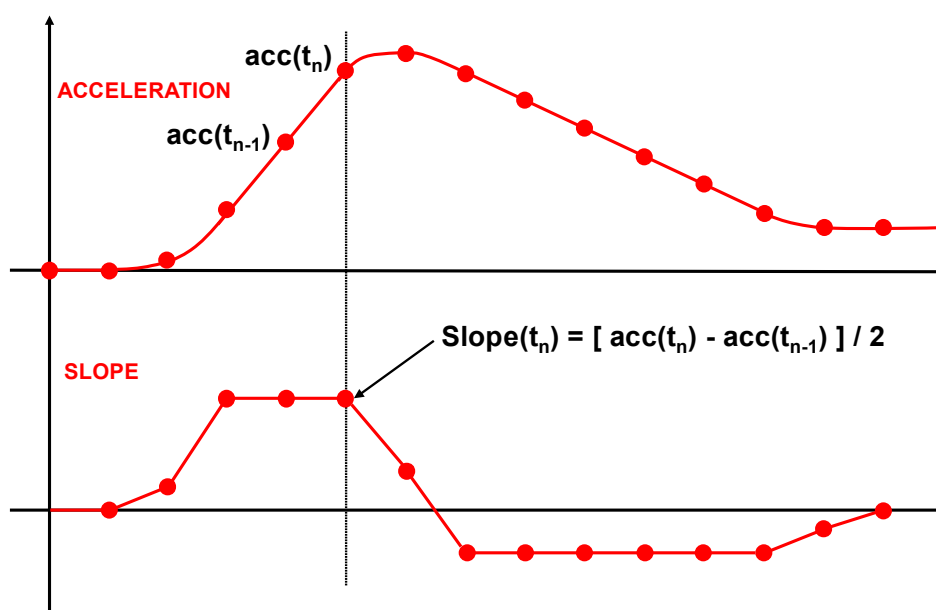
As shown in Figure 2. Accelerometer filtering chain, the device embeds a digital slope filter, which can also be used for wake-up detection and activity/inactivity embedded features.

The slope filter output data is computed using the following formula:

$$\text{slope}(t_n) = [\text{acc}(t_n) - \text{acc}(t_{n-1})] / 2$$

An example of a slope data signal is illustrated in the following figure.

**Figure 3. Accelerometer slope filter**



### 3.5 Accelerometer turn-on/off time

The accelerometer reading chain contains low-pass filtering to improve signal-to-noise performance and to reduce aliasing effects. For this reason, it is necessary to take into account the settling time of the filters when the accelerometer power mode is switched or when the accelerometer ODR is changed.

Accelerometer chain settling time is dependent on the output data rate selected for the following configurations:

- LPF2 and HP filters disabled
- LPF2 or HP filter enabled with ODR/4 bandwidth selection

For these two possible configurations, the maximum overall turn-on/off in order to switch accelerometer power modes or accelerometer ODR is the one shown below in [Table 7. Accelerometer turn-on/off time \(LPF2 and HP disabled\)](#) and [Table 8. Accelerometer samples to be discarded](#)

**Table 7. Accelerometer turn-on/off time (LPF2 and HP disabled)**

Starting mode	Target mode	Max turn-on/off time <sup>(1)</sup>
Power-down	High-performance	See <a href="#">Table 8</a>
High-performance	High-performance @ ODR < 6.66 kHz	Discard 3 samples
High-performance	High-performance @ ODR = 6.66 kHz	Discard 3 samples
High-performance	Power-down	1 $\mu$ s

1. Settling time @ 99% of the final value

**Table 8. Accelerometer samples to be discarded**

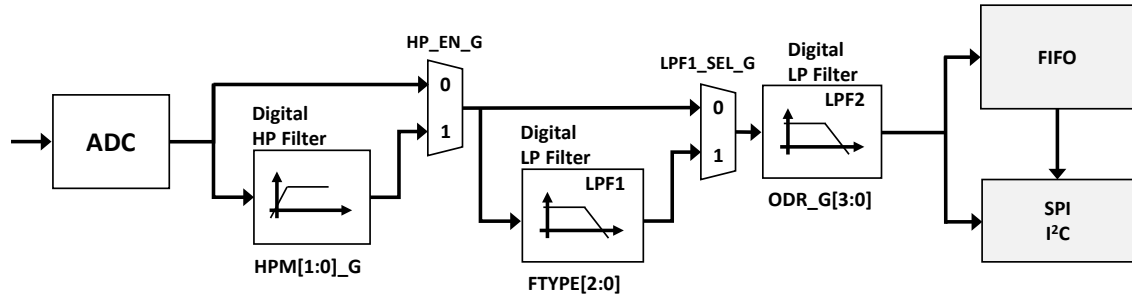
Target mode Accelerometer ODR [Hz]	Number of samples to be discarded (LPF2 and HP filters disabled)	Number of samples to be discarded (LPF2 or HP filter enabled @ODR/4 bandwidth)
12.5 (high-performance)	2	3
26 (high-performance)	2	3
52 (high-performance)	2	3
104 (high-performance)	2	3
208 (high-performance)	2	3
416 (high-performance)	2	3
833 (high-performance)	2	3
1667 (high-performance)	3	3
3333 (high-performance)	5	5
6667 (high-performance)	11	11

Overall settling time if LPF2 or HP digital filters are enabled with bandwidth different from ODR/4 has been already indicated in [Table 6. Accelerometer bandwidth selection](#).

### 3.6 Gyroscope bandwidth

The gyroscope filtering chain configuration is the one shown in [Figure 4. Gyroscope digital chain](#). It is a cascade of three filters: a selectable digital high-pass filter (HPF), a selectable digital low-pass filter (LPF1) and a digital low-pass filter (LPF2).

**Figure 4. Gyroscope digital chain**



The digital HP filter can be enabled by setting the bit HP\_EN\_G of CTRL7\_G register to 1 and its cutoff frequency can be selected through the field HPM\_G[1:0] of CTRL7\_G register, according to the following table.

**Table 9. Gyroscope digital HP filter cutoff selection**

HPM_G[1:0]	High-pass filter cutoff frequency [Hz]	Overall maximum settling time [s] <sup>(1)</sup>
00	0.016	45
01	0.065	11
10	0.260	3
11	1.040	0.7

1. Settling time @ 99% of the final value

The digital LPF1 filter can be enabled by setting the LPF1\_SEL\_G bit of CTRL4\_C register to 1 and its bandwidth can be selected through the field FTYPE\_[2:0] of CTRL6\_C register.

The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR. When the gyroscope ODR is equal to 6.66 kHz, the LPF2 filter is bypassed.

The overall gyroscope bandwidth for different gyroscope ODR values and for different configurations of the LPF1\_SEL\_G bit of CTRL4\_C register and FTYPE\_[2:0] of CTRL6\_C register is summarized in the following table.

**Table 10. Gyroscope overall bandwidth selection**

Gyroscope ODR [Hz]	LPF1_SEL_G	FTYPE[2:0]	Bandwidth [Hz] (phase delay @ 20 Hz)
12.5	0	-	4.3 (-35° @ 1.3 Hz)
	1	0xx	4.3 (-35° @ 1.3 Hz)
	1	100	4.3 (-35° @ 1.3 Hz)
	1	101	4.3 (-35° @ 1.3 Hz)
	1	110	4.3 (-35° @ 1.3 Hz)
	1	111	4.3 (-35° @ 1.3 Hz)
26	0	-	8.3 (-35° @ 2.5 Hz)
	1	0xx	8.3 (-35° @ 2.5 Hz)
	1	100	8.3 (-35° @ 2.5 Hz)
	1	101	8.3 (-35° @ 2.5 Hz)
	1	110	8.3 (-35° @ 2.5 Hz)

Gyroscope ODR [Hz]	LPF1_SEL_G	FTYPE[2:0]	Bandwidth [Hz] (phase delay @ 20 Hz)
26	1	111	8.3 (-35° @ 2.5 Hz)
52	0	-	16.7 (-35° @ 5 Hz)
	1	0xx	16.7 (-36° @ 5 Hz)
	1	100	16.7 (-39° @ 5 Hz)
	1	101	16.9 (-43° @ 5 Hz)
	1	110	13.4 (-44° @ 5 Hz)
	1	111	9.8 (-49° @ 5 Hz)
	1	111	9.8 (-49° @ 5 Hz)
104	0	-	33 (-35° @ 10 Hz)
	1	0xx	33 (-38° @ 10 Hz)
	1	100	34 (-43° @ 10 Hz)
	1	101	31 (-51° @ 10 Hz)
	1	110	19 (-54° @ 10 Hz)
	1	111	11.6 (-64° @ 10 Hz)
	1	111	11.6 (-64° @ 10 Hz)
208	0	-	67 (-35°)
	1	0xx	67 (-41°)
	1	100	62 (-51°)
	1	101	43 (-68°)
	1	110	23 (-74°)
	1	111	12.2 (-93°)
	1	111	12.2 (-93°)
416	0	-	133 (-18°)
	1	000	133 (-23°)
	1	001	128 (-25°)
	1	010	112 (-28°)
	1	011	134 (-21°)
	1	100	86 (-34°)
	1	101	48 (-51°)
	1	110	24.6 (-57°)
	1	111	12.4 (-76°)
	1	111	12.4 (-76°)
833	0	-	267 (-9°)
	1	000	222 (-14°)
	1	001	186 (-16°)
	1	010	140 (-20°)
	1	011	260 (-12°)
	1	100	96 (-25°)
	1	101	49 (-43°)
	1	110	25 (-48°)
	1	111	12.6 (-68°)
	1	111	12.6 (-68°)
1667	0	-	539 (-5°)
	1	000	274 (-10°)
	1	001	212 (-12°)
	1	010	150 (-15°)
	1	011	390 (-8°)
	1	100	99 (-21°)
	1	101	50 (-38°)
	1	101	50 (-38°)

Gyroscope ODR [Hz]	LPF1_SEL_G	FTYPE[2:0]	Bandwidth [Hz] (phase delay @ 20 Hz)
1667	1	110	25 (-44°)
	1	111	12.6 (-63°)
3333	0	-	1137 (-3°)
	1	000	292 (-8°)
	1	001	220 (-10°)
	1	010	153 (-13°)
	1	011	451 (-6°)
	1	1xx	Not available
6667	0	-	>3333 (-2°)
	1	000	297 (-7°)
	1	001	223 (-9°)
	1	010	154 (-12°)
	1	011	470 (-5°)
	1	1xx	Not available

### 3.7 Gyroscope turn-on/off time

Turn-on/off time has to be considered also for the gyroscope sensor when switching its modes or when the gyroscope ODR is changed.

The maximum overall turn-on/off time (with HP filter disabled) in order to switch gyroscope power modes or gyroscope ODR is the one shown in Table 11. Gyroscope turn-on/off time (HP disabled).

**Table 11. Gyroscope turn-on/off time (HP disabled)**

Starting mode	Target mode	Max turn-on/off time <sup>(1)</sup>
Power-down	Sleep	70 ms
Power-down	High-performance	70 ms + see Table 12 or Table 13
Sleep	High-performance	See Table 12 or Table 13
High-performance	High-performance (ODR change)	Discard 2 samples
High-performance	Power-down	1 $\mu$ s if both XL and Gyro in PD 300 $\mu$ s if XL not in PD

1. Settling time @ 99% of the final value

**Table 12. Gyroscope samples to be discarded (LPF1 disabled)**

Gyroscope ODR [Hz]	Number of samples to be discarded <sup>(1)</sup>
12.5 Hz	2
26 Hz	3
52 Hz	3
104 Hz	3
208 Hz	3
416 Hz	3
833 Hz	3
1.66 kHz	4
3.33 kHz	5
6.66 kHz	6

1. Settling time @ 99% of the final value

**Table 13. Gyroscope chain settling time (LPF1 enabled)**

FTYPE[2:0]	Maximum settling time @ each ODR [ms] <sup>(1)</sup>
000	3.5
001	4.8
010	6.9
011	2.1
100	11
101	22
110	30
111	60

1. Settling time @ 99% of the final value

When there is a mode change to high-performance mode and the HP filter is enabled, or the HP filter is turned on, the HP filter settling time must be added to Table 11. Gyroscope turn-on/off time (HP disabled). The HP filter settling time is independent from the ODR and is shown in Table 9. Gyroscope digital HP filter cutoff selection.



## 4 Reading output data

### 4.1 Startup sequence

Once the device is powered up, it automatically downloads the calibration coefficients from the embedded flash to the internal registers. When the boot procedure is completed, that is, after approximately 10 milliseconds, the accelerometer and gyroscope automatically enter power-down mode.

To turn on the accelerometer and gather acceleration data through the primary I<sup>2</sup>C / SPI interface, it is necessary to select one of the operating modes through the CTRL1\_XL register.

The following general-purpose sequence can be used to configure the accelerometer:

1. Write INT1\_CTRL = 01h // Accelerometer data-ready interrupt on INT1
2. Write CTRL1\_XL = 60h // Accelerometer = 416 Hz (high-performance mode)

To turn on the gyroscope and gather angular rate data through the primary I<sup>2</sup>C / SPI interface, it is necessary to select one of the operating modes through CTRL2\_G.

The following general-purpose sequence can be used to configure the gyroscope:

1. Write INT1\_CTRL = 02h // Gyroscope data-ready interrupt on INT1
2. Write CTRL2\_G = 60h // Gyroscope = 416 Hz (high-performance mode)

### 4.2 Using the status register

The device is provided with a STATUS\_REG register which should be polled to check when a new set of data is available. The XLDA bit is set to 1 when a new set of data is available at the accelerometer output. The GDA bit is set to 1 when a new set of data is available at the gyroscope output.

For the accelerometer (the gyroscope is similar), the read of the output registers should be performed as follows:

1. Read STATUS\_REG.
2. If XLDA = 0, then go to 1.
3. Read OUTX\_L\_A.
4. Read OUTX\_H\_A.
5. Read OUTY\_L\_A.
6. Read OUTY\_H\_A.
7. Read OUTZ\_L\_A.
8. Read OUTZ\_H\_A.
9. Data processing
10. Go to 1.

### 4.3 Using the data-ready signal

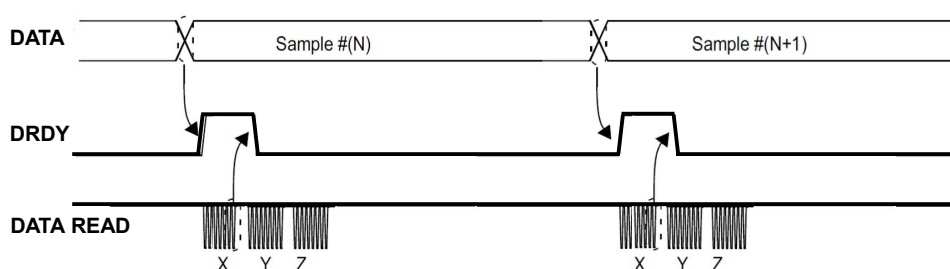
The device can be configured to have a hardware signal to determine when a new set of measurement data is available to be read.

For the accelerometer sensor, the data-ready signal is represented by the XLDA bit of the STATUS\_REG register. The signal can be driven to the INT1 pin by setting the INT1\_DRDY\_XL bit of the INT1\_CTRL register to 1 and to the INT2 pin by setting the INT2\_DRDY\_XL bit of the INT2\_CTRL register to 1.

For the gyroscope sensor, the data-ready signal is represented by the GDA bit of the STATUS\_REG register. The signal can be driven to the INT1 pin by setting the INT1\_DRDY\_G bit of the INT1\_CTRL register to 1 and to the INT2 pin by setting the INT2\_DRDY\_G bit of the INT2\_CTRL register to 1.

The data-ready signal rises to 1 when a new set of data has been generated and it is available to be read. The data-ready signal can be either latched or pulsed. If the dataready\_pulsed bit of the COUNTER\_BDR\_REG1 register is set to 0 (default value), then the data-ready signal is latched and the interrupt is reset when the higher part of one axis is read (29h, 2Bh, 2Dh for the accelerometer; 23h, 25h, 27h for the gyroscope). If the dataready\_pulsed bit of the COUNTER\_BDR\_REG1 register is set to 1, then the data-ready is pulsed and the duration of the pulse observed on the interrupt pins is 75  $\mu$ s. Pulsed mode is not applied to the XLDA and GDA bits, which are always latched.

Figure 5. Data-ready signal



#### 4.3.1 DRDY mask functionality

Setting the DRDY\_MASK bit of the CTRL4\_C register to 1, the accelerometer and gyroscope data-ready signals are masked until the settling of the sensor filters is completed.

When FIFO is active and the DRDY\_MASK bit is set to 1, accelerometer/gyroscope invalid samples stored in FIFO can be equal to 7FFFh, 7FFEh or 7FFDh. In this way, a tag is applied to the invalid samples stored in the FIFO buffer so that they can be easily identified and discarded during data post-processing.

**Note:** The DRDY\_MASK bit acts only on the accelerometer LPF1 digital filter settling time for every accelerometer ODR and on the gyroscope LPF2 digital filter settling time for gyroscope ODR  $\leq$  833 Hz.

### 4.4 Using the block data update (BDU) feature

If reading the accelerometer/gyroscope data is not synchronized with either the XLDA/GDA bits in the STATUS\_REG register or with the DRDY signal driven to the INT1/INT2 pins, it is strongly recommended to set the BDU (block data update) bit to 1 in the CTRL3\_C register.

This feature avoids reading values (most significant and least significant bytes of the output data) related to different samples. In particular, when the BDU is activated, the data registers related to each axis always contain the most recent output data produced by the device, but, in case the read of a given pair (that is, OUTX\_H\_A(G) and OUTX\_L\_A(G), OUTY\_H\_A(G) and OUTY\_L\_A(G), OUTZ\_H\_A(G) and OUTZ\_L\_A(G)) is initiated, the refresh for that pair is blocked until both the MSB and LSB of the data are read.

**Note:** BDU only guarantees that the LSB and MSB have been sampled at the same moment. For example, if the reading speed is too slow, X and Y can be read at T1 and Z sampled at T2.

The BDU feature also acts on the FIFO\_STATUS1 and FIFO\_STATUS2 registers. When the BDU bit is set to 1, it is mandatory to read FIFO\_STATUS1 first and then FIFO\_STATUS2.

## 4.5 Understanding output data

The measured acceleration data are sent to the OUTX\_H\_A, OUTX\_L\_A, OUTY\_H\_A, OUTY\_L\_A, OUTZ\_H\_A, and OUTZ\_L\_A registers. These registers contain, respectively, the most significant part and the least significant part of the acceleration signals acting on the X, Y, and Z axes.

The measured angular rate data are sent to the OUTX\_H\_G, OUTX\_L\_G, OUTY\_H\_G, OUTY\_L\_G, OUTZ\_H\_G, and OUTZ\_L\_G registers. These registers contain, respectively, the most significant part and the least significant part of the angular rate signals acting on the X, Y, and Z axes.

The complete output data for the X, Y, Z channels is given by the concatenation OUTX\_H\_A(G) & OUTX\_L\_A(G), OUTY\_H\_A(G) & OUTY\_L\_A(G), OUTZ\_H\_A(G) & OUTZ\_L\_A(G) and it is expressed as a two's complement number.

Both acceleration data and angular rate data are represented as 16-bit numbers.

### 4.5.1 Examples of output data

Table 14. Content of output data registers vs. acceleration (FS\_XL =  $\pm 2$  g) provides a few basic examples of the accelerometer data that is read in the data registers when the device is subjected to a given acceleration.

Table 15. Content of output data registers vs. angular rate (FS\_G =  $\pm 250$  dps) provides a few basic examples of the gyroscope data that is read in the data registers when the device is subjected to a given angular rate.

The values listed in the following tables are given under the hypothesis of perfect device calibration (that is, no offset, no gain error, and so forth).

**Table 14. Content of output data registers vs. acceleration (FS\_XL =  $\pm 2$  g)**

Acceleration values	Register address	
	OUTX_H_A (29h)	OUTX_L_A (28h)
0 g	00h	00h
350 mg	16h	69h
1 g	40h	09h
-350 mg	E9h	97h
-1 g	BFh	F7h

**Table 15. Content of output data registers vs. angular rate (FS\_G =  $\pm 250$  dps)**

Angular rate values	Register address	
	OUTX_H_G (23h)	OUTX_L_G (22h)
0 dps	00h	00h
100 dps	2Ch	A4h
200 dps	59h	49h
-100 dps	D3h	5Ch
-200 dps	A6h	B7h

## 4.6 Accelerometer offset registers

The device provides accelerometer offset registers (X\_OFS\_USR, Y\_OFS\_USR, Z\_OFS\_USR) which can be used for zero-g offset correction or, in general, to apply an offset to the accelerometer output data.

The accelerometer offset block can be enabled by setting the USR\_OFF\_ON\_OUT bit of the CTRL7\_G register. The offset value set in the offset registers is internally subtracted from the measured acceleration value for the respective axis. Internally processed data are then sent to the accelerometer output register and to the FIFO (if enabled). These register values are expressed as an 8-bit word in two's complement and must be in the range [-127, 127].

The weight [g/LSB] to be applied to the offset register values is independent of the accelerometer selected full scale and can be configured using the USR\_OFF\_W bit of the CTRL6\_C register:

- $2^{-10}$  g/LSB if the USR\_OFF\_W bit is set to 0
- $2^{-6}$  g/LSB if the USR\_OFF\_W bit is set to 1

## 4.7 Wraparound functions

The wraparound function can be used to auto address the device registers for a circular burst-mode read.

Basically, with a multiple read operation, the address of the register that is being read goes automatically from the first register to the last register of the pattern and then goes back to the first one.

### 4.7.1 FIFO output registers

The wraparound function is automatically enabled when performing a multiple read operation of the FIFO output registers. After reading FIFO\_DATA\_OUT\_Z\_H (7Eh), the address of the next register that is read goes automatically back to FIFO\_DATA\_OUT\_TAG (78h), allowing the user to read many data with a unique multiple read.

### 4.7.2 Sensor output registers

It is possible to apply the wraparound function to the other output registers.

The wraparound function can also be enabled for the following groups of output registers:

- Accelerometer output registers, from OUTX\_L\_A (28h) to OUTZ\_H\_A (2Dh)
- Gyroscope output registers, from OUTX\_L\_G (22h) to OUTZ\_H\_G (27h)
- Gyroscope and accelerometer output registers, from OUTX\_L\_G (22h) to OUTZ\_H\_A (2Dh)

The output register wraparound pattern can be configured using the bits ROUNDING[1:0] of the CTRL5\_C register, as indicated in the following table.

**Table 16. Output register wraparound pattern**

ROUNDING[1:0]	Wraparound pattern
00	No wraparound
01	Accelerometer only
10	Gyroscope only
11	Gyroscope + accelerometer

## 4.8 DEN (data enable)

The device allows an external trigger level recognition by enabling the TRIG\_EN, LVL1\_EN, LVL2\_EN bits in the CTRL6\_C register.

Four different modes can be selected (see [Table 17. DEN configurations](#)):

- Edge-sensitive trigger mode
- Level-sensitive trigger mode
- Level-sensitive latched mode
- Level-sensitive FIFO enable mode

The data enable (DEN) input signal must be driven on the INT2 pin, which is configured as an input pin when one of these modes is enabled.

The DEN functionality is active by default on the gyroscope data only. To extend this feature to the accelerometer data, the bit DEN\_XL\_EN in the CTRL9\_XL register must be set to 1.

The DEN active level is low by default. It can be changed to active-high by setting the bit DEN\_LH in the CTRL9\_XL register to 1.

**Table 17. DEN configurations**

TRIG_EN	LVL1_EN	LVL2_EN	Function	Trigger type	Action
0	0	0	Data enable off	-	-
1	0	0	Edge-sensitive trigger mode	Edge	Data generation
0	1	0	Level-sensitive trigger mode	Level	Data stamping
0	1	1	Level-sensitive latched mode	Edge	Data stamping
1	1	0	Level-sensitive FIFO enable mode	Level	Data generation in FIFO and stamping

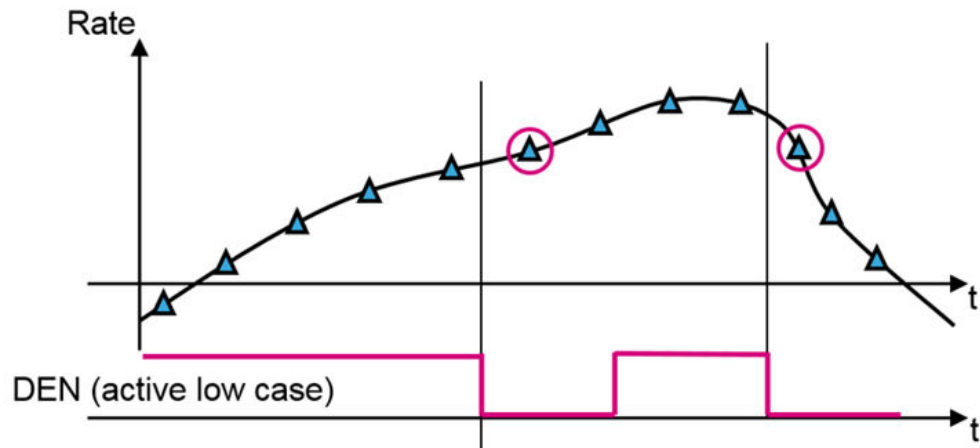
#### 4.8.1 Edge-sensitive trigger mode

Edge-sensitive trigger mode can be enabled by setting the TRIG\_EN bit in CTRL6\_C to 1, and LVL1\_EN, LVL2\_EN bits in the CTRL6\_C register to 0.

Once the edge-sensitive trigger mode is enabled, the FIFO buffer and output registers are filled with the first sample acquired after every rising edge (if DEN\_LH bit is equal to 1) or falling edge (if DEN\_LH bit is equal to 0) of the DEN input signal.

Figure 6 shows, with red circles, the samples acquired after the falling edges (DEN active-low).

**Figure 6. Edge-sensitive trigger mode, DEN active-low**



Edge-sensitive trigger mode, when enabled, acts only on the gyroscope output registers. GDA is related only to downsampled data, while the accelerometer output registers and XLDA are updated according to ODR\_XL. If the DEN\_XL\_EN bit is set to 1, the accelerometer sensor is downsampled too. In this case, the gyroscope and accelerometer have to be set in combo mode at the same ODR. The accelerometer standalone mode can be used by setting the gyroscope in power-down.

Note that the DEN level is internally read just before the update of the data registers. If a level change occurs after the read, DEN is acknowledged at the next ODR.

There are three possible configurations for the edge-sensitive trigger in FIFO, described below:

1. Only the gyroscope in trigger mode but not saved in FIFO. In this case, FIFO is related only to the accelerometer and works as usual.
2. Only the gyroscope in trigger mode and saved in FIFO. In this configuration there are the following limitations in FIFO:
  - Gyroscope batch data rate (BDR\_GY\_[3:0] bits of the FIFO\_CTRL3 register) and gyroscope output data rate (ODR\_G[3:0] of the CTRL2\_G register) must be set to the same value.
  - Configuration-change sensor (CFG-change) is not allowed (ODRCHG\_EN bit of the FIFO\_CTRL2 register must be set to 0).
  - Timestamp decimation in FIFO is not allowed (DEC\_TS\_BATCH\_[1:0] bits of the FIFO\_CTRL4 register must be set to 00).
3. Gyroscope and accelerometer in trigger mode and saved in FIFO. In this configuration there are the following limitations in FIFO:
  - Gyroscope batch data rate (BDR\_GY\_[3:0] bits of the FIFO\_CTRL3 register) and gyroscope output data rate (ODR\_G[3:0] of the CTRL2\_G register) must be set to the same value.
  - Accelerometer batch data rate (BDR\_XL\_[3:0] bits of the FIFO\_CTRL3 register) and accelerometer output data rate (ODR\_XL[3:0] of the CTRL1\_XL register) must be set to the same value.
  - Gyroscope and accelerometer must be set at the same output data rate, or the gyroscope must be configured in power-down mode.
  - Configuration-change sensor (CFG-change) is not allowed (ODRCHG\_EN bit of the FIFO\_CTRL2 register must be set to 0).
  - Timestamp decimation in FIFO is not allowed (DEC\_TS\_BATCH\_[1:0] bits of the FIFO\_CTRL4 register must be set to 00).

Edge-sensitive trigger mode allows, for example, the synchronization of the camera frames with the samples coming from the gyroscope for electrical image stabilization (EIS) applications. The synchronization signal from the camera module must be connected to the INT2 pin.

In the example shown below, the FIFO has been configured to store both the gyroscope data and the accelerometer data in the FIFO buffer. When the DEN signal toggles, the data are written to FIFO on the falling edge.

- |                            |  |
|----------------------------|--|
| 1. Write 44h to FIFO_CTRL3 | // Enable accelerometer and gyroscope in FIFO @ 104 Hz           |
| 2. Write 06h to FIFO_CTRL4 | // Set FIFO in continuous mode                                   |
|                            | // Enable the edge-sensitive trigger                             |
| 3. Write 80h to CTRL6_C    | // INT2 pin is switched to input mode (DEN signal)               |
| 4. Write EAh to CTRL9_XL   | // Extend DEN functionality to accelerometer sensor              |
|                            | // Select DEN active level (active low)                          |
| 5. Write 40h to CTRL1_XL   | // Turn on the accelerometer: ODR_XL = 104 Hz, FS_XL = $\pm 2 g$ |
| 6. Write 4Ch to CTRL2_G    | // Turn on the gyroscope: ODR_G = 104 Hz, FS_G = $\pm 2000 dps$  |

#### 4.8.2 Level-sensitive trigger mode

Level-sensitive trigger mode can be enabled by setting the LVL1\_EN bit in the CTRL6\_C register to 1, and the TRIG\_EN, LVL2\_EN bits in the CTRL6\_C register to 0.

Once the level-sensitive trigger mode is enabled, the LSB bit of the selected data (in output registers and FIFO) is replaced by 1 if the DEN level is active, or 0 if the DEN level is not active. The selected data can be the X, Y, Z axes of the accelerometer or gyroscope sensor (see [Section 4.8.5 LSB selection for DEN stamping](#) for details).

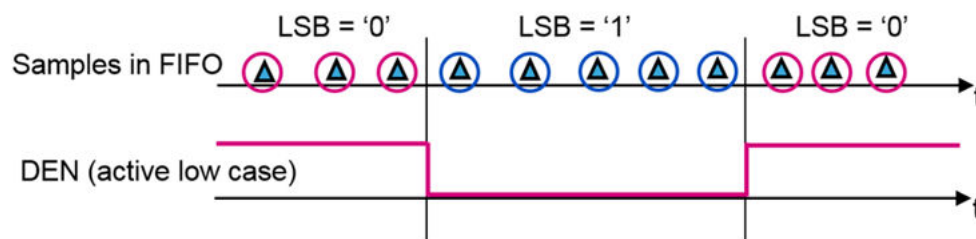
All data can be stored in the FIFO according to the FIFO settings.

Note that the DEN level is internally read just before the update of the data registers. If a level change occurs after the read, DEN is acknowledged at the next ODR.

If the DEN feature is enabled on the accelerometer sensor by asserting the DEN\_XL\_EN bit of the CTRL9\_XL register, the accelerometer and gyroscope sensors must be configured at the same ODR or the gyroscope must be set in power-down mode.

[Figure 7. Level-sensitive trigger mode, DEN active-low](#) shows with red circles the samples stored in the FIFO with LSB = 0 (DEN not active) and with blue circles the samples stored in the FIFO with LSB = 1 (DEN active).

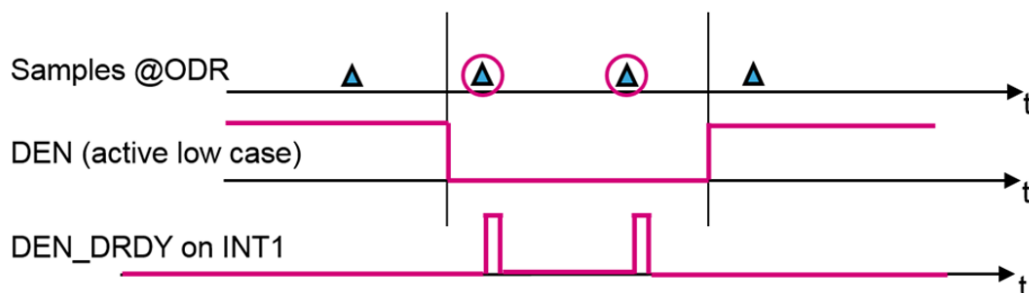
**Figure 7. Level-sensitive trigger mode, DEN active-low**



When the level-sensitive trigger mode is enabled, the DEN signal can also be used to filter the data-ready signal on the INT1 pin. INT1 shows data-ready information only when the DEN pin is in the active state. To do this, the bit DEN\_DRDY\_flag of the INT1\_CTRL register must be set to 1. The interrupt signal can be latched or pulsed according to the dataready\_pulsed bit of the COUNTER\_BDR\_REG1 register.

[Figure 8. Level-sensitive trigger mode, DEN active-low, DEN\\_DRDY on INT1](#) shows an example of data-ready on INT1 when the DEN level is low (active state).

**Figure 8. Level-sensitive trigger mode, DEN active-low, DEN\_DRDY on INT1**





### 4.8.3 Level-sensitive latched mode

Level-sensitive latched mode can be enabled by setting the LVL1\_EN and LVL2\_EN bits in the CTRL6\_C register to 1, and the TRIG\_EN bit in the CTRL6\_C register to 0.

When the level-sensitive latched mode is enabled, the LSB bit of the selected data (in output registers and FIFO) is normally set to 0 and becomes 1 only on the first sample after a pulse on the DEN pin.

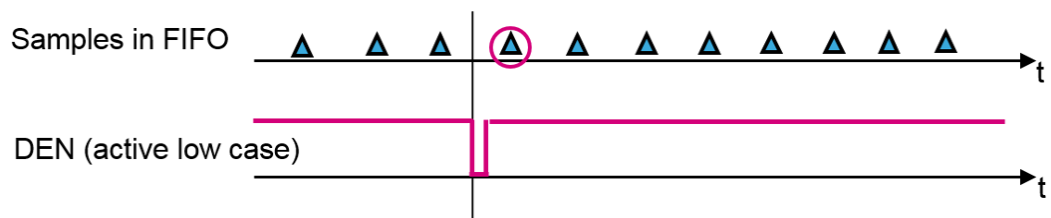
Note that the DEN level is internally read just before the update of the data registers. If a level change occurs after the read, DEN is acknowledged at the next ODR.

If the DEN feature is enabled on the accelerometer sensor by asserting the DEN\_XL\_EN bit of the CTRL9\_XL register, the accelerometer and gyroscope sensors must be configured at the same ODR or the gyroscope must be set in power-down mode.

Data can be selected through the DEN\_X, DEN\_Y, DEN\_Z, DEN\_XL\_G bits in CTRL9\_XL (see [Section 4.8.5 LSB selection for DEN stamping](#) for details).

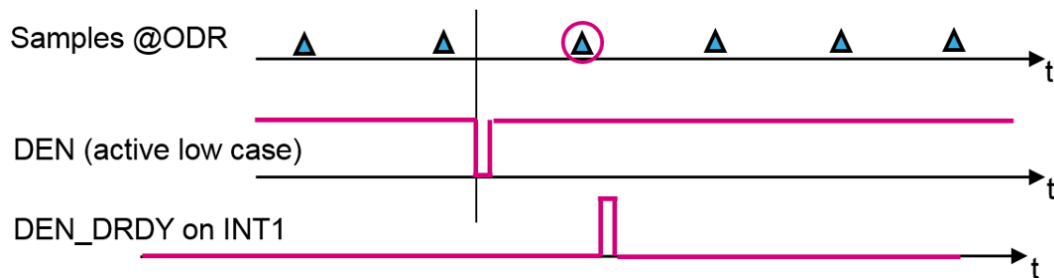
Figure 9 shows an example of level-sensitive latched mode with DEN active-low. After the pulse on the DEN pin, the sample with a red circle has the value 1 on the LSB bit. All the other samples have LSB bit 0.

**Figure 9. Level-sensitive latched mode, DEN active-low**



When the level-sensitive latched mode is enabled and the bit DEN\_DRDY\_flag of the INT1\_CTRL register is set to 1, a pulse is generated on the INT1 pin corresponding to the availability of the first sample generated after the DEN pulse occurrence (see [Figure 10. Level-sensitive latched mode, DEN active-low, DEN\\_DRDY on INT1](#)).

**Figure 10. Level-sensitive latched mode, DEN active-low, DEN\_DRDY on INT1**



#### 4.8.4 Level-sensitive FIFO enable mode

Level-sensitive FIFO enable mode can be enabled by setting the TRIG\_EN and LVL1\_EN bits in the CTRL6\_C register to 1, and the LVL2\_EN bit in the CTRL6\_C register to 0.

Once the level-sensitive FIFO enable mode is enabled, data is stored in the FIFO only when the DEN pin is equal to the active state.

In this mode, the LSB bit of the selected data (in output registers and FIFO) is replaced by 0 for odd DEN events and by 1 for even DEN events. This feature allows distinguishing the data stored in FIFO during the current DEN active window from the data stored in FIFO during the next DEN active window.

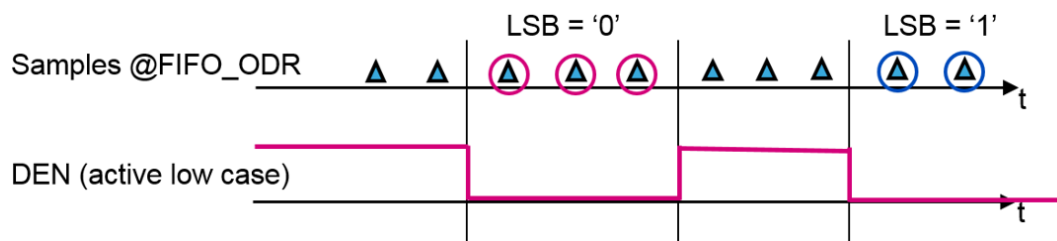
Note that the DEN level is internally read just before the update of the data registers. If a level change occurs after the reading, DEN is acknowledged at the next ODR.

If the DEN feature is enabled on the accelerometer sensor by asserting the DEN\_XL\_EN bit of the CTRL9\_XL register, the accelerometer and gyroscope sensors must be configured at the same ODR or the gyroscope must be set in power-down mode.

The selected data can be the X, Y, Z axes of the accelerometer or gyroscope sensor. Data can be selected through the DEN\_X, DEN\_Y, DEN\_Z, DEN\_XL\_G bits in the CTRL9\_XL register (see [Section 4.8.5 LSB selection for DEN stamping](#) for details).

An example of level-sensitive FIFO enable mode is shown in [Figure 11](#), the red circles show the samples stored in the FIFO with LSB bit 0, while the blue circles show the samples with LSB bit 1.

**Figure 11. Level-sensitive FIFO enable mode, DEN active-low**



When using level-sensitive FIFO enabled mode, some limitations must be taken into account in the FIFO configuration:

- Gyroscope batch data rate (BDR\_GY\_[3:0] bits of the FIFO\_CTRL3 register) and gyroscope output data rate (ODR\_G[3:0] of the CTRL2\_G register) must be set to the same value.
- Accelerometer batch data rate (BDR\_XL\_[3:0] bits of the FIFO\_CTRL3 register) and accelerometer output data rate (ODR\_XL[3:0] of the CTRL1\_XL register) must be set to the same value if the DEN\_XL\_EN bit of the CTRL9\_XL register is set to 1.
- Configuration-change sensor (CFG-change) is not allowed (ODRCHG\_EN bit of the FIFO\_CTRL2 register must be set to 0).
- Timestamp decimation in FIFO is not allowed (DEC\_TS\_BATCH\_[1:0] bits of the FIFO\_CTRL4 register must be set to 00).

#### 4.8.5 LSB selection for DEN stamping

When level-sensitive modes (trigger or latched) are used, it is possible to select which LSB have to contain the information related to DEN pin behavior. This information can be stamped on the accelerometer or gyroscope axes in accordance with bits DEN\_X, DEN\_Y, DEN\_Z and DEN\_XL\_G of the CTRL9\_XL register. Setting to 1 the DEN\_X, DEN\_Y, DEN\_Z bits, DEN information is stamped in the LSB of the corresponding axes of the sensor selected with the DEN\_XL\_G bit. By setting DEN\_XL\_G to 0, the DEN information is stamped in the selected gyroscope axes, while by setting DEN\_XL\_G to 1, the DEN information is stamped in the selected accelerometer axes.

By default, the bits are configured to have information on all the gyroscope axes.

## 5 Interrupt generation

Interrupt generation is based on accelerometer data only, so, for interrupt-generation purposes, the accelerometer sensor has to be set in an active operating mode (not in power-down). The gyroscope sensor can be configured in power-down mode since it's not involved in interrupt generation.

The interrupt generator can be configured to detect:

- Free-fall
- Wake-up
- 6D/4D orientation detection
- Activity/inactivity and motion/stationary recognition

All these interrupt signals, together with the FIFO interrupt signals, can be independently driven to the INT1 and INT2 interrupt pins or checked by reading the dedicated source register bits.

The H\_LACTIVE bit of the CTRL3\_C register must be used to select the polarity of the interrupt pins. If this bit is set to 0 (default value), the interrupt pins are active high and they change from low to high level when the related interrupt condition is verified. Otherwise, if the H\_LACTIVE bit is set to 1 (active low), the interrupt pins are normally at high level and they change from high to low when interrupt condition is reached.

The PP\_OD bit of CTRL3\_C allows changing the behavior of the interrupt pins from push-pull to open drain. If the PP\_OD bit is set to 0, the interrupt pins are in push-pull configuration (low-impedance output for both high and low level). When the PP\_OD bit is set to 1, only the interrupt active state is a low-impedance output.

### 5.1 Interrupt pin configuration

The device is provided with two pins that can be activated to generate either data-ready or interrupt signals. The functionality of these pins is selected through the MD1\_CFG and INT1\_CTRL registers for the INT1 pin, and through the MD2\_CFG and INT2\_CTRL registers for the INT2 pin.

A brief description of these interrupt control registers is given in the following summary. The default value of their bits is equal to 0, which corresponds to 'disable'. In order to enable the routing of a specific interrupt signal on the pin, the related bit has to be set to 1.

**Table 18. INT1\_CTRL register**

b7	b6	b5	b4	b3	b2	b1	b0
DEN_DRDY_flag	INT1_CNT_BDR	INT1_FIFO_FULL	INT1_FIFO_OVR	INT1_FIFO_TH	INT1_BOOT	INT1_DRDY_G	INT1_DRDY_XL

- DEN\_DRDY\_flag: DEN\_DRDY flag interrupt on INT1
- INT1\_CNT\_BDR: FIFO COUNTER\_BDR\_IA interrupt on INT1
- INT1\_FIFO\_FULL: FIFO full flag interrupt on INT1
- INT1\_FIFO\_OVR: FIFO overrun flag interrupt on INT1
- INT1\_FIFO\_TH: FIFO threshold interrupt on INT1
- INT1\_BOOT: boot interrupt on INT1
- INT1\_DRDY\_G: gyroscope data-ready on INT1
- INT1\_DRDY\_XL: accelerometer data-ready on INT1

**Table 19. MD1\_CFG register**

b7	b6	b5	b4	b3	b2	b1	b0
INT1_SLEEP_CHANGE	0	INT1_WU	INT1_FF	0	INT1_6D	0	0

- INT1\_SLEEP\_CHANGE: activity/inactivity recognition event interrupt on INT1
- INT1\_WU: wake-up interrupt on INT1
- INT1\_FF: free-fall interrupt on INT1
- INT1\_6D: 6D detection interrupt on INT1

**Table 20. INT2\_CTRL register**

b7	b6	b5	b4	b3	b2	b1	b0
0	INT2_CNT_BDR	INT2_FIFO_FULL	INT2_FIFO_OVR	INT2_FIFO_TH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL

- INT2\_CNT\_BDR: FIFO COUNTER\_BDR\_IA interrupt on INT2
- INT2\_FIFO\_FULL: FIFO full flag interrupt on INT2
- INT2\_FIFO\_OVR: FIFO overrun flag interrupt on INT2
- INT2\_FIFO\_TH: FIFO threshold interrupt on INT2
- INT2\_DRDY\_TEMP: temperature data-ready on INT2
- INT2\_DRDY\_G: gyroscope data-ready on INT2
- INT2\_DRDY\_XL: accelerometer data-ready on INT2

**Table 21. MD2\_CFG register**

b7	b6	b5	b4	b3	b2	b1	b0
INT2_SLEEP_CHANGE	0	INT2_WU	INT2_FF	0	INT2_6D	0	INT2_TIMESTAMP

- INT2\_SLEEP\_CHANGE: activity/inactivity recognition event interrupt on INT2
- INT2\_WU: wake-up interrupt on INT2
- INT2\_FF: free-fall interrupt on INT2
- INT2\_6D: 6D detection interrupt on INT2
- INT2\_TIMESTAMP: timestamp overflow alert interrupt on INT2

If multiple interrupt signals are routed on the same pin (INTx), the logic level of this pin is the “OR” combination of the selected interrupt signals. In order to know which event has generated the interrupt condition, the related source registers have to be read:

- WAKE\_UP\_SRC, D6D\_SRC (basic interrupt functions)
- STATUS\_REG (for data-ready signals)
- FIFO\_STATUS2 (for FIFO)

The ALL\_INT\_SRC register groups the basic interrupts functions event status (6D/4D, free-fall, wake-up, activity/inactivity, timestamp) in a single register. It is possible to read this register in order to address a subsequent specific source register read.

The INT2\_on\_INT1 pin of CTRL4\_C register allows driving all the enabled interrupt signals in logic “OR” on the INT1 pin (by setting this bit to 1). When this bit is set to 0, the interrupt signals are divided between the INT1 and INT2 pins.

The basic interrupts have to be enabled by setting the INTERRUPTS\_ENABLE bit in the INT\_CFG1 register.

The LIR bit of the INT\_CFG0 register enables the latched interrupt for the basic interrupt functions. When this bit is set to 1 and the interrupt flag is sent to the INT1 pin and/or INT2 pin, the interrupt remains active until the ALL\_INT\_SRC register or the corresponding source register is read, and it is reset at the next ODR cycle. The latched interrupt is enabled on a function only if a function is routed to the INT1 or INT2 pin. If latched mode is enabled but the interrupt signal is not driven to the interrupt pins, the latch feature does not take effect.

**Note:**

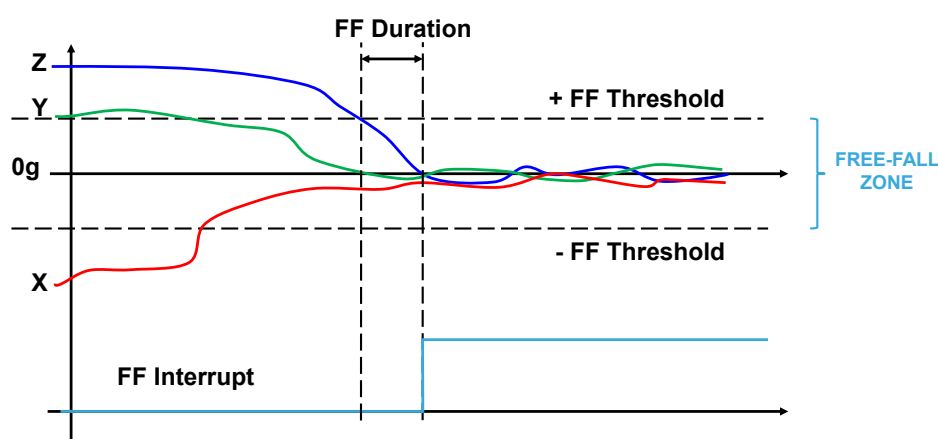
*If latched mode is enabled (LIR = 1), it is not recommended to continuously poll the ALL\_INT\_SRC or the dedicated source registers, because by reading them the embedded functions are internally reset. A synchronous (with interrupt event) read of the source registers is recommended in this case.*

When latched mode is enabled (LIR = 1), it is possible to force the immediate reset of the interrupt signal routed on the INT1 or INT2 pin and its corresponding interrupt status bit when ALL\_INT\_SRC (or the related source register) is read. In order to perform this immediate reset, the INT\_CLR\_ON\_READ bit of the INT\_CFG0 register must be set to 1. When bit INT\_CLR\_ON\_READ is equal to 0, the reset occurs at the next ODR cycle.

## 5.2 Free-fall interrupt

Free-fall detection refers to a specific register configuration that allows recognizing when the device is in free-fall: the acceleration measured along all the axes goes to zero. In a real case, a “free-fall zone” is defined around the zero-*g* level where all the accelerations are small enough to generate the interrupt. Configurable threshold and duration parameters are associated to free-fall event detection. The threshold parameter defines the free-fall zone amplitude. The duration parameter defines the minimum duration of the free-fall interrupt event to be recognized (Figure 12. Free-fall interrupt).

**Figure 12. Free-fall interrupt**



The free-fall interrupt signal can be enabled by setting the `INTERRUPTS_ENABLE` bit in the `INT_CFG1` register to 1 and can be driven to the two interrupt pins by setting the `INT1_FF` bit of the `MD1_CFG` register to 1 or the `INT2_FF` bit of the `MD2_CFG` register to 1. It can also be checked by reading the `FF_IA` bit of the `WAKE_UP_SRC` register.

If latched mode is disabled (`LIR` bit of `INT_CFG0` is set to 0), the interrupt signal is automatically reset when the free-fall condition is no longer verified. If latched mode is enabled and the free-fall interrupt signal is driven to the interrupt pins, once a free-fall event has occurred and the interrupt pin is asserted, it must be reset by reading the `WAKE_UP_SRC` or `ALL_INT_SRC` register. If latched mode is enabled but the interrupt signal is not driven to the interrupt pins, the latch feature does not take effect.

The `FREE_FALL` register is used to configure the threshold parameter. The unsigned threshold value is related to the value of the `FF_THS[2:0]` field value as indicated in Table 22. Free-fall threshold LSB value. The values given in this table are valid for each accelerometer full-scale value.

**Table 22. Free-fall threshold LSB value**

<code>FREE_FALL - FF_THS[2:0]</code>	Threshold LSB value [mg]
000	156
001	219
010	250
011	312
100	344
101	406
110	469
111	500

Duration time is measured in  $N/ODR_{XL}$ , where  $N$  is the content of the `FF_DUR[5:0]` field of the `FREE_FALL` / `WAKE_UP_DUR` registers and  $ODR_{XL}$  is the accelerometer data rate.

A basic software routine for free-fall event recognition is given below.

1. Write 60h to CTRL1\_XL // Turn on the accelerometer  
// ODR\_XL = 416 Hz, FS\_XL =  $\pm 2 g$
2. Write 41h to INT\_CFG0 // Enable latched mode with reset on read
3. Write 80h to INT\_CFG1 // Enable interrupt function
4. Write 00h to WAKE\_UP\_DUR // Set event duration (FF\_DUR5 bit)
5. Write 33h to FREE\_FALL // Set FF threshold (FF\_THS[2:0] = 011)  
// Set six samples event duration (FF\_DUR[5:0] = 000110)
6. Write 10h to MD1\_CFG // FF interrupt driven to INT1 pin

The sample code exploits a threshold set to 312 mg for free-fall recognition and the event is notified by hardware through the INT1 pin. The FF\_DUR[5:0] field of the FREE\_FALL / WAKE\_UP\_DUR registers is configured like this to ignore events that are shorter than  $6/ODR\_XL = 6/412 \text{ Hz} \approx 15 \text{ msec}$  in order to avoid false detections.

### 5.3 Wake-up interrupt

The wake-up feature can be implemented using either the slope filter (see [Section 3.4.1 Accelerometer slope filter](#) for more details) or the high-pass digital filter, as illustrated in [Figure 2. Accelerometer filtering chain](#). The filter to be applied can be selected using the SLOPE\_FDS bit of the INT\_CFG0 register. If this bit is set to 0 (default value), the slope filter is used. If it is set to 1, the HPF digital filter is used. Moreover, it is possible to configure the wake-up feature as an absolute wake-up with respect to a programmable position. This can be done by setting both the SLOPE\_FDS bit of the INT\_CFG0 register and the USR\_OFF\_ON\_WU bit of the WAKE\_UP\_THS register to 1. Using this configuration, the input data for the wake-up function comes from the low-pass filter path and the programmable position is subtracted as an offset. The programmable position can be configured through the X\_OFS\_USR, Y\_OFS\_USR and Z\_OFS\_USR registers (refer to [Section 4.6 Accelerometer offset registers](#) for more details).

The wake-up interrupt signal is generated if a certain number of consecutive filtered data exceed the configured threshold ([Figure 13. Wake-up interrupt \(using the slope filter\)](#)).

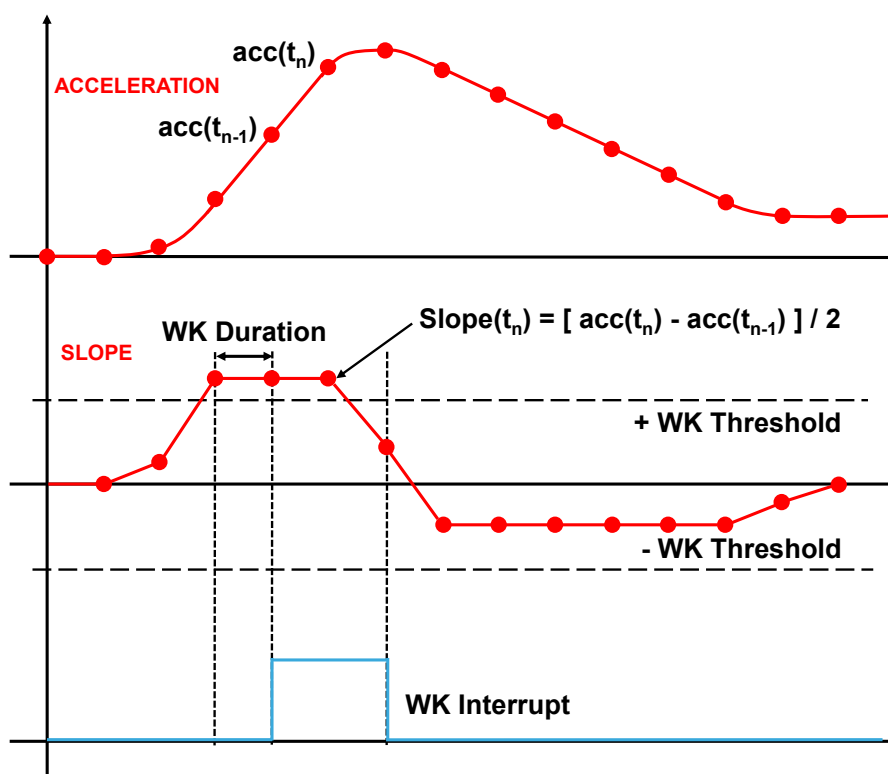
The unsigned threshold value is defined using the WK\_THS[5:0] bits of the WAKE\_UP\_THS register. The value of 1 LSB of these 6 bits depends on the selected accelerometer full scale and on the value of the WAKE\_THS\_W bit of the WAKE\_UP\_DUR register:

- If WAKE\_THS\_W = 0, 1 LSB =  $FS\_XL / 2^6$
- If WAKE\_THS\_W = 1, 1 LSB =  $FS\_XL / 2^8$

The threshold is applied to both positive and negative data. For wake-up interrupt generation, the absolute value of the filtered data must be bigger than the threshold.

The duration parameter defines the minimum duration of the wake-up event to be recognized. Its value is set using the WAKE\_DUR[1:0] bits of the WAKE\_UP\_DUR register: 1 LSB corresponds to  $1/ODR\_XL$  time, where ODR\_XL is the accelerometer output data rate. It is important to appropriately define the duration parameter to avoid unwanted wake-up interrupts due to spurious spikes of the input signal.

This interrupt signal can be enabled by setting the INTERRUPTS\_ENABLE bit in the INT\_CFG1 register to 1 and can be driven to the two interrupt pins by setting to 1 the INT1\_WU bit of the MD1\_CFG register or the INT2\_WU bit of the MD2\_CFG register. It can also be checked by reading the WU\_IA bit of the WAKE\_UP\_SRC or ALL\_INT\_SRC register. The X\_WU, Y\_WU, Z\_WU bits of the WAKE\_UP\_SRC register indicate which axes have triggered the wake-up event.

**Figure 13. Wake-up interrupt (using the slope filter)**


If latched mode is disabled (the LIR bit of INT\_CFG0 is set to 0), the interrupt signal is automatically reset when the filtered data falls below the threshold. If latched mode is enabled and the wake-up interrupt signal is driven to the interrupt pins, once a wake-up event has occurred and the interrupt pin is asserted, it must be reset by reading the WAKE\_UP\_SRC register or the ALL\_INT\_SRC register. The X\_WU, Y\_WU, Z\_WU bits are maintained at the state in which the interrupt was generated until the read is performed, and released at the next ODR cycle. In case the WU\_X, WU\_Y, WU\_Z bits have to be evaluated (in addition to the WU\_IA bit), it is recommended to directly read the WAKE\_UP\_SRC register (do not use the ALL\_INT\_SRC register for this specific case). If latched mode is enabled, but the interrupt signal is not driven to the interrupt pins, the latch feature does not take effect.

A basic software routine for wake-up event recognition using the high-pass digital filter is given below.

1. Write 60h to CTRL1\_XL // Turn on the accelerometer  
// ODR\_XL = 416 Hz, FS\_XL =  $\pm 2 g$
2. Write 51h to INT\_CFG0 // Enable latched mode with reset on read and digital high-pass filter
3. Write 80h to INT\_CFG1 // Enable interrupt function
4. Write 00h to WAKE\_UP\_DUR // No duration and selection of wake-up threshold weight (1 LSB =  $FS\_XL / 2^6$ )
5. Write 02h to WAKE\_UP\_THS // Set wake-up threshold
6. Write 20h to MD1\_CFG // Wake-up interrupt driven to INT1 pin

Since the duration time is set to zero, the wake-up interrupt signal is generated for each X,Y,Z filtered data exceeding the configured threshold. The WK\_THS field of the WAKE\_UP\_THS register is set to 000010, therefore the wake-up threshold is 62.5 mg ( $= 2 * FS\_XL / 2^6$ ).

If the wake-up functionality is implemented using the slope/high-pass digital filter, it is necessary to consider the settling time of the filter just after this functionality is enabled. For example, when using the slope filter (but a similar consideration can be done for the high-pass digital filter usage) the wake-up functionality is based on the comparison of the threshold value with half of the difference of the acceleration of the current (x,y,z) sample and the previous one (refer to [Section 3.4.1 Accelerometer slope filter](#)).

At the very first sample, the slope filter output is calculated as half of the difference of the current sample [for example, (x,y,z) = (0,0,1g)] with the previous one which is (x,y,z)=(0,0,0) since it doesn't exist. For this reason, on the z-axis the first output value of the slope filter is  $(1g - 0)/2 = 500 \text{ mg}$  and it could be higher than the threshold value in which case a spurious interrupt event is generated. The interrupt signal is kept high for 1 ODR then it goes low.

In order to avoid this spurious interrupt generation, multiple solutions are possible. Hereafter are three alternative solutions (for the slope filter case):

- a.** Ignore the first generated wake-up signal.
- b.** Add a wait time higher than 1 ODR before driving the interrupt signal to the INT1/2 pin.
- c.** Initially set a higher ODR (833 Hz) so the first two samples are generated in a shorter period of time, reducing the slope filter latency time, then set the desired ODR (for example, 12.5 Hz) and drive the interrupt signal on the pin, as indicated in the procedure below.

1. Write 00h to WAKE\_UP\_DUR      // No duration and selection of wake-up threshold weight (1 LSB =  $FS\_XL / 2^6$ )
2. Write 02h to WAKE\_UP\_THS      // Set wake-up threshold
3. Write 51h to INT\_CFG0      // Enable interrupts and apply slope filter; latched mode disabled
4. Write 80h to INT\_CFG1      // Enable interrupt function
5. Write 70h to CTRL1\_XL      // Turn on the accelerometer  
    // ODR\_XL = 833 Hz, FS\_XL =  $\pm 2 \text{ g}$
6. Wait 4 ms      // Insert (reduced) wait time
7. Write 10h to CTRL1\_XL      // ODR\_XL = 12.5 Hz
8. Write 20h to MD1\_CFG      // Wake-up interrupt driven to INT1 pin



## 5.4 6D/4D orientation detection

The device provides the capability to detect the orientation of the device in space, enabling easy implementation of energy-saving procedures and automatic image rotation for mobile devices.

### 5.4.1 6D orientation detection

Six orientations of the device in space can be detected. The interrupt signal is asserted when the device switches from one orientation to another. The interrupt is not reasserted as long as the position is maintained.

6D interrupt is generated when, for two consecutive samples, only one axis exceeds a selected threshold and the acceleration values measured from the other two axes are lower than the threshold. The ZH, ZL, YH, YL, XH, XL bits of the D6D\_SRC register indicate which axis has triggered the 6D event.

In more detail:

**Table 23. D6D\_SRC register**

b7	b6	b5	b4	b3	b2	b1	b0
DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	XH	XL

- D6D\_IA is set high when the device switches from one orientation to another.
- ZH (YH, XH) is set high when the face perpendicular to the Z (Y, X) axis is almost flat and the acceleration measured on the Z (Y, X) axis is positive and in the absolute value bigger than the threshold.
- ZL (YL, XL) is set high when the face perpendicular to the Z (Y, X) axis is almost flat and the acceleration measured on the Z (Y, X) axis is negative and in the absolute value bigger than the threshold.

The SIXD\_THS[1:0] bits of the THS\_6D register are used to select the threshold value used to detect the change in device orientation. The threshold values given in the following table are valid for each accelerometer full-scale value.

**Table 24. Threshold for 4D/6D function**

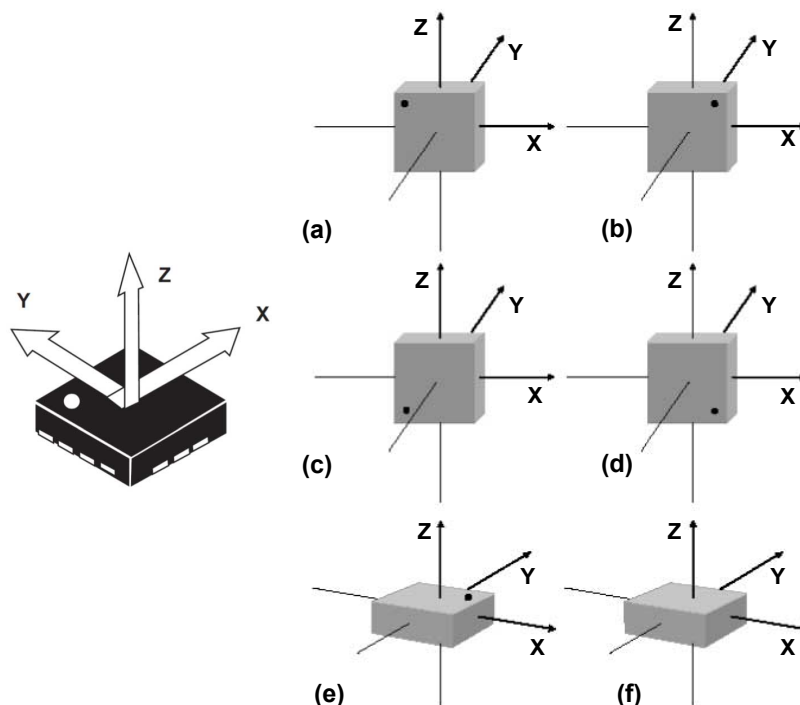
SIXD_THS[1:0]	Threshold value [degrees]
00	80
01	70
10	60
11	50

The low-pass filter LPF2 can also be used in 6D functionality by setting the LOW\_PASS\_ON\_6D bit of the CTRL8\_XL register to 1.

This interrupt signal can be enabled by setting the INTERRUPTS\_ENABLE bit in the INT\_CFG1 register to 1 and can be driven to the two interrupt pins by setting to 1 the INT1\_6D bit of the MD1\_CFG register or the INT2\_6D bit of the MD2\_CFG register. It can also be checked by reading the D6D\_IA bit of the D6D\_SRC register.

If latched mode is disabled (LIR bit of INT\_CFG0 is set to 0), the interrupt signal is active only for 1/ODR\_XL[s] then it is automatically disserted (ODR\_XL is the accelerometer output data rate). If latched mode is enabled and the 6D interrupt signal is driven to the interrupt pins, once an orientation change has occurred and the interrupt pin is asserted, a read of the D6D\_SRC or ALL\_INT\_SRC register clears the request and the device is ready to recognize a different orientation. The XL, XH, YL, YH, ZL, ZH bits are not affected by the LIR configuration. They correspond to the current state of the device when the D6D\_SRC register is read. If latched mode is enabled but the interrupt signal is not driven to the interrupt pins, the latch feature does not take effect.

Referring to the six possible cases illustrated in [Figure 14. 6D recognized orientations](#), the content of the D6D\_SRC register for each position is shown in [Table 25. D6D\\_SRC register in 6D positions](#).

**Figure 14. 6D recognized orientations**

**Table 25. D6D\_SRC register in 6D positions**

Case	D6D_IA	ZH	ZL	YH	YL	XH	XL
(a)	1	0	0	1	0	0	0
(b)	1	0	0	0	0	0	1
(c)	1	0	0	0	0	1	0
(d)	1	0	0	0	1	0	0
(e)	1	1	0	0	0	0	0
(f)	1	0	1	0	0	0	0

A basic SW routine for 6D orientation detection is as follows.

- Write 60h to CTRL1\_XL // Turn on the accelerometer  
// ODR\_XL = 416 Hz, FS\_XL =  $\pm 2 g$
- Write 41h to INT\_CFG0 // Enable latched mode with reset on read
- Write 80h to INT\_CFG1 // Enable interrupt function
- Write 40h to THS\_6D // Set 6D threshold (SIXD\_THS[1:0] = 10 = 60 degrees)
- Write 01h to CTRL8\_XL // Enable LPF2 filter to 6D functionality
- Write 04h to MD1\_CFG // 6D interrupt driven to INT1 pin

## 5.4.2 4D orientation detection

The 4D direction function is a subset of the 6D function especially defined to be implemented in mobile devices for portrait and landscape computation. It can be enabled by setting the D4D\_EN bit of the THS\_6D register to 1. In this configuration, the Z-axis position detection is disabled, therefore reducing position recognition to cases (a), (b), (c), and (d) of Table 25. D6D\_SRC register in 6D positions.

## 5.5 Activity/inactivity and motion/stationary recognition

The working principle of activity/inactivity and motion/stationary embedded functions is similar to wake-up. If no movement condition is detected for a programmable time, an inactivity/stationary condition event is generated. Otherwise, when the accelerometer data exceed the configurable threshold, an activity/motion condition event is generated.

When the activity/inactivity recognition function is activated, the device is able to automatically decrease the accelerometer sampling rate to 12.5 Hz and to automatically increase the accelerometer ODR and bandwidth as soon as the wake-up interrupt event has been detected. This feature can be extended to the gyroscope, with three possible options:

- Gyroscope configurations do not change.
- Gyroscope enters in sleep mode.
- Gyroscope enters in power-down mode.

With this feature the system may be efficiently switched from low-power consumption (accelerometer-only mode) to full performance and vice versa depending on user-selectable acceleration events, thus ensuring power saving and flexibility.

The activity/inactivity recognition function is enabled by setting the INTERRUPTS\_ENABLE bit to 1 and configuring the INACT\_EN[1:0] bits of the INT\_CFG1 register. If the INACT\_EN[1:0] bits of the INT\_CFG1 register are equal to 00, the motion/stationary embedded function is enabled. Possible configurations of the inactivity event are summarized in the following table.

**Table 26. Inactivity event configuration**

INACT_EN[1:0]	Accelerometer	Gyroscope
00	Inactivity event disabled	Inactivity event disabled
01	XL ODR = 12.5 Hz	Gyroscope configuration unchanged
10	XL ODR = 12.5 Hz	Gyroscope in sleep mode
11	XL ODR = 12.5 Hz	Gyroscope in power-down mode

The activity/inactivity and motion/stationary recognition functions can be implemented using either the slope filter (see Section 3.4.1 Accelerometer slope filter for more details) or the high-pass digital filter, as illustrated in Figure 2. Accelerometer filtering chain. The filter to be applied can be selected using the SLOPE\_FDS bit of the INT\_CFG1 register. If this bit is set to 0 (default value), the slope filter is used. If it is set to 1, the high-pass digital filter is used.

This function can be fully programmed by the user in terms of expected amplitude and timing of the filtered data by means of a dedicated set of registers (Figure 15. Activity/inactivity recognition (using the slope filter)).

The unsigned threshold value is defined using the WK\_THS[5:0] bits of the WAKE\_UP\_THS register. The value of 1 LSB of these 6 bits depends on the selected accelerometer full scale and on the value of the WAKE\_THS\_W bit of the WAKE\_UP\_DUR register:

- If WAKE\_THS\_W = 0, 1 LSB =  $FS_{XL} / 2^6$
- If WAKE\_THS\_W = 1, 1 LSB =  $FS_{XL} / 2^8$

The threshold is applied to both positive and negative filtered data.

When a certain number of consecutive X,Y,Z filtered data is smaller than the configured threshold, the ODR\_XL[3:0] bits of the CTRL1\_XL register are bypassed (inactivity) and the accelerometer is internally set to 12.5 Hz although the content of CTRL1\_XL is left untouched. The gyroscope behavior varies according to the configuration of the INACT\_EN[1:0] bits of the INT\_CFG1 register. The duration of the Inactivity status to be recognized is defined by the SLEEP\_DUR[3:0] bits of the WAKE\_UP\_DUR register: 1 LSB corresponds to  $512/ODR_{XL}$  time, where  $ODR_{XL}$  is the accelerometer output data rate. If the SLEEP\_DUR[3:0] bits are set to 0000, the duration of the inactivity status to be recognized is equal to  $16 / ODR_{XL}$  time.

When the inactivity status is detected, the interrupt is set high for  $1/\text{ODR\_XL[s]}$  period then it is automatically deasserted.

When filtered data on one axis becomes bigger than the threshold for a configurable time, the CTRL1\_XL register settings are immediately restored (activity) and the gyroscope is restored to the previous state. The duration of the activity status to be recognize is defined by the WAKE\_DUR[1:0] bits of the WAKE\_UP\_DURATION register. 1 LSB corresponds to  $1 / \text{ODR\_XL}$  time, where ODR\_XL is the accelerometer output data rate.

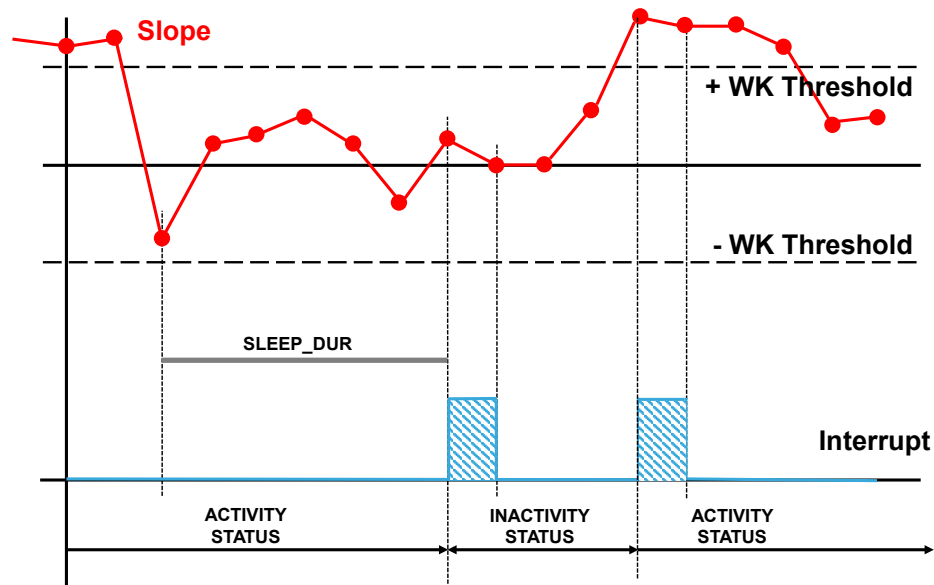
When the activity status is detected, the interrupt is set high for  $1/\text{ODR\_XL[s]}$  period then it is automatically deasserted.

Once the activity/inactivity detection function is enabled, the status can be driven to the two interrupt pins by setting to 1 the INT1\_SLEEP\_CHANGE bit of the MD1\_CFG register or the INT2\_SLEEP\_CHANGE bit of the MD2\_CFG register. It can also be checked by reading the SLEEP\_CHANGE\_IA bit of the WAKE\_UP\_SRC or ALL\_INT\_SRC register.

The SLEEP\_CHANGE\_IA bit is by default in pulsed mode. Latched mode can be selected by setting the LIR bit of the INT\_CFG0 register to 1 and the the INT1\_SLEEP\_CHANGE of the MD1\_CFG register or INT2\_SLEEP\_CHANGE of the MD2\_CFG register to 1. The SLEEP\_STATE bit of the WAKE\_UP\_SRC register is not affected by the LIR configuration. It corresponds to the current state of the device when the WAKE\_UP\_SRC register is read.

By setting the SLEEP\_STATUS\_ON\_INT bit of the INT\_CFG0 register to 1, the signal routed to the INT1 or INT2 pins is configured to be the activity/inactivity state (SLEEP\_STATE bit of WAKE\_UP\_SRC register) instead of the sleep-change signal. It goes high during inactivity state and it goes low during activity state. Latched mode is not supported in this configuration.

Figure 15. Activity/inactivity recognition (using the slope filter)



A basic software routine for activity/inactivity detection is as follows:

1. Write 50h to CTRL1\_XL // Turn on the accelerometer  
// ODR\_XL = 208 Hz, FS\_XL =  $\pm 2 g$
2. Write 40h to CTRL2\_G // Turn on the gyroscope  
// ODR\_G = 104 Hz, FS\_G =  $\pm 250 dps$
3. Write 02h to WAKE\_UP\_DUR // Set duration for Inactivity detection  
// Select activity/inactivity threshold resolution and duration
4. Write 02h to WAKE\_UP\_THS // Set activity/inactivity threshold
5. Write 00h to INT\_CFG0 // Select sleep-change notification  
// Select slope filter
6. Write E0h to INT\_CFG1 // Enable interrupt  
// Inactivity configuration: accelerometer to 12.5 Hz  
// Gyroscope to power-down mode
7. Write 80h to MD1\_CFG // Activity/inactivity interrupt driven to INT1 pin

In this example the WK\_THS field of the WAKE\_UP\_THS register is set to 000010, therefore the activity/inactivity threshold is 62.5 mg ( $= 2 * FS\_XL / 2^6$  since the WAKE\_THS\_W bit of the WAKE\_UP\_DUR register is set to 0).

Before inactivity detection, the X,Y,Z slope data must be smaller than the configured threshold for a period of time defined by the SLEEP\_DUR field of the WAKE\_UP\_DUR register. This field is set to 0010, corresponding to 4.92 s ( $= 2 * 512 / ODR\_XL$ ). After this period of time has elapsed, the accelerometer ODR is internally set to 12.5 Hz and the gyroscope is internally set to power-down mode.

The activity status is detected and the CTRL1\_XL register settings are immediately restored and the gyroscope is turned on as soon as the slope data of (at least) one axis are bigger than the threshold for one sample, since the WAKE\_DUR[1:0] bits of the WAKE\_UP\_DUR register are configured to 00.

### 5.5.1 Stationary/motion detection

Stationary/motion detection is a particular case of the activity/inactivity functionality in which no ODR / power mode changes occur when a sleep condition (equivalent to a stationary condition) is detected. Stationary/motion detection is activated by setting the INACT\_EN[1:0] bits of the INT\_CFG1 register to 00.

## 5.6 Boot status

After the device is powered up, it performs a 10 ms (maximum) boot procedure to load the trimming parameters. After the boot is completed, both the accelerometer and the gyroscope are automatically configured in power-down mode. During the boot time the registers are not accessible.

After power-up, the trimming parameters can be reloaded by setting the BOOT bit of the CTRL3\_C register to 1. No toggle of the device power lines is required and the content of the device control registers is not modified, so the device operating mode does not change after boot. If the reset to the default value of the control registers is required, it can be performed by setting the SW\_RESET bit of the CTRL3\_C register to 1. When this bit is set to 1, the following registers are reset to their default value:

- PIN\_CTRL (02h)
- FIFO\_CTRL1 (07h) through FIFO\_CTRL4 (0Ah)
- COUNTER\_BDR\_REG1 (0Bh) and COUNTER\_BDR\_REG2 (0Ch)
- INT1\_CTRL (0Dh) and INT2\_CTRL (0Eh)
- CTRL1\_XL (10h) through CTRL10\_C (19h)
- FIFO\_STATUS1 (3Ah) and FIFO\_STATUS2 (3Bh)
- INT\_CFG0 (56h) through MD2\_CFG (5Fh)
- X\_OFS\_USR (73h), Y\_OFS\_USR (74h) and Z\_OFS\_USR (75h)

The SW\_RESET procedure can take 50  $\mu$ s. The status of the reset is signaled by the status of the SW\_RESET bit of the CTRL3\_C register. Once the reset is completed, this bit is automatically set low.

The boot status signal is driven to the INT1 interrupt pin by setting the INT1\_BOOT bit of the INT1\_CTRL register to 1. This signal is set high while the boot is running and it is set low again at the end of the boot procedure.

The reboot flow is as follows:

1. Set both accelerometer and gyroscope in power-down mode.
2. Set the INT1\_BOOT bit of the INT1\_CTRL register to 1 [optional].
3. Set the BOOT bit of the CTRL3\_C register to 1.
4. Monitor the reboot status, there are three possibilities:
  - a. Wait 10 ms.
  - b. Monitor the INT1 pin until it returns to 0 (step 2. is mandatory in this case).
  - c. Poll the BOOT bit of CTRL3\_C until it returns to 0.

Reset flow is as follows:

1. Set both the accelerometer and gyroscope in power-down mode.
2. Set the SW\_RESET bit of CTRL3\_C to 1.
3. Monitor the software reset status, there are two possibilities:
  - a. Wait 50  $\mu$ s.
  - b. Poll the SW\_RESET bit of CTRL3\_C until it returns to 0.

In order to avoid conflicts, the reboot, and the sw reset must not be executed at the same time (do not set to 1 at the same time both the BOOT bit and SW\_RESET bit of CTRL3\_C register). The above flows must be performed serially.

## 6 Timestamp

Together with sensor data the device can provide timestamp information.

To enable this functionality the `TIMESTAMP_EN` bit of the `CTRL10_C` register has to be set to 1. The time step count is given by the concatenation of the `TIMESTAMP3` & `TIMESTAMP2` & `TIMESTAMP1` & `TIMESTAMP0` registers and is represented as a 32-bit unsigned number. The nominal timestamp resolution is 25  $\mu$ s. It is possible to get the actual timestamp resolution value through the `FREQ_FINE[7:0]` bits of the `INTERNAL_FREQ_FINE` register, which contains the difference in percentage of the actual ODR (and timestamp rate) with respect to the nominal value.

$$t_{actual}[s] = \frac{1}{40000 \cdot (1 + 0.0015 \cdot FREQ\_FINE)}$$

Similarly, it is possible to get the actual output data rate by using the following formula:

$$ODR_{actual}[Hz] = \frac{6667 + 0.0015 \cdot FREQ\_FINE \cdot 6667}{ODR_{coeff}}$$

where the  $ODR_{coeff}$  values are indicated in the table below.

**Table 27.  $ODR_{coeff}$  values**

Selected ODR [Hz]	$ODR_{coeff}$
12.5	512
26	256
52	128
104	64
208	32
416	16
833	8
1667	4
3333	2
6667	1

If both the accelerometer and the gyroscope are in power-down mode, the timestamp counter does not work and the timestamp value is frozen at the last value.

When the maximum value 4294967295 LSB (equal to FFFFFFFFh) is reached corresponding to approximately 30 hours, the counter is automatically reset to 00000000h and continues to count. The timer count can be reset to zero at any time by writing the reset value AAh in the `TIMESTAMP2` register.

The `TIMESTAMP_ENDCOUNT` bit of the `ALL_INT_SRC` goes high 6.4 ms before the occurrence of a timestamp overrun condition. This flag is reset when the `ALL_INT_SRC` register is read. It is also possible to route this signal on the INT2 pin (75  $\mu$ s duration pulse) by setting the `INT2_TIMESTAMP` bit of `MD2_CFG` to 1.

The timestamp can be batched in FIFO (see [Section 7 First-in, first-out buffer](#) for details).

## 7 First-in, first-out buffer

In order to limit intervention by the host processor and facilitate post-processing data for event recognition, the ASM330LHH embeds a 3 KB first-in, first-out buffer (FIFO).

The FIFO can be configured to store the following data:

- Gyroscope sensor data
- Accelerometer sensor data
- Timestamp data
- Temperature sensor data

Saving the data in FIFO is based on FIFO words. A FIFO word is composed of:

- Tag, 1 byte
- Data, 6 bytes

Data can be retrieved from the FIFO through six dedicated registers, from address 79h to 7Eh: FIFO\_DATA\_OUT\_X\_L, FIFO\_DATA\_OUT\_X\_H, FIFO\_DATA\_OUT\_Y\_L, FIFO\_DATA\_OUT\_Y\_H, FIFO\_DATA\_OUT\_Z\_L, FIFO\_DATA\_OUT\_Z\_H.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO\_TAG field of the FIFO\_DATA\_OUT\_TAG register that allows recognizing the meaning of a word in FIFO. The applications have maximum flexibility in choosing the rate of batching for sensors with dedicated FIFO configurations.

Six different FIFO operating modes can be chosen through the FIFO\_MODE[2:0] bits of the FIFO\_CTRL4 register:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

To monitor the FIFO status (full, overrun, number of samples stored, and so forth), two dedicated registers are available: FIFO\_STATUS1 and FIFO\_STATUS2.

Programmable FIFO threshold can be set in FIFO\_CTRL1 and FIFO\_CTRL2 using the WTM[8:0] bits.

FIFO full, FIFO threshold, and FIFO overrun events can be enabled to generate dedicated interrupts on the two interrupt pins (INT1 and INT2) through the INT1\_FIFO\_FULL, INT1\_FIFO\_FTH and INT1\_FIFO\_OVR bits of the INT1\_CTRL register, and through the INT2\_FIFO\_FULL, INT2\_FIFO\_FTH and INT2\_FIFO\_OVR bits of the INT2\_CTRL register.



## 7.1 FIFO description and batched sensors

FIFO is divided into 512 words of 7 bytes each. A FIFO word contains one byte with TAG information and 6 bytes of data. The overall FIFO buffer dimension is equal to 3584 bytes and can contain 3072 bytes of data. The TAG byte contains the information indicating which data is stored in the FIFO data field and other useful information.

FIFO is runtime configurable. A meta-information tag can be enabled in order to notify the user if batched sensor configurations have changed.

Batched sensors can be classified in two different categories:

1. Main sensors, which are physical sensors:
  - a. Accelerometer sensor
  - b. Gyroscope sensor
2. Auxiliary sensors, which contain information of the status of the device:
  - a. Timestamp sensor
  - b. Configuration-change sensor (CFG-change)
  - c. Temperature sensor

Data can be retrieved from the FIFO through six dedicated registers: FIFO\_DATA\_OUT\_X\_L, FIFO\_DATA\_OUT\_X\_H, FIFO\_DATA\_OUT\_Y\_L, FIFO\_DATA\_OUT\_Y\_H, FIFO\_DATA\_OUT\_Z\_L, FIFO\_DATA\_OUT\_Z\_H.

Each write to FIFO is triggered by the internal data-ready signal (faster sensor between accelerometer and gyroscope).

## 7.2 FIFO registers

The FIFO buffer is managed by:

- Six control registers: FIFO\_CTRL1, FIFO\_CTRL2, FIFO\_CTRL3, FIFO\_CTRL4, COUNTER\_BDR\_REG1, COUNTER\_BDR\_REG2
- Two status registers: FIFO\_STATUS1 and FIFO\_STATUS2
- Seven output registers (tag + data): FIFO\_DATA\_OUT\_TAG, FIFO\_DATA\_OUT\_X\_L, FIFO\_DATA\_OUT\_X\_H, FIFO\_DATA\_OUT\_Y\_L, FIFO\_DATA\_OUT\_Y\_H, FIFO\_DATA\_OUT\_Z\_L, FIFO\_DATA\_OUT\_Z\_H
- Some additional bits to route FIFO events to the two interrupt lines: INT1\_CNT\_BDR, INT1\_FIFO\_FULL, INT1\_FIFO\_OVR, INT1\_FIFO\_TH bits of the INT1\_CTRL register and INT2\_CNT\_BDR, INT2\_FIFO\_FULL, INT2\_FIFO\_OVR, INT2\_FIFO\_TH bits of the INT2\_CTRL register

### 7.2.1 FIFO\_CTRL1

The FIFO\_CTRL1 register contains the lower part of the 9-bit FIFO watermark threshold level. For the complete watermark threshold level configuration, consider also the WTM8 bit of the FIFO\_CTRL2 register. 1 LSB value of the FIFO threshold level is referred to as a FIFO word (7 bytes).

The FIFO watermark flag (FIFO\_WTM\_IA bit in the FIFO\_STATUS2 register) rises when the number of bytes stored in the FIFO is equal to or higher than the watermark threshold level.

In order to limit the FIFO depth to the watermark level, the STOP\_ON\_WTM bit must be set to 1 in the FIFO\_CTRL2 register.

**Table 28. FIFO\_CTRL1 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

### 7.2.2 FIFO\_CTRL2

**Table 29. FIFO\_CTRL2 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOP_ON_WTM	0	0	ODRCHG_EN	0	0	0	WTM8

The FIFO\_CTRL2 register contains the upper part of the 9-bit FIFO watermark threshold level (WTM8 bit). For the complete watermark threshold level configuration, consider also the WTM[7:0] bits of the FIFO\_CTRL1 register. The register contains the bit STOP\_ON\_WTM, which allows limiting the FIFO depth to the watermark level.

Moreover, the FIFO\_CTRL2 register contains the ODRCHG\_EN bit, which can be set to 1 in order to enable the CFG-change auxiliary sensor to be batched in FIFO (described in the next sections).

### 7.2.3 FIFO\_CTRL3

**Table 30. FIFO\_CTRL3 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0

The FIFO\_CTRL3 register contains the fields to select the write frequency in FIFO for accelerometer and gyroscope sensor data. The selected batch data rate must be equal to or lower than the output data rate configured through the ODR\_XL and ODR\_G fields of the CTRL1\_XL and CTRL2\_G registers.

The following tables indicate all the selectable batch data rates.

**Table 31. Accelerometer batch data rate**

BDR_XL[3:0]	Batch data rate [Hz]
0000	Not batched in FIFO
0001	12.5
0010	26
0011	52
0100	104
0101	208
0110	416
0111	833
1000	1667
1001	3333
1010	6667

**Table 32. Gyroscope batch data rate**

BDR_GY[3:0]	Batch data rate [Hz]
0000	Not batched in FIFO
0001	12.5
0010	26
0011	52
0100	104
0101	208
0110	416
0111	833
1000	1667
1001	3333
1010	6667
1011	6.5

## 7.2.4 FIFO\_CTRL4

The FIFO\_CTRL4 register contains the fields to select the decimation factor for timestamp batching in FIFO and the batch data rate for the temperature sensor.

The timestamp write rate is configured to the maximum rate between the accelerometer and gyroscope batch data rate divided by the decimation factor specified in the DEC\_TS\_BATCH\_[1:0] field. The programmable decimation factors are indicated in the table below.

**Table 33. Timestamp batch data rate**

DEC_TS_BATCH[1:0]	Timestamp batch data rate [Hz]
00	Not batched in FIFO
01	$\max(\text{BDR\_GY}[\text{Hz}], \text{BDR\_XL}[\text{Hz}])$
10	$\max(\text{BDR\_GY}[\text{Hz}], \text{BDR\_XL}[\text{Hz}]) / 8$
11	$\max(\text{BDR\_GY}[\text{Hz}], \text{BDR\_XL}[\text{Hz}]) / 32$

The temperature batch data rate is configurable through the ODR\_T\_BATCH\_[1:0] field as shown in the table below.

**Table 34. Temperature sensor batch data rate**

ODR_T_BATCH[1:0]	Temperature batch data rate [Hz]
00	Not batched in FIFO
01	1.6
10	12.5
11	52

The FIFO\_CTRL4 register also contains the FIFO operating modes bits. FIFO operating modes are described in [Section 7.6 FIFO modes](#).

**Table 35. FIFO\_CTRL4 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEC_TS_BATCH_1	DEC_TS_BATCH_0	ODR_T_BATCH_1	ODR_T_BATCH_0	0	FIFO_MODE2	FIFO_MODE1	FIFO_MODE0

### 7.2.5 COUNTER\_BDR\_REG1

Since the FIFO might contain temperature data, timestamp data and meta-information (that is, CFG-change sensor), the FIFO provides a way to synchronize reading FIFO on the basis of the accelerometer or gyroscope actual number of samples stored in FIFO: the BDR counter.

The BDR counter can be configured through the COUNTER\_BDR\_REG1 and COUNTER\_BDR\_REG2 registers.

**Table 36. COUNTER\_BDR\_REG1 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	RST_COUNTER_BDR	TRIG_COUNTER_BDR	0	0	0	CNT_BDR_TH_9	CNT_BDR_TH_8

RST\_COUNTER\_BDR can be asserted to reset the BDR counter. It is automatically reset to zero.

TRIG\_COUNTER\_BDR selects the trigger for the BDR counter. If it is configured to 0, the accelerometer sensor is selected, otherwise the gyroscope sensor is selected.

The user can select the threshold which generates the COUNTER\_BDR\_IA event in the FIFO\_STATUS2 register. Once the internal BDR counter reaches the threshold, the COUNTER\_BDR\_IA bit is set to 1. The threshold is configurable through the CNT\_BDR\_TH[9:0] bits. The upper part of the field is contained in the COUNTER\_BDR\_REG1 register. 1 LSB value of the CNT\_BDR\_TH threshold level is referred to as one accelerometer/gyroscope sample (X, Y, and Z data).

### 7.2.6 COUNTER\_BDR\_REG2

The COUNTER\_BDR\_REG2 register contains the lower part of the BDR-counter threshold.

**Table 37. COUNTER\_BDR\_REG2 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT_BDR_TH_7	CNT_BDR_TH_6	CNT_BDR_TH_5	CNT_BDR_TH_4	CNT_BDR_TH_3	CNT_BDR_TH_2	CNT_BDR_TH_1	CNT_BDR_TH_0

### 7.2.7 FIFO\_STATUS1

The FIFO\_STATUS1 register, together with the FIFO\_STATUS2 register, provides information about the number of samples stored in the FIFO. 1 LSB value of the DIFF\_FIFO level is referred to as a FIFO word (7 bytes).

**Table 38. FIFO\_STATUS1 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIFF_FIFO_7	DIFF_FIFO_6	DIFF_FIFO_5	DIFF_FIFO_4	DIFF_FIFO_3	DIFF_FIFO_2	DIFF_FIFO_1	DIFF_FIFO_0

**7.2.8**
**FIFO\_STATUS2**

The FIFO\_STATUS2 register, together with the FIFO\_STATUS1 register, provides information about the number of samples stored in the FIFO and about the current status (watermark, overrun, full, BDR counter) of the FIFO buffer.

**Table 39. FIFO\_STATUS2 register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO_WTM_IA	FIFO_OVR_IA	FIFO_FULL_IA	COUNTER_BDR_IA	FIFO_OVR_LATCHED	0	DIFF_FIFO_9	DIFF_FIFO_8

- FIFO\_WTM\_IA represents the watermark status. This bit goes high when the number of FIFO words (7 bytes each) already stored in the FIFO is equal to or higher than the watermark threshold level. The watermark status signal can be driven to the two interrupt pins by setting to 1 the INT1\_FIFO\_TH bit of the INT1\_CTRL register or the INT2\_FIFO\_TH bit of the INT2\_CTRL register.
- FIFO\_OVR\_IA goes high when the FIFO is completely filled and at least one sample has already been overwritten to store the new data. This signal can be driven to the two interrupt pins by setting to 1 the INT1\_FIFO\_OVR bit of the INT1\_CTRL register or the INT2\_FIFO\_OVR bit of the INT2\_CTRL register.
- FIFO\_FULL\_IA goes high when the next set of data that is stored in FIFO makes the FIFO completely full (that is, DIFF\_FIFO\_9 = 1) or generate a FIFO overrun. This signal can be driven to the two interrupt pins by setting to 1 the INT1\_FIFO\_FULL bit of the INT1\_CTRL register or the INT2\_FIFO\_FULL bit of the INT2\_CTRL register.
- COUNTER\_BDR\_IA represents the BDR-counter status. This bit goes high when the number of accelerometer or gyroscope batched samples reaches the BDR-counter threshold level configured through the CNT\_BDR\_TH [9:0] bits of the COUNTER\_BDR\_REG1 and COUNTER\_BDR\_REG2 registers. The COUNTER\_BDR\_IA bit is automatically reset when the FIFO\_STATUS2 register is read. The BDR-counter status can be driven to the two interrupt pins by setting to 1 the INT1\_CNT\_BDR bit of the INT1\_CTRL register or the INT2\_CNT\_BDR bit of the INT2\_CTRL register.
- FIFO\_OVR\_LATCHED, as FIFO\_OVR\_IA, goes high when the FIFO is completely filled and at least one sample has already been overwritten to store the new data. The difference between the two flags is that FIFO\_OVR\_LATCHED is reset when the FIFO\_STATUS2 register is read, whereas the FIFO\_OVR\_IA is reset when at least one FIFO word is read. This allows detecting a FIFO overrun condition during reading data from FIFO.
- DIFF\_FIFO\_9[8] contains the upper part of the number of unread words stored in the FIFO. The lower part is represented by the DIFF\_FIFO\_7[0] bits in FIFO\_STATUS1. The value of the DIFF\_FIFO\_9[0] field corresponds to the number of 7-byte words in the FIFO.

Register content is updated synchronously to the FIFO write and read operations.

**Note:** *The BDU feature also acts on the FIFO\_STATUS1 and FIFO\_STATUS2 registers. When the BDU bit is set to 1, it is mandatory to read FIFO\_STATUS1 first and then FIFO\_STATUS2.*

### 7.2.9 FIFO\_DATA\_OUT\_TAG

By reading the FIFO\_DATA\_OUT\_TAG register, it is possible to understand to which sensor the data of the current reading belongs and to check if data are consistent.

**Table 40. FIFO\_DATA\_OUT\_TAG register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAG_SENSOR_4	TAG_SENSOR_3	TAG_SENSOR_2	TAG_SENSOR_1	TAG_SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_PARITY

- TAG\_SENSOR\_[4:0] field identifies the sensors stored in the 6 data bytes (Table 41).
- TAG\_CNT\_[1:0] field identifies the FIFO time slot (described in next sections).
- TAG\_PARITY bit recognizes if the content of the FIFO\_DATA\_OUT\_TAG register is corrupted.

The table below contains all the possible values and associated type of sensor for the TAG\_SENSOR\_[4:0] field.

**Table 41. TAG\_SENSOR field and associated sensor**

TAG_SENSOR_[4:0]	Sensor name	Sensor category	Description
0x01	Gyroscope	Main	Gyroscope data
0x02	Accelerometer	Main	Accelerometer data
0x03	Temperature	Auxiliary	Temperature data
0x04	Timestamp	Auxiliary	Timestamp data
0x05	CFG_Change	Auxiliary	Meta-information data

The TAG\_PARITY bit can be used to check the content of the FIFO\_DATA\_OUT\_TAG register. In order to do this, the user can implement the following routine:

1. Read the FIFO\_DATA\_OUT\_TAG register.
2. Count the number of bits equal to 1.
3. If the number of bits equal to 1 is even, then the FIFO\_DATA\_OUT\_TAG content is reliable, otherwise it is unreliable.

### 7.2.10 FIFO\_DATA\_OUT

Data can be retrieved from the FIFO through six dedicated registers, from address 79h to address 7Eh: FIFO\_DATA\_OUT\_X\_L, FIFO\_DATA\_OUT\_X\_H, FIFO\_DATA\_OUT\_Y\_L, FIFO\_DATA\_OUT\_Y\_H, FIFO\_DATA\_OUT\_Z\_L, FIFO\_DATA\_OUT\_Z\_H.

The FIFO output registers content depends on the sensor category and type, as described in the next section.

## 7.3 FIFO batched sensors

As previously described, batched sensors can be classified in two different categories:

1. Main sensors
2. Auxiliary sensors

In the following sections, all the details about each category are presented.

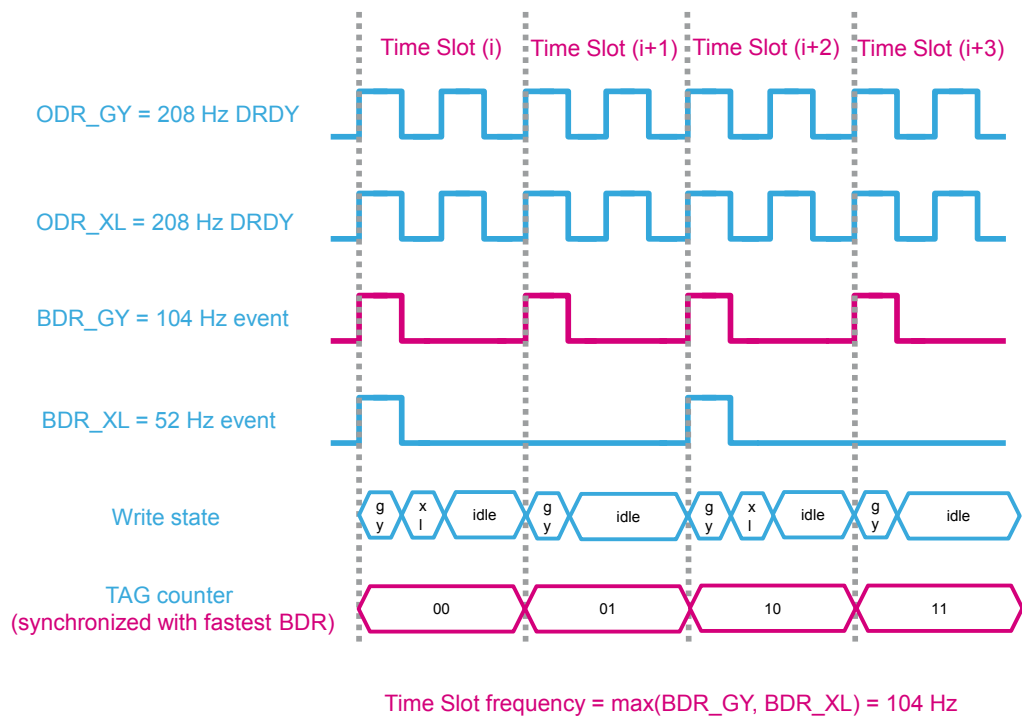
## 7.4 Main sensors

Main sensors are ASM330LHH device physical sensors: accelerometer and gyroscope. The batch data rate can be configured through the BDR\_XL[3:0] and BDR\_GY[3:0] fields of the FIFO\_CTRL3 register. The batch data rate must be equal to or lower than the relative sensor output data rate configured through the ODR\_XL[3:0] and ODR\_G[3:0] field of the CTRL1\_XL and CTRL2\_G registers.

The main sensors define the FIFO time base. This means that each one of the other sensors can be associated to a time base slot defined by the main sensors. A batch event of the fastest main sensor also increments the TAG counter (TAG\_CNT field of the FIFO\_DATA\_OUT\_TAG register). This counter is composed of two bits and its value is continuously incremented (from 00 to 11) to identify different time slots.

An example of a batch data rate event is shown in Figure 16. Main sensors and time slot definitions. The BDR\_GY event and BDR\_XL event identify the time in which the corresponding sensor data is written to the FIFO. The evolution of the TAG counter identifies different time slots and its frequency is equivalent to the maximum value between BDR\_XL and BDR\_GY.

**Figure 16. Main sensors and time slot definitions**



The FIFO word format of the main sensors is presented in the table below, representing the device addresses from 78h to 7Eh.

**Table 42. Main sensors output data format in FIFO**

TAG	X_L	X_H	Y_L	Y_H	Z_L	Z_H
-----	-----	-----	-----	-----	-----	-----



## 7.5 Auxiliary sensors

Auxiliary sensors are considered as service sensors for the main sensors. Auxiliary sensors include the:

- Temperature sensor (ODR\_T\_BATCH\_[1:0] bits of the FIFO\_CTRL4 register must be configured properly).
- Timestamp sensor: it stores the timestamp corresponding to a FIFO time slot (TIMESTAMP\_EN bit of the CTRL10\_C register must be set to 1 and the DEC\_TS\_BATCH\_[1:0] bits of the FIFO\_CTRL4 register must be configured properly).
- CFG-change sensor: it identifies a change in some configuration of the device (ODRCHG\_EN bit of the FIFO\_CTRL2 register must be set to 1).

Auxiliary sensors cannot trigger a write in FIFO. Their registers are written when the first main sensor event occurs (even if they are configured at a higher batch data rate).

The temperature output data format in FIFO is presented in the following table.

**Table 43. Temperature output data format in FIFO**

Data	FIFO_DATA_OUT registers
TEMPERATURE[7:0]	FIFO_DATA_OUT_X_L
TEMPERATURE[15:8]	FIFO_DATA_OUT_X_H
0	FIFO_DATA_OUT_Y_L
0	FIFO_DATA_OUT_Y_H
0	FIFO_DATA_OUT_Z_L
0	FIFO_DATA_OUT_Z_H

The timestamp output data format in FIFO is presented in the following table.

**Table 44. Timestamp output data format in FIFO**

Data	FIFO_DATA_OUT registers
TIMESTAMP[7:0]	FIFO_DATA_OUT_X_L
TIMESTAMP[15:8]	FIFO_DATA_OUT_X_H
TIMESTAMP[23:16]	FIFO_DATA_OUT_Y_L
TIMESTAMP[31:24]	FIFO_DATA_OUT_Y_H
0	FIFO_DATA_OUT_Z_L[3:0]
0	FIFO_DATA_OUT_Z_L[7:4]
BDR_XL	FIFO_DATA_OUT_Z_H[3:0]
BDR_GY	FIFO_DATA_OUT_Z_H[7:4]

As shown in Table 44, timestamp data contain also some meta-information which can be used to detect a BDR change if the CFG-change sensor is not batched in FIFO: the batch data rate of the main sensors.

CFG-change identifies a runtime change in the output data rate, the batch data rate or other configurations of the main sensors. When a supported runtime change is applied, this sensor is written at the first new main sensor event followed by a timestamp sensor (also if the timestamp sensor is not batched).

This sensor can be used to correlate data from the sensors to the device timestamp without storing the timestamp each time. It could be used also to notify the user to discard data due to embedded filters settling or to other configuration changes (that is, switching mode, output data rate, ...).

The CFG-change output data format in FIFO is presented in the following table.

**Table 45. CFG-change output data format in FIFO**

Data	FIFO_DATA_OUT registers
LPF1_SEL_G	FIFO_DATA_OUT_X_H[0]
FTYPE[2:0]	FIFO_DATA_OUT_X_H[3:1]
0	FIFO_DATA_OUT_X_H[4]
FS_125	FIFO_DATA_OUT_X_H[5]
FS[1:0]_G	FIFO_DATA_OUT_X_H[7:6]
LPF2_XL_EN	FIFO_DATA_OUT_Y_L[0]
HPCF_XL[2:0]	FIFO_DATA_OUT_Y_L[3:1]
0	FIFO_DATA_OUT_Y_L[4]
0	FIFO_DATA_OUT_Y_L[5]
FS[1:0]_XL	FIFO_DATA_OUT_Y_L[7:6]
0	FIFO_DATA_OUT_Y_H[3:0]
0	FIFO_DATA_OUT_Y_H[5]
Gyroscope startup <sup>(1)</sup>	FIFO_DATA_OUT_Y_H[6]
0	FIFO_DATA_OUT_Y_H[7]
ODR_XL	FIFO_DATA_OUT_Z_L[3:0]
ODR_GY	FIFO_DATA_OUT_Z_L[7:4]
BDR_XL	FIFO_DATA_OUT_Z_H[3:0]
BDR_GY	FIFO_DATA_OUT_Z_H[7:4]

1. Internal signal, which is deasserted when the gyroscope finishes the startup phase (max startup time is 70 ms).

## 7.6 FIFO modes

The ASM330LHH FIFO buffer can be configured to operate in six different modes, selectable through the FIFO\_MODE\_[2:0] field of the FIFO\_CTRL4 register. The available configurations ensure a high level of flexibility and extend the number of functions usable in application development.

Bypass, FIFO, continuous, continuous-to-FIFO, bypass-to-continuous, and bypass-to-FIFO modes are described in the following paragraphs.

### 7.6.1 Bypass mode

When bypass mode is enabled, the FIFO is not used, the buffer content is cleared, and it remains empty until another mode is selected. Bypass mode is selected when the FIFO\_MODE\_[2:0] bits are set to 000. Bypass mode must be used in order to stop and reset the FIFO buffer when a different mode is intended to be used. Note that by placing the FIFO buffer in bypass mode, the whole buffer content is cleared.

### 7.6.2 FIFO mode

In FIFO mode, the buffer continues filling until it becomes full. Then it stops collecting data and the FIFO content remains unchanged until a different mode is selected.

Follow these steps for FIFO mode configuration:

1. Enable the sensor data to be stored in FIFO with the corresponding batch data rate (if configurable).
2. Set the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 register to 001 to enable FIFO mode.

When this mode is selected, the FIFO starts collecting data. The FIFO\_STATUS1 and FIFO\_STATUS2 registers are updated according to the number of samples stored.

When the FIFO is full, the DIFF\_FIFO\_9 bit of the FIFO\_STATUS2 register is set to 1 and no more data are stored in the FIFO buffer. Data can be retrieved by reading all the FIFO\_DATA\_OUT (from 78h to 7Eh) registers for the number of times specified by the DIFF\_FIFO\_[9:0] bits of the FIFO\_STATUS1 and FIFO\_STATUS2 registers.

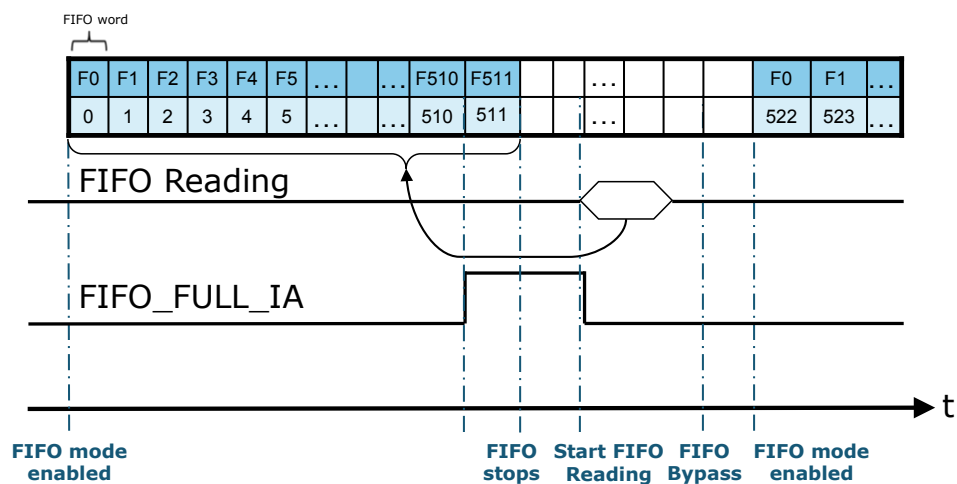
Using the FIFO\_WTM\_IA bit of the FIFO\_STATUS2 register, data can also be retrieved when a threshold level (WTM[8:0] in FIFO\_CTRL1 and FIFO\_CTRL2 registers) is reached if the application requires a lower number of samples in the FIFO.

If the STOP\_ON\_WTM bit of the FIFO\_CTRL2 register is set to 1, the FIFO size is limited to the value of the WTM[8:0] bits in the FIFO\_CTRL1 and FIFO\_CTRL2 registers. In this case, the FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register is set high when the number of samples in FIFO reaches or exceeds the WTM[8:0] value at the next FIFO write operation.

Communication speed is not very important in FIFO mode because the data collection is stopped and there is no risk of overwriting data already acquired. Before restarting the FIFO mode, it is necessary to set to bypass mode first in order to completely clear the FIFO content.

Figure 17. FIFO mode (STOP\_ON\_WTM = 0) shows an example of FIFO mode usage. The data from just one sensor are stored in the FIFO. In these conditions, the number of samples that can be stored in the FIFO buffer is 512. The FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register goes high just after the level labeled as 510 to notify that the FIFO buffer will be completely filled at the next FIFO write operation. After the FIFO is full (FIFO\_DIFF\_9 = 1), the data collection stops.

**Figure 17. FIFO mode (STOP\_ON\_WTM = 0)**



### 7.6.3 Continuous mode

In continuous mode, the FIFO continues filling. When the buffer is full, the FIFO index restarts from the beginning, and older data are replaced by the new data. The oldest values continue to be overwritten until a read operation frees FIFO slots. The host processor reading speed is important in order to free slots faster than new data is made available. To stop this configuration, bypass mode must be selected.

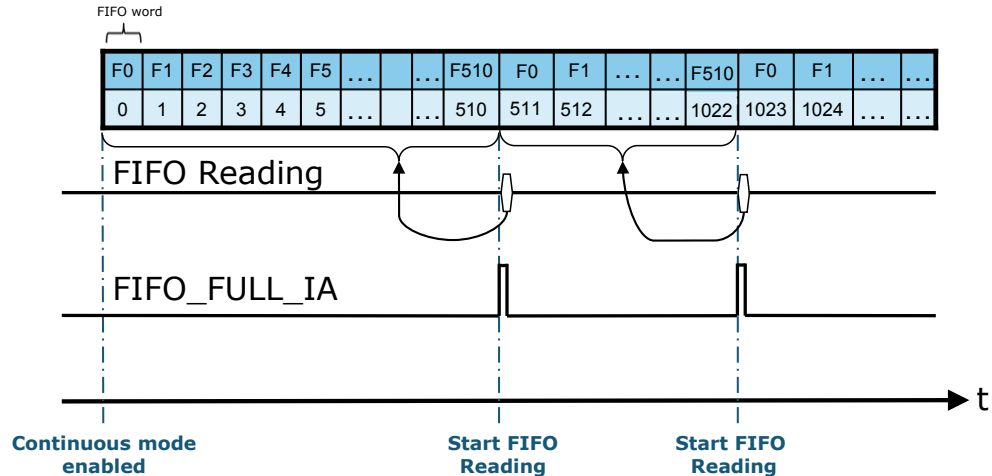
Follow these steps for continuous mode configuration (if the accelerometer/gyroscope data-ready is used as the FIFO trigger):

1. Enable the sensor data to be stored in FIFO with the corresponding batch data rate (if configurable).
2. Set the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 register to 110 to enable FIFO mode.

When this mode is selected, the FIFO collects data continuously. The FIFO\_STATUS1 and FIFO\_STATUS2 registers are updated according to the number of samples stored. When the next FIFO write operation makes the FIFO completely full or generates a FIFO overrun, the FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register goes to 1. The FIFO\_OVR\_IA and FIFO\_OVR\_LATCHED bits in the FIFO\_STATUS2 register indicates when at least one FIFO word has been overwritten to store the new data. Data can be retrieved after the FIFO\_FULL\_IA event by reading the FIFO\_DATA\_OUT (from 78h to 7Eh) registers for the number of times specified by the DIFF\_FIFO\_[9:0] bits in the FIFO\_STATUS1 and FIFO\_STATUS2 registers. Using the FIFO\_WTM\_IA bit of the FIFO\_STATUS2 register, data can also be retrieved when a threshold level (WTM[8:0] in the FIFO\_CTRL1 and FIFO\_CTRL2 registers) is reached. If the STOP\_ON\_WTM bit of the FIFO\_CTRL2 register is set to 1, the FIFO size is limited to the value of the WTM[8:0] bits in the FIFO\_CTRL1 and FIFO\_CTRL2 registers. In this case, the FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register goes high when the number of samples in FIFO reaches or surpasses the WTM[8:0] value at the next FIFO write operation.

**Figure 18. Continuous mode** shows an example of the continuous mode usage. In the example, data from just one sensor are stored in the FIFO and the FIFO samples are read on the FIFO\_FULL\_IA event and faster than 1 \* ODR so that no data is lost. In these conditions, the number of samples stored is 511.

**Figure 18. Continuous mode**



#### 7.6.4 Continuous-to-FIFO mode

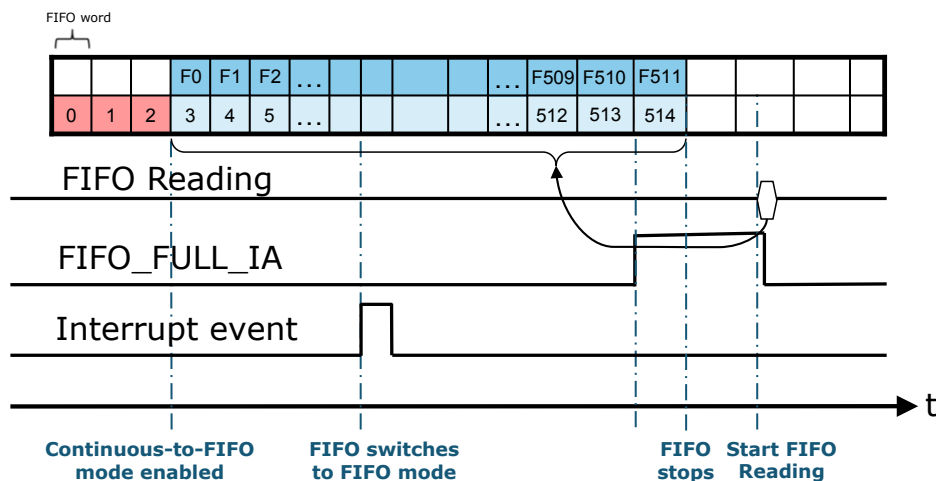
This mode is a combination of the continuous and FIFO modes previously described. In continuous-to-FIFO mode, the FIFO buffer starts operating in continuous mode and switches to FIFO mode when an event condition occurs.

The event condition can be one of the following:

- Free-fall: event detection has to be configured and the INT2\_FF bit of the MD2\_CFG register has to be set to 1.
- Wake-up: event detection has to be configured and the INT2\_WU bit of the MD2\_CFG register has to be set to 1.
- 6D: event detection has to be configured and the INT2\_6D bit of the MD2\_CFG register has to be set to 1.

Continuous-to-FIFO mode is sensitive to the edge of the interrupt signal. At the first interrupt event, FIFO changes from continuous mode to FIFO mode and maintains it until bypass mode is set.

**Figure 19. Continuous-to-FIFO mode**



Follow these steps for continuous-to-FIFO mode configuration (if the accelerometer/gyroscope data-ready is used as the FIFO trigger):

1. Configure one of the events as previously described.
2. Enable the sensor data to be stored in FIFO with the corresponding batch data rate (if configurable).
3. Set the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 register to 011 to enable FIFO continuous-to-FIFO mode.

In continuous-to-FIFO mode the FIFO buffer continues filling. When the FIFO is full or overrun at the next FIFO write operation, the FIFO\_FULL\_IA bit goes high.

If the STOP\_ON\_WTM bit of the FIFO\_CTRL2 register is set to 1, the FIFO size is limited to the value of the WTM[8:0] bits in the FIFO\_CTRL1 and FIFO\_CTRL2 registers. In this case, the FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register goes high when the number of samples in FIFO reaches or exceeds the WTM[8:0] value at the next FIFO write operation.

When the trigger event occurs, two different cases can be observed:

1. If the FIFO buffer is already full, it stops collecting data at the first sample after the event trigger. The FIFO content is composed of the samples collected before the event.
2. If FIFO buffer is not full yet, it continues filling until it becomes full and then it stops collecting data.

Continuous-to-FIFO can be used in order to analyze the history of the samples which have generated an interrupt. The standard operation is to read the FIFO content when the FIFO mode is triggered and the FIFO buffer is full and stopped.

### 7.6.5 Bypass-to-continuous mode

This mode is a combination of the bypass and continuous modes previously described. In bypass-to-continuous mode, the FIFO buffer starts operating in bypass mode and switches to continuous mode when an event condition occurs.

The event condition can be one of the following:

- Free-fall: event detection has to be configured and the INT2\_FF bit of the MD2\_CFG register has to be set to 1.
- Wake-up: event detection has to be configured and the INT2\_WU bit of the MD2\_CFG register has to be set to 1.
- 6D: event detection has to be configured and the INT2\_6D bit of the MD2\_CFG register has to be set to 1.

Bypass-to-continuous mode is sensitive to the edge of the interrupt signal. At the first interrupt event, FIFO changes from bypass mode to continuous mode and maintains it until bypass mode is set.

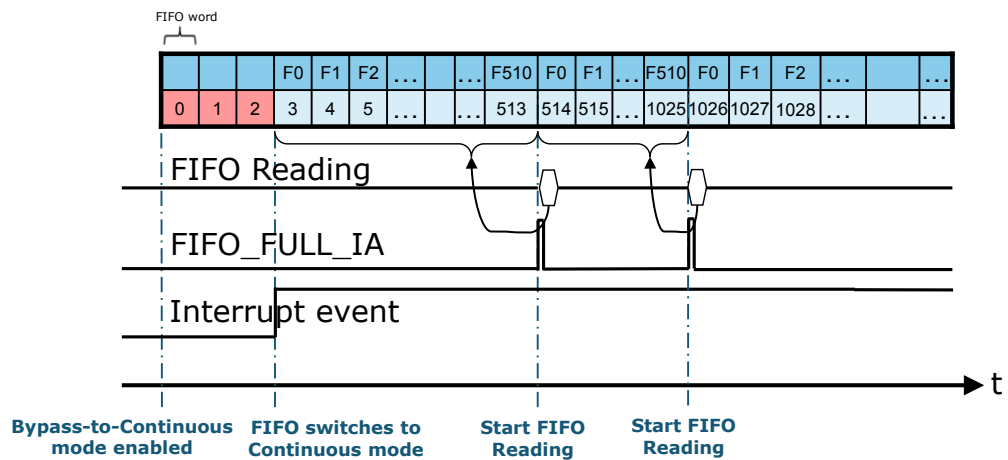
Follow these steps for bypass-to-continuous mode configuration (if the accelerometer / gyroscope data-ready is used as the FIFO trigger):

1. Configure one of the events as previously described.
2. Enable the sensor data to be stored in FIFO with the corresponding batch data rate (if configurable).
3. Set the FIFO\_MODE[2:0] bits in the FIFO\_CTRL4 register to 100 to enable FIFO bypass-to-continuous mode.

Once the trigger condition appears and the buffer switches to continuous mode, the FIFO buffer continues filling. When the next stored set of data makes the FIFO full or overrun, the FIFO\_FULL\_IA bit is set high.

Bypass-to-continuous can be used in order to start the acquisition when the configured interrupt is generated.

**Figure 20. Bypass-to-continuous mode**



### 7.6.6 Bypass-to-FIFO mode

This mode is a combination of the bypass and FIFO modes previously described. In bypass-to-FIFO mode, the FIFO buffer starts operating in bypass mode and switches to FIFO mode when an event condition occurs.

The event condition can be one of the following:

- Free-fall: event detection has to be configured and the INT2\_FF bit of the MD2\_CFG register has to be set to 1.
- Wake-up: event detection has to be configured and the INT2\_WU bit of the MD2\_CFG register has to be set to 1.
- 6D: event detection has to be configured and the INT2\_6D bit of the MD2\_CFG register has to be set to 1.

Bypass-to-FIFO mode is sensitive to the edge of the interrupt signal. At the first interrupt event, FIFO changes from bypass mode to FIFO mode and maintains it until bypass mode is set.

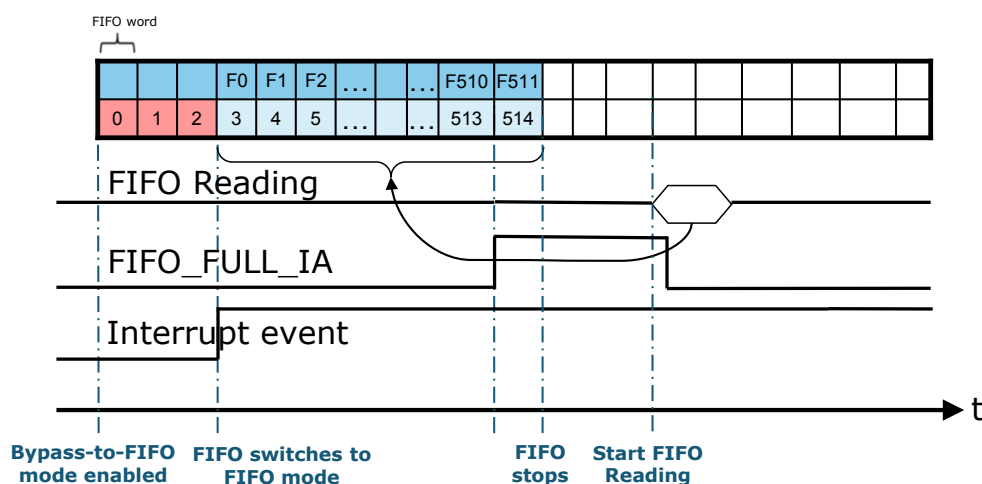
Follow these steps for bypass-to-FIFO mode configuration (if the accelerometer / gyroscope data-ready is used as the FIFO trigger):

1. Configure one of the events as previously described.
2. Enable the sensor data to be stored in FIFO with the corresponding batch data rate (if configurable).
3. Set the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 register to 111 to enable FIFO bypass-to-FIFO mode.

Once the trigger condition appears and the buffer switches to FIFO mode, the FIFO buffer starts filling. When the next stored set of data makes the FIFO full or overrun, the FIFO\_FULL\_IA bit is set high and the FIFO stops.

Bypass-to-FIFO can be used in order to analyze the history of the samples which have generated an interrupt.

**Figure 21. Bypass-to-FIFO mode**



### 7.6.7 Retrieving data from FIFO

When FIFO is enabled and the mode is different from Bypass, reading the FIFO output registers return the oldest FIFO sample set. Whenever these registers are read, their content is moved to the SPI/I<sup>2</sup>C output buffer.

FIFO slots are ideally shifted up one level in order to release room for a new sample, and the FIFO output registers load the current oldest value stored in the FIFO buffer.

The recommended way to retrieve data from the FIFO is the following:

1. Read the FIFO\_STATUS1 and FIFO\_STATUS2 registers to check how many words are stored in the FIFO. This information is contained in the DIFF\_FIFO\_[9:0] bits.
2. For each word in FIFO, read the FIFO word (tag and output data) and interpret it on the basis of the FIFO tag.
3. Go to step 1.

The entire FIFO content is retrieved by performing a certain number of read operations from the FIFO output registers until the buffer becomes empty (DIFF\_FIFO\_[9:0] bits of the FIFO\_STATUS1 and FIFO\_STATUS2 register are equal to 0).

It is recommended to avoid reading from FIFO when it is empty.

FIFO output data must be read with multiple of 7 bytes reads starting from the FIFO\_DATA\_OUT\_TAG register. The wraparound function from address FIFO\_DATA\_OUT\_Z\_H to FIFO\_DATA\_OUT\_TAG is done automatically in the device, in order to allow reading many words with a unique multiple read operation.



## 7.7 FIFO watermark threshold

The FIFO threshold is a functionality of the ASM330LHH FIFO which can be used to check when the number of samples in the FIFO reaches a defined watermark threshold level.

The bits WTM[8:0] in the FIFO\_CTRL1 and FIFO\_CTRL2 registers contain the watermark threshold level. The resolution of the WTM[8:0] field is 7 bytes, corresponding to a complete FIFO word. So, the user can select the desired level in a range between 0 and 511.

The bit FIFO\_WTM\_IA in the FIFO\_STATUS2 register represents the watermark status. This bit is set high if the number of words in the FIFO reaches or exceeds the watermark level. FIFO size can be limited to the threshold level by setting the STOP\_ON\_WTM bit in the FIFO\_CTRL2 register to 1.

Figure 22. FIFO threshold (STOP\_ON\_WTM = 0)

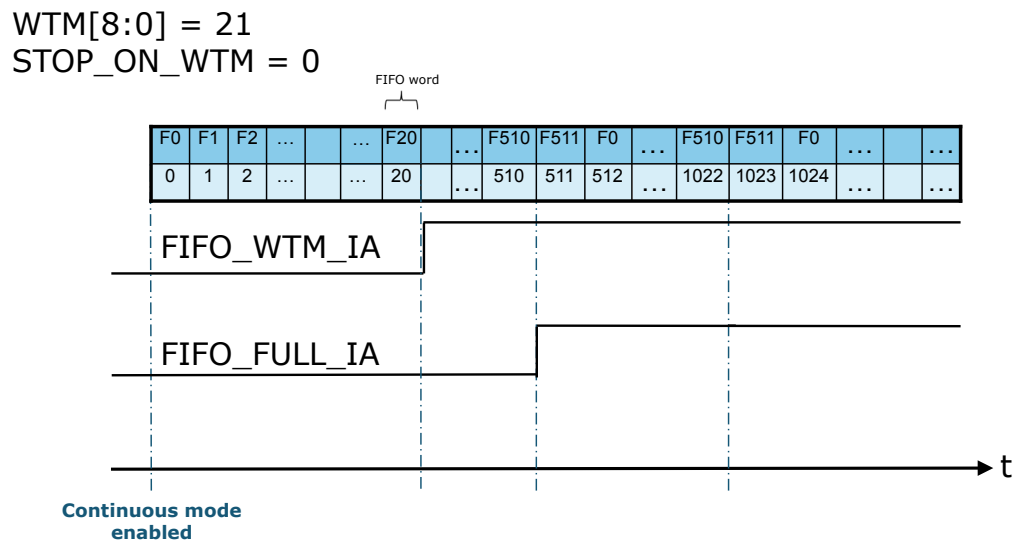


Figure 22. FIFO threshold (STOP\_ON\_WTM = 0) shows an example of FIFO threshold level usage when just accelerometer (or gyroscope) data are stored. The STOP\_ON\_WTM bit set to 0 in the FIFO\_CTRL2 register. The threshold level is set to 21 through the WTM[8:0] bits. The FIFO\_WTM\_IA bit of the FIFO\_STATUS2 register rises after the 21<sup>st</sup> level has been reached (21 words in the FIFO). Since the STOP\_ON\_WTM bit is set to 0, the FIFO does not stop at the 21<sup>st</sup> set of data, but keeps storing data until the FIFO\_FULL\_IA flag is set high.

Figure 23. FIFO threshold (STOP\_ON\_WTM = 1) in FIFO mode

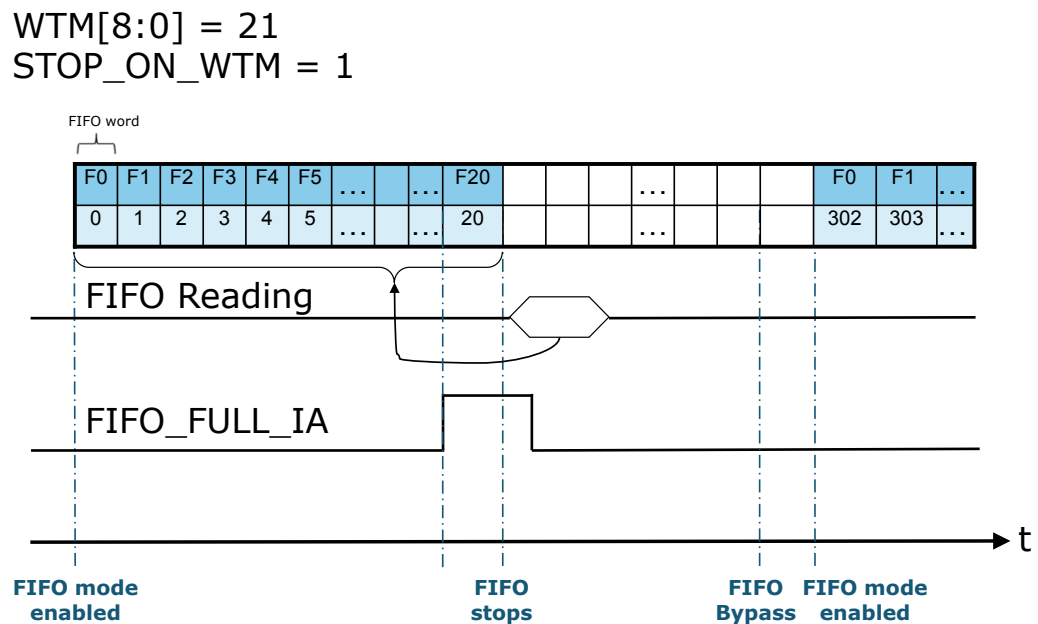


Figure 23. FIFO threshold (STOP\_ON\_WTM = 1) in FIFO mode shows an example of FIFO threshold level usage in FIFO mode with the STOP\_ON\_WTM bit set to 1 in the FIFO\_CTRL2 register. Just accelerometer (or gyroscope) data are stored in this example. The threshold level is set to 21 through the WTM[8:0] bits and defines the current FIFO size. In FIFO mode, data are stored in the FIFO buffer until the FIFO is full. The FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register rises when the next data stored in the FIFO generates the FIFO full or overrun condition. The FIFO\_WTM\_IA bit of the FIFO\_STATUS2 register goes high when the FIFO is full.

Figure 24. FIFO threshold (STOP\_ON\_WTM = 1) in continuous mode

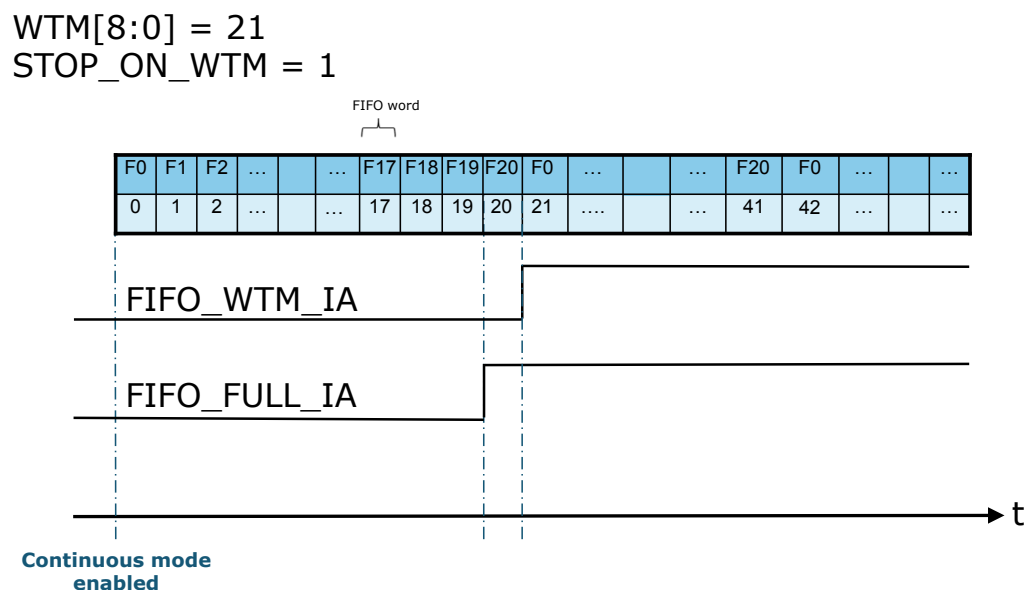


Figure 24. FIFO threshold (STOP\_ON\_WTM = 1) in continuous mode shows an example of FIFO threshold level usage in continuous mode with the STOP\_ON\_WTM bit set to 1 in the FIFO\_CTRL2 register. Just accelerometer (or gyroscope) data are stored in this example. The threshold level is set to 21 through the WTM[8:0] bits. The FIFO\_FULL\_IA bit of the FIFO\_STATUS2 register rises when the next data stored in the FIFO makes the FIFO full. The FIFO\_WTM\_IA bit of the FIFO\_STATUS2 goes high when the FIFO is full. If data are not retrieved from FIFO, new data (labeled as sample 21) overrides the older data stored in FIFO (labeled as sample F0).

## 7.8 Timestamp correlation

It is possible to reconstruct the timestamp of FIFO stream with three different approaches:

1. Basic, using only timestamp sensor information
2. Memory-saving, based on the TAG\_CNT field in FIFO\_DATA\_OUT\_TAG
3. Hybrid, based on combined usage of the TAG\_CNT field and decimated timestamp sensor

The basic approach guarantees the highest precision in timestamp reconstruction but wastes a lot of memory space available in FIFO. The timestamp sensor is written in FIFO at each time slot. If the overrun condition occurs, the correct procedure to retrieve the data from FIFO is to discard each data read before a new timestamp sensor.

The memory-saving approach uses only the TAG\_CNT information and, when the TAG\_CNT value increases, the timestamp stored at the software layer should be updated as follows:

$$timestamp = timestamp(i - 1) + \frac{1}{\max(BDR_{XL}, BDR_{GY})}$$

The memory-saving approach allows the user to maximize the data stored in FIFO. With this method all the timestamp correlation is forwarded to the application processor.

This approach is not recommended when the overrun condition can occur.

The hybrid approach is a trade-off and a combination of the two previous solutions. The timestamp is configured to be written in FIFO with decimation. When the TAG\_CNT value increases, the timestamp stored at the software layer should be updated as in the memory-saving approach, while when the timestamp sensor is read, the timestamp stored at the software layer should be realigned with the correct value from the sensor.

## 8 Temperature sensor

The device is provided with an internal temperature sensor that is suitable for ambient temperature measurement. If both the accelerometer and the gyroscope sensors are in power-down mode, the temperature sensor is off.

The temperature data rate is equal to 52 Hz, regardless of the accelerometer and gyroscope configuration.

For the temperature sensor, the data-ready signal is represented by the TDA bit of the STATUS\_REG register. The signal can be driven to the INT2 pin by setting the INT2\_DRDY\_TEMP bit of the INT2\_CTRL register to 1.

The temperature data is given by the concatenation of the OUT\_TEMP\_H and OUT\_TEMP\_L registers and it is represented as a number of 16 bits in two's complement format with a sensitivity of 256 LSB/°C. The output zero level corresponds to 25 °C.

Temperature sensor data can also be stored in FIFO with a configurable batch data rate (see [Section 7 First-in, first-out buffer](#) for details).

### 8.1 Example of temperature data calculation

The following table provides a few basic examples of the data that is read from the temperature data registers at different ambient temperature values. The values listed in this table are given under the hypothesis of perfect device calibration (that is, no offset, no gain error, and so forth).

**Table 46. Content of output data registers vs. temperature**

Temperature values	Register address	
	OUT_TEMP_H (21h)	OUT_TEMP_L (20h)
0 °C	E7h	00h
25 °C	00h	00h
50 °C	19h	00h

## 9 Self-test

The embedded self-test functions allow checking the device functionality without moving it.

### 9.1 Accelerometer self-test

When the accelerometer self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the sensitivity value.

The accelerometer self-test function is off when the ST[1:0]\_XL bits of the CTRL5\_C register are programmed to 00. It is enabled when the ST[1:0]\_XL bits are set to 01 (positive sign self-test) or 10 (negative sign self-test).

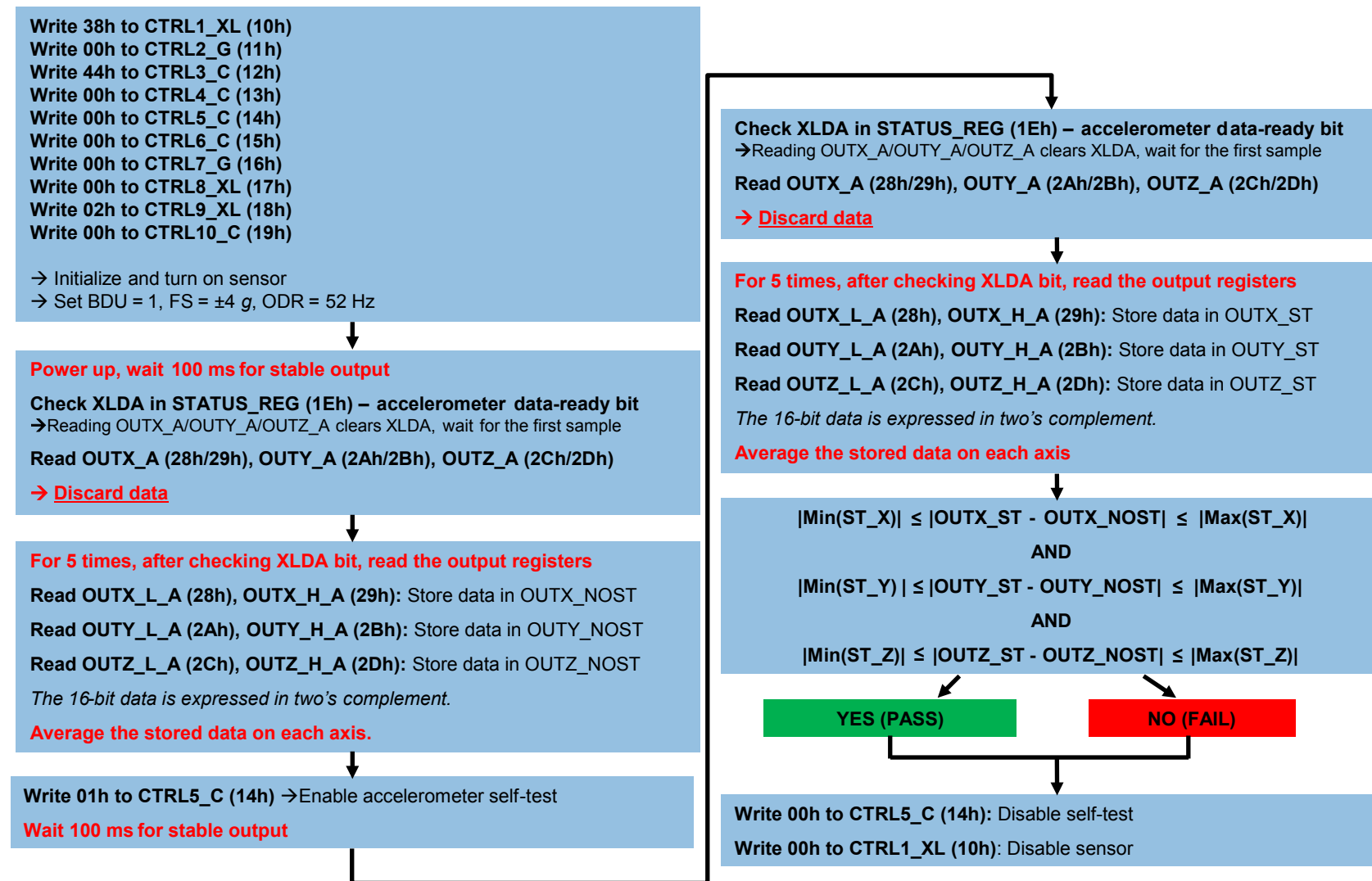
When the accelerometer self-test is activated, the sensor output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

The complete accelerometer self-test procedure is indicated in [Figure 25. Accelerometer self-test procedure](#).

Figure 25. Accelerometer self-test procedure

*Note: Keep the device still during the self-test procedure.*

## Accelerometer self-test



## 9.2 Gyroscope self-test

The gyroscope self-test allows testing the mechanical and electrical parts of the gyroscope sensor. When it is activated, an equivalent Coriolis signal is emulated at the input of the ASIC front-end and the sensor output exhibits an output change.

The gyroscope self-test function is off when the ST[1:0]\_G bits of the CTRL5\_C register are programmed to 00. It is enabled when the ST[1:0]\_G bits are set to 01 (positive sign self-test) or 11 (negative sign self-test).

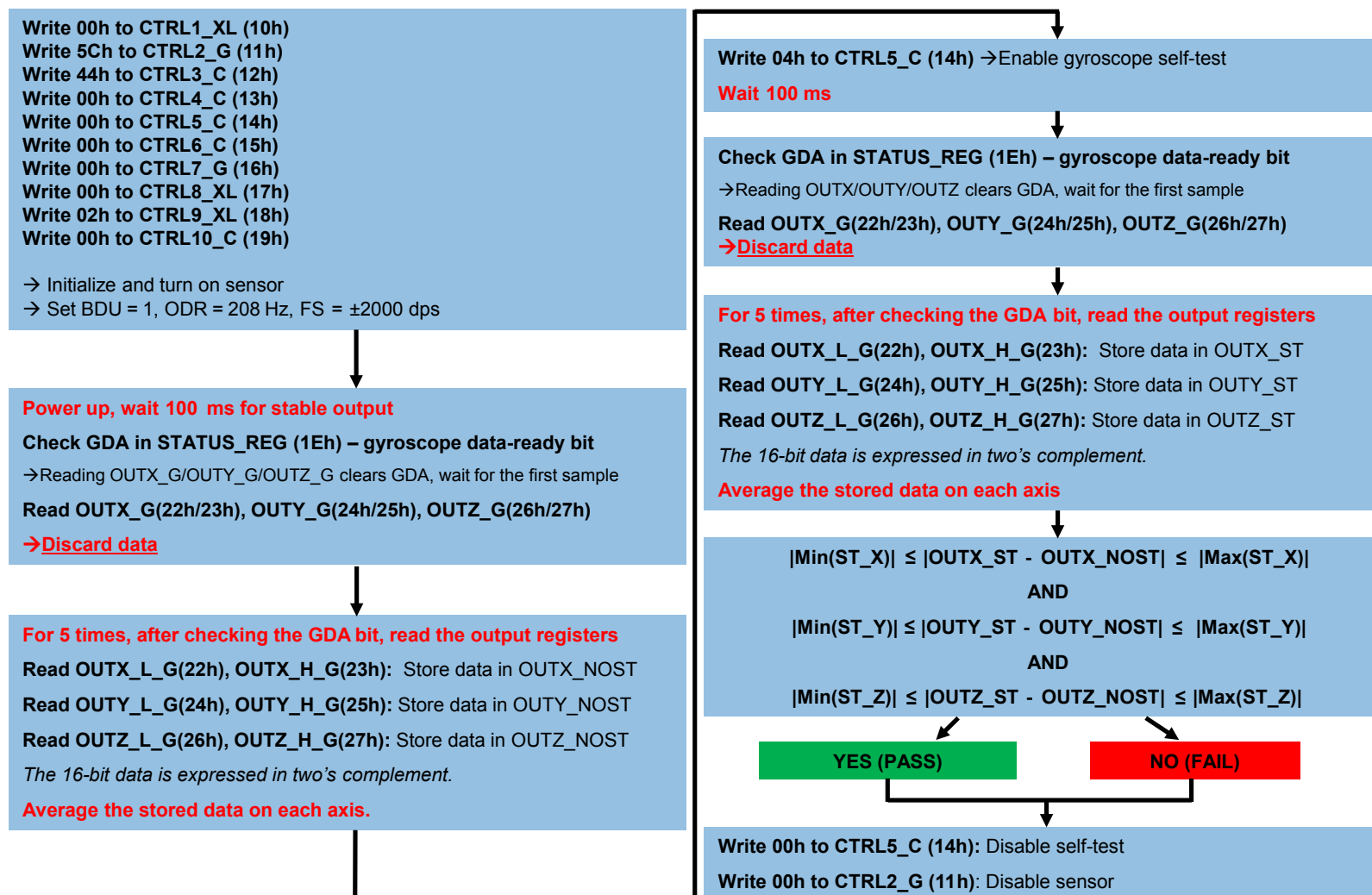
When the gyroscope self-test is active, the sensor output level is given by the algebraic sum of the signals produced by the angular rate acting on the sensor and by the electrostatic test-force.

The complete gyroscope self-test procedure is indicated in [Figure 26. Gyroscope self-test procedure](#).

Figure 26. Gyroscope self-test procedure

*Note: Keep the device still during the self-test procedure.*

## Gyroscope self-test





## Revision history

**Table 47. Document revision history**

Date	Version	Changes
13-Mar-2019	1	Initial release
12-Jun-2020	2	Added footnotes regarding connectivity to INT1 and INT2 in Table 1. Internal pin status Updated Section 3 Operating modes Updated unit of $t_{\text{actual}}$ to seconds in Section 6 Timestamp Updated Section 9.2 Gyroscope self-test
21-Jan-2021	3	Updated step 4 in software routine in Section 4.8.1 Edge-sensitive trigger mode Updated Figure 25. Accelerometer self-test procedure and Figure 26. Gyroscope self-test procedure
23-Feb-2021	4	Updated VDD (min) in Section 3 Operating modes
23-Jan-2023	5	Added procedure (see Note) for accelerometer activation in high-performance mode to Section 3 Operating modes Updated ODR to 416 Hz throughout datasheet Minor textual updates
14-Feb-2023	6	Updated the procedure in <a href="#">Section 3 Operating modes</a>

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