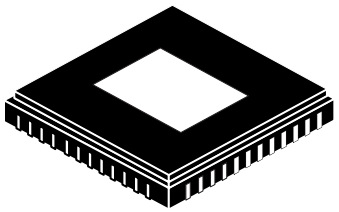
1/3-Inch Wide-VGA CMOS Digital Image Sensor

MT9V034



CLCC48 11.43 x 11.43
CASE 848AN

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

General Description

The MT9V034 is a 1/3−inch wide−VGA format CMOS active−pixel digital image sensor with global shutter and high dynamic range (HDR) operation. The sensor has specifically been designed to support the demanding interior and exterior surveillance imaging needs, which makes this part ideal for a wide variety of imaging applications in real−world environments.

This wide−VGA CMOS image sensor features **onsemi**'s breakthrough low−noise CMOS imaging technology that achieves CCD image quality (based on signal−to−noise ratio and low−light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The active imaging pixel array is 752 H x 480 V. It incorporates sophisticated camera functions on−chip−such as binning 2 x 2 and 4 x 4, to improve sensitivity when operating in smaller resolutions−as well as windowing, column and row mirroring. It is programmable through a simple two−wire serial interface.

The MT9V034 can be operated in its default mode or be programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide−VGA−size image at 60 frames per second (fps).

An on−chip analog−to−digital converter (ADC) provides 10 bits per pixel. A 12−bit resolution companded for 10 bits for small signals can be alternatively enabled, allowing more accurate digitization for darker areas in the image.

In addition to a traditional, parallel logic output the MT9V034 also features a serial low−voltage differential signaling (LVDS) output. The sensor can be operated in a stereo−camera, and the sensor, designated as a stereo−master, is able to merge the data from itself and the stereo−slave sensor into one serial LVDS stream.

The sensor is designed to operate in a wide temperature range (−30°C to +70°C).

Features

- Array format: Wide−VGA, Active 752 H x 480 V (360,960 Pixels)
- Global Shutter Photodiode Pixels; Simultaneous Integration and Readout
- RGB Bayer or Monochrome: NIR Enhanced Performance for Use with Non−visible NIR Illumination
- Readout Modes: Progressive or Interlaced
- Shutter Efficiency: >99%
- Simple Two−wire Serial Interface
- Real−Time Exposure Context Switching − Dual Register Set
- Register Lock Capability
- Window Size: User Programmable to any Smaller Format (QVGA, CIF, QCIF). Data Rate can be Maintained Independent of Window Size
- Binning: 2 x 2 and 4 x 4 of the Full Resolution
- ADC: On−chip, 10−bit Column−parallel (Option to Operate in 12−bit to 10−bit Companding Mode)
- Automatic Controls: Auto Exposure Control (AEC) and Auto Gain Control (AGC); Variable Regional and Variable Weight AEC/AGC
- Support for Four Unique Serial Control Register IDs to Control Multiple Imagers on the Same Bus
- Data Output Formats:
- Single Sensor Mode:
  10−bit Parallel/stand−alone
  8−bit or 10−bit Serial LVDS
- Stereo Sensor Mode:
  Interspersed 8−bit Serial LVDS
- High Dynamic Range (HDR) Mode

Applications

- Security
- High Dynamic Range Imaging
- Unattended Surveillance
- Stereo Vision
- Video as Input
- Machine Vision
- Automation

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Value
Optical Format	1/3−inch
Active Imager Size	4.51 mm (H) x 2.88 mm (V) 5.35 mm diagonal
Active Pixels	752 H x 480 V
Pixel Size	6.0 x 6.0 μm
Color Filter Array	Monochrome or color RGB Bayer
Shutter Type	Global Shutter
Maximum Data Rate Master Clock	27 Mp/s 27 MHz
Full Resolution	752 x 480
Frame Rate	60 fps (at full resolution)
ADC Resolution	10−bit column−parallel
Responsivity	4.8 V/lux−sec (550 nm)
Dynamic Range	>55 dB linear; >100 dB in HDR mode
Supply Voltage	3.3 V ± 0.3 V (all supplies)
Power Consumption	<160 mW at maximum data rate (LVDS disabled); 120 μW standby power at 3.3 V
Operating Temperature	−30°C to + 70°C ambient
Packaging	48−pin CLCC

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9V034C12STC−DP	VGA 1/3” GS CIS	Dry Pack with Protective Film
MT9V034C12STC−DR	VGA 1/3” GS CIS	Dry Pack without Protective Film
MT9V034C12STM−DP	VGA 1/3” GS CIS	Dry Pack with Protective Film
MT9V034C12STM−DR	VGA 1/3” GS CIS	Dry Pack without Protective Film
MT9V034C12STM−DR1	VGA 1/3” GS CIS	Dry Pack Single Tray without Protective Film
MT9V034C12STM−TP	VGA 1/3” GS CIS	Tape & Reel with Protective Film
MT9V034C12STM−TR	VGA 1/3” GS CIS	Tape & Reel without Protective Film
MT9V034D00STMC13CC1−200	VGA 1/3” GS CIS	Die Sales, 200 mm Thickness
MT9V034W00STMC13CC1−750	VGA 1/3” GS CIS	Wafer Sales, 750 mm Thickness

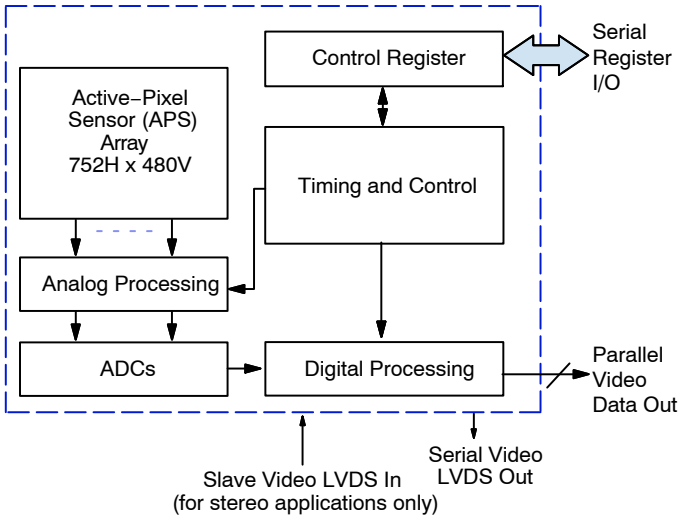


Figure 1. Block Diagram

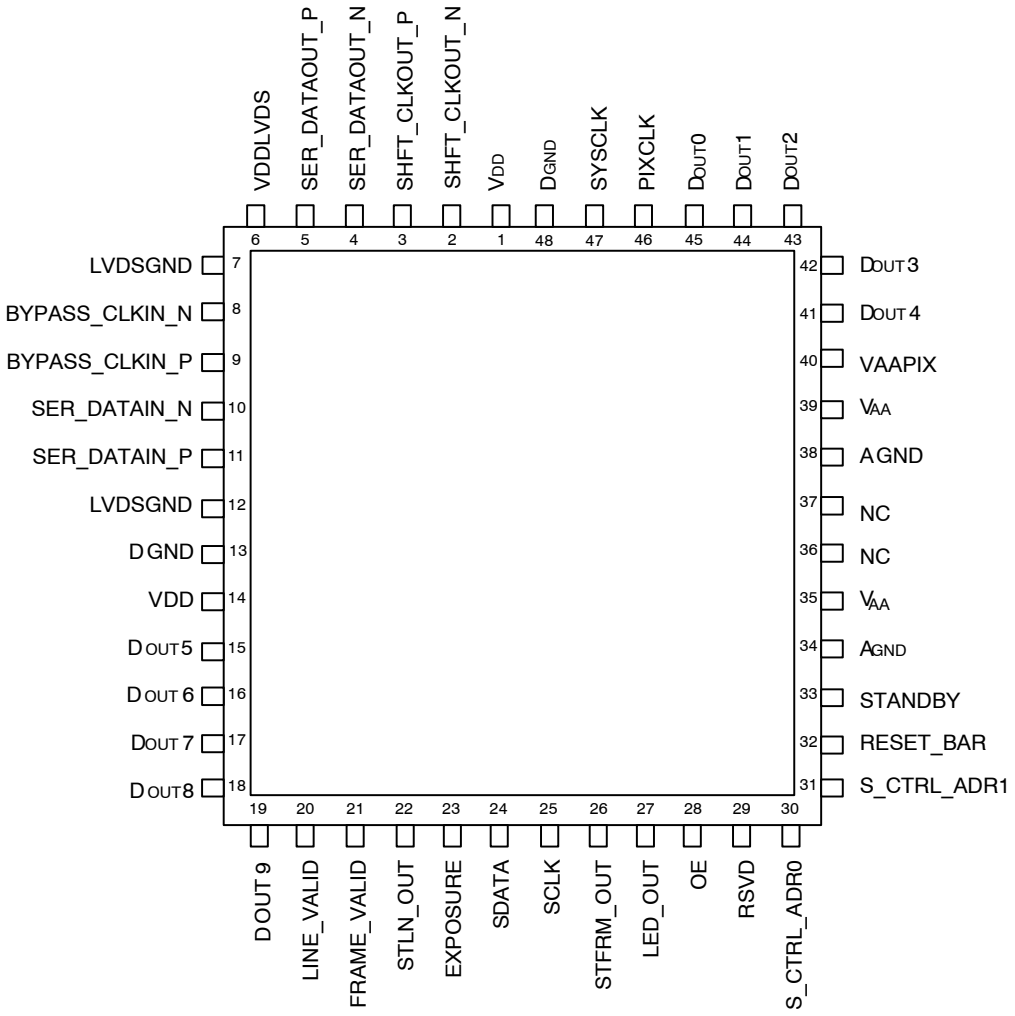


Figure 2. 48−Pin CLCC Package Pinout Diagram

BALL DESCRIPTIONS

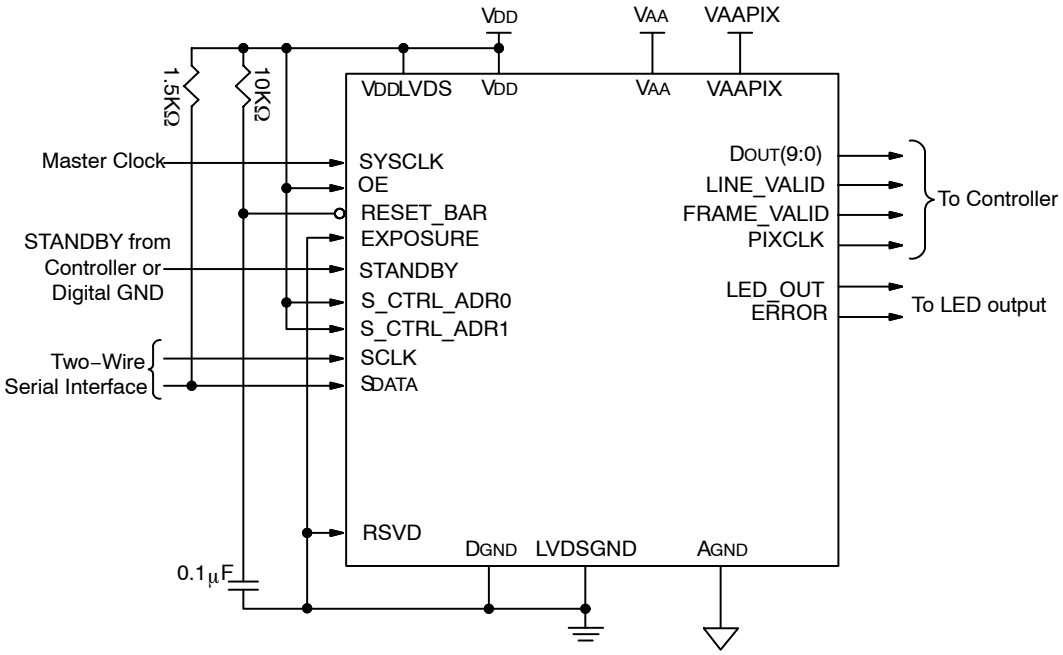
Table 3. BALL DESCRIPTIONS

52−Ball IBA Numbers	Symbol	Type	Description	Note
29	RSVD	Input	Connect to DGND.	1
10	SER_DATAIN_N	Input	Serial data in for stereoscopy (differential negative). Tie to 1 kΩ pull−up (to 3.3 V) in non−stereoscopy mode.	
11	SER_DATAIN_P	Input	Serial data in for stereoscopy (differential positive). Tie to DGND in non−stereoscopy mode.	
8	BYPASS_CLKIN_N	Input	Input bypass shift−CLK (differential negative). Tie to 1 kΩ pull−up (to 3.3 V) in non−stereoscopy mode.	
9	BYPASS_CLKIN_P	Input	Input bypass shift−CLK (differential positive). Tie to DGND in non−stereoscopy mode.	
23	EXPOSURE	Input	Rising edge starts exposure in snapshot and slave modes.	
25	SCLK	Input	Two−wire serial interface clock. Connect to VDD with 1.5k resistor even when no other two−wire serial interface peripheral is attached.	
28	OE	Input	DOUT enable pad, active HIGH.	2
30	S_CTRL_ADR0	Input	Two−wire serial interface slave address select (see Table 6).	
31	S_CTRL_ADR1	Input	Two−wire serial interface slave address select (see Table 6).	
32	RESET_BAR	Input	Asynchronous reset. All registers assume defaults.	
33	STANDBY	Input	Shut down sensor operation for power saving.	
47	SYSCLK	Input	Master clock (26.6 MHz; 13 MHz − 27 MHz).	
24	SDATA	I/O	Two−wire serial interface data. Connect to VDD with 1.5k resistor even when no other two−wire serial interface peripheral is attached.	
22	STLN_OUT	I/O	Output in master mode−start line sync to drive slave chip in−phase; input in slave mode.	
26	STFRM_OUT	I/O	Output in master mode−start frame sync to drive a slave chip in−phase; input in slave mode.	
20	LINE_VALID	Output	Asserted when DOUT data is valid.	
21	FRAME_VALID	Output	Asserted when DOUT data is valid.	
15	DOUT5	Output	Parallel pixel data output 5.	
16	DOUT6	Output	Parallel pixel data output 6.	
17	DOUT7	Output	Parallel pixel data output 7.	
18	DOUT8	Output	Parallel pixel data output 8.	
19	DOUT9	Output	Parallel pixel data output 9.	
27	LED_OUT	Output	LED strobe output.	
41	DOUT4	Output	Parallel pixel data output 4.	
42	DOUT3	Output	Parallel pixel data output 3.	
43	DOUT2	Output	Parallel pixel data output 2.	
44	DOUT1	Output	Parallel pixel data output 1.	
45	DOUT0	Output	Parallel pixel data output 0.	
46	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.	
2	SHFT_CLKOUT_N	Output	Output shift CLK (differential negative).	

Table 3. BALL DESCRIPTIONS (continued)

52−Ball IBA Numbers	Symbol	Type	Description	Note
3	SHFT_CLKOUT_P	Output	Output shift CLK (differential positive).	
4	SER_DATAOUT_N	Output	Serial data out (differential negative).	
5	SER_DATAOUT_P	Output	Serial data out (differential positive).	
1, 14	VDD	Supply	Digital power 3.3 V.	
35, 39	VAA	Supply	Analog power 3.3 V.	
40	VAAPIX	Supply	Pixel power 3.3 V.	
6	VDDLVDS	Supply	Dedicated power for LVDS pads.	
7, 12	LVDSGND	Ground	Dedicated GND for LVDS pads.	
13, 48	DGND	Ground	Digital GND.	
34, 38	AGND	Ground	Analog GND.	
36, 37	NC	NC	No connect.	3

1. Pin 29, (RSVD) must be tied to GND.
2. Output enable (OE) tri−states signals DOUT0−DOUT9, LINE_VALID, FRAME_VALID, and PIXCLK.
3. No connect. These pins must be left floating for proper operation.



NOTE: LVDS signals are to be left floating.

Figure 3. Typical Configuration (Connection) − Parallel Output Mode

PIXEL DATA FORMAT

Pixel Array Structure

The MT9V034 pixel array is configured as 809 columns by 499 rows, shown in Figure 4. The dark pixels are optically black and are used internally to monitor black level. Of the left 52 columns, 36 are dark pixels used for row noise correction. Of the top 14 rows of pixels, two of the dark rows are used for black level correction. Also, three black rows from the top black rows can be read out by setting the show dark rows bit in the Read Mode register; setting show dark columns will display the 36 dark columns. There are 753 columns by 481 rows of optically active pixels. While the sensor's format is 752 x 480, one additional active column and active row are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. This one pixel adjustment is always performed, for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Neither dummy pixels nor barrier pixels can be read out.

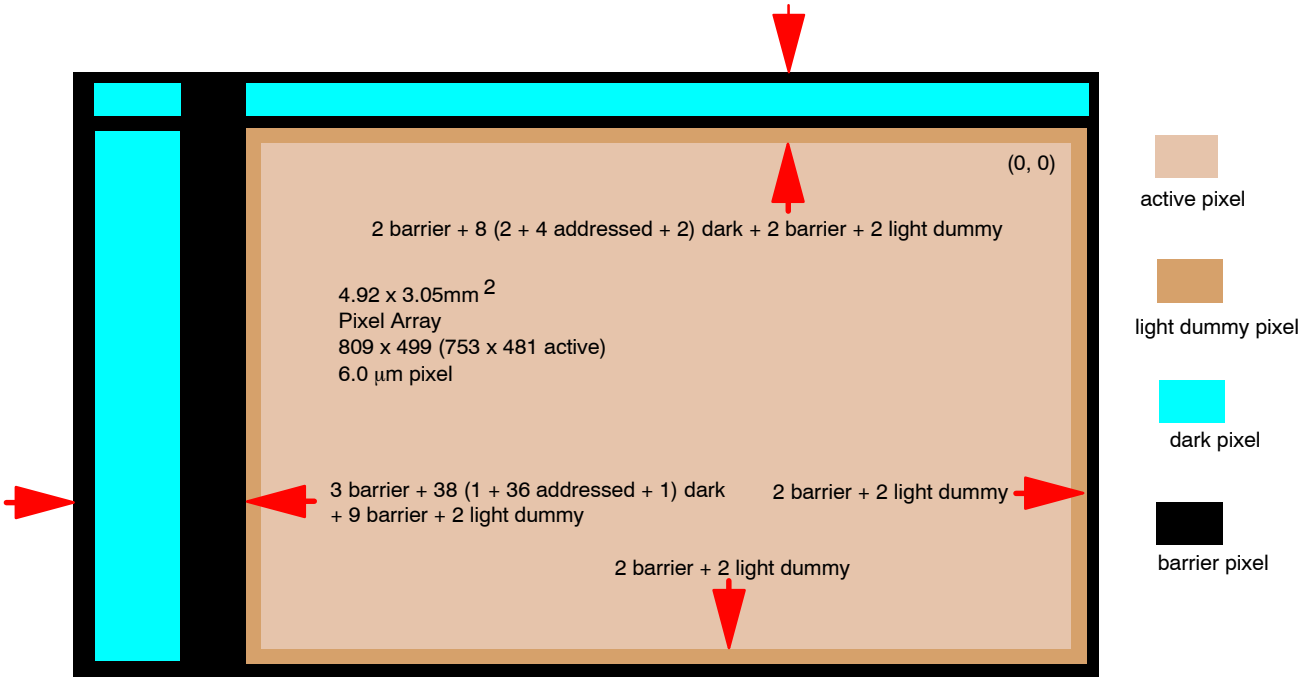


Figure 4. Pixel Array Description

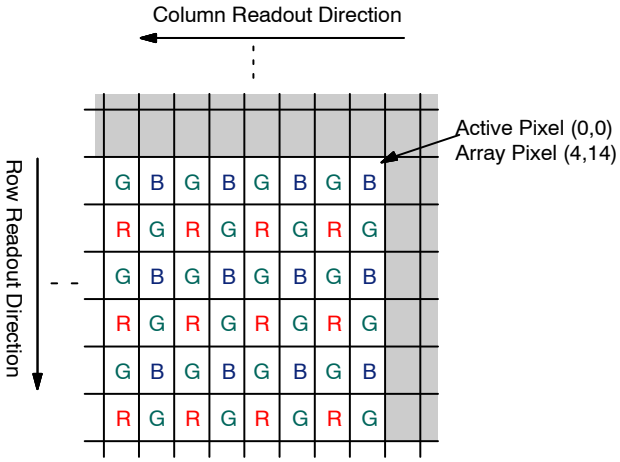


Figure 5. Pixel Color Pattern Detail RGB Bayer (Top Right Corner)

COLOR (RGB BAYER) DEVICE LIMITATIONS

The color version of the MT9V034 does not support or offers reduced performance for the following functionalities.

Pixel Binning

Pixel binning is done on immediate neighbor pixels only, no facility is provided to skip pixels according to a Bayer pattern. Therefore, the result of binning combines pixels of different colors. See “Pixel Binning” for additional information.

Interlaced Readout

Interlaced readout yields one field consisting only of red and green pixels and another consisting only of blue and green pixels. This is due to the Bayer pattern of the CFA.

Automatic Black Level Calibration

When the color bit is set (R0x0F[1] = 1), the sensor uses black level correction values from one green plane, which are applied to all colors. To use the calibration value based on all dark pixels’ offset values, the color bit should be cleared.

Defective Pixel Correction

For defective pixel correction to calculate replacement pixel values correctly, for color sensors the color bit must be set (R0x0F[1] = 1). However, the color bit also applies unequal offset to the color planes, and the results might not be acceptable for some applications.

Other Limiting Factors

Black level correction and row−wise noise correction are applied uniformly to each color. The row−wise noise correction algorithm does not work well in color sensors. Automatic exposure and gain control calculations are made based on all three colors, not just the green channel. High dynamic range does operate in color; however, **onsemi** strongly recommends limiting use to linear operation where good color fidelity is required.

OUTPUT DATA FORMAT

The MT9V034 image data can be read out in a progressive scan or interlaced scan mode. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 6. The amount of horizontal and vertical blanking is programmable through R0x05 and R0x06, respectively (R0xCD and R0xCE for context B). LV is HIGH during the shaded region of the figure. See “Output Data Timing” for the description of FV timing.

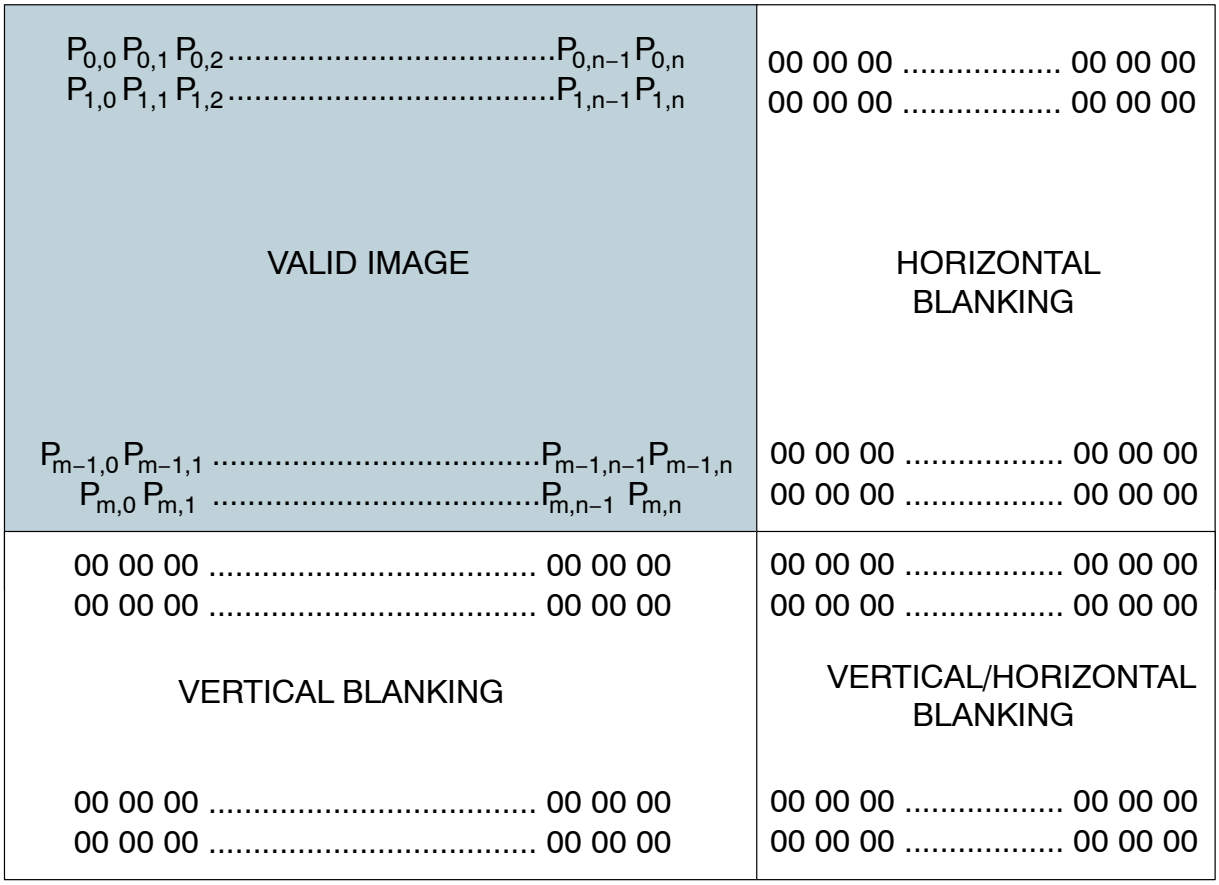


Figure 6. Spatial Illustration of Image Readout

OUTPUT DATA TIMING

The data output of the MT9V034 is synchronized with the PIXCLK output. When LINE_VALID (LV) is HIGH, one 10−bit pixel datum is output every PIXCLK period.

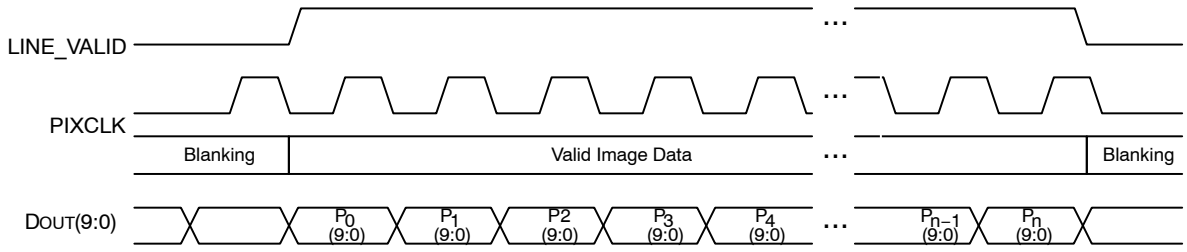


Figure 7. Timing Example of Pixel Data

The PIXCLK is a nominally inverted version of the master clock (SYSCLK). This allows PIXCLK to be used as a clock to latch the data. However, when column bin 2 is enabled, the PIXCLK is HIGH for one complete master clock master period and then LOW for one complete master clock period; when column bin 4 is enabled, the PIXCLK is HIGH for two complete master clock periods and then LOW for two complete master clock periods. It is continuously enabled, even during the blanking period. Setting R0x72 bit[4] = 1 causes the MT9V034 to invert the polarity of the PIXCLK.

The parameters P1, A, Q, and P2 in Figure 8 are defined in Table 4.

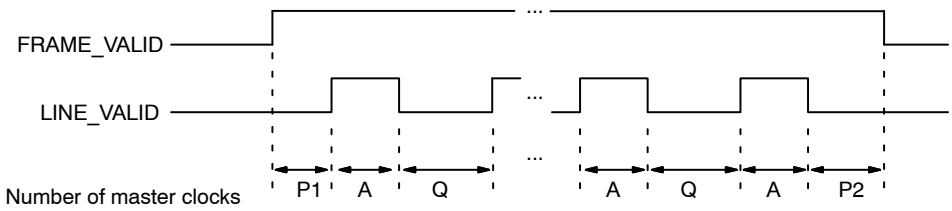


Figure 8. Row Timing and FRAME_VALID/LINE_VALID Signals

Table 4. FRAME TIME

Parameters	Name	Equation	Default Timing at 26.66 MHz
A	Active data time	Context A: R0x04 Context B: R0xCC	752 pixel clocks = 752 master = 28.2 µs
P1	Frame start blanking	Context A: R0x05 − 23 Context B: R0xCD − 23	71 pixel clocks = 71 master = 2.66 µs
P2	Frame end blanking	23 (fixed)	23 pixel clocks = 23 master = 0.86 µs
Q	Horizontal blanking	Context A: R0x05 Context B: R0xCD	94 pixel clocks = 94 master = 3.52 µs
A+Q	Row time	Context A: R0x04 + R0x05 Context B: R0xCC + R0xCD	846 pixel clocks = 846 master = 31.72 µs
V	Vertical blanking	Context A: (R0x06) x (A + Q) + 4 Context B: (R0xCE) x (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43 ms

Table 4. FRAME TIME (continued)

Parameters	Name	Equation	Default Timing at 26.66 MHz
Nrows x (A + Q)	Frame valid time	Context A: (R0x03) × (A + Q) Context B: (R0xCB) x (A + Q)	406,080 pixel clocks = 406,080 master = 15.23 ms
F	Total frame time	V + (Nrows x (A + Q))	444,154 pixel clocks = 444,154 master = 16.66 ms

Sensor timing is shown above in terms of pixel clock and master clock cycles (refer to Figure 7). The recommended master clock frequency is 26.66 MHz. The vertical blanking and the total frame time equations assume that the integration time (Coarse Shutter Width plus Fine Shutter Width) is less than the number of active rows plus the blanking rows minus the overhead rows:

$$\text{Window Height} + \text{Vertical Blanking} - 2 \qquad \text{(eq.1)}$$

If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 5. In this example it is assumed that the Coarse Shutter Width Control is programmed with 523 rows, and the Fine Shutter Width Total is zero.

For Simultaneous mode, if the exposure time registers (Coarse Shutter Width Total plus Fine Shutter Width Total) exceed the total readout time, then the vertical blanking time is internally extended automatically to adjust for the additional integration time required. This extended value is *not* written back to the vertical blanking registers. The Vertical Blank register can be used to adjust frame−to−frame readout time. This register does not affect the exposure time but it may extend the readout time.

Table 5. FRAME TIME−LONG INTEGRATION TIME

Parameter	Name	Equation (Number of Master Clock Cycles)	Default Timing at 26.66 MHz
V’	Vertical blanking (long integration time)	Context A: (R0x0B + 2 − R0x03) y (A + Q) + R0xD5 + 4 Context B: (R0xD2 + 2 − R0xCB) x (A + Q) + R0xD8 + 4	38,074 pixel clocks = 38,074 master = 1.43 ms
F’	Total frame time (long integration time)	Context A: (R0x0B + 2) y (A + Q) + R0xD5 +4 Context B: (R0xD2 + 2) x (A + Q) + R0xD8 +4	444,154 pixel clocks = 444,154 master = 16.66 ms

4. The MT9V034 uses column parallel analog−digital converters; thus short row timing is not possible. The minimum total row time is 704 columns (horizontal width + horizontal blanking). The minimum horizontal blanking is 61 for normal mode, 71 for column bin 2 mode, and 91 for column bin 4 mode. When the window width is set below 643, horizontal blanking must be increased. In binning mode, the minimum row time is R0x04+R0x05 = 704.

SERIAL BUS DESCRIPTION

Registers are written to and read from the MT9V034 through the two−wire serial interface bus. The MT9V034 is a serial interface slave with four possible IDs (0x90, 0x98, 0xB0 and 0xB8) determined by the S_CTRL_ADR0 and S_CTRL_ADR1 input pins. Data is transferred into the MT9V034 and out through the serial data (SDATA) line. The SDATA line is pulled up to VDD off−chip by a 1.5 kΩ resistor. Either the slave or master device can pull the SDATA line down−the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16−bit wide, and can be accessed through 16− or 8−bit two−wire serial interface sequences.

Protocol

The two−wire serial interface defines several different transmission codes, as shown in the following sequence:

1. a start bit
2. the slave device 8−bit address
3. a(n) (no) acknowledge bit
4. an 8−bit message
5. a stop bit

Start Bit

The start bit is defined as a HIGH−to−LOW transition of the data line while the clock line is HIGH.

Slave Address

The 8−bit address of a two−wire serial interface device consists of 7 bits of address and 1 bit of direction. A “0” in the LSB of the address indicates write mode, and a “1” indicates read mode. As indicated above, the MT9V034 allows four possible slave addresses determined by the two input pins, S_CTRL_ADR0 and S_CTRL_ADR1.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No−Acknowledge Bit

The no−acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no−acknowledge bit is used to terminate a read sequence.

Stop Bit

The stop bit is defined as a LOW−to−HIGH transition of the data line while the clock line is HIGH.

Sequence

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device’s 8−bit address. The last bit of the address determines if the request is a read or a write, where a “0” indicates a WRITE and a “1” indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8−bit register address to which a WRITE should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9V034 uses 16−bit data for its internal registers, thus requiring two 8−bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write mode slave address and 8−bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is automatically incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit. The MT9V034 allows for 8−bit data transfers through the two−wire serial interface by writing (or reading) the most significant 8 bits to the register and then writing (or reading) the least significant 8 bits to Byte−Wise Address register (0x0F0).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Table 6. SLAVE ADDRESS MODES

{S_CTRL_ADR1, S_CTRL_ADR0}	Slave Address	Write/Read Mode
00	0x90	Write
	0x91	Read
01	0x98	Write
	0x99	Read
10	0xB0	Write
	0xB1	Read
11	0xB8	Write
	0xB9	Read

Data Bit Transfer

One data bit is transferred during each clock pulse. The two−wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock−it can only change when the two−wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

TWO−WIRE SERIAL INTERFACE SAMPLE READ AND WRITE SEQUENCES

16−Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 9. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16−bit data. After each 8−bit the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

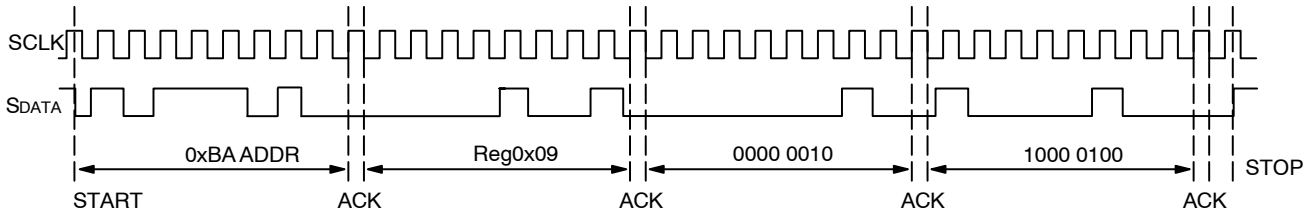


Figure 9. Timing Diagram Showing a WRITE to Reg0x09 with the Value 0x0284

16−Bit Read Sequence

A typical read sequence is shown in Figure 10. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is auto−incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

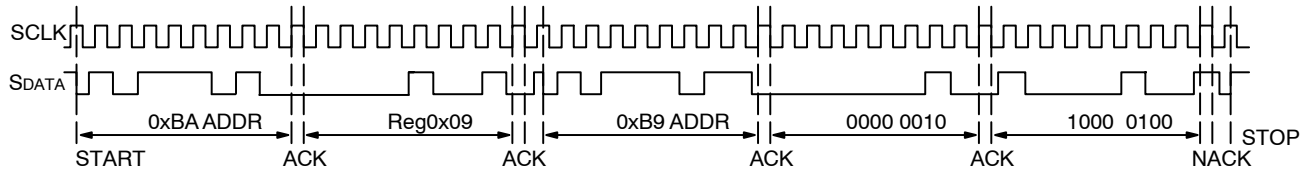


Figure 10. Timing Diagram Showing a READ from Reg0x09, Returned Value 0x0284

8−Bit Write Sequence

To be able to write 1 byte at a time to the register a special register address is added. The 8−bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the Bytewise Address register (R0xF0). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 11, a typical sequence for 8−bit writing is shown. The second byte is written to the Bytewise register (R0xF0).

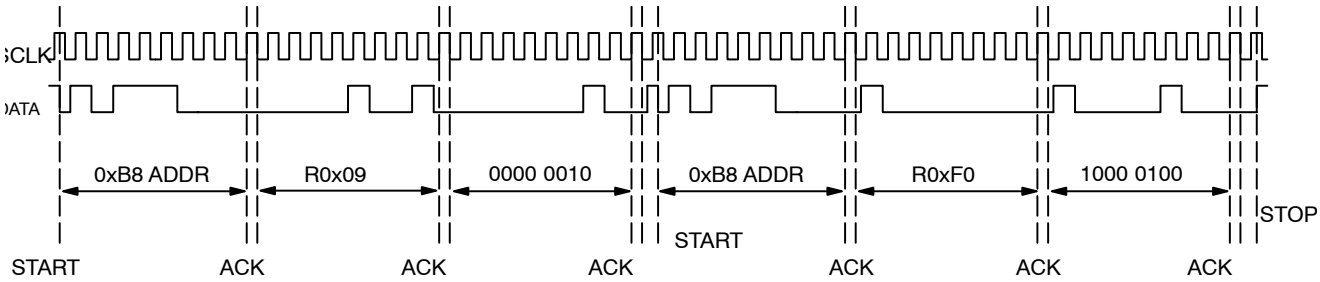


Figure 11. Timing Diagram Showing a Bytewise Write to R0x09 with the Value 0x0284

8−Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the Bytewise Address register (R0xF0) the lower 8 bits are accessed (Figure 12). The master sets the no−acknowledge bits shown.

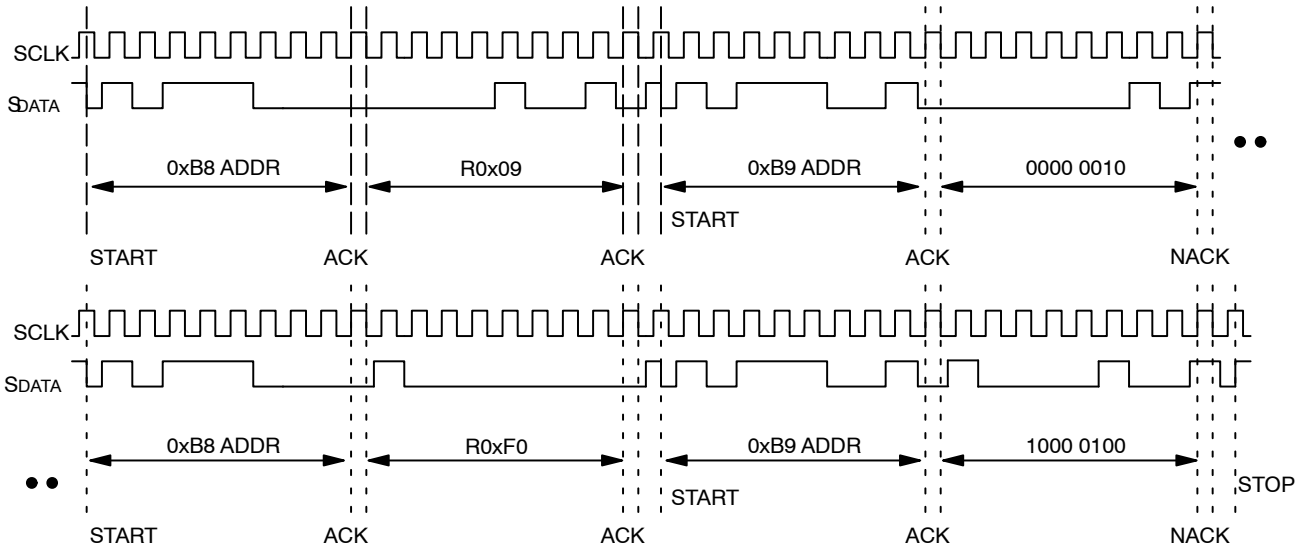


Figure 12. Timing Diagram Showing a Bytewise Read from R0x09; Returned Value 0x0284

Register Lock

Included in the MT9V034 is a register lock (R0xFE) feature that can be used as a solution to reduce the probability of an inadvertent noise−triggered two−wire serial interface write to the sensor. All registers, or only the Read Mode registers− R0x0D and R0x0E, can be locked. It is important to prevent an inadvertent two−wire serial interface write to the Read Mode registers in automotive applications since this register controls the image orientation and any unintended flip to an image can cause serious results.

At power−up, the register lock defaults to a value of 0xBEEF, which implies that all registers are unlocked and any two−wire serial interface writes to the register gets committed.

Lock All Registers

If a unique pattern (0xDEAD) to R0xFE is programmed, any subsequent two−wire serial interface writes to registers (except R0xFE) are NOT committed. Alternatively, if the user writes a 0xBEEF to the register lock register, all registers are unlocked and any subsequent two−wire serial interface writes to the register are committed.

Lock Only Read Mode Registers (R0x0D and R0x0E)

If a unique pattern (0xDEAF) to R0xFE is programmed, any subsequent two−wire serial interface writes to R0x0D or R0x0E are NOT committed. Alternatively, if the user writes a 0xBEEF to register lock register, registers R0x0D and R0x0E are unlocked and any subsequent two−wire serial interface writes to these registers are committed.

Real−Time Context Switching

In the MT9V034, the user may switch between two full register sets (listed in Table 7) by writing to a context switch change bit in register 0x07. This context switch will change all registers (no shadowing) at the frame start time and have the new values apply to the immediate next exposure and readout time (frame n+1), except for shutter width and V1−V4 control, which will take effect for next exposure but will show up in the n+2 image.

Table 7. REAL−TIME CONTEXT−SWITCHABLE REGISTERS

Register Name	Register Number (Hex) For Context A	Register Number (Hex) for Context B
Column Start	0x01	0xC9
Row Start	0x02	0xCA
Window Height	0x03	0xCB
Window Width	0x04	0xCC
Horizontal Blanking	0x05	0xCD
Vertical Blanking	0x06	0xCE
Coarse Shutter Width 1	0x08	0xCF
Coarse Shutter Width 2	0x09	0xD0
Coarse Shutter Width Control	0x0A	0xD1
Coarse Shutter Width Total	0x0B	0xD2
Fine Shutter Width 1	0xD3	0xD6
Fine Shutter Width 2	0xD4	0xD7
Fine Shutter Width Total	0xD5	0xD8
Read Mode	0x0D [5:0]	0x0E [5:0]
High Dynamic Range enable	0x0F [0]	0x0F [8]
ADC Resolution Control	0x1C [1:0]	0x1C [9:8]
V1 Control – V4 Control	0x31 – 0x34	0x39 – 0x3C
Analog Gain Control	0x35	0x36
Row Noise Correction Control 1	0x70 [1:0]	0x70 [9:8]
Tiled Digital Gain	0x80 [3:0] – 0x98 [3:0]	0x80 [11:8] – 0x98 [11:8]
AEC/AGC Enable	0xAF [1:0]	0xAF [9:8]

Recommended Register Settings

Table 8 describes new suggested register settings, and descriptions of performance improvements and conditions:

Table 8. RECOMMENDED REGISTER SETTINGS AND PERFORMANCE IMPACT (RESERVED REGISTERS)

Register	Current Default	New Setting	Performance Impact
R0x20	0x01C1	0x03C7	Recommended by design to improve performance in HDR mode and when frame rate is low. We also recommended using R0x13 = 0x2D2E with this setting for better column FPN. NOTE: When coarse integration time set to 0 and fine integration time less than 456, R0x20 should be set to 0x01C7
R0x24	0x0010	0x001B	Corrects pixel negative dark offset when global reset in R0x20[9] is enabled.
R0x2B	0x0004	0x0003	Improves column FPN.
R0x2F	0x0004	0x0003	Improves FPN at near−saturation.

FEATURE DESCRIPTION

Operational Modes

The MT9V034 works in master, snapshot, or slave mode. In master mode the sensor generates the readout timing. In snapshot mode it accepts an external trigger to start integration, then generates the readout timing. In slave mode the sensor accepts both external integration and readout controls. The integration time is programmed through the two−wire serial interface during master or snapshot modes, or controlled through an externally generated control signal during slave mode.

Master Mode

There are two possible operation methods for master mode: simultaneous and sequential. One of these operation modes must be selected through the two−wire serial interface.

Simultaneous Master Mode

In simultaneous master mode, the exposure period occurs during readout. The frame synchronization waveforms are shown in Figures 13 and 14. The exposure and readout happen in parallel rather than sequential, making this the fastest mode of operation.

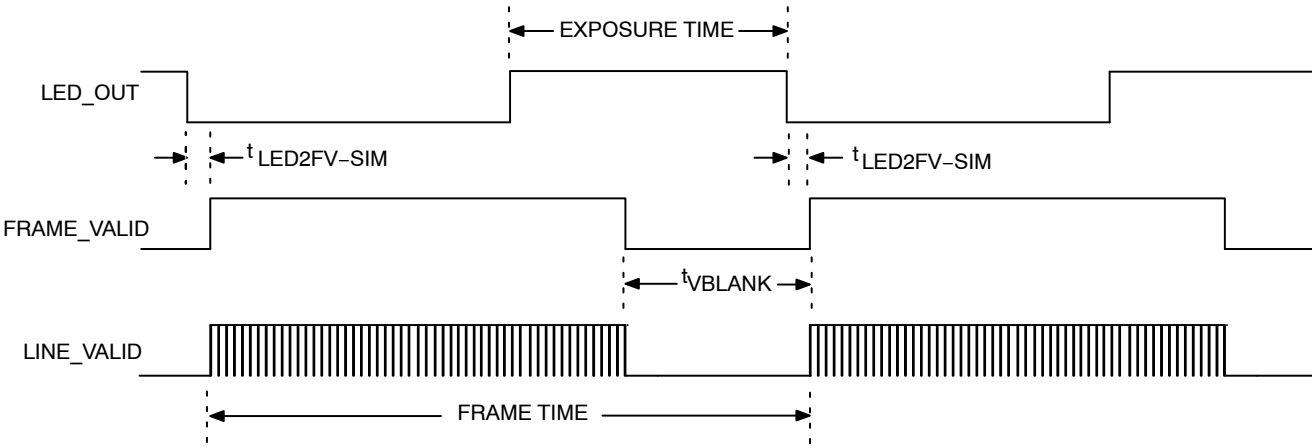


Figure 13. Simultaneous Master Mode Synchronization Waveforms #1

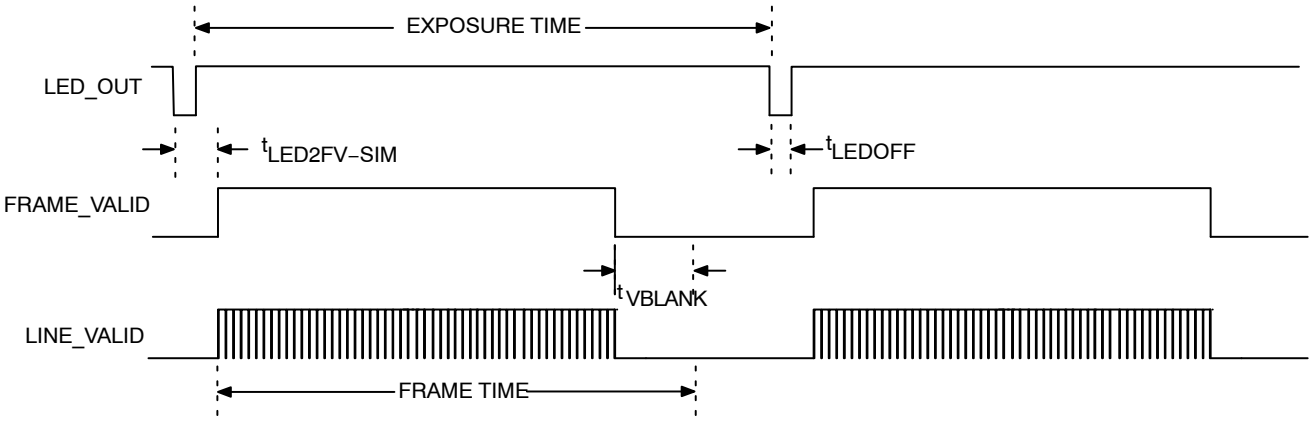


Figure 14. Simultaneous Master Mode Synchronization Waveforms #2

When exposure time is greater than the sum of vertical blank and window height, the number of vertical blank rows is increased automatically to accommodate the exposure time.

Sequential Master Mode

In sequential master mode the exposure period is followed by readout. The frame synchronization waveforms for sequential master mode are shown in Figure 15. The frame rate changes as the integration time changes.

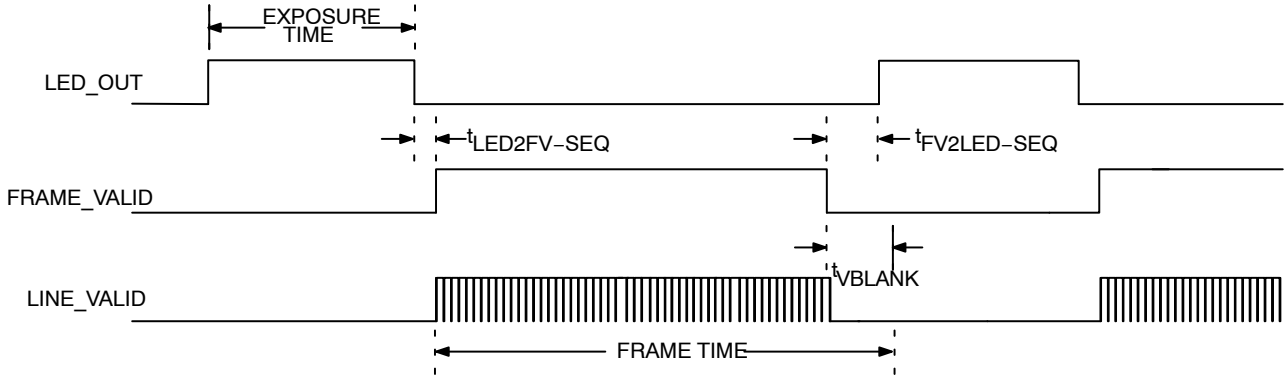


Figure 15. Sequential Master Mode Synchronization Waveforms

Snapshot Mode

In snapshot mode the sensor accepts an input trigger signal which initiates exposure, and is immediately followed by readout. Figure 16 shows the interface signals used in snapshot mode. In snapshot mode, the start of the integration period is determined by the externally applied EXPOSURE pulse that is input to the MT9V034. The integration time is preprogrammed at R0x0B or R0xD2 through the two−wire serial interface. After the frame's integration period is complete the readout process commences and the syncs and data are output. Sensor in snapshot mode can capture a single image or a sequence of images. The frame rate may only be controlled by changing the period of the user supplied EXPOSURE pulse train. The frame synchronization waveforms for snapshot mode are shown in Figure 17.

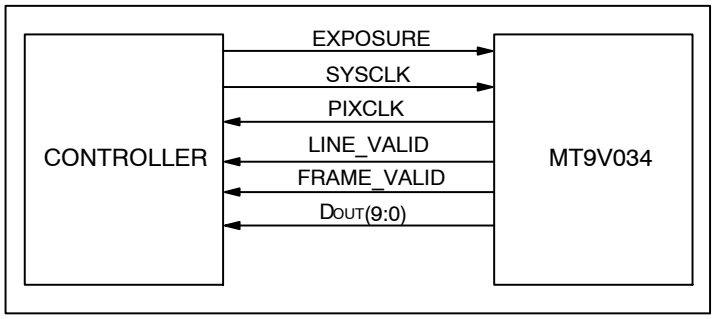


Figure 16. Snapshot Mode Interface Signals

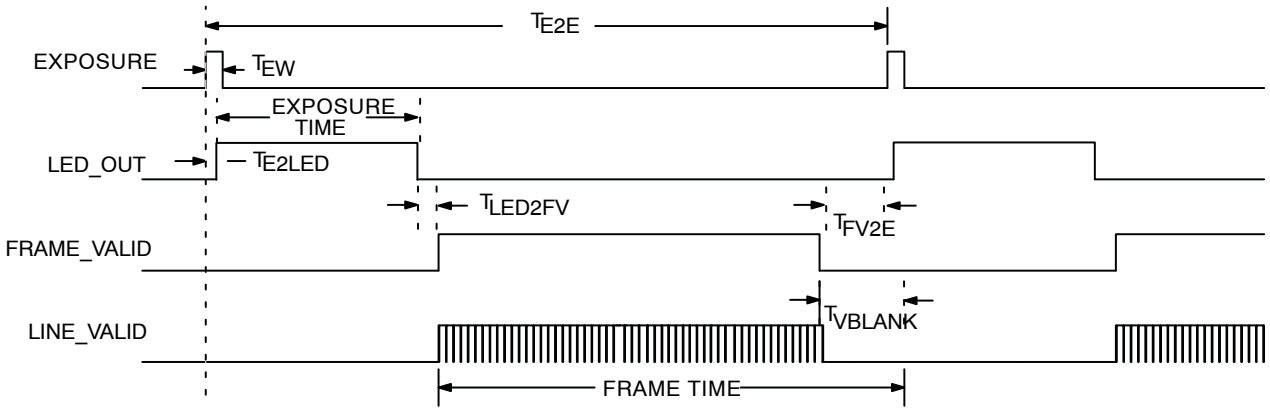


Figure 17. Snapshot Mode Frame Synchronization Waveforms

Slave Mode

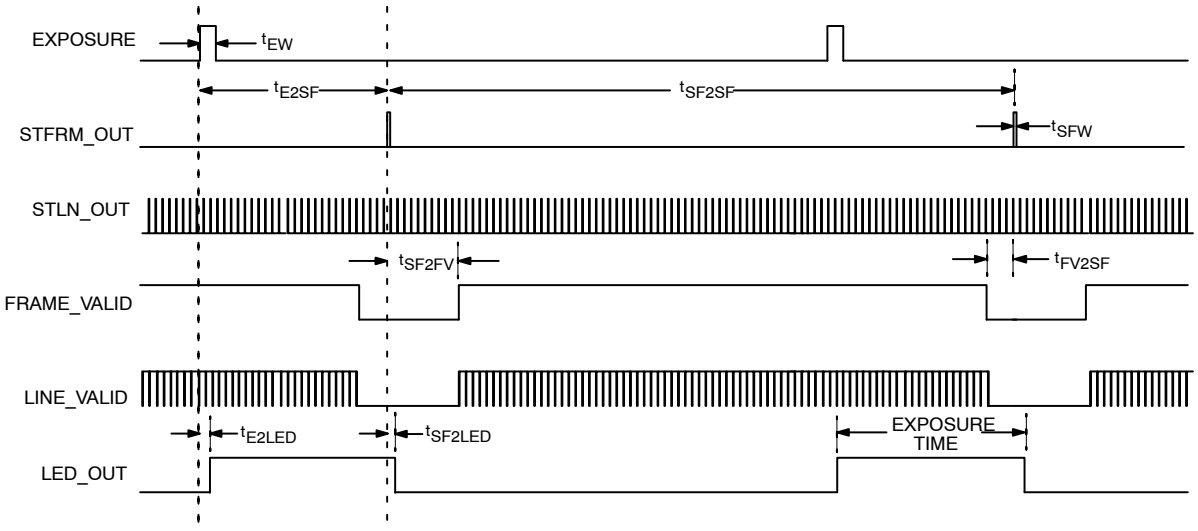
In slave mode, the exposure and readout are controlled using the EXPOSURE, STFRM_OUT, and STLN_OUT pins. When the slave mode is enabled, STFRM_OUT and STLN_OUT become input pins.

The start and end of integration are controlled by EXPOSURE and STFRM_OUT pulses, respectively. While a STFRM_OUT pulse is used to stop integration, it is also used to enable the readout process.

After integration is stopped, the user provides STLN_OUT pulses to trigger row readout. A full row of data is read out with each STLN_OUT pulse. The user must provide enough time between successive STLN_OUT pulses to allow the complete readout of one row.

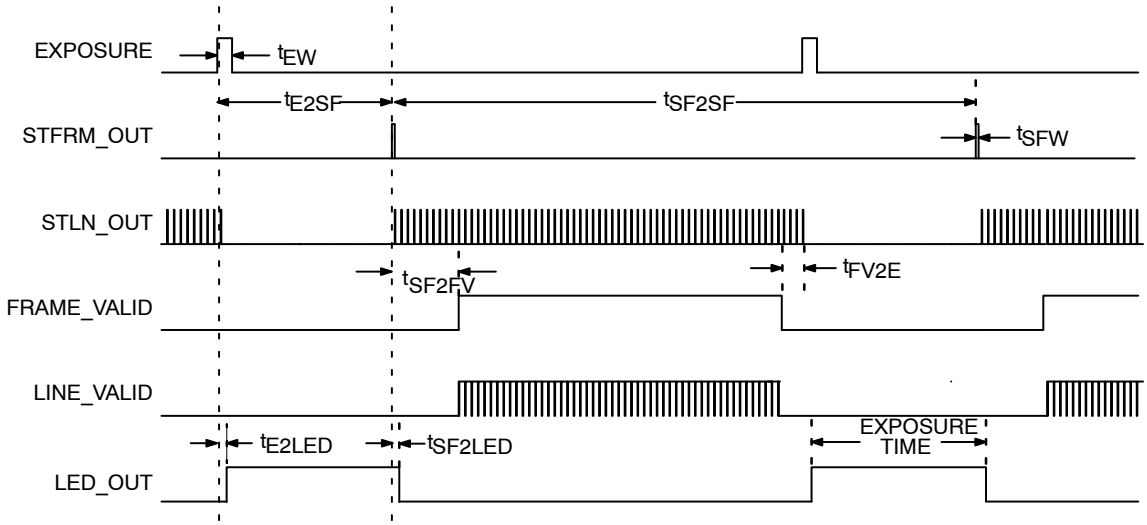
It is also important to provide additional STLN_OUT pulses to allow the sensors to read the vertical blanking rows. It is recommended that the user program the vertical blank register (R0x06) with a value of 4, and achieve additional vertical blanking between frames by delaying the application of the STFRM_OUT pulse.

The elapsed time between the rising edge of STLN_OUT and the first valid pixel data is calculated for context A by [horizontal blanking register (R0x05) + 4] clock cycles. For context B, the time is (R0xCD + 4) clock cycles.



1. Not drawn to scale.
2. Frame readout shortened for clarity.
3. Simultaneous progressive scan readout mode shown.

Figure 18. Exposure and Readout Timing (Simultaneous Mode)



1. Not drawn to scale.
2. Frame readout shortened for clarity.
3. STLN_OUT pulses are optional during exposure time.
4. Sequential progressive scan readout mode shown.

Figure 19. Exposure and Readout Timing (Sequential Mode)

Signal Path

The MT9V034 signal path consists of a programmable gain, a programmable analog offset, and a 10−bit ADC. See "Black Level Calibration" for the programmable offset operation description.

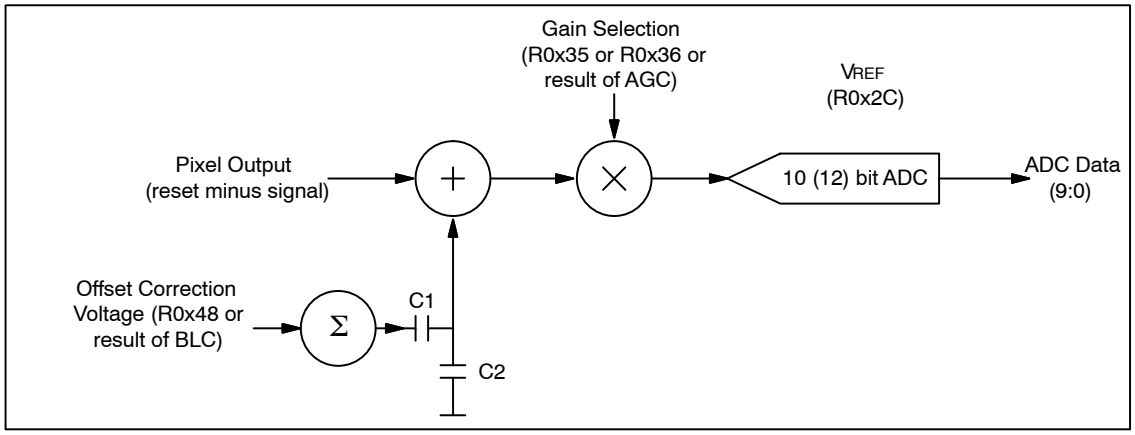


Figure 20. Signal Path

On−Chip Biases

ADC Voltage Reference

The ADC voltage reference is programmed through R0x2C, bits 2:0. The ADC reference ranges from 1.0 V to 2.1 V. The default value is 1.4 V. The increment size of the voltage reference is 0.1 V from 1.0 V to 1.6 V (R0x2C[2:0] values 0 to 6). At R0x2C[2:0] = 7, the reference voltage jumps to 2.1 V.

It is very important to preserve the correct values of the other bits in R0x2C. The default register setting is 0x0004. This corresponds to 1.4 V − at this setting 1 mV input to the ADC equals approximately 1 LSB.

V_Step Voltage Reference

This voltage is used for pixel high dynamic range operations, programmable from R0x31 through R0x34 for Context A, or R0x39 through R0x3B for context B.

Chip Version

Chip version register R0x00 is read−only.

Window Control

Registers Column Start A/B, Row Start A/B, Window Height A/B (row size), and Window Width (column size) A/B control the size and starting coordinates of the window.

The values programmed in the window height and width registers are the exact window height and width out of the sensor. The window start value should never be set below four.

To read out the dark rows set bit 6 of R0x0D. In addition, bit 7 of R0x0D can be used to display the dark columns in the image. Note that there are Show Dark settings only for Context A.

Blanking Control

Horizontal Blank and Vertical Blank registers R0x05 and R0x06 (B: 0xCD and R0xCE), respectively, control the blanking time in a row (horizontal blanking) and between frames (vertical blanking).

- Horizontal blanking is specified in terms of pixel clocks.
- Vertical blanking is specified in terms of numbers of rows.

The actual imager timing can be calculated using Table 4 and Table 5 which describe "Row Timing and FV/LV signals".The minimum number of vertical blank rows is 4.

Pixel Integration Control

Total Integration

Total integration time is the result of coarse shutter width and fine shutter width registers, and depends also on whether manual or automatic exposure is selected.

The actual total integration time, t_{INT} is defined as:

$$t_{INT} - t_{INTCoarse} + t_{INTFint} \quad \text{(eq. 2)}$$

= (number of rows of integration x row time) + (number of pixels of integration x pixel time)

where:

Number of Rows of Integration
(Auto Exposure Control: Enabled)

When automatic exposure control (AEC) is enabled, the number of rows of integration may vary from frame to frame, with the limits controlled by R0xAC (minimum coarse shutter width) and R0xAD (maximum coarse shutter width).

Number of Rows of Integration
(Auto Exposure Control: Disabled)

If AEC is disabled, the number of rows of integration equals the value in R0x0B
or
If context B is enabled, the number of rows of integration equals the value in R0xD2.

Number of Pixels of Integration

The number of fine shutter width pixels is independent of AEC mode (enabled or disabled):

- Context A: the number of pixels of integration equals the value in R0xD5.
- Context B: the number of pixels of integration equals the value in R0xD8.

Row Timing

$$\text{Context A : Row time} = (\text{R0x04} + \text{R0x05}) \text{ master clock periods} \quad \text{(eq. 3)}$$

$$\text{Context B : Row time} = (\text{R0xCC} + \text{R0xCD}) \text{ master clock periods} \quad \text{(eq. 4)}$$

Typically, the value of the Coarse Shutter Width Total registers is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If the Coarse Shutter Width Total is increased beyond the total number of rows per frame, the user must add additional blanking rows using the Vertical Blanking registers as needed. See descriptions of the Vertical Blanking registers, R0x06 and R0xCE in Tables 1 and 2 of the MT9V034 register reference.

A second constraint is that tINT must be adjusted to avoid banding in the image from light flicker. Under 60 Hz flicker, this means the frame time must be a multiple of 1/120 of a second. Under 50 Hz flicker, the frame time must be a multiple of 1/100 of a second.

Changes to Integration Time

With automatic exposure control disabled (R0xAF[0] for context A, or R0xAF[8] for context B) and if the total integration time (R0x0B or R0xD2) is changed through the two−wire serial interface while FV is asserted for frame n, the first frame output using the new integration time is frame (n + 2). Similarly, when automatic exposure control is enabled, any change to the integration time for frame n first appears in frame (n + 2) output.

The sequence is as follows:

1. During frame *n*, the new integration time is held in the R0x0B or R0D2 live register.
2. Prior to the start of frame (n + 1) readout, the new integration time is transferred to the exposure control module. Integration for each row of frame (n + 1) has been completed using the old integration time. The earliest time that a row can start integrating using the new integration time is immediately after that row has been read for frame (n + 1). The actual time that rows start integrating using the new integration time is dependent on the new value of the integration time.
3. When frame (n + 2) is read out, it is integrated using the new integration time. If the integration time is changed (R0x0B or R0xD2 written) on successive frames, each value written is applied to a single frame; the latency between writing a value and it affecting the frame readout remains at two frames.

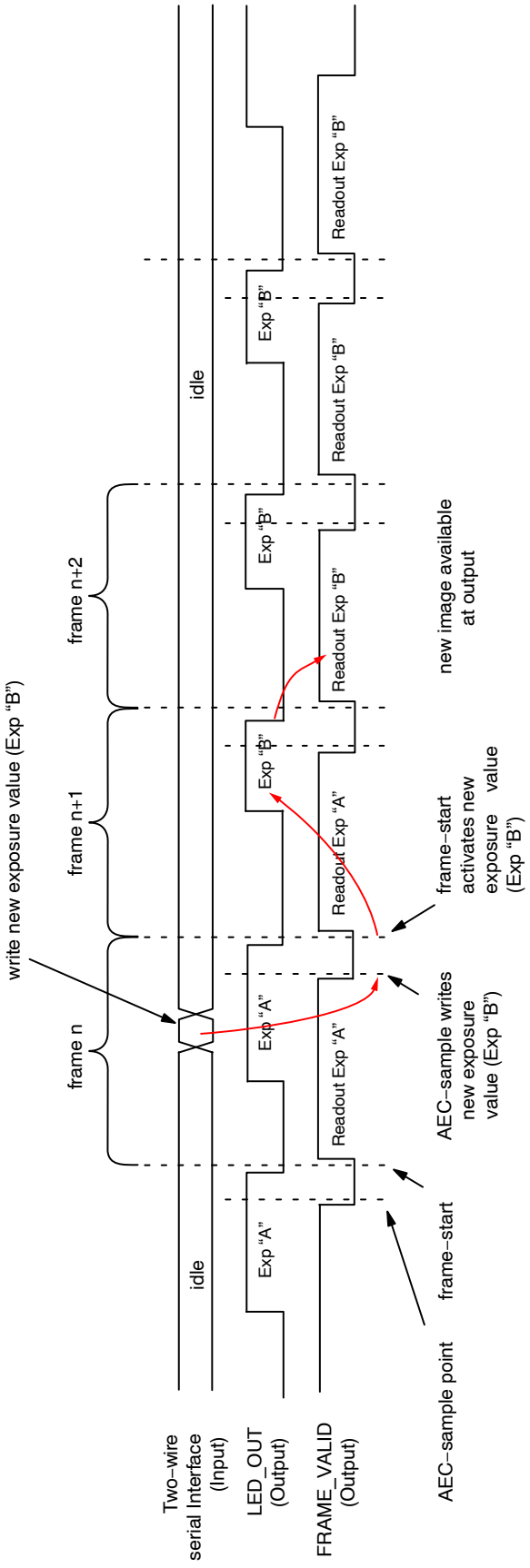


Figure 21. Latency of Exposure Register in Master Mode

Exposure Indicator

The exposure indicator is controlled by:

- R0x1B LED_OUT Control

The MT9V034 provides an output pin, LED_OUT, to indicate when the exposure takes place. When R0x1B bit 0 is clear, LED_OUT is HIGH during exposure. By using R0x1B, bit 1, the polarity of the LED_OUT pin can be inverted.

High Dynamic Range

High dynamic range is controlled by:

Table 9. HIGH DYNAMIC RANGE

	Context A	Context B
High Dynamic Enable	R0x0F[0]	R0x0F[8]
Shutter Width 1	R0x08	R0xCF
Shutter Width 2	R0x09	R0xD0
Shutter Width Control	R0x0A	R0xD1
V_Step Voltages	R0x31–R0x34	R0x39–R0x3C

In the MT9V034, high dynamic range (by setting R0x0F, bit 0 or 8 to 1) is achieved by controlling the saturation level of the pixel (HDR or high dynamic range gate) during the exposure period. The sequence of the control voltages at the HDR gate is shown in Figure 22. After the pixels are reset, the step voltage, V_Step, which is applied to HDR gate, is set up at V1 for integration time t_1, then to V2 for time t_2, then V3 for time t_3, and finally it is parked at V4, which also serves as an antiblooming voltage for the photodetector. This sequence of voltages leads to a piecewise linear pixel response, illustrated (approximately) in Figure 22 and Figure 23.

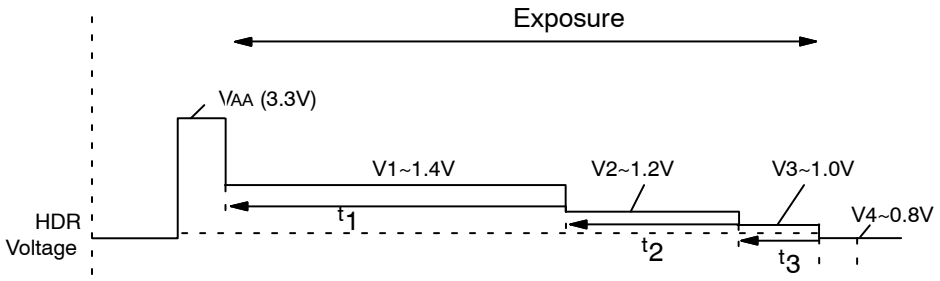


Figure 22. Sequence of Control Voltages at the HDR Gate

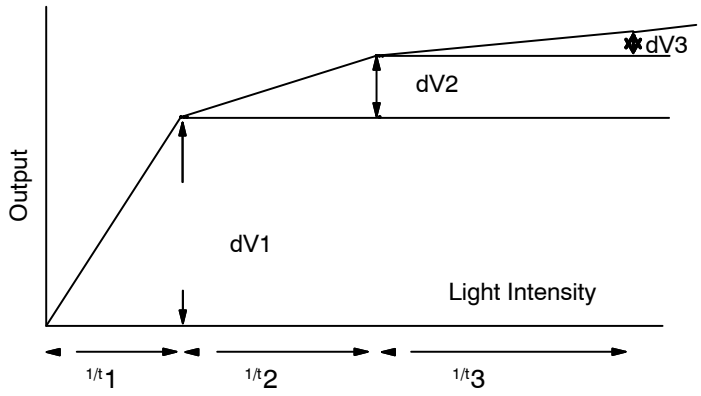


Figure 23. Sequence of Voltages in a Piecewise Linear Pixel Response

The parameters of the step voltage V_Step which take values V1, V2, and V3 directly affect the position of the knee points in Figure 23.

Light intensities work approximately as a reciprocal of the partial exposure time. Typically, t1 is the longest exposure, $^{t}2$ shorter, and so on. Thus the range of light intensities is shortest for the first slope, providing the highest sensitivity.

The register settings for V_Step and partial exposures are:

- V1 = R0x31, bits 5:0 (Context B: R0x39, bits 5:0)
- V2 = R0x32, bits 5:0 (Context B: R0x3A, bits 5:0)
- V3 = R0x33, bits 5:0 (Context B: R0x3B, bits 5:0)
- V4 = R0x34, bits 5:0 (Context B: R0x3C, bits 5:0)
- $^{t}INT = {}^{t}1 + {}^{t}2 + {}^{t}3$

There are two ways to specify the knee points timing, the first by manual setting and the second by automatic knee point adjustment. Knee point auto adjust is controlled for context A by R0x0A[8] (where default is ON), and for context B by R0xD1[8] (where default is OFF).

When the knee point auto adjust enabler is enabled (set HIGH), the MT9V034 calculates the knee points automatically using the following equations:

$$t_1 = {}^{t}INT - t_2 - t_3 \quad \text{(eq. 5)}$$

$$t_2 = {}^{t}INT \times (1/2)^{R0x0A[3:0] \text{ or } R0xD1[3:0]} \quad \text{(eq. 6)}$$

$$t_2 = {}^{t}INT \times (1/2)^{R0x0A[7:4] \text{ or } R0xD1[7:4]} \quad \text{(eq. 7)}$$

As a default for auto exposure, $^{t}2$ is 1/16 of ^{t}INT, $^{t}3$ is 1/64 of ^{t}INT.

When the auto adjust enabler is disabled (set LOW), *$^{t}1$, $^{t}2$,* and *$^{t}3$* may be programmed through the two−wire serial interface:

$$t_1 = \text{Coarse SW1 (row − times)} + \text{Fine SW1 (pixel − times)} \quad \text{(eq. 8)}$$

$$t_2 = \text{Coarse SW2} - \text{Coarse SW1} + \text{Fine SW2} - \text{Fine SW1} \quad \text{(eq. 9)}$$

$$t_3 = \text{Total Integration} - t_1 - t_2 = \text{Coarse Total Shutter Width} + \text{Fine Shutter Width Total} - t_1 - t_2 \quad \text{(eq. 10)}$$

For context A these become:

$$t_1 = \text{R0x08} + \text{R0xD3} \quad \text{(eq. 11)}$$

$$t_2 = \text{R0x09} - \text{ROx08} + \text{R0xD4} - \text{R0xD3} \quad \text{(eq. 12)}$$

$$t_3 = \text{R0x0B} + \text{R0xD4} - t_1 - t_2 \quad \text{(eq. 13)}$$

For context B these are:

$$t_1 = \text{R0xCF} + \text{R0xD6} \quad \text{(eq. 14)}$$

$$t_2 = \text{R0xD0} - \text{ROxCF} + \text{R0xD7} - \text{R0xD6} \quad \text{(eq. 15)}$$

$$t_3 = \text{R0xD2} + \text{R0xD8} - t_1 - t_2 \quad \text{(eq. 16)}$$

In all cases above, the coarse component of total integration time may be based on the result of AEC or values in Reg0x0B and Reg0xD2, depending on the settings.

Similar to Fine Shutter Width Total registers, the user must not set the Fine Shutter Width 1 or Fine Shutter Width 2 register to exceed the row time (Horizontal Blanking + Window Width). The absolute maximum value for the Fine Shutter Width registers is 1774 master clocks.

ADC Companding Mode

By default, ADC resolution of the sensor is 10−bit. Additionally, a companding scheme of 12−bit into 10−bit is enabled by the ADC Companding Mode register. This mode allows higher ADC resolution, which means less quantization noise at low−light, and lower resolution at high light, where good ADC quantization is not so critical because of the high level of the photon's shot noise.

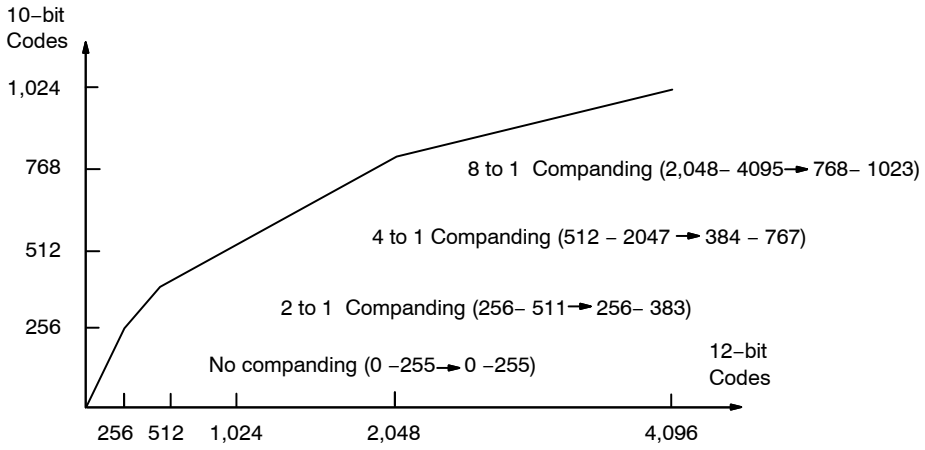


Figure 24. 12− to 10−Bit Companding Chart

Gain Settings

Changes to Gain Settings

When the analog gain (R0x35 for context A or R0x36 for context B) or the digital gain settings (R0x80-R0x98) are changed, the gain is updated on the next frame start. The gain setting must be written before the frame boundary to take effect the next frame. The frame boundary is slightly after the falling edge of Frame_Valid. In Figure 25 this is shown by the dashed vertical line labeled Frame Start.

Both analog and digital gain change regardless of whether the integration time is also changed simultaneously. Digital gain will change as soon as the register is written.

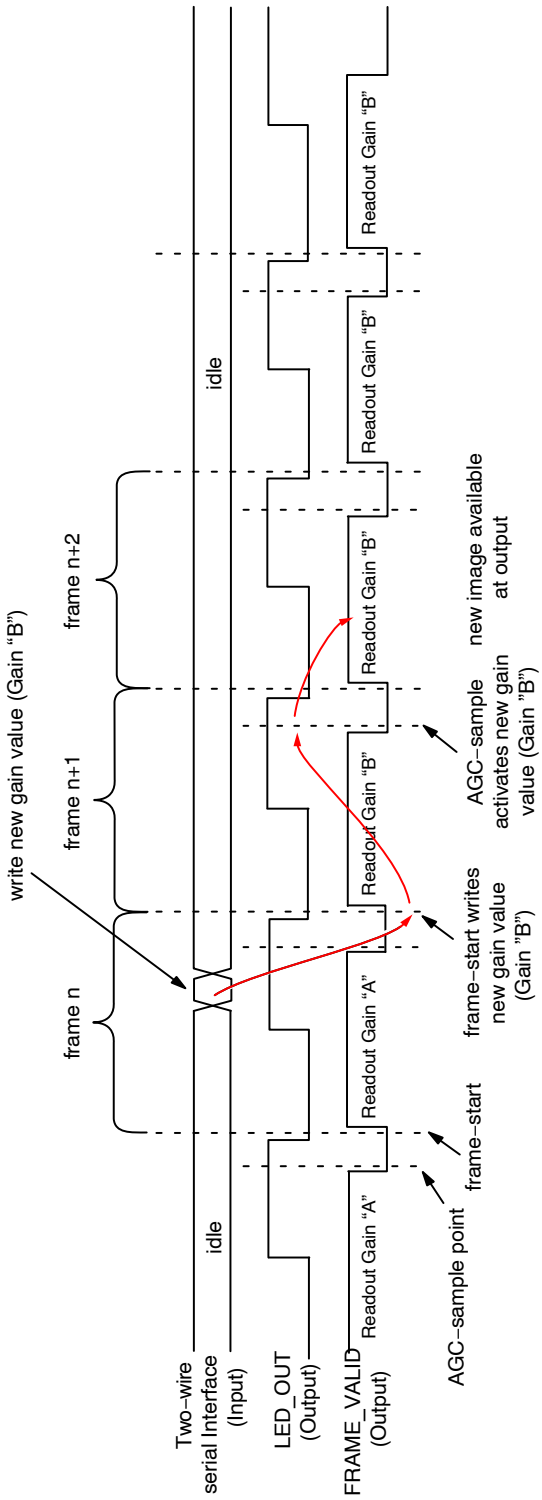


Figure 25. Latency of Gain Register(s) in Master Mode

Analog Gain

Analog gain is controlled by:

- R0x35 Global Gain context A
- R0x36 Global Gain context B

The formula for gain setting is:

$$\text{Gain} = \text{Bits}[6:0] \times 0.0625 \quad \text{(eq. 17)}$$

The analog gain range supported in the MT9V034 is 1X-4X with a step size of 6.25%. To control gain manually with this register, the sensor must NOT be in AGC mode. When adjusting the luminosity of an image, it is recommended to alter exposure first and yield to gain increases only when the exposure value has reached a maximum limit.

- Analog gain = bits (6:0) x 0.0625 for values 16−31
- Analog gain = bits (6:0)/2 x 0.125 for values 32−64

For values 16−31: each LSB increases analog gain 0.0625 v/v. A value of 16 = 1X gain. Range: 1X to 1.9375X.

For values 32−64: each 2 LSB increases analog gain 0.125 v/v (that is, double the gain increase for 2 LSB). Range: 2X to 4X. Odd values do not result in gain increases; the gain increases by 0.125 for values 32, 34, 36, and so on.

Digital Gain

Digital gain is controlled by:

- R0x99−R0xA4 Tile Coordinates
- R0x80−R0x98 Tiled Digital Gain and Weight

In the MT9V034, the gain logic divides the image into 25 tiles, as shown in Figure 25 The size and gain of each tile can be adjusted using the above digital gain control registers. Separate tile gains can be assigned for context A and context B.

Registers 0x99−0x9E and 0x9F−0xA4 represent the coordinates X0/5−X5/5 and Y0/5−Y5/5 in Figure 25, respectively.

Digital gains of registers 0x80−0x98 apply to their corresponding tiles. The MT9V034 supports a digital gain of 0.25−3.75X.

When binning is enabled, the tile offsets maintain their absolute values; that is, tile coordinates do not scale with row or column bin setting. Digital gain is applied as soon as register is written.

NOTE: There is one exception, for the condition when Column Bin 4 is enabled (R0x0D[3:2] or R0x0E[3:2] = 2). For this case, the value for Digital Tile Coordinate X−direction must be doubled.

The formula for digital gain setting is:

$$\text{Digital Gain} = \text{Bits}[3:0] \times 0.25 \quad \text{(eq. 18)}$$

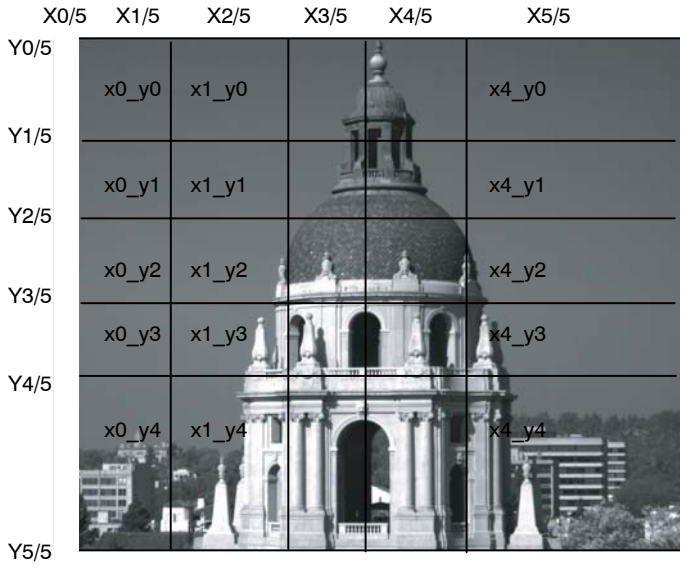


Figure 26. Tiled Sample

Black Level Calibration

Black level calibration is controlled by:

- Frame Dark Average: R0x42
- Dark Average Thresholds: R0x46
- Black Level Calibration Control: R0x47
- Black Level Calibration Value: R0x48
- Black Level Calibration Value Step Size: R0x4C

The MT9V034 has automatic black level calibration on−chip, and if enabled, its result may be used in the offset correction shown in Figure 27.

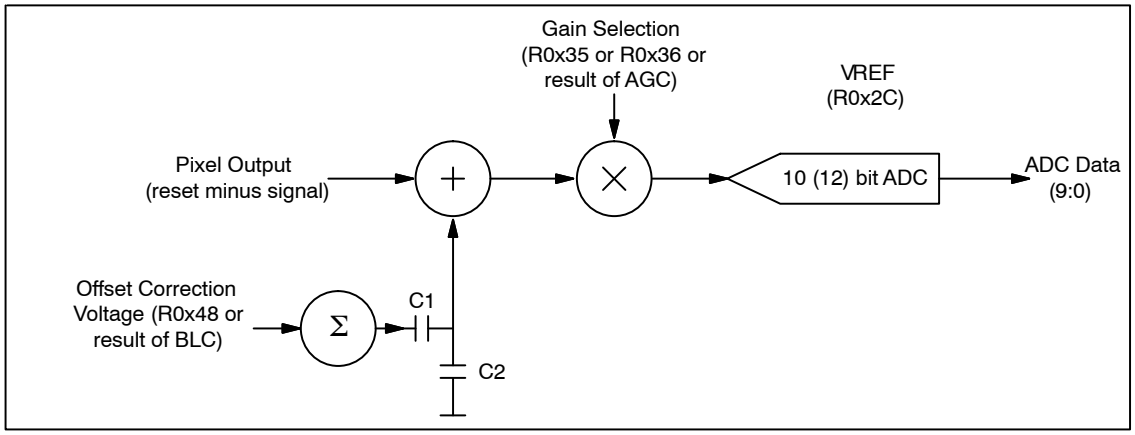


Figure 27. Black Level Calibration Flow Chart

The automatic black level calibration measures the average value of pixels from two dark rows (1 dark row if row bin 4 is enabled) of the chip. (The pixels are averaged as if they were light−sensitive and passed through the appropriate gain.)

This row average is then digitally low−pass filtered over many frames (R0x47, bits 7:5) to remove temporal noise and random instabilities associated with this measurement.

Then, the new filtered average is compared to a minimum acceptable level, low threshold, and a maximum acceptable level, high threshold.

If the average is lower than the minimum acceptable level, the offset correction voltage is increased by a programmable offset LSB in R0x4C. (Default step size is 2 LSB Offset = 1 ADC LSB at analog gain = 1X.)

If it is above the maximum level, the offset correction voltage is decreased by 2 LSB (default).

To avoid oscillation of the black level from below to above, the region the thresholds should be programmed so the difference is at least two times the offset DAC step size.

In normal operation, the black level calibration value/offset correction value is calculated at the beginning of each frame and can be read through the two−wire serial interface from R0x48. This register is an 8−bit signed two's complement value.

However, if R0x47, bit 0 is set to "1," the calibration value in R0x48 is used rather than the automatic black level calculation result. This feature can be used in conjunction with the "show dark rows" feature (R0x0D[6]) if using an external black level calibration circuit.

The offset correction voltage is generated according to the following formulas:

$$\text{Offset Correction Voltage} = (8 - \text{bit signed two's complement calibration value}, -127 \text{ to } 127) \times 0.25 \text{ mV} \quad \text{(eq. 19)}$$

$$\text{ADC input voltage} = (\text{Pixel Output Voltage}) \times \text{Analog Gain} + \text{Offset Correction Voltage} \times (\text{Analog Gain} + 1) \quad \text{(eq. 20)}$$

Defective Pixel Correction

Defective pixel correction is intended to compensate for defective pixels by replacing their value with a value based on the surrounding pixels, making the defect less noticeable to the human eye. The locations of defective pixels are stored in a ROM on chip during the manufacturing process; the maximum number of defects stored is 32. There is no provision for later augmenting the table of programmed defects. In the defect correction block, bad pixels will be substituted by either the average of its neighboring pixels, or its nearest−neighbor pixel, depending on pixel location.

Defective Pixel Correction is enabled by R0x07[9]. By default, correction is enabled, and pixels mapped in internal ROM are replaced with corrected values. This might be unacceptable to some applications, in which case pixel correction should be disabled (R0x07[9] = 0).

Row−wise Noise Correction

Row−wise noise correction is controlled by the following registers:

- R0x70 Row Noise Control
- R0x72 Row Noise Constant

Row−wise noise cancellation is performed by calculating a row average from a set of optically black pixels at the start of each row and then applying each average to all the active pixels of the row. Read Dark Columns register bit and Row Noise Correction Enable register bit must both be set to enable row−wise noise cancellation to be performed. The behavior when Read Dark Columns register bit = 0 and Row Noise Correction Enable register bit = 1 is undefined.

The algorithm works as follows:

Logical columns 755−790 in the pixel array provide 36 optically black pixel values. Of the 36 values, two smallest value and two largest values are discarded. The remaining 32 values are averaged by summing them and discarding the 5 LSB of the result. The 10−bit result is subtracted from each pixel value on the row in turn. In addition, a positive constant will be added (Reg0x71, bits 7:0). This constant should be set to the dark level targeted by the black level algorithm plus

the noise expected on the measurements of the averaged values from dark columns; it is meant to prevent clipping from negative noise fluctuations.

$$\text{Pixel value} = \text{ADC value} - \text{dark column average} + \text{R0x71[9 : 0]} \quad \text{(eq. 21)}$$

Note that this algorithm does not work in color sensor.

Automatic Gain Control and Automatic Exposure Control

The integrated AEC/AGC unit is responsible for ensuring that optimal auto settings of exposure and (analog) gain are computed and updated every frame.

AEC and AGC can be individually enabled or disabled by R0xAF. When AEC is disabled (R0xAF[0] = 0), the sensor uses the manual exposure value in coarse and fine shutter width registers. When AGC is disabled (R0xAF[1] = 0), the sensor uses the manual gain value in R0x35 or R0x36. See "Pixel Integration Control" and the MT9V034 Developer Guide, for more information.

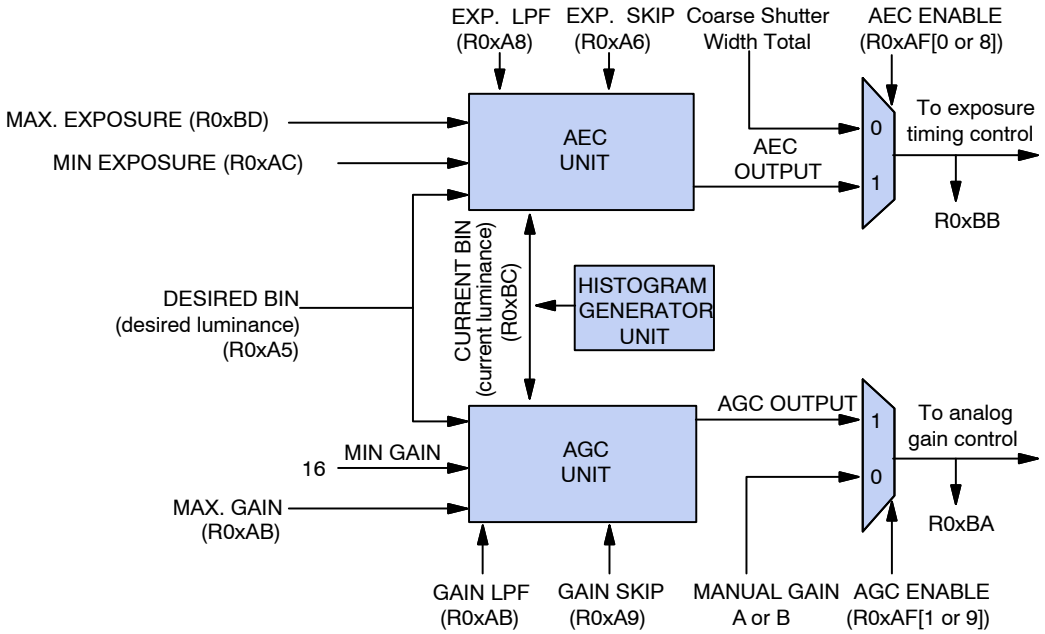


Figure 28. Controllable and Observable AEC/AGC Registers

The exposure is measured in row−time by reading R0xBB. The exposure range is 1 to 2047. The gain is measured in gain−units by reading R0xBA. The gain range is 16 to 63 (unity gain = 16 gain−units; multiply by 1/16 to get the true gain).

When AEC is enabled (R0xAF), the maximum auto exposure value is limited by R0xBD; minimum auto exposure is limited by AEC Minimum Exposure, R0xAC.

NOTE: AEC does not support sub−row timing; calculated exposure values are rounded down to the nearest row−time. For smoother response, manual control is recommended for short exposure times.

When AGC is enabled (R0xAF), the maximum auto gain value is limited by R0xAB; minimum auto gain is fixed to 16 gain−units.

The exposure control measures current scene luminosity and desired output luminosity by accumulating a histogram of pixel values while reading out a frame. All pixels are used, whether in color or mono mode. The desired exposure and gain are then calculated from this for subsequent frame.

When binning is enabled, tuning of the AEC may be required. The histogram pixel count register, R0xB0, may be adjusted to reflect reduced pixel count. Desired bin register, R0xA5, may be adjusted as required.

Pixel Clock Speed

The pixel clock speed is same as the master clock (SYSCLK) at 26.66 MHz by default. However, when column binning 2 or 4 (R0x0D or R0x0E, bit 2 or 3) is enabled, the pixel clock speed is reduced by half and one−fourth of the master clock speed respectively. See "Read Mode Options" and "Column Binning" for additional information.

Hard Reset of Logic

The RC circuit for the MT9V034 uses a 10 kΩ resistor and a 0.1 µF capacitor. The rise time for the RC circuit is 1µs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by:

- R0x0C Reset

Bit 0 is used to reset the digital logic of the sensor while preserving the existing two−wire serial interface configuration. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. Bit 1 is a shadowed reset control register bit to explicitly reset the automatic gain and exposure control feature.

These two bits are self−resetting bits and also return to "0" during two−wire serial interface reads.

STANDBY Control

The sensor goes into standby mode by setting STANDBY to HIGH. Once the sensor detects that STANDBY is asserted, it completes the current frame before disabling the digital logic, internal clocks, and analog power enable signal. To release the sensor out from the standby mode, reset STANDBY back to LOW. The LVDS must be powered to ensure that the device is in standby mode. See "Appendix A − Power−On Reset and Standby Timing" for more information on standby.

Monitor Mode Control

Monitor mode is controlled by:

- R0xD9 Monitor Mode Enable
- R0xC0 Monitor Mode Image Capture Control

The sensor goes into monitor mode when R0xD9[0] is set to HIGH. In this mode, the sensor first captures a programmable number of frames (R0xC0), then goes into a sleep period for five minutes. The cycle of sleeping for five minutes and waking up to capture a number of frames continues until R0xD9[0] is cleared to return to normal operation.

In some applications when monitor mode is enabled, the purpose of capturing frames is to calibrate the gain and exposure of the scene using automatic gain and exposure control feature. This feature typically takes less than 10 frames to settle. In case a larger number of frames is needed, the value of R0xC0 may be increased to capture more frames.

During the sleep period, none of the analog circuitry and a very small fraction of digital logic (including a five−minute timer) is powered. The master clock (SYSCLK) is therefore always required.

Read Mode Options

(Also see "Output Data Format" and "Output Data Timing").

Column Flip

By setting bit 5 of R0x0D or R0x0E the readout order of the columns is reversed, as shown in Figure 29.

Row Flip

By setting bit 4 of R0x0D or R0x0E the readout order of the rows is reversed, as shown in Figure 30.

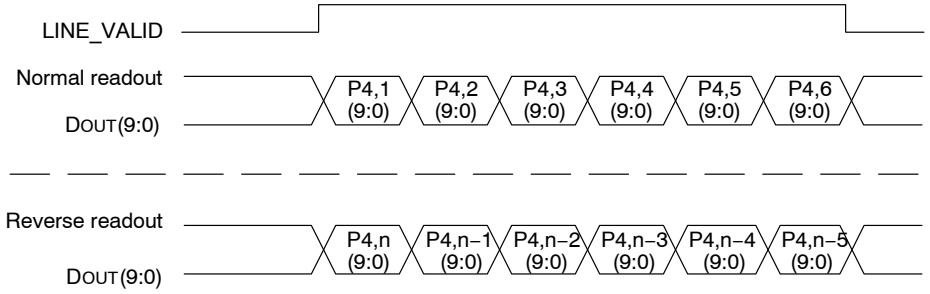


Figure 29. Readout of Six Pixels in Normal and Column Flip Output Mode

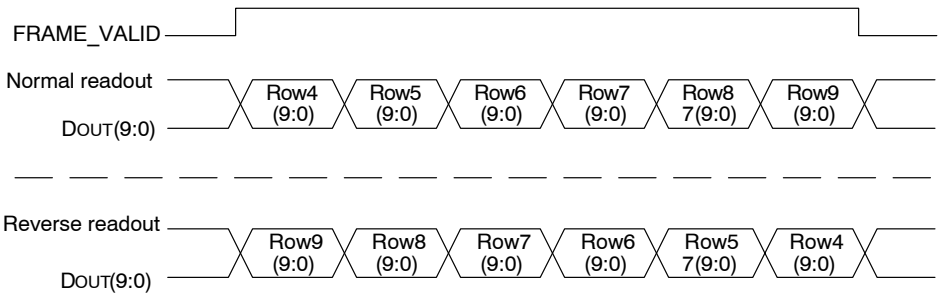


Figure 30. Readout of Six Rows in Normal and Row Flip Output Mode

Pixel Binning

In addition to windowing mode in which smaller resolutions (CIF, QCIF) are obtained by selecting a smaller window from the sensor array, the MT9V034 also provides the ability to down−sample the entire image captured by the pixel array using pixel binning.

There are two resolution options: binning 2 and binning 4, which reduce resolution by two or by four, respectively. Row and column binning are separately selected. Image mirroring options will work in conjunction with binning.

For column binning, either two or four columns are combined by averaging to create the resulting column. For row binning, the binning result value depends on the difference in pixel values: for pixel signal differences of less than 200 LSBs, the result is the average of the pixel values. For pixel differences of greater than 200 LSBs, the result is the value of the darker pixel value.

Binning operation increases SNR but decreases resolution. Enabling row bin2 and row bin4 improves frame rate by 2x and 4x respectively. Column binning does not increase the frame rate.

Row Binning

By setting bit 0 or 1 of R0x0D or R0x0E, only half or one−fourth of the row set is read out, as shown in Figure 30. The number of rows read out is half or one−fourth of the value set in R0x03. The row binning result depends on the difference in pixel values: for pixel signal differences less than 200 LSB's, the result is the average of the pixel values.

For pixel differences of 200 LSB's or more, the result is the value of the darker pixel value.

Column Binning

For column binning, either two or four columns are combined by averaging to create the result. In setting bit 2 or 3 of R0x0D or R0x0E, the pixel data rate is slowed down by a factor of either two or four, respectively. This is due to the overhead time in the digital pixel data processing chain. As a result, the pixel clock speed is also reduced accordingly.

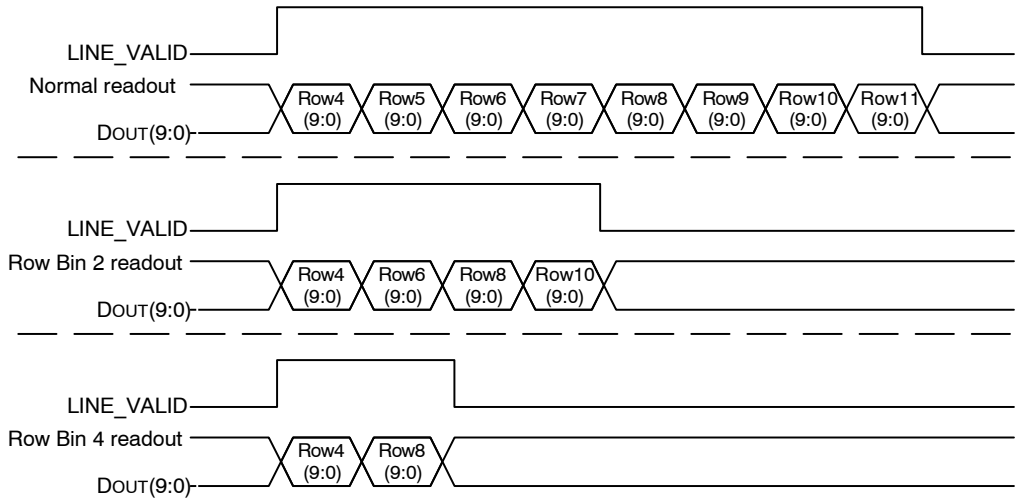


Figure 31. Readout of 8 Pixels in Normal and Row Bin Output Mode

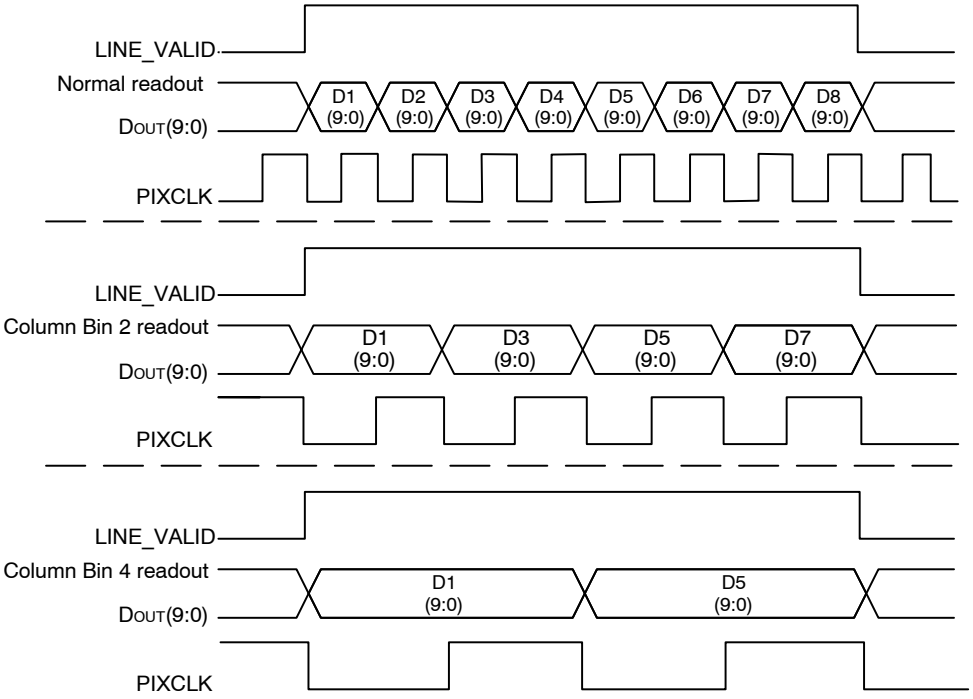


Figure 32. Readout of 8 Pixels in Normal and Column Bin Output Mode

Interlaced Readout

The MT9V034 has two interlaced readout options. By setting R0x07[2:0] = 1, all the even−numbered rows are read out first, followed by a number of programmable field blanking rows (set by R0xBF[7:0]), then the odd−numbered rows, and finally the vertical blanking rows. By setting R0x07[2:0] = 2 only one field row is read out.

Consequently, the number of rows read out is half what is set in the window height register. The row start register determines which field gets read out; if the row start register is even, then the even field is read out; if row start address is odd, then the odd field is read out.

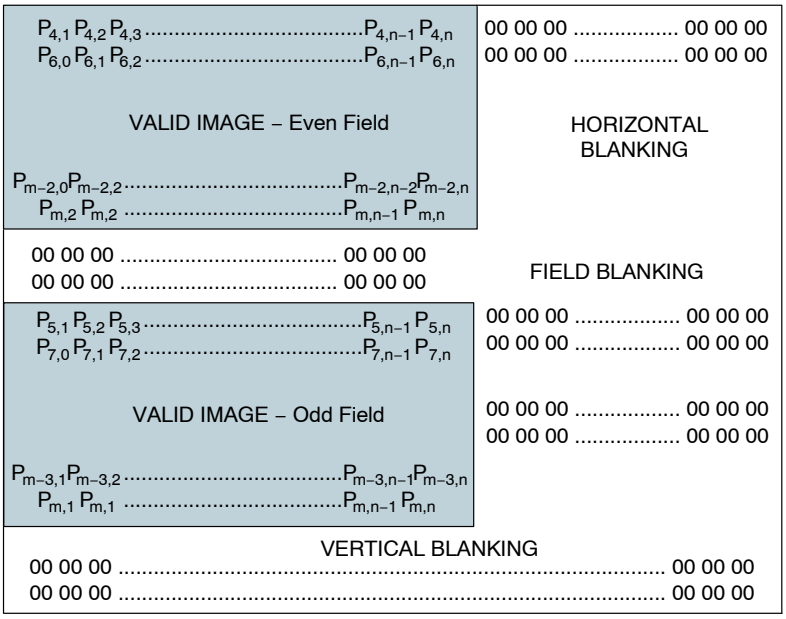


Figure 33. Spatial Illustration of Interlaced Image Readout

When interlaced mode is enabled, the total number of blanking rows are determined by both Field Blanking register (R0xBF) and Vertical Blanking register (R0x06 or R0xCE). The followings are their equations.

$$\text{Field Blanking} = \text{R0xBF[7 : 0]} \quad \text{(eq. 22)}$$

$$\text{Vertical Blanking} = \text{R0x06[8 : 0]} - \text{R0xBF[7 : 0] (contextA) or R0xCE[8 : 0]} - \text{R0xBF[7 : 0] (contextB)} \quad \text{(eq. 23)}$$

with

$$\text{minimum vertical blanking requirement} = 4 \text{ (absolute minimum operate; see Vertical Blanking Registers description for VBlank minimums for valid image output)} \quad \text{(eq. 24)}$$

Similar to progressive scan, FV is logic LOW during the valid image row only. Binning should not be used in conjunction with interlaced mode.

LINE_VALID

By setting bit 2 and 3 of R0x72, the LV signal can get three different output formats. The formats for reading out four rows and two vertical blanking rows are shown in Figure 34. In the last format, the LV signal is the XOR between the continuous LV signal and the FV signal.

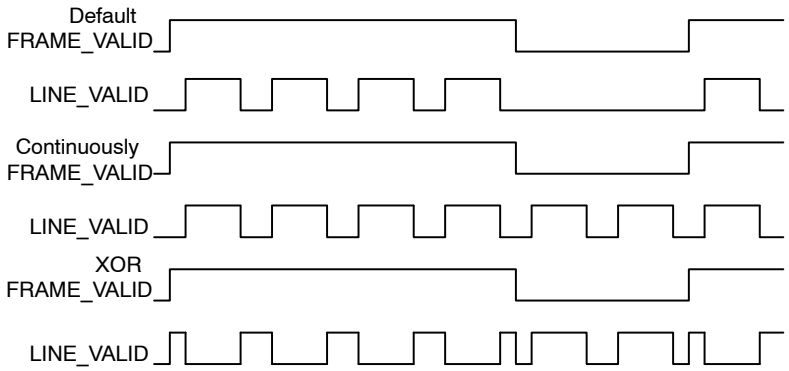


Figure 34. Different LINE_VALID Formats

LVDS Serial (Stand−Alone/Stereo) Output

The LVDS interface allows for the streaming of sensor data serially to a standard off−the−shelf deserializer up to eight meters away from the sensor. The pixels (and controls) are packeted−12−bit packets for stand−alone mode and 18−bit packets for stereoscopy mode. All serial signalling (CLK and data) is LVDS. The LVDS serial output could either be data from a single sensor (stand−alone) or stream−merged data from two sensors (self and its stereoscopic slave pair). The appendices describe in detail the topologies for both stand−alone and stereoscopic modes.

There are two standard deserializers that can be used. One for a stand−alone sensor stream and the other from a stereoscopic stream. The deserializer attached to a stand−alone sensor is able to reproduce the standard parallel output (8−bit pixel data, LV, FV, and PIXCLK). The deserializer attached to a stereoscopic sensor is able to reproduce 8−bit pixel data from each sensor (with embedded LV and FV) and pixel−clk. An additional (simple) piece of logic is required to extract LV and FV from the 8−bit pixel data. Irrespective of the mode (stereoscopy/stand−alone), LV and FV are always embedded in the pixel data.

In stereoscopic mode, the two sensors run in lock−step, implying all state machines are in the same state at any given time. This is ensured by the sensor−pair getting their sys−clks and sys−resets in the same instance. Configuration writes through the two−wire serial interface are done in such a way that both sensors can get their configuration updates at once. The inter−sensor serial link is designed in such a way that once the slave PLL locks and the data−dly, shft−clk−dly and stream−latency−sel are configured, the master sensor streams valid stereo content irrespective of any variation voltage and/or temperature as long as it is within specification. The configuration values of data−dly, shft−clk−dly and stream−latency−sel are either predetermined from the board−layout or can be empirically determined by reading back the stereo−error flag. This flag is asserted when the two sensor streams are not in sync when merged. The combo_reg is used for out−of−sync diagnosis.

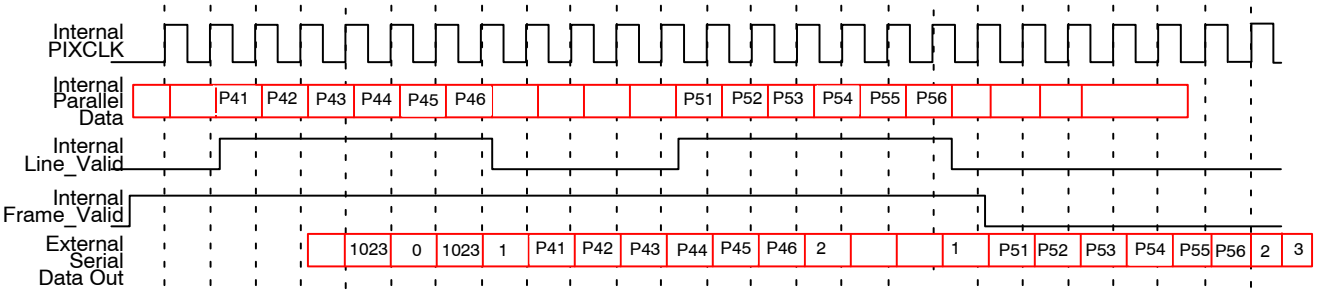


Figure 35. Serial Output Format for a 6x2 Frame

1. External pixel values of 0, 1, 2, 3, are reserved (they only convey control information). Any raw pixel of value 0, 1, 2 and 3 will be substituted with 4.
2. The external pixel sequence 1023, 0, 1023 is a reserved sequence (conveys control information for legacy support of MT9V021 applications). Any raw pixel sequence of 1023, 0, 1023 will be substituted with an output serial stream of 1023, 4, 1023.

LVDS Output Format

In stand−alone mode, the packet size is 12 bits (2 frame bits and 10 payload bits); 10−bit pixels or 8−bit pixels can be selected. In 8−bit pixel mode (R0xB6[0] = 0), the packet consists of a start bit, 8−bit pixel data (with sync codes), the line valid bit, the frame valid bit and the stop bit. For 10−bit pixel mode (R0xB6[0] = 1), the packet consists of a start bit, 10−bit pixel data, and the stop bit.

Table 10. LVDS PACKET FORMAT IN STAND−ALONE MODE (Stereoscopy Mode Bit De−Asserted)

12−Bit Packet	use_10−bit_pixels Bit De−Asserted (8−Bit Mode)	use_10−bit_pixels Bit Asserted (10−Bit Mode)
Bit[0]	1'b1 (Start bit)	1'b1 (Start bit)
Bit[1]	PixelData[2]	PixelData[0]
Bit2]	PixelData[3]	PixelData[1]
Bit[3]	PixelData[4]	PixelData[2]
Bit4]	PixelData[5]	PixelData[3]
Bit[5]	PixelData[6]	PixelData[4]
Bit[6]	PixelData[7]	PixelData[5]
Bit[7]	PixelData[8]	PixelData[6]
Bit[8]	PixelData[9]	PixelData[7]
Bit[9]	Line_Valid	PixelData[8]
Bit[10]	Frame_Valid	PixelData[9]
Bit[11]	1'b0 (Stop bit)	1'b0 (Stop bit)

In stereoscopic mode, the packet size is 18 bits (2 frame bits and 16 payload bits). The packet consists of a start bit, the master pixel byte (with sync codes), the slave byte (with sync codes), and the stop bit.)

Table 11. LVDS PACKET FORMAT IN STEREOSCOPY MODE (Stereoscopy Mode Bit Asserted)

18−bit Packet	Function
Bit[0]	1'b1 (Start bit)
Bit[1]	MasterSensorPixelData[2]
Bit[2]	MasterSensorPixelData[3]
Bit[3]	MasterSensorPixelData[4]
Bit[4]	MasterSensorPixelData[5]
Bit[5]	MasterSensorPixelData[6]
Bit[6]	MasterSensorPixelData[7]
Bit[7]	MasterSensorPixelData[8]
Bit[8]	MasterSensorPixelData[9]
Bit[9]	SlaveSensorPixelData[2]
Bit[10]	SlaveSensorPixelData[3]
Bit[11]	SlaveSensorPixelData[4]
Bit[12]	SlaveSensorPixelData[5]
Bit[13]	SlaveSensorPixelData[6]
Bit[14]	SlaveSensorPixelData[7]
Bit[15]	SlaveSensorPixelData[8]
Bit[16]	SlaveSensorPixelData[9]
Bit[17]	1'b0 (Stop bit)

Control signals LV and FV can be reconstructed from their respective preceding and succeeding flags that are always embedded within the pixel data in the form of reserved words.

Table 12. RESERVED WORDS IN THE PIXEL DATA STREAM

Pixel Data Reserved Word	Flag
0	Precedes frame valid assertion
1	Precedes line valid assertion
2	Succeeds line valid de−assertion
3	Succeeds frame valid de−assertion

When LVDS mode is enabled along with column binning (bin 2 or bin 4, R0x0D[3:2], the packet size remains the same but the serial pixel data stream repeats itself depending on whether 2X or 4X binning is set:

- For bin 2, LVDS outputs double the expected data (post−binning pixel 0,0 is output twice in sequence, followed by pixel 0,1 twice, …).
- For bin 4, LVDS outputs 4 times the expected data (pixel 0,0 is output 4 times in sequence followed by pixel 0,1 times 4, …).

The receiving hardware will need to undersample the output stream, getting data either every 2 clocks (bin 2) or every 4 (bin 4) clocks.

If the sensor provides a pixel whose value is 0,1, 2, or 3 (that is, the same as a reserved word) then the outgoing serial pixel value is switched to 4.

LVDS Enable and Disable

The Tables 13 and 14 further explain the state of the LVDS output pins depending on LVDS control settings. When the LVDS block is not used, it may be left powered down to reduce power consumption.

Table 13. SER_DATAOUT_* STATE

R0xB1[1] LVDS power down	R0xB3[4] LVDS data power down	SER_DATAOUT_*
0	0	Active
0	1	Active
1	0	Z
1	1	Z

Table 14. SHFT_CLK_* STATE

R0xB1[1] LVDS power down	R0xB2[4] LVDS shift−clk power down	SHFT_CLKOUT_*
0	0	Active
0	1	Z
1	0	Z
1	1	Z

5. ERROR pin: When the sensor is not in stereo mode, the ERROR pin is at LOW.

LVDS Data Bus Timing

The LVDS bus timing waveforms and timing specifications are shown in Table 15 and Figure 36.

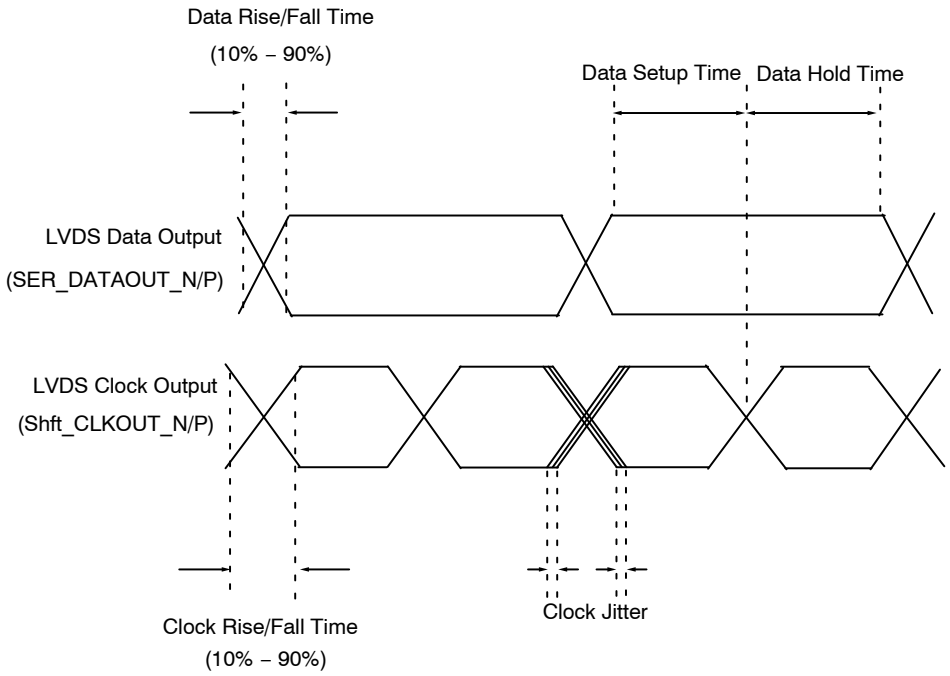


Figure 36. LVDS Timing

Table 15. LVDS AC TIMING SPECIFICATIONS

(V_{PWR} = 3.3 V ±0.3 V; TJ = – 30°C to +70°C; output load = 100 Ω; frequency 27 MHz)

Parameter	Min	Typ	Max	Unit
LVDS clock rise time	–	0.22	0.30	ns
LVDS clock fall time	–	0.22	0.30	ns
LVDS data rise time	–	0.28	0.30	ns
LVDS data fall time	–	0.28	0.30	ns
LVDS data setup time	0.3	0.67	–	ns
LVDS data hold time	0.1	1.34	–	ns
LVDS clock jitter	–		92	ps

ELECTRICAL SPECIFICATIONS

Table 16. DC ELECTRICAL CHARACTERISTICS OVER TEMPERATURE
(V_{PWR} = 3.3 V ±0.3 V; T_J = – 30°C to +70°C; Output Load = 10 pF; Frequency 13 MHz to 27 MHz; LVDS off)

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH voltage		V_{PWR} – 1.4	–		V
V_{IL}	Input LOW voltage			–	1.3	V
I_{IN}	Input leakage current	No pull–up resistor; V_{IN} = V_{PWR} or V_{GND}	–5	–	5	μA
V_{OH}	Output HIGH voltage	I_{OH} = –4.0 mA	V_{PWR} – 0.3	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 4.0 mA	–	–	0.3	V
I_{OH}	Output HIGH current	V_{OH} = V_{DD} – 0.7	–11	–	–	mA
I_{OL}	Output LOW current	V_{OL} = 0.7	–	–	11	mA
I_{PWR}A	Analog supply current	Default settings	–	12	20	mA
I_{PIX}	Pixel supply current	Default settings	–	1.1	3	mA
I_{PWR}D	Digital supply current	Default settings, C_{LOAD} = 10 pF	–	42	60	mA
I_{LVDS}	LVDS supply current	Default settings with LVDS on	–	13	16	mA
I_{PWR}A Standby	Analog standby supply current	STDBY = V_{DD}	–	0.2	3	μA
I_{PWR}D Standby Clock Off	Digital standby supply current with clock off	STDBY = V_{DD}, CLKIN = 0 MHz	–	0.1	10	μA
I_{PWR}D Standby Clock On	Digital standby supply current with clock on	STDBY = V_{DD}, CLKIN = 27 MHz	–	1	2	mA

Table 17. DC ELECTRICAL CHARACTERISTICS (V_{PWR} = 3.3 V ±0.3 V; T_A = Ambient = 25°C)

Symbol	Definition	Condition	Min	Typ	Max	Unit
LVDS Driver DC Specifications						
|V_{OD}|	Output differential voltage	Rload = 100 Ω + 1%	250	–	400	mV
|DV_{OD}|	Change in V_{OD} between complementary output states		–	–	50	mV
V_{OS}	Output offset voltage		1.0	1.2	1.4	V
DV_{OS}	Pixel array current		–	–	35	mV
I_{OS}	Digital supply current			±10		mA
I_{OZ}	Output current when driver is tri–state			±1		μA
LVDS Receiver DC Specifications						
Vidth+	Input differential	|V_{GPD}| < 925 mV	–100	–	100	mV
Iin	Input current		–	–	±20	μA

Table 18. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	−0.3	4.5	V
I_{SUPPLY}	Total power supply current	–	200	mA
I_{GND}	Total ground current	–	200	mA
V_{IN}	DC input voltage	−0.3	V_{DD} + 0.3	V
V_{OUT}	DC output voltage	−0.3	V_{DD} + 0.3	V
T_{STG}[1]	Storage temperature	−50	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19. AE ELECTRICAL CHARACTERISTICS

(V_{PWR} = 3.3 V ±0.3 V; T_J= −30°C to +70°C; Output Load = 10 pF)

Symbol	Definition	Condition	Min	Typ	Max	Unit
SYSCLK	Input clock frequency	Note 1	13.0	26.6	27.0	MHz
	Clock duty cycle		45.0	50.0	55.0	%
tR	Input clock rise time		–	3	5	ns
tF	Input clock fall time		–	3	5	ns
t_{PLHP}	SYSCLK to PIXCLK propagation delay	CLOAD = 10 pF	4	6	8	ns
tPD	PIXCLK to valid D_{OUT}(9:0) propagation delay	CLOAD = 10 pF	−3	0.6	3	ns
tSD	Data setup time		14	16	–	ns
tHD	Data hold time		14	16	–	
tPFLR	PIXCLK to LV propagation delay	CLOAD = 10 pF	5	7	9	ns
tPFLF	PIXCLK to FV propagation delay	CLOAD = 10 pF	5	7	9	ns

Propagation Delays for PIXCLK and Data Out Signals

The pixel clock is inverted and delayed relative to the master clock. The relative delay from the master clock (SYSCLK) rising edge to both the pixel clock (PIXCLK) falling edge and the data output transition is typically 7 ns. Note that the falling edge of the pixel clock occurs at approximately the same time as the data output transitions. See Table 19 for data setup and hold times.

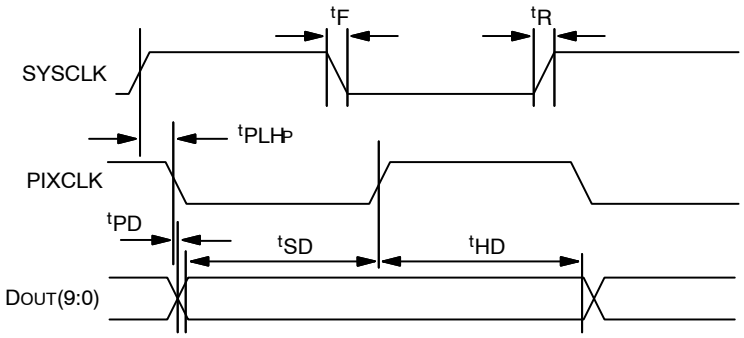


Figure 37. Propagation Delays for PIXCLK and Data Out Signals

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LV and FV signals change on the same rising master clock edge as the data output. The LV goes HIGH on the same rising master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock rising edge as the end of the output of the last valid pixel's data.

As shown in the “Output Data Timing”, FV goes HIGH 143 pixel clocks before the first LV goes HIGH. It returns LOW 23 pixel clocks after the last LV goes LOW.

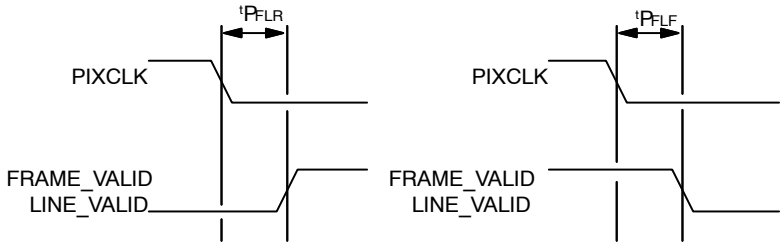


Figure 38. Propagation Delays for FRAME_VALID and LINE_VALID Signals

Two−Wire Serial Bus Timing

Detailed timing waveforms and parameters for the two−wire serial interface bus are shown in Figure 39 and Table 20.

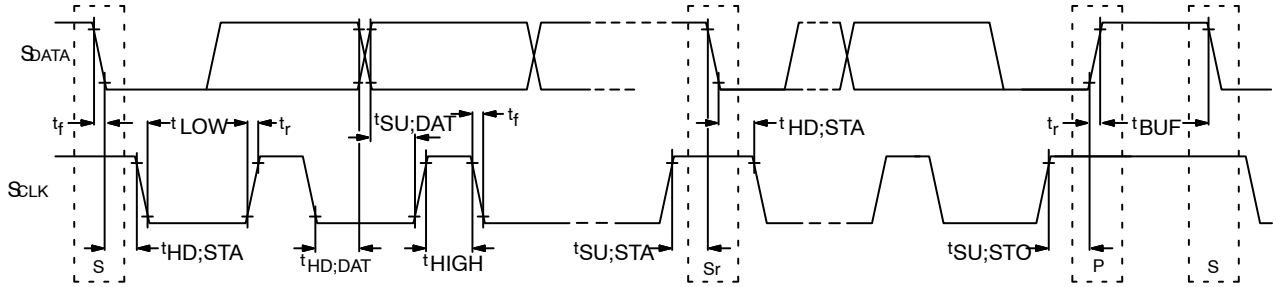


Figure 39. Two−Wire Serial Bus Timing Parameters

Table 20. TWO−WIRE SERIAL BUS CHARACTERISTICS (^{f}EXTCLK = 27 MHz; V_{PWR} = 3.3 V +0.3 V; T_A = 25°C)

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	fSCL	0	100	0	400	KHz
After this period, the first clock pulse is generated	tHD;STA	4.0	–	0.6	–	μs
LOW period of the SCLK clock	tLOW	4.7	–	1.3	–	μs
HIGH period of the SCLK clock	tHIGH	4.0	–	0.6	–	μs
Set−up time for a repeated START condition	tSU;STA	4.7	–	0.6	–	μs
Data hold time:	$t_{HD;DAT}$	0 (Note 10)	3.45 (Note 11)	0 (Note 12)	0.9 (Note 11)	μs
Data set−up time	tSU;DAT	250	–	100 (Note 12)	–	ns
Rise time of both SDATA and SCLK signals	tr	–	1000	20 + 0.1Cb (Note 13)	300	ns
Fall time of both SDATA and SCLK signals	tf	–	300	20 + 0.1Cb (Note 13)	300	ns
Set−up time for STOP condition	tSU;STO	4.0	–	0.6	–	μs
Bus free time between a STOP and START condition	tBUF	4.7	–	1.3	–	μs
Capacitive load for each bus line	Cb	–	400	–	400	pF
Serial interface input pin capacitance	CIN_SI	–	3.3	–	3.3	pF
SDATA max load capacitance	CLOAD_SD	–	30	–	30	pF
SDATA pull−up resistor	RSD	1.5	4.7	1.5	4.7	kΩ

7. This table is based on I2C standard (v2.1 January 2000). Philips Semiconductor.
8. Two−wire control is I2C−compatible.
9. All values referred to VIHmin = 0.9 VDD and VILmax = 0.1 VDD levels. Sensor EXCLK = 27 MHz.
10. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
11. The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
12. A Fast−mode I2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA linetr max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I2C−bus specification) before the SCLK line is released.
13. Cb = total capacitance of one bus line in pF.

Minimum Master Clock Cycles

In addition to the AC timing requirements described in Table 20, the two−wire serial bus operation also requires certain minimum master clock cycles between transitions. These are specified in Figures 40 through 45, in units of master clock cycles.

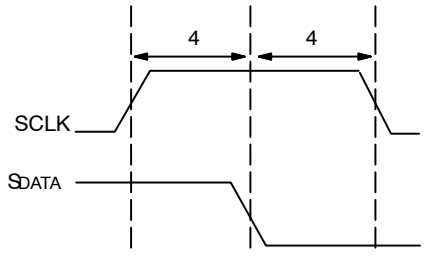
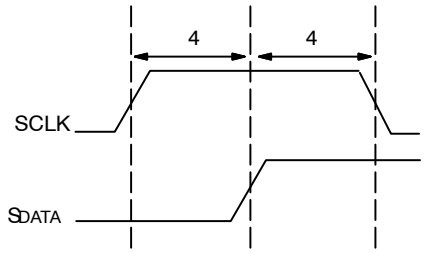
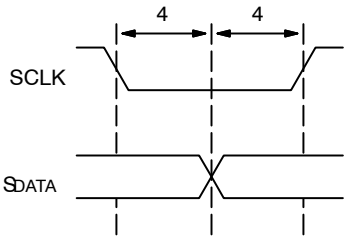


Figure 40. Serial Host Interface Start Condition Timing



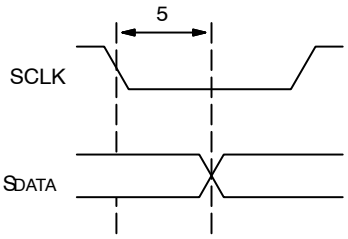
NOTE: All timing are in units of master clock cycle.

Figure 41. Serial Host Interface Stop Condition Timing



NOTE: SDATA is driven by an off−chip transmitter.

Figure 42. Serial Host Interface Data Timing for WRITE



NOTE: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull−up resistor off−chip.

Figure 43. Serial Host Interface Data Timing for Read

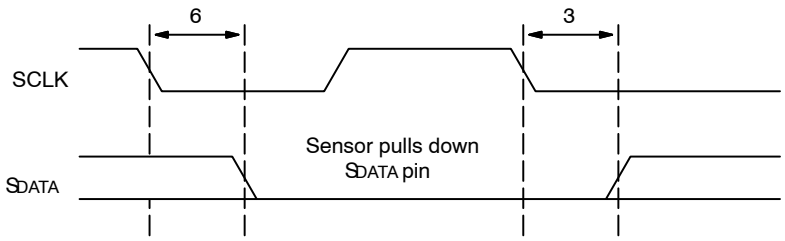
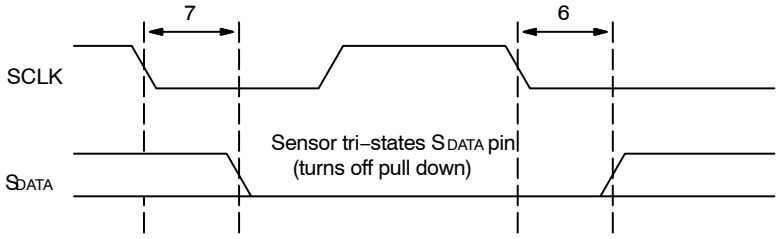


Figure 44. Acknowledge Signal Timing After an 8−Bit WRITE to the Sensor



NOTE: After a READ, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a “No Acknowledge” by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Figure 45. Acknowledge Signal Timing After an 8−Bit READ from the Sensor

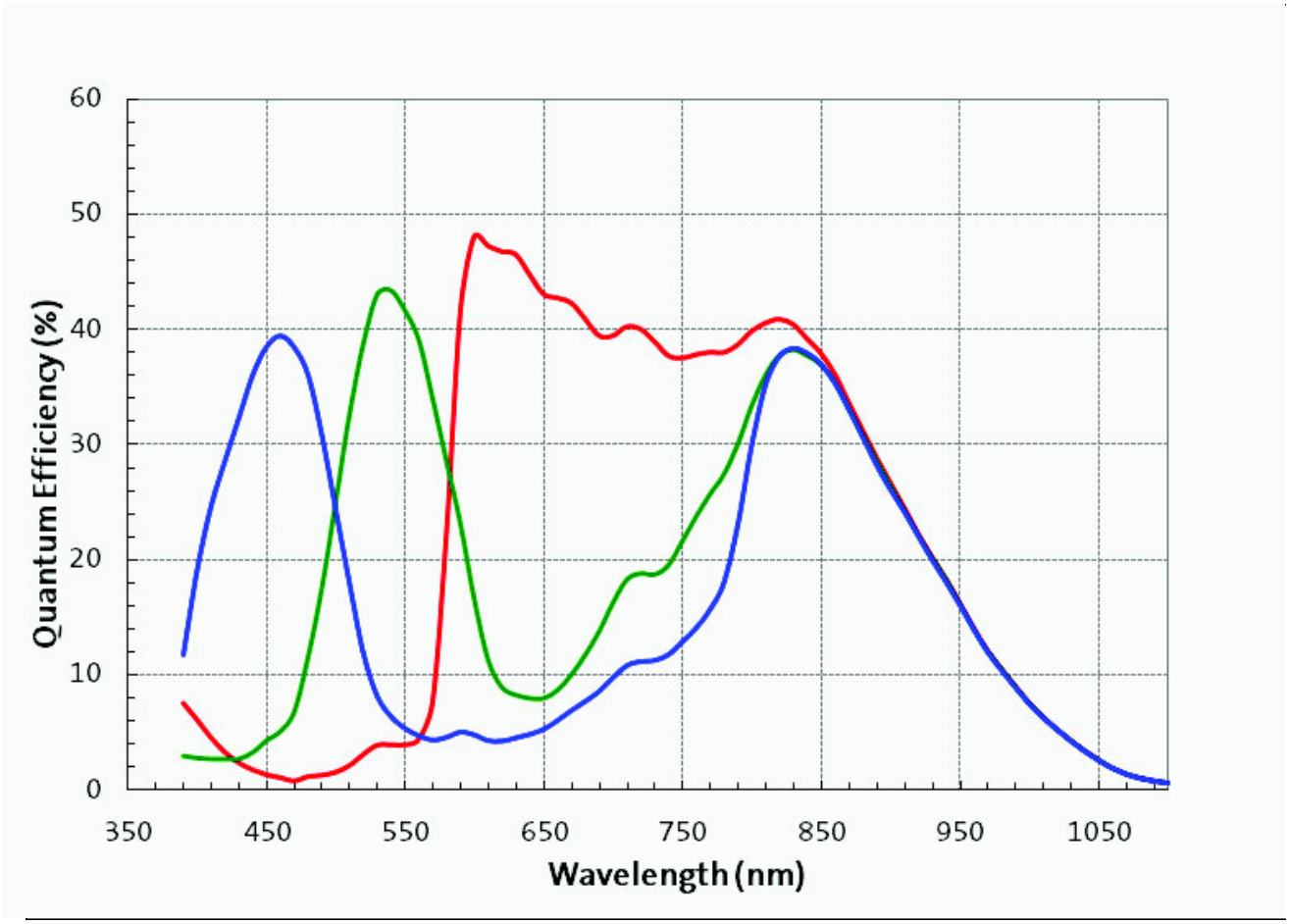


Figure 46. Typical Quantum Efficiency − RGB Bayer

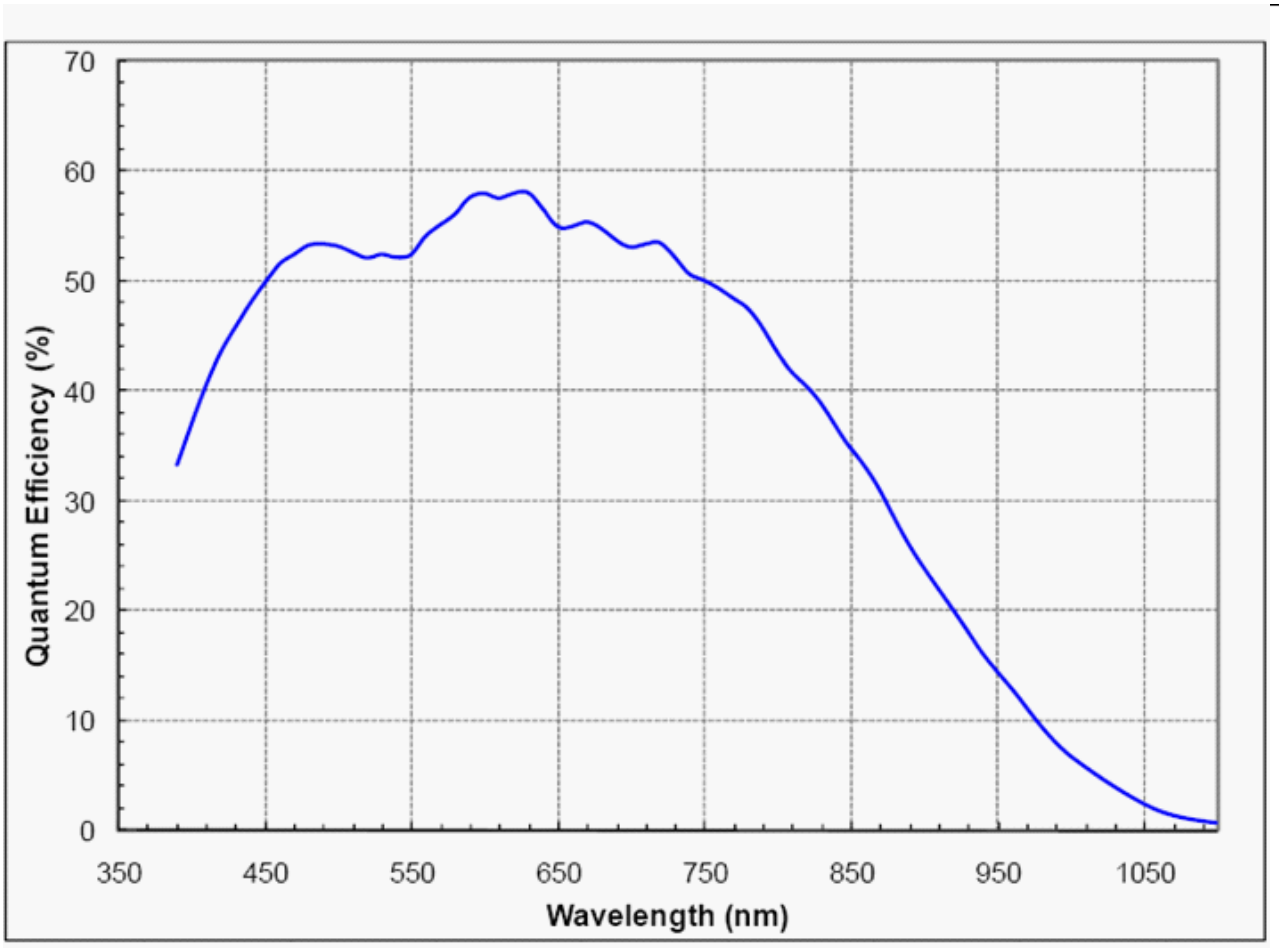
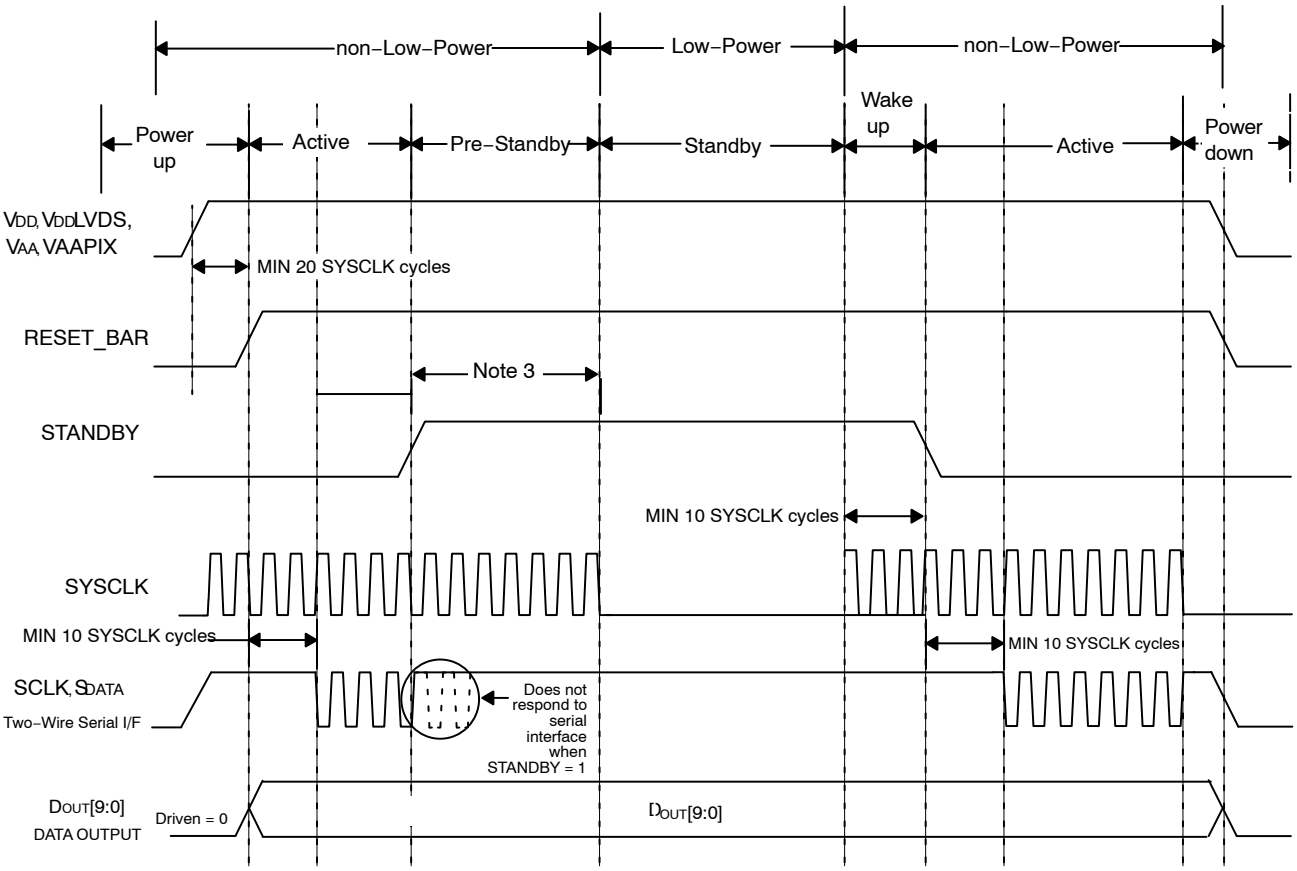


Figure 47. Typical Quantum Efficiency – Monochrome

APPENDIX A – POWER–ON RESET AND STANDBY TIMING

There are no constraints concerning the order in which the various power supplies are applied; however, the MT9V034 requires reset to operate properly at power–up. Refer to Figure 48 for the power–up, reset, and standby sequences.



1. All output signals are defined during initial power–up with RESET_BAR held LOW without SYSCLK being active. To properly reset the rest of the sensor, during initial power–up, assert RESET_BAR (set to LOW state) for at least 750 ns after all power supplies have stabilized and SYSCLK is active (being clocked). Driving RESET_BAR to LOW state does not put the part in a low power state.
2. Before using two–wire serial interface, wait for 10 SYSCLK rising edges after RESET_BAR is de–asserted.
3. Once the sensor detects that STANDBY has been asserted, it completes the current frame readout before entering standby mode. The user must supply enough SYSCLKs to allow a complete frame readout. See Table 4 for more information.
4. In standby, all video data and synchronization output signals are driven to a low state.
5. In standby, the two–wire serial interface is not active.

Figure 48. Power–up, Reset, Clock and Standby Sequence

APPENDIX B: ELECTRICAL IDENTIFICATION OF CFA TYPE

In order to identify the CFA type (RGB Bayer, Monochrome) that
a specific MT9V034 has been, the following table may be used.

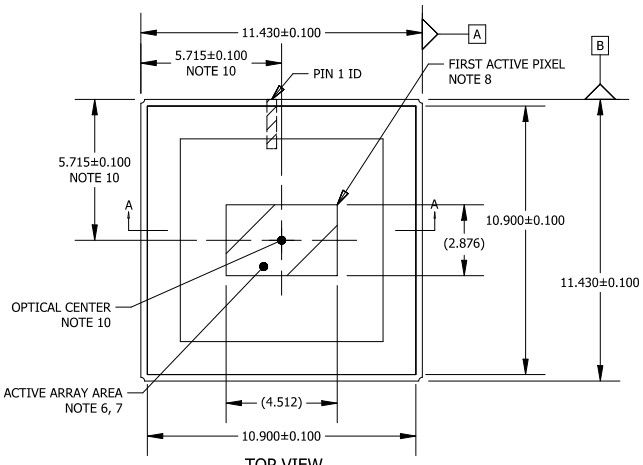
Table 21. ELECTRICAL IDENTIFICATION OF CFA

CFA	R0x6B[11:9]	R0x6B[8:0]
RGB	6	4
Mono	0	4

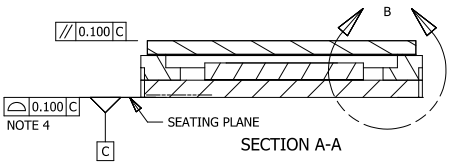
PACKAGE DIMENSIONS

CLCC48 11.43x11.43
CASE 848AN
ISSUE A

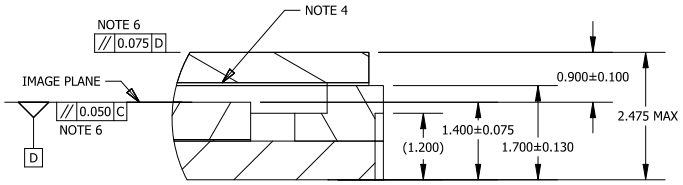
DATE 21 OCT 2019



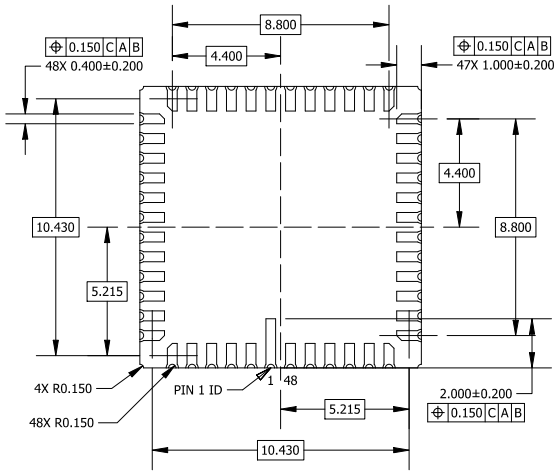
TOP VIEW



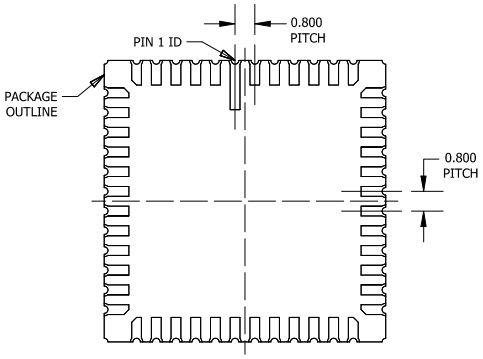
SECTION A-A



DETAIL B
SCALE 9: 1



BOTTOM VIEW



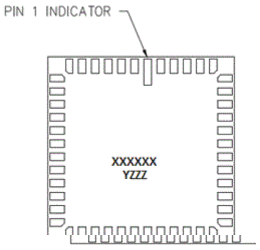
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. GLASS: 0.550 THICKNESS; REFRACTIVE INDEX = 1.52.
4. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.350 THICKNESS.
5. COPLANARITY APPLIES TO THE PLATED LAND PADS.
6. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
7. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 1°.
8. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
9. PACKAGE CENTER (X, Y) = (0.000, 0.000).
10. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (0.000, 0.000).

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
Y = Year
ZZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales