Process Technology:
TSMC CL013G

High-Speed/Density Two-Port Register File

sram_256x16
256X16, Mux 4, Drive 4

Features

- Precise Optimization for TSMC's Eight-Layer Metal 0.13µm CL013G CMOS Process
- High Density (area is 0.040mm^2)
- Fast Access Time (1.09ns at typical process, 1.20V, 25˚C)
- Fast Cycle Time (1.57ns at typical process, 1.20V, 25˚C)
- Two Ports (One Read, One Write)
- Completely Static Operation
- Near-Zero Hold Time (Data, Address, and Control Inputs)

Memory Description

The 256X16 register file is a high-performance, synchronous two-port, 256-word by 16-bit memory designed to take full advantage of TSMC's eight-layer metal, 0.13µm CL013G CMOS process.

The register file's storage array is composed of eight-transistor cells with fully static memory circuitry. The register file operates at a voltage of 1.2V ± 10% and a junction temperature range of -40˚C to +125˚C.

Port Description

Port	Description
A	Dedicated Read Port
B	Dedicated Write Port

Pin Description

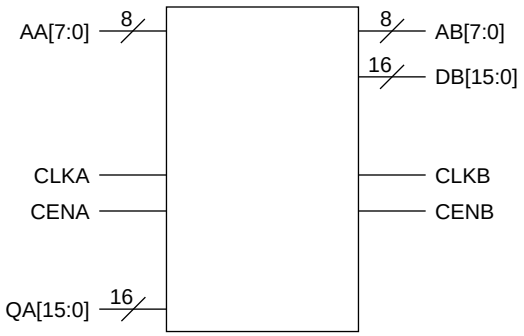
Pin	Description
AA[7:0]	Addresses (AA[0] = LSB)
AB[7:0]	Addresses (AB[0] = LSB)
DB[15:0]	Data Inputs (DB[0] = LSB)
CLKA, CLKB	Clock Inputs
CENA, CENB	Chip Enables
QA[15:0]	Data Outputs (QA[0] = LSB)

Area

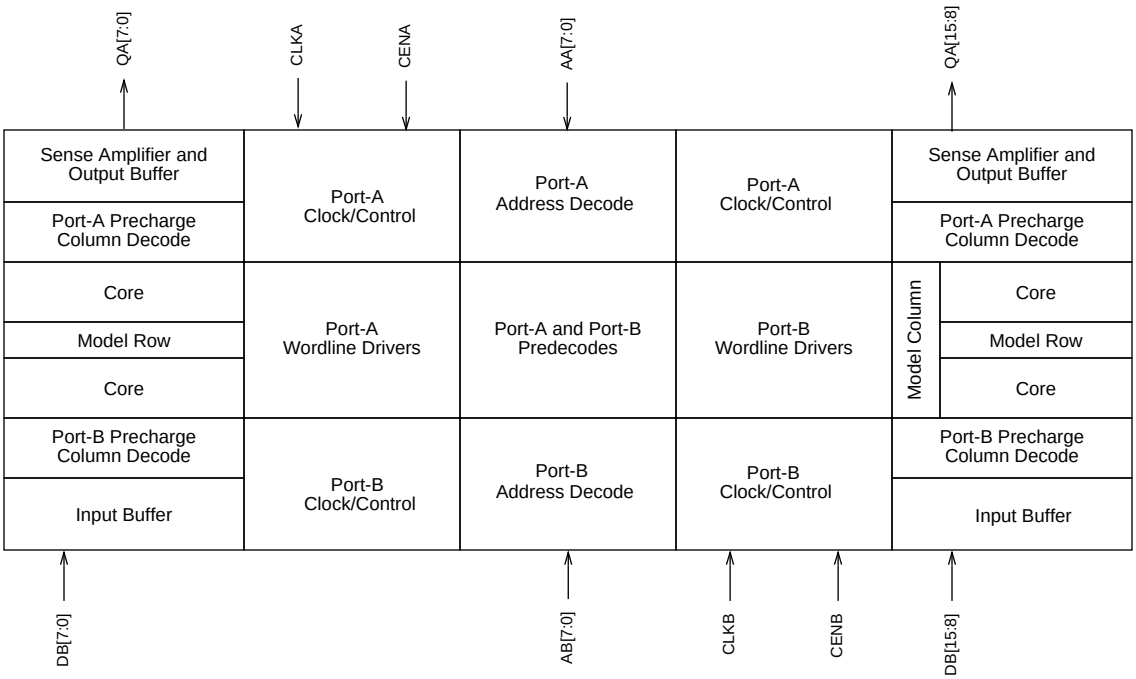
Area Type[a]	Width (mm)	Height (mm)	Area (mm^2)
Core	0.221	0.183	0.040
Footprint	0.231	0.193	0.045

a. The footprint area includes the core area and user-defined power ring and pin spacing areas.

Symbol

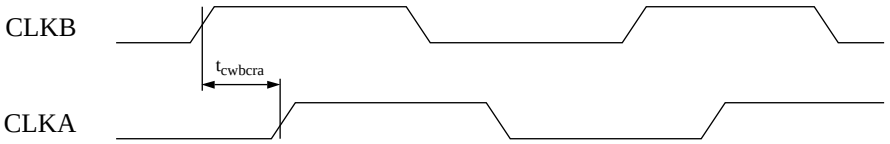


Register File Block Diagram



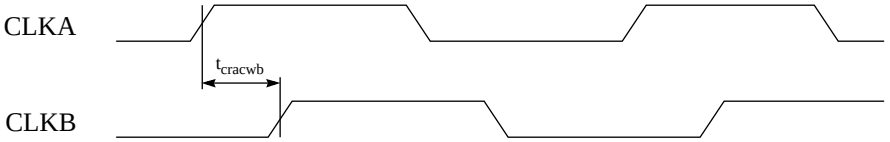
Mission Mode

Figure 1. Two-Port Register File Write-Read Clock Timing (Accessing Same Address)



Rising delays are measured at 50% of VDD and falling delays are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

Figure 2. Two-Port Register File Read-Write Clock Timing (Accessing Same Address)



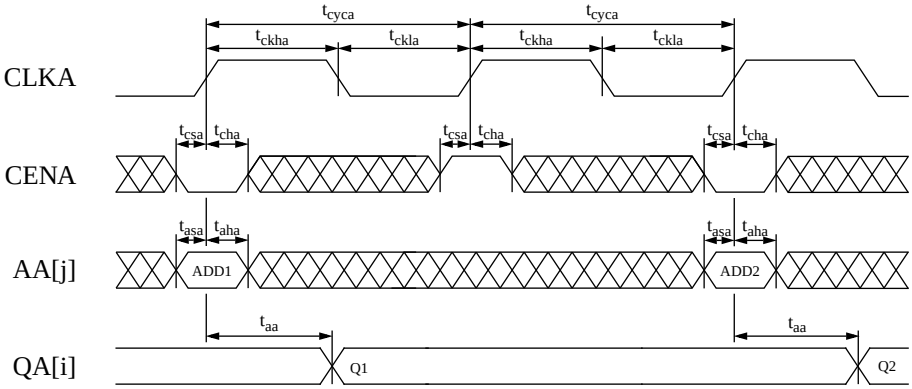
Rising delays are measured at 50% of VDD and falling delays are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

Read and Write Behavior When Accessing Same Address

Action	Condition[A]	Behavior
write from port B then read from port A	t_{cc} is satisfied (see Figure 1)	write OK read (new data) OK
	t_{cc} is not satisfied (see Figure 1)	write fails read fails
read from port A then write from port B	t_{cc} is satisfied (see Figure 2)	write OK read (old data) OK
	t_{cc} is not satisfied (see Figure 2)	write fails read fails

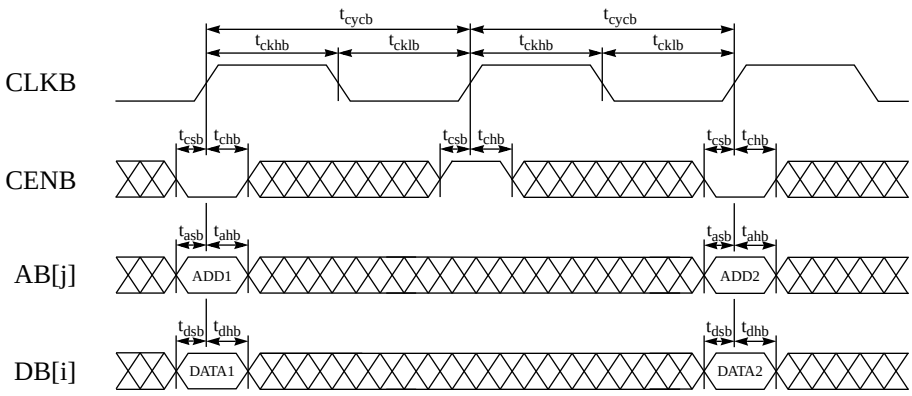
a. Tcc represents the clock collision time and is a general term for Tcwbcra and Tcracwb.

Figure 3. Two-Port Register File Read-Cycle Timing



Rising delays are measured at 50% of VDD and falling delays are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

Figure 4. Two-Port Register File Write-Cycle Timing



Rising delays are measured at 50% of VDD and falling delays are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

Register File Logic Table

CENA	CENB	Data Out	Mode	Function
H	X	Last Data	Port-A Standby	Address inputs are disabled; data stored in the memory is retained, but the port cannot be accessed for new reads. Data outputs remain stable.
X	H	N/A	Port-B Standby	Address and data inputs are disabled; data stored in the memory is retained, but the port cannot be accessed for new writes.
X	L	N/A	Write	Data on the write port's data input bus DB[n-1:0] is written to the memory location specified on the address bus AB[m-1:0].
L	X	Register File Data	Read	Data on the read port's data output bus QA[n-1:0] is read from the memory location specified on the address bus AA[m-1:0].

Register File Timing: Mission Mode

Parameter	Symbol	Fast@-40C Process 1.32V, -40˚C		Fast@0C Process 1.32V, 0˚C		Typical Process 1.20V, 25˚C		Slow Process 1.08V, 125˚C	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Port-A cycle time	t_{cyca}	1.07		1.13		1.57		2.45	
Port-B cycle time	t_{cycb}	0.92		0.98		1.35		2.12	
Port-A access time[a, b]	t_{aa}	0.67		0.71			1.09		1.72
Port-A address setup	t_{asa}	0.30		0.31		0.34		0.48	
Port-B address setup	t_{asb}	0.30		0.31		0.34		0.49	
Port-A address hold	t_{aha}	0.00		0.00		0.00		0.00	
Port-B address hold	t_{ahb}	0.00		0.00		0.00		0.00	
Port-A chip enable setup	t_{csa}	0.21		0.22		0.28		0.44	
Port-B chip enable setup	t_{csb}	0.21		0.22		0.28		0.43	
Port-A chip enable hold	t_{cha}	0.00		0.00		0.00		0.00	
Port-B chip enable hold	t_{chb}	0.00		0.00		0.00		0.00	
Port-B data setup	t_{dsb}	0.12		0.13		0.14		0.21	
Port-B data hold	t_{dhb}	0.05		0.05		0.08		0.14	
Port-A clock high	t_{ckha}	0.04		0.04		0.06		0.09	
Port-B clock high	t_{ckhb}	0.04		0.04		0.06		0.09	
Port-A clock low	t_{ckla}	0.17		0.18		0.28		0.47	
Port-B clock low	t_{cklb}	0.16		0.17		0.26		0.44	
Port-A clock collision (read follows write)	t_{cwbcra}	0.43		0.45		0.65		1.03	
Port-B clock collision (write follows read)	t_{cracwb}	0.59		0.62		0.87		1.36	
Clock rise slew	t_{ckr}		4.00		4.00		4.00		4.00
Output load factor (ns/pF)	K_{load}		0.87		0.89		1.26		1.90

a. Parameters have a load dependence (K_{load}), which is used to calculate: $TotalDelay = FixedDelay + (Kload \times Cload)$.

b. Access time is defined as the slowest possible output transition for the typical and slow corners, and the fastest possible output transition for the fast corner.

Pin Capacitance

Pin	Fast@-40C Process 1.32V, -40˚C	Fast@0C Process 1.32V, 0˚C	Typical Process 1.20V, 25˚C	Slow Process 1.08V, 125˚C
	Value (pF)	Value (pF)	Value (pF)	Value (pF)
AA[j]	0.006	0.006	0.006	0.005
AB[j]	0.005	0.006	0.005	0.005
DB[i]	0.002	0.003	0.002	0.002
CLKA	0.038	0.038	0.037	0.036
CLKB	0.032	0.033	0.031	0.030
CENA	0.004	0.005	0.004	0.004
CENB	0.003	0.004	0.003	0.003

Power

333.00MHz Operation

Condition	Fast@-40C Process 1.32V, -40˚C	Fast@0C Process 1.32V, 0˚C	Typical Process 1.20V, 25˚C	Slow Process 1.08V, 125˚C
	Value (mA)	Value (mA)	Value (mA)	Value (mA)
Port-A AC Current[1]	4.038	4.144	3.448	3.023
Port-B AC Current[1]	3.023	3.177	2.676	2.387
Port-A Peak Current	20.978	19.958	12.696	6.998
Port-B Peak Current	17.685	16.717	10.061	5.501
Port-A Deselected Current[2]	0.893	0.996	0.771	0.737
Port-B Deselected Current[2]	0.893	0.996	0.771	0.737
Standby Current[3]	0.025	0.100	0.023	0.087

[1] Value assumes 50% read and write operations.

[2] Value assumes register file is deselected, all addresses switch, and 50% of input pins switch. The logic-switching component of deselected power becomes negligibly small if the input pins are held stable by externally controlling these signals with chip select.

[3] Value is independent of frequency and assumes all inputs and outputs are stable.

Clock Noise Limit

Signal	Fast@-40C Process 1.32V, -40˚C		Fast@0C Process 1.32V, 0˚C		Typical Process 1.20V, 25˚C		Slow Process 1.08V, 125˚C	
	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)
CLKA/B	10.000	0.476	10.000	0.461	10.000	0.467	10.000	0.442

The clock noise limit is the maximum CLK voltage allowable for the indicated pulse width without causing a spurious memory cycle or other memory failure.

Power and Ground Noise Limit

Signal	Fast@-40C Process 1.32V, -40˚C	Fast@0C Process 1.32V, 0˚C	Typical Process 1.20V, 25˚C	Slow Process 1.08V, 125˚C
	Voltage (V)	Voltage (V)	Voltage (V)	Voltage (V)
Power	0.132	0.132	0.120	0.108
Ground	0.132	0.132	0.120	0.108

The power/ground noise limit is the maximum supply voltage transition allowable without causing a memory failure.