2022 NYCU EE VLSI Lab Report

Final Project

6-Bit Multiplier and Accumulator Design

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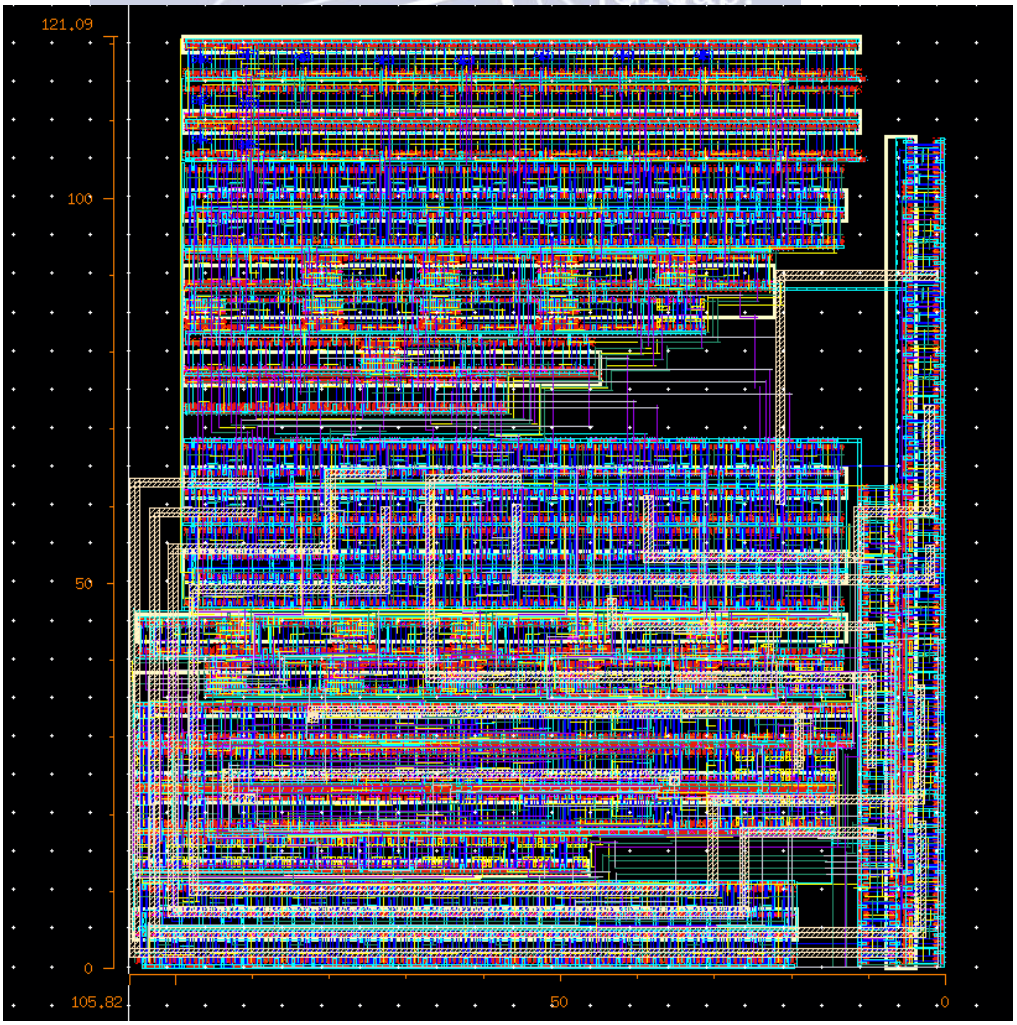
Date: 2022/01/13

I. Layout result

1. Layout picture with ruler

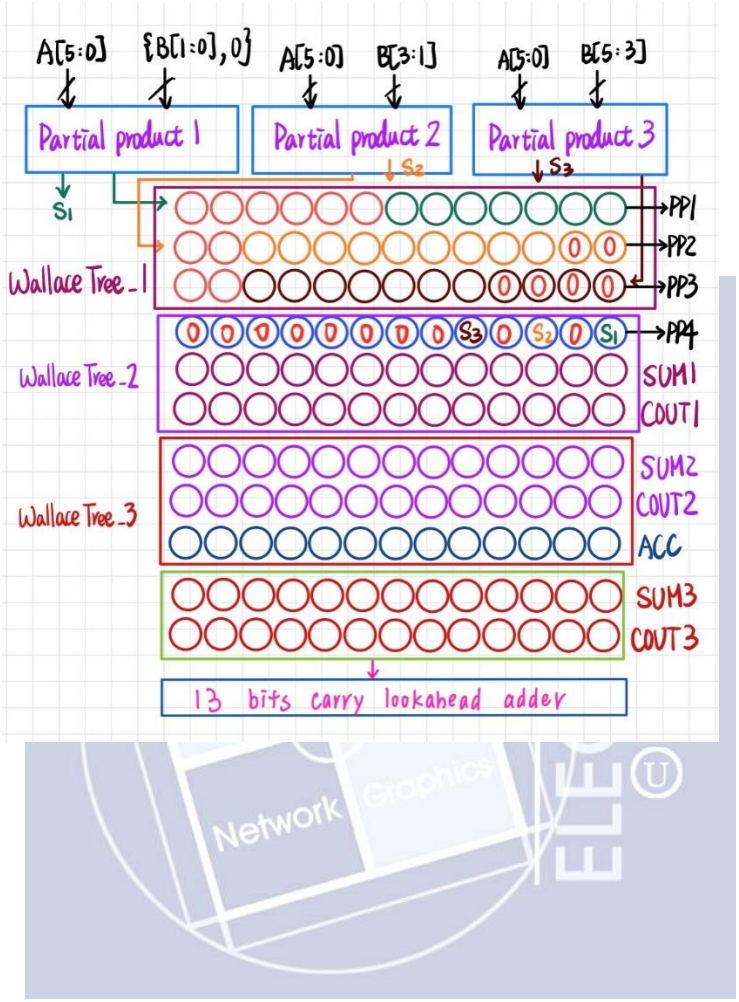
105.82*121.09



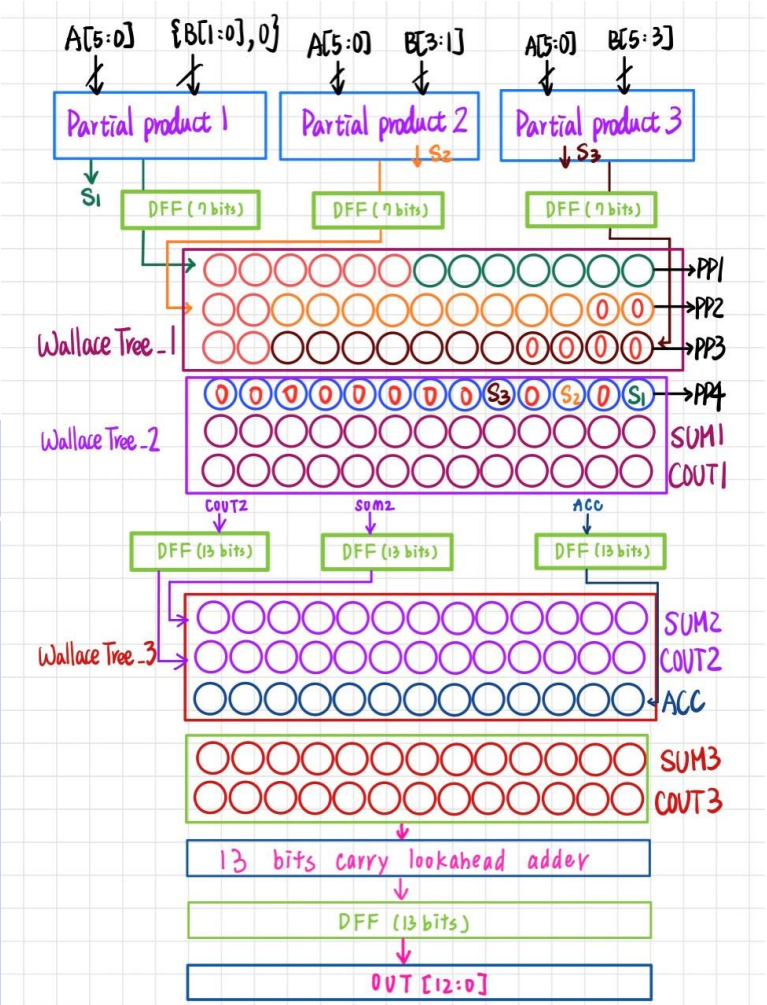
2. Design concept

(1) Pipeline multiplier design

- 還沒有切 pipeline 時:

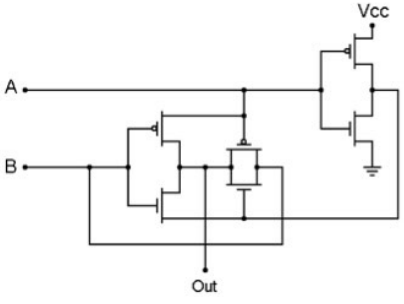


➢ 切 pipeline 後:



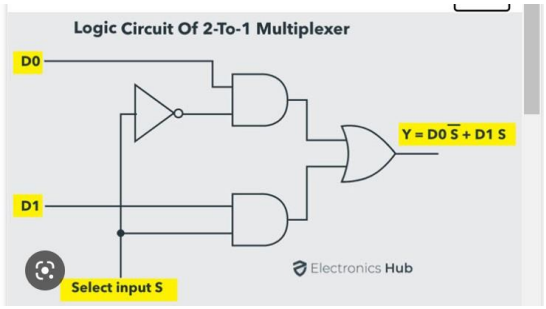
(2) Summary of structure (Roughly number of transistor / logic gate is used)

➢ XOR2(6 顆):



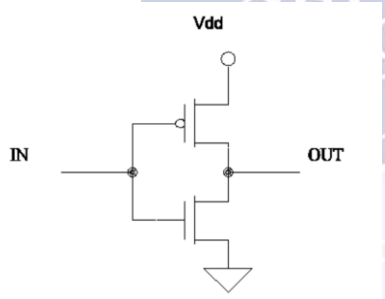
資料來源: https://en.wikipedia.org/wiki/File:TransmissionCmosXORGate.png

- MUX(16 顆):



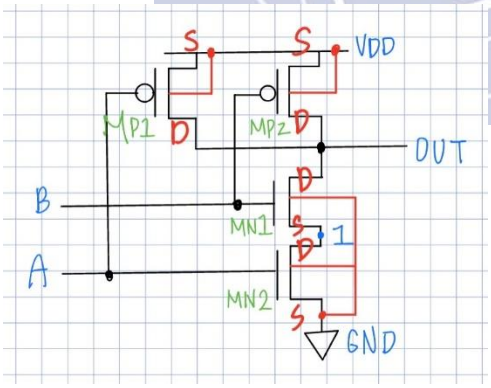
資料來源: https://www.electronicshub.org/multiplexerandmultiplexing/

- NOT(2 顆):

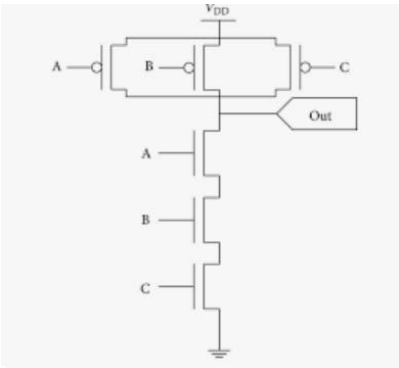


資料來源: https://tiij.org/issues/issues/spring97/electronics/cmos/cmostran.html

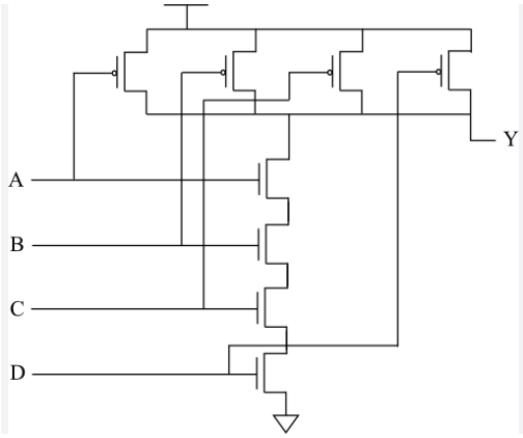
- NAND2(4 顆):



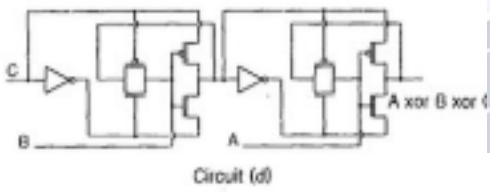
- NAND3(6 顆):



- NAND4(8 顆):

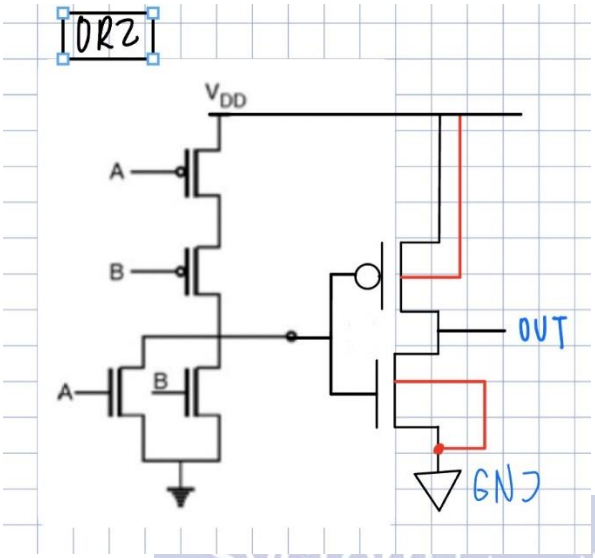


- XOR3(12 顆):

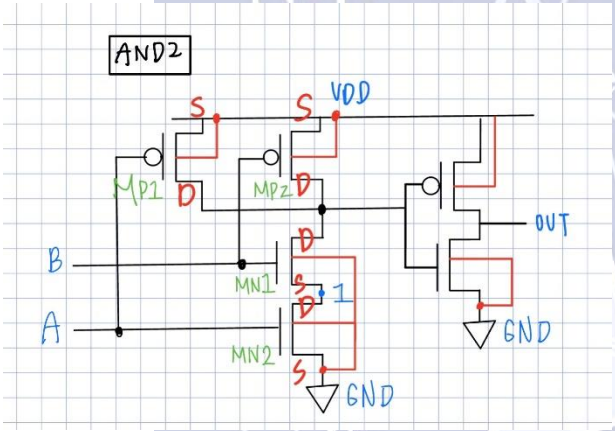


資料來源: https://ieeexplore.ieee.org/document/824054

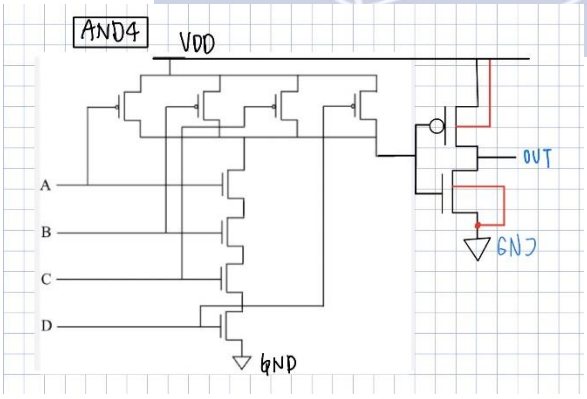
- OR2(6 顆):



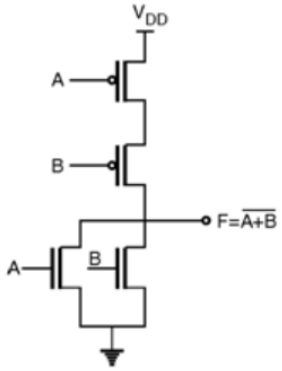
- AND2(6 顆):



- AND4(10 顆):



- NOR(4 顆):



資料來源:https://www.electronics-tutorial.net/Digital-CMOS-Design/CMOS-Layout-Design/Layout-of-logic-gates/

- DFF(22 顆，包括 NCLK 的 inverter):

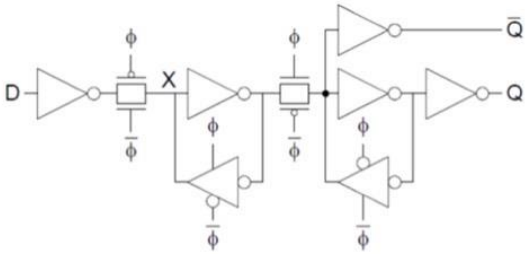
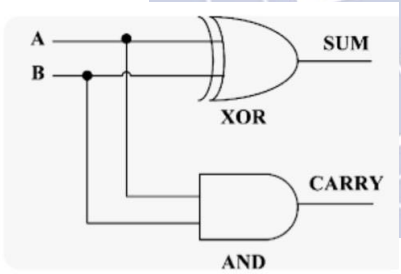


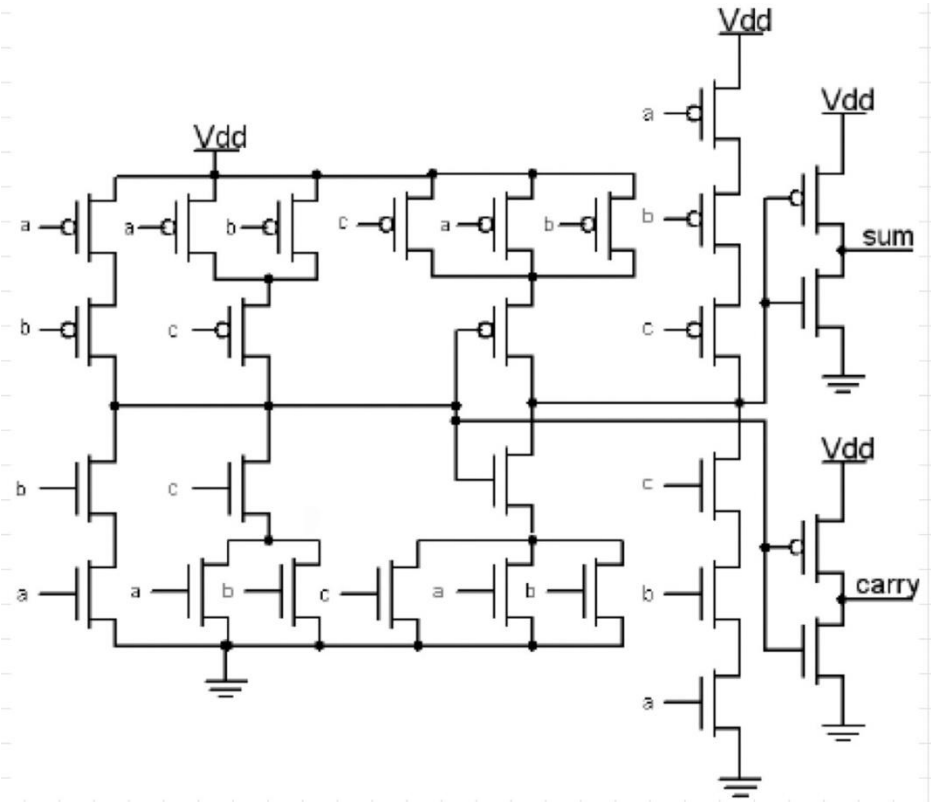
Fig.1 Schematic of D Flip-Flop (positive trigger)

- HA(10 顆):



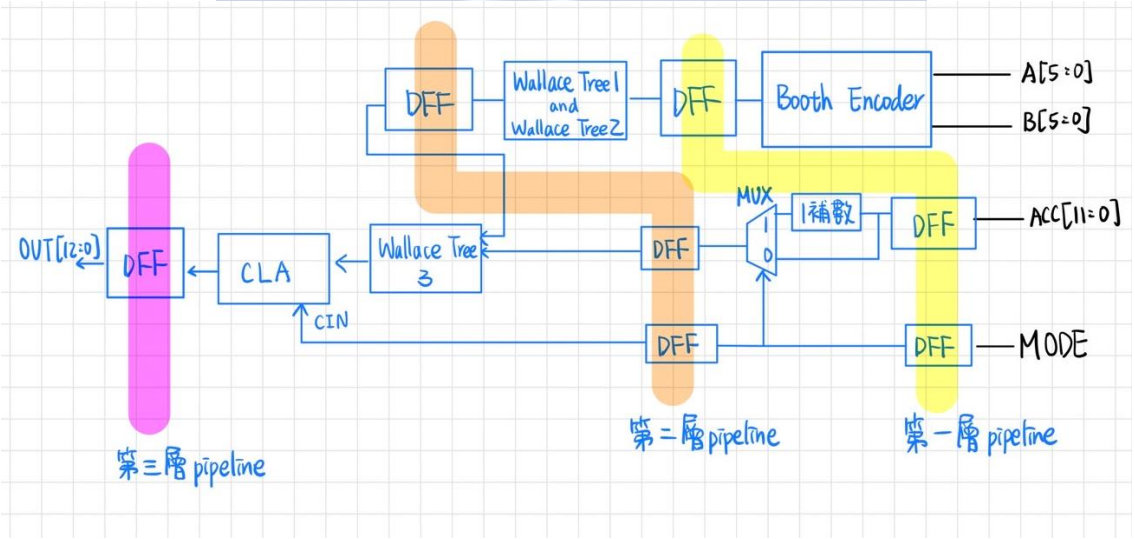
資料來源: https://www.researchgate.net/figure/A-half-adder-constructed-with-a-XOR-and-AND-gate_fig1_325747900

- FA(28 顆):

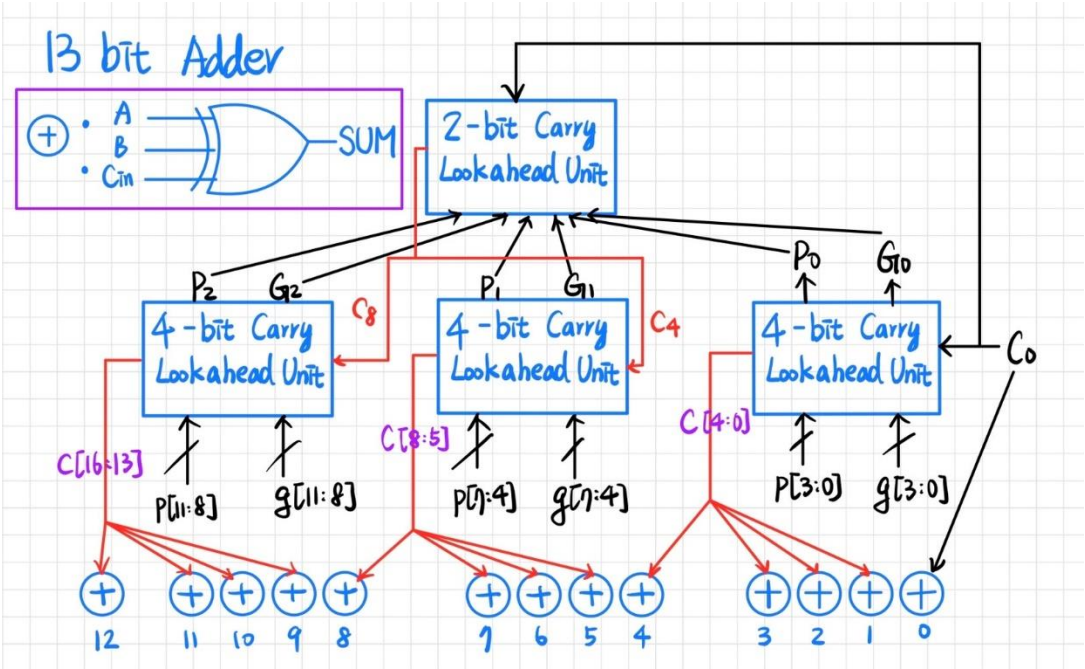


這次的電路一共用了 Half Adder 14 顆，Full Adder 19 顆，3-bit 的 XOR 15 顆，2-bit 的 XOR 25 顆，2-bit 的 OR 15 顆，2-bit 的 AND 顆，3-bit 的 NAND 17 顆，2-bit 的 NAND 84 顆，4-bit 的 NAND 12 顆， DFF 87 顆，MUX 13 顆，再加上約 25 左右的 inverter(不包含在 logic gate 裡面)，此次的電路約用了 3888 顆 transistor。

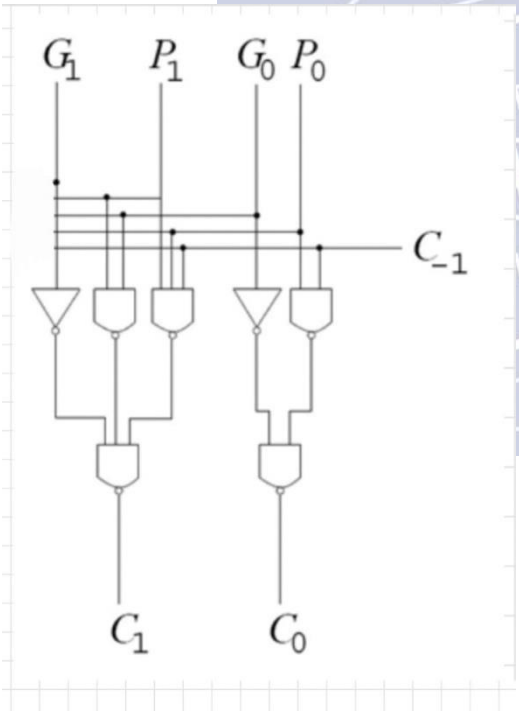
(3) Circuit Schematic / Building Blocks



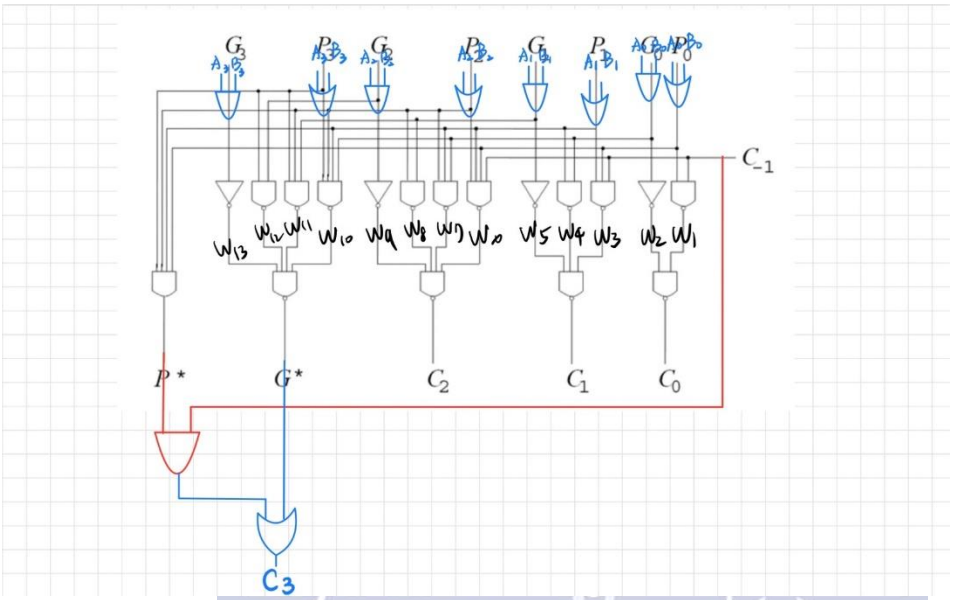
CLA:



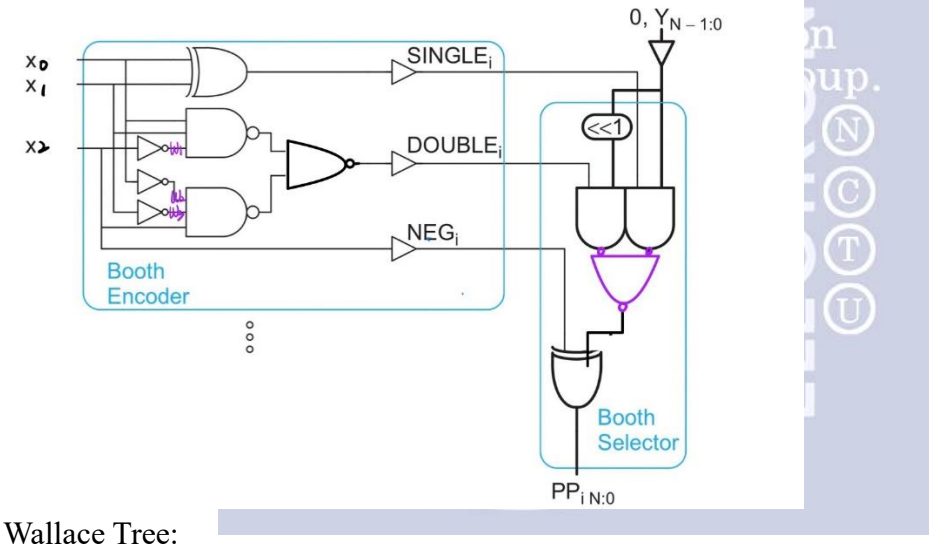
2-bit Carry Lookahead Unit:



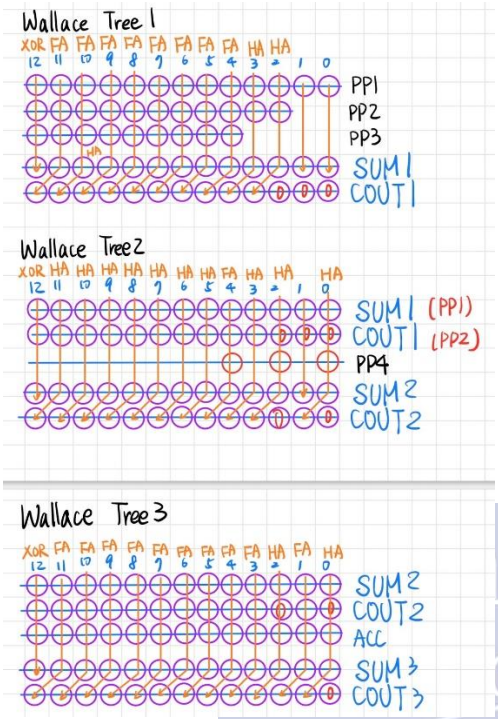
4-bit Carry Lookahead Unit:



Booth Encoder:



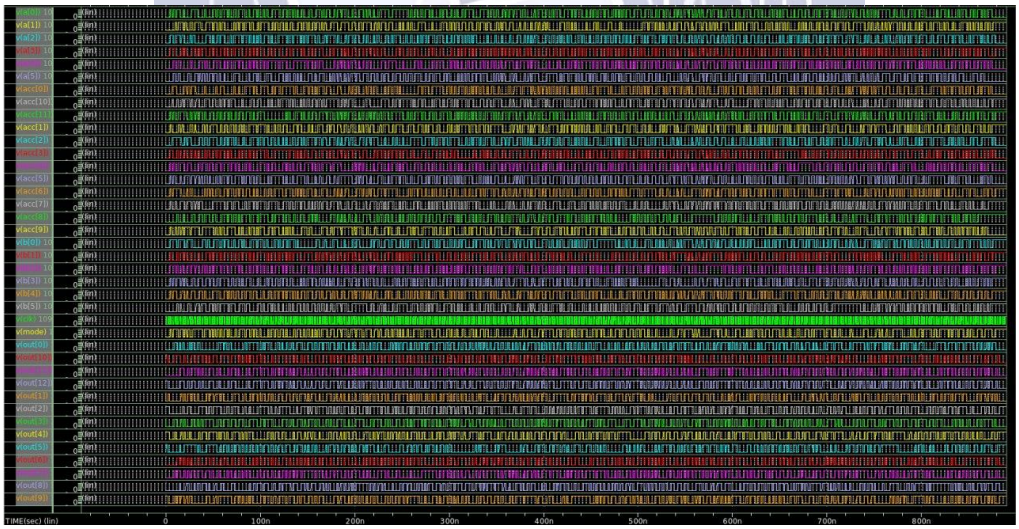
Wallace Tree:



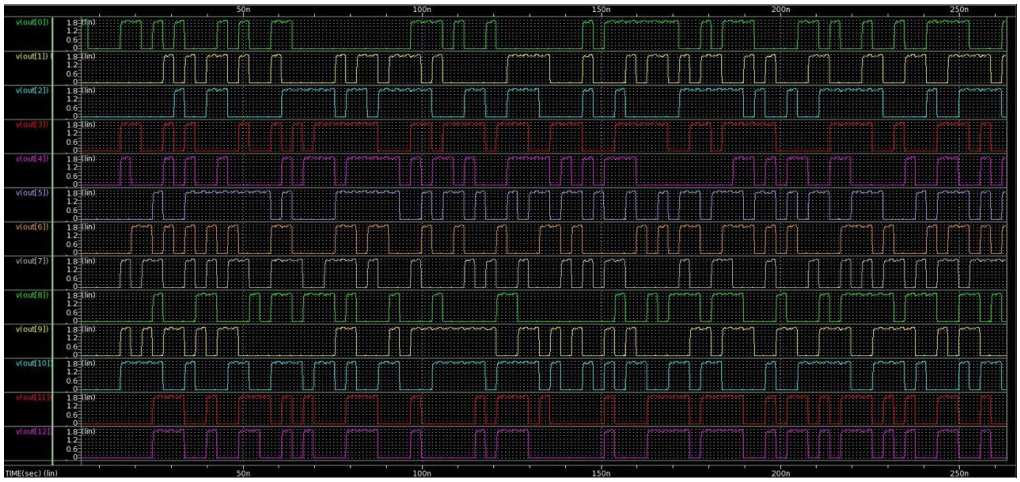
II. Simulation result

1. Output waveform (with input from MAC6.vec)

(1) Pre-sim (Output waveform)



(2) Post-sim (Output waveform)

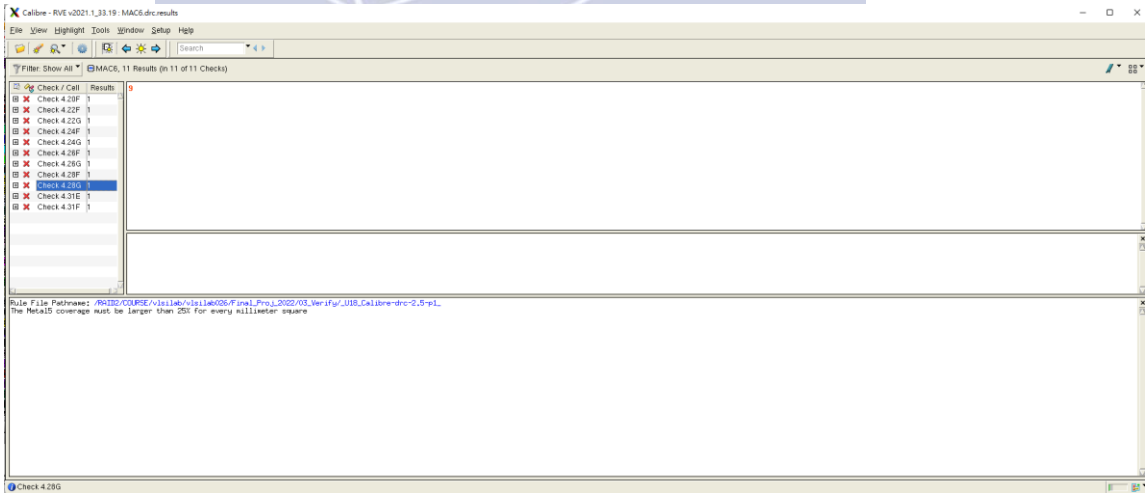


(3) Performance list (TT case under worst case input pattern)

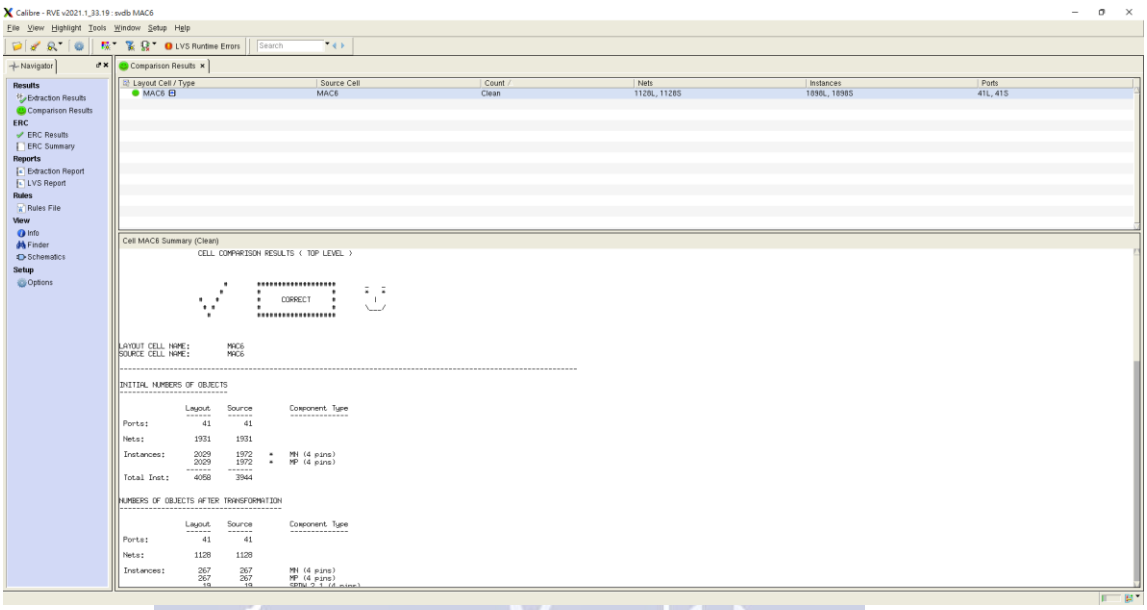
Maximum operation frequency	Pre-sim: 0.581G Hz (1.72ns)
	Post-sim: 0.333 GHz (3ns)
Average power	Pre-sim: 4.6263e-3 w
	Post-sim: 3.9608e-3 w
Layout area	105.82*121.09
Multiplier and adder structure	Radix-4 mult + Wallace tree + CLA
Glitch control (Yes/No)	No

III. Verification result

1. DRC



2. LVS



IV. Discussion

1. Optimization or anything worth sharing

(1) 在做 Wallace Tree 的時候會特別注意是否一定要用 Full Adder，可以視情況把某些 bit 變成 Half Adder，甚至有些 bit 可以直接拉線就可以得到我們要的結果，如此一來就可以減少面積以及減少 delay，也因此我們的 Wallace Tree 有三種不同的 Adder 組合方式。

(2) 在切 pipeline 的時候，我們一開始會先測在還沒切之前完整的 combinational circuit 運算需要的完整週期，這樣也比較好判斷我們之後切的 pipeline 是否是最佳的位置，良好的 pipeline 應讓每一段的 combinational circuit 的運算時間相近，所以良好的 pipeline 切法最後測出來的週期應約為還沒切 pipeline 之前的三分之一。

(3) 在畫 FA 時，因為有幾顆 mosfet 的 width 特別長，所以特別採用助教在 Lab04 推薦的 folded layout 以此來減低寄生電容的效應以及 leakage current 的效應(降低 power)。

(4) 在畫 layout 時會盡可能地共用 diffusion，如此一來也可以減少寄生電容的效應，也可以縮小面積。

(5) 在拉遠線時，在情況允許下會盡可能用較高層的 metal 來拉線以此降低寄生電容跟寄生電阻的效應。

2. Your thoughts about VLSI LAB course and exercises

(1) 109511204 吳燕琳

這學期的課程中助教給與我們豐富的學識內容，讓我在 VLSI LAB 中學到的不僅僅是 layout，還有許多跟設計相關的知識，讓我在這堂課收穫頗多。作業題目也出得很扎實，讓我能將上課時老師所教的知識有所應用，對於 VLSI 的知識也更加深刻，修了這門課後我發現交大的日出很燦爛。

(2) 109511231 林品妤

助教從一開始的 hspice 到後來的 verilog，一步一步教起，讓我能夠穩扎穩打的練習，從一開始的完全陌生，但現在對於整個的操作都有一定的概念，也對於老師上課時講解的內容更有概念。

(3) 109511298 阮珩

真的非常感謝這學期在各個助教的教學，以及認真準的每個 lab 還有 final project，讓我真的學到很多有關 vlsi 導論學到的理論，如何在 layout 中實現，雖然中途遇到很多的困難，但在最後回想起來也是蠻有成就感的。