NYCU EE-VLSI 2022

Final Project: 6-Bit Multiplier and Accumulator Design

Due at 2022/01/09 12:00

I. Abstract

In this lab, you are required to design a 6-bit MAC with Two-Mode in full custom design. This document includes the specification and requirement of your design, and grading policy.

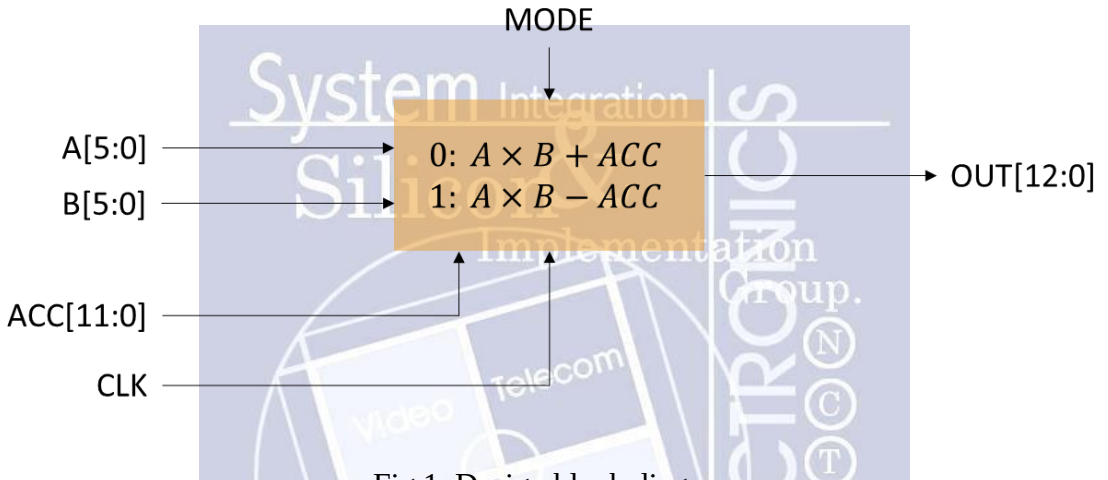

Fig 1. Design block diagram

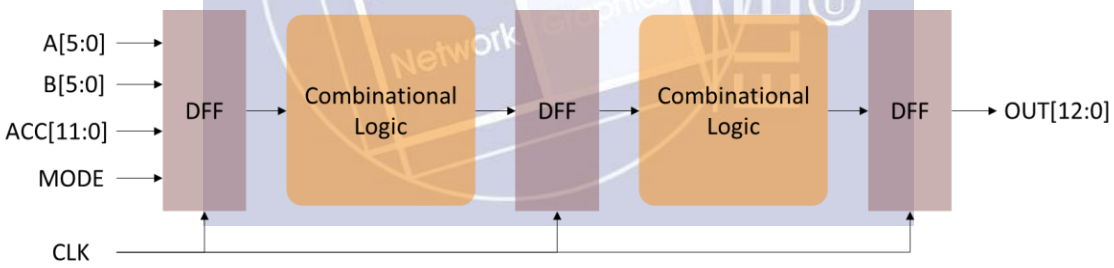

Fig 2. Pipeline example

II. Please design a 6-bit multiplier and accumulator. The design specifications are given as follows:

- File name: MAC6.sp
- Sub-circuit name: MAC6 (including top cell name in layout)
- Input port (signed): A [5:0], B [5:0], ACC [11:0], MODE, CLK
- Output port(signed): OUT [12:0]

III. The specification is described as the following:

- ✓ Rise time and fall time of input signal: 0.1ns
- ✓ Output loading of OUT [12:0]: 10f

- ✓ Supply voltage: 1.8V
- ✓ Only metal 1 ~ metal 6 are allowed, others are prohibited.

IV. Try to optimize your design as possible as you can. A suggested performance of your design (under TT case):

- ✓ Maximum propagation delay should be shorter as possible as you can.
- ✓ Peak power & average power should be improved as possible as you can.
- ✓ The art of layout will be considered and discussed for this work.
- ✓ Try to reduce parasitic capacitance and resistance to narrow the gap between pre-sim and post-sim performance.
- ✓ Area is defined as the smallest rectangle which includes whole layout, and the rectangle ratio should fall in the range of 2 ~ 0.5 as possible.

V. Grading Policy:

1. Pre-sim (HSPICE): 15%
2. Layout: 20% (partial scoring)
3. DRC, LVS: 10%
4. Post-sim (HSPICE): 10%
5. Performance: 25%
   (1) Pre-sim frequency: 5% (need to pass pre-sim with SPEC in **III.**)
   (2) Layout Figure-of-merit(FoM) = (Layout area)*(Post-sim Period)*(Power) 20%

   Note that: Layout area including N-well, need to pass DRC and LVS verification and need to pass post-sim with SPEC in III.
6. Report: 20%
   (1) Please follow attached report format for this part.

Note:

1. Copy the files to your own account：
   “tar -xvf ~vlsita01/Final_Proj_2022.tar”
2. RTL part is provided for you to design the circuit from system level. Use it or not depends on you and won’t be graded.
3. You need to hand in the following files on New E3

File	Description
(1) studentID_MAC6.gds	From LVS directory
(2) studentID_MAC6.sp	Pre-sim design. Only add codes under the line 61 (comment) and submit this part; do not touch the part above except for cycle period.
(3) studentID_period.txt	List your pre-sim clock period and post-sim clock period. Pre-sim: ### ns Post-sim: ### ns (you must follow the attached format)
(4) studentID_report.pdf	Just report

4. Since a script for standard verification flow is used for demo in this project, make sure that submitted pre-sim file is consistent with layout file, e.g. port names, MOS width and so on.
5. Naming error rules: **(You will get 5-point penalty if you break any of the followingrules)**
   (1) File names are consistent with the table above. DON’T submit compressed files.
   (2) For studentID_MAC6.sp, only codes under the line 61 (comment) are submit.
   (3) Please use P_18_G2 and N_18_G2 as MOS model in studentID_MAC6.sp
   (4) Do NOT modify port names, VDD, GND and CLK in your pre-sim file and layout.
   (5) Student ID, which is first one of your team members, need to be same in the four file names.

Team No.	Team Name	Member #1	Member #2	Member #3
0	統神端火鍋	甄基極	艾閘極	倪涉極

6. You can make good use of forum on Facebook in there is any ambiguity in this project and document.
7. Enjoy the fun from this assigned work