REPORT-1-MOS CAPACITOR

Abstract:

In this report the process to fabricate MOS capacitor and methods to calculate its various parameters are studied. This process includes various steps like oxidation, oxide etching, deposition of aluminum and etc. For oxidation we will be using dry oxidation method. Resistivity of substrate can be calculated by applying some current to the substrate and measuring the voltage. For cleaning the wafer we are using AMD cleaning method. To etch the oxide layer on only one side of the wafer we will be applying photo-resist on another side of the wafer by spin coating method. For making contact we will be using two different methods one is using Nitride Sputter tool and second is deposition of aluminum directly. Finally the C-V curves of MOS capacitor will be studied which will show us the frequency dependency of MOS capacitor.

I- Introduction:

The MOS capacitor also called as MOS cap is the most important device in semiconductor device physics because, it is the control gate of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). MOSFETS are used on a large scale in integrated circuits. To understand the working of MOSFETS we need to know the working of MOS capacitors. By understanding how MOS capacitors work we will also learn about how its operation is frequency dependent.

II- Theory

It is very important to understand the working of MOS capacitors. The working of the MOS capacitors depends on three regions of operation. We will consider p-type semiconductor in our MOS capacitor. The operation will be nearly same for n-type substrate MOS capacitor, but voltage polarities will be reversed.

1- Accumulation mode

For p-type substrate if we apply negative voltage at the gate, the holes which are majority carriers in p-type substrate will accumulate near the oxide-semiconductor surface. That is the reason this mode is called as accumulation mode. The best way to understand the operation is by looking at the energy band diagram. Following is the energy band diagram of P-type semiconductor MOS capacitor in accumulation mode. As we can observe from diagram there is a band bending due to accumulation of majority carriers (holes) at the oxide-semiconductor surface. The total capacitance in accumulation mode is only due to capacitance across oxide layer.

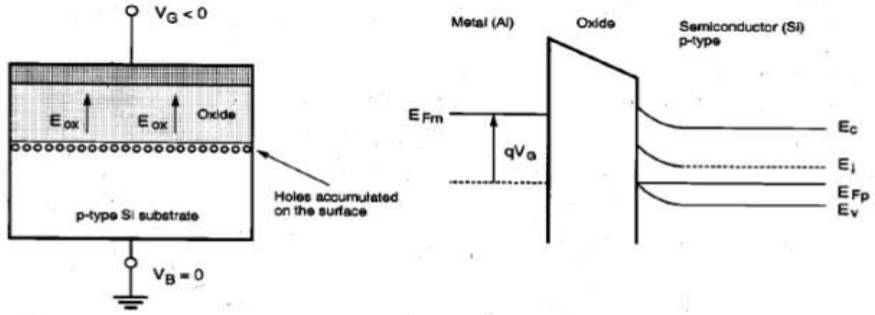

FIG 1 – ENERGY BAND DIAGRAM OF MOS CAPACITOR IN ACCUMULATION MODE

2- Depletion mode.

Now we slowly move towards the positive voltage. While sweeping voltage from negative value to positive value, at a certain voltage value the total capacitance begins to decrease. That particular voltage is called as flat band voltage (Vfb). This region where total capacitance continues to fall is called as depletion region. In depletion mode the majority carriers are depleted near the oxide-semiconductor interface. Depletion layer width continues to increase as we keep increasing the voltage. We can observe this behavior by looking at the energy band diagram of MOS capacitor in depletion mode. Following is the energy band diagram of MOS capacitor in depletion mode. The total capacitance is because of oxide layer as well as depleted layer in semiconductor.

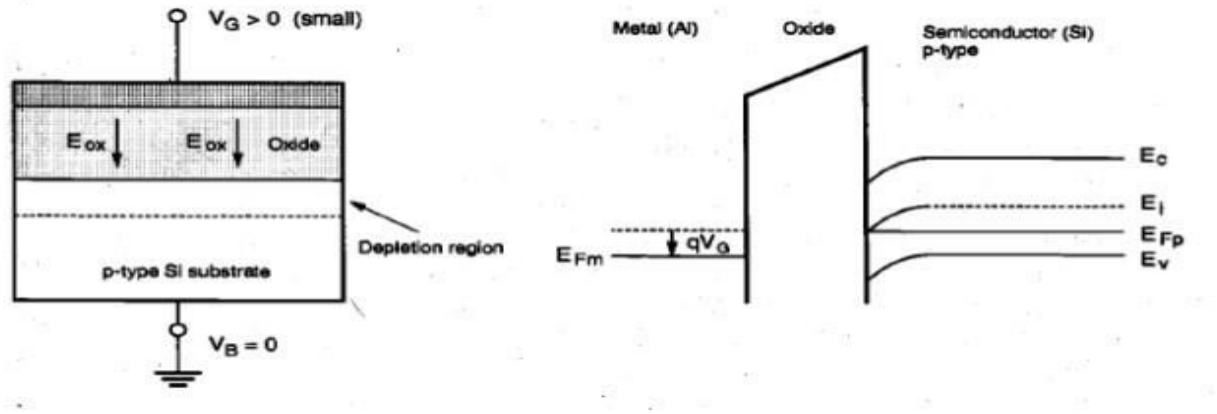

FIG 2 –ENERGY BAND DIAGRAM OF MOS CAPACITOR IN DEPLETION MODE

3- Inversion Mode.

If we further go on increasing the voltage, then the oxide-semiconductor surface is inverted from p-type to more n-type. This mode is called as inversion mode. In inversion mode we apply positive voltage at the gate and due to positive voltage at gate minority electrons which are present in semiconductor are attracted towards the oxide-semiconductor interface. The operation of MOS capacitor in inversion mode can be best understood by looking at the energy band diagram. Following is the energy band diagram of MOS capacitor in inversion mode. The total capacitance is only due to oxide layer.

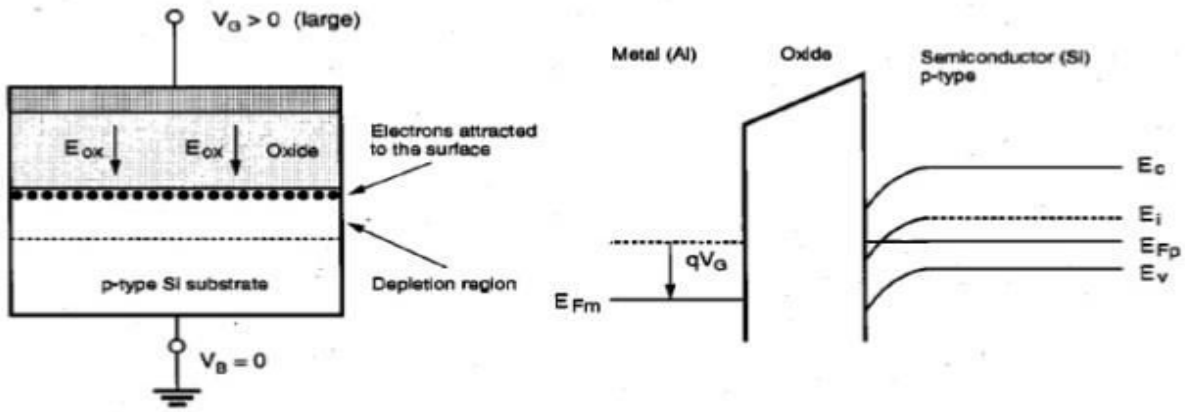

FIG 3 –ENERGY BAND DIAGRAM OF MOS CAPACITOR IN INVERSION MODE

C-V curve of MOS capacitor (p-type semiconductor) in 3 different modes of operation.

In inversion during high frequency, number of depleted carriers near the interface increase, results in increase in depletion width and reduce capacitance. During low frequency carriers get time to repel from surface and total capacitance is only due to oxide and total capacitance again increases.

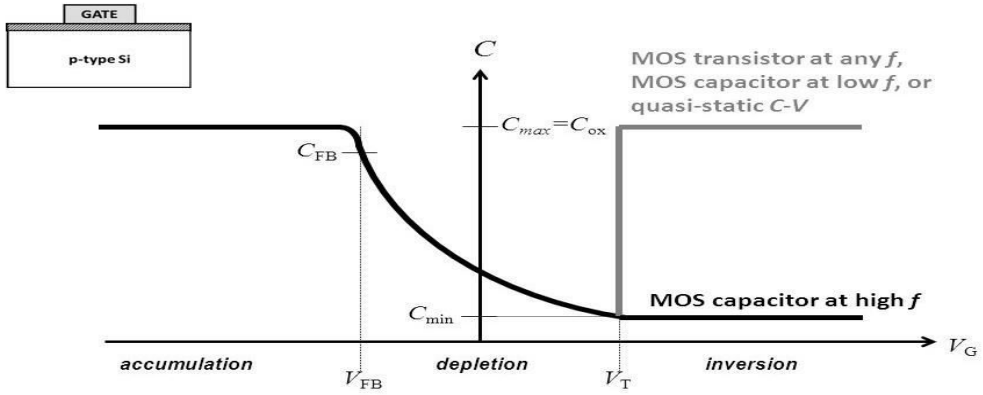

FIG 4 –C-V CURVE OF MOS CAPACITOR IN ALL THREE REGIONS OF OPERATION

III- **Experimental:**

The experiment started with the process of oxidation. Before that we had to clean the wafer. The technique used for cleaning wafer was AMD cleaning. Then we tested the initial parameters and performed dry oxidation on wafer to form SiO2 on both the sides of wafer. Next step was to etch the back side oxide layer. This process was done by applying photo-resist by spin coating method on front side. After applying photo-resist wafer was immersed in BOE (buffered oxide etch). Next step was to make back contact on wafer. This process was done by using Nitride Sputter tool. No mask was used during this process. After creating backside contact the only thing which was remaining was the front side contact. These front side contacts were made by depositing aluminum dots on wafer using shadow mask. Now last step was to test all parameters like c-v curve, flatband voltage etc.

IV- **Results and discussions.**

First results which we found were the resistivity of substrate. Table showing different values of resistivity on different voltages and currents is as follows.

May be substrate have resistivity because of collision of carriers.

Resistivity = $\frac{\Pi * t * V}{In(2) * I}$ …….. Equation (1)

Where

t = substrate thickness = 0.325 nm

V = Voltage

I = current

CURRENT	VOLTAGE	RESISTIVITY
50 uA	2.31 mV	6.8 Ohm-cm
100 uA	4.38mV	6.4 Ohm-cm
200 uA	8.93mV	6.6 Ohm-cm
300 uA	13.35mV	6.5 Ohm-cm

After finishing the entire wafer processing, we found out the C-V curves and oxide thickness.
C-V curves of different regions are as follows.

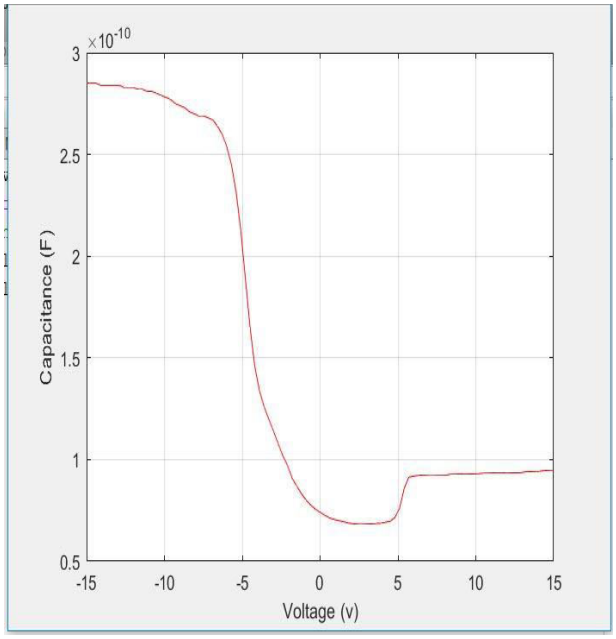

FIG 5 –C-V CURVE OF MOS CAPACITOR AT HF

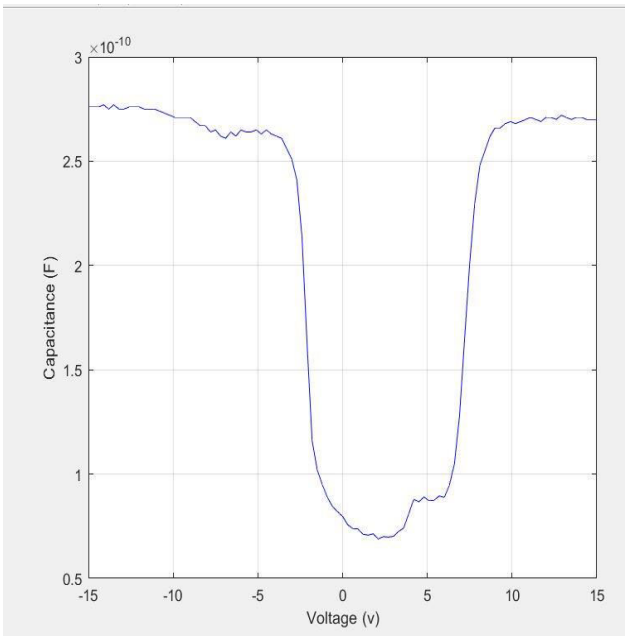

FIG 6 –C-V CURVE OF MOS CAPACITOR AT LF

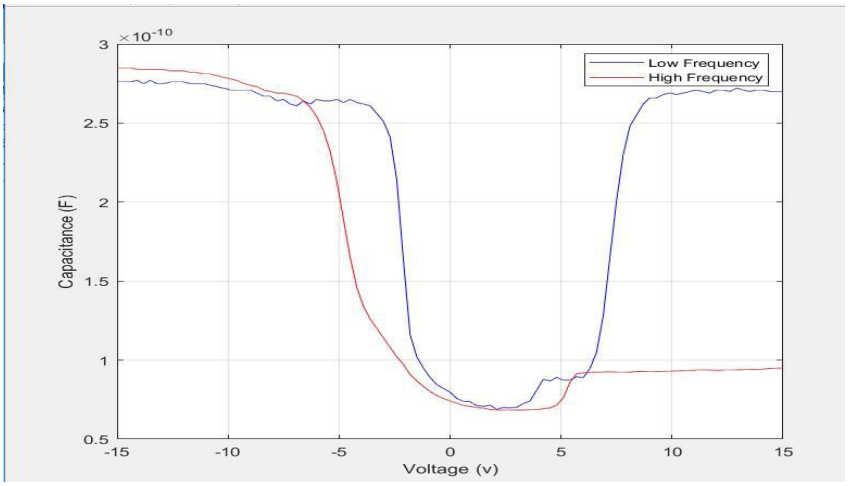

FIG 7 –C-V CURVES OF MOS CAPACITOR

For high frequency graph total capacitance decreases because there are two capacitors namely oxide capacitance and depletion capacitance. For low frequency total capacitance increases because there is only one capacitance which is oxide capacitance.

Oxide thickness came out to be 625.36 A.

V- CONCLUSION

Entire process of fabrication MOS capacitor took four steps in total. First step was oxidation, second step was applying photo-resist and etching backside oxide layer, third step was backside contact and final step was the front side contact. All the steps were completed successfully. The C-V curve of MOS capacitor shown us how its operation is depending on frequency, also all the reading which include oxide thickness and resistivity were the same as expected.

REFERENCES

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2- https://www.researchgate.net/post/Can_you_please_elaborate_the_meaning_of_three_different_terms_mentioned_in_LF_region_namely_MOS_transistor_at_any_f_of_attached_C-V_curve_below