REPORT-1-MOS CAPACITOR

Abstract:

In this report the process to fabricate MOS capacitor and methods to calculate its various parameters are studied. This process includes various steps like oxidation, oxide etching, deposition of aluminum and etc. For oxidation we will be using dry oxidation method. Resistivity of substrate can be calculated by applying some current to the substrate and measuring the voltage. For cleaning the wafer we are using AMD cleaning method. To etch the oxide layer on only one side of the wafer we will be applying photo-resist on another side of the wafer by spin coating method. For making contact we will be using two different methods one is using Nitride Sputter tool and second is deposition of aluminum directly. Finally the C-V curves of MOS capacitor will be studied which will show us the frequency dependency of MOS capacitor.

I- Introduction:

The MOS capacitor also called as MOS cap is the most important device in semiconductor device physics because, it is the control gate of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). MOSFETS are used on a large scale in integrated circuits. To understand the working of MOSFETS we need to know the working of MOS capacitors. By understanding how MOS capacitors work we will also learn about how its operation is frequency dependent.

II- Theory

It is very important to understand the working of MOS capacitors. The working of the MOS capacitors depends on three regions of operation. We will consider p-type semiconductor in our MOS capacitor. The operation will be nearly same for n-type substrate MOS capacitor, but voltage polarities will be reversed.

1- Accumulation mode

For p-type substrate if we apply negative voltage at the gate, the holes which are majority carriers in p-type substrate will accumulate near the oxide-semiconductor surface [3]. That is the reason why this mode is called as accumulation mode. The best way to understand the operation is by looking at the energy band diagram. Following is the energy band diagram of P-type semiconductor MOS capacitor in accumulation mode. As we can observe from diagram there is a band bending due to accumulation of majority carriers (holes) at the oxide-semiconductor surface. The total capacitance in accumulation mode is only due to capacitance across oxide layer [3].

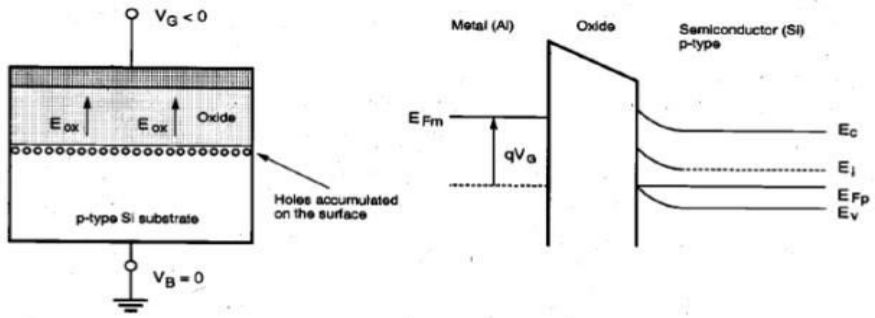

FIG 1 – ENERGY BAND DIAGRAM OF MOS CAPACITOR IN ACCUMULATION MODE [1]

2- Depletion mode.

Now we slowly move towards the positive voltage. While sweeping voltage from negative value to positive value, at a certain voltage value the total capacitance begins to decrease. This region where total capacitance continues to fall is called as depletion region. In depletion mode the majority carriers are depleted near the oxide-semiconductor interface [4]. Depletion layer width continues to increase as we keep increasing the voltage [4]. We can observe this behavior by looking at the energy band diagram of MOS capacitor in depletion mode. Following is the energy band diagram of MOS capacitor in depletion mode. The total capacitance is because of oxide layer as well as depleted layer in semiconductor [4].

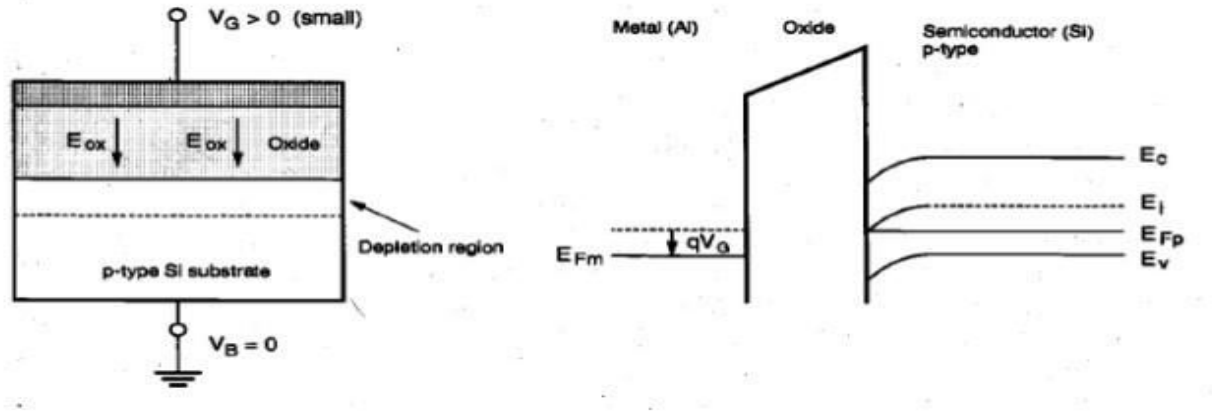

FIG 2 –ENERGY BAND DIAGRAM OF MOS CAPACITOR IN DEPLETION MODE [1]

3- Inversion Mode.

If we further go on increasing the voltage, then the oxide-semiconductor surface is inverted from p-type to more n-type. This mode is called as inversion mode. In inversion mode we apply positive voltage at the gate and due to positive voltage at gate minority electrons which are present in semiconductor are attracted towards the oxide-semiconductor interface [4]. The operation of MOS capacitor in inversion mode can be best understood by looking at the energy band diagram. Following is the energy band diagram of MOS capacitor in inversion mode. The total capacitance is only due to oxide layer [4].

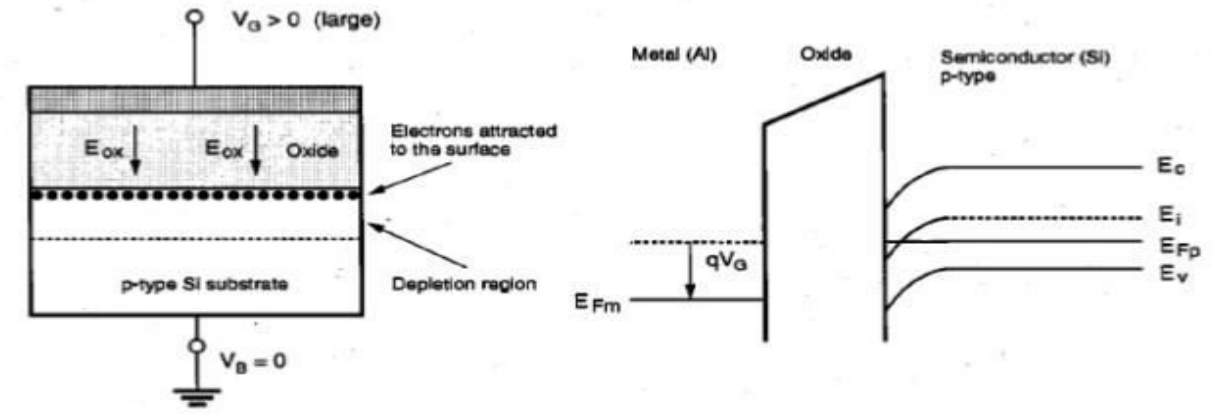

FIG 3 –ENERGY BAND DIAGRAM OF MOS CAPACITOR IN INVERSION MODE [1]

C-V curve of MOS capacitor (p-type semiconductor) in 3 different modes of operation.

In inversion mode during high frequency, number of depleted carriers near the interface increase, results in increase in depletion width and reduce capacitance [4]. During low frequency carriers get time to repel from surface and total capacitance is only due to oxide and total capacitance again increases [4].

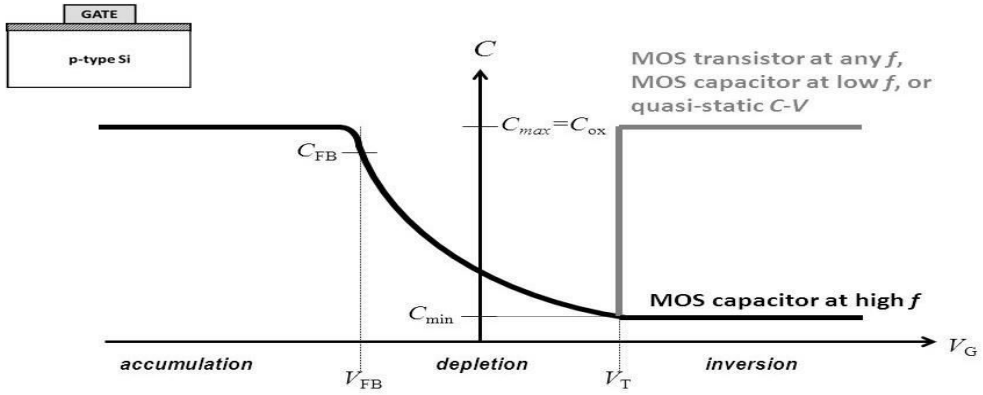

FIG 4 –C-V CURVE OF MOS CAPACITOR IN ALL THREE REGIONS OF OPERATION [2]

III- Experimental

The experiment starts with the process of oxidation. Before that the wafer has to be clean. The technique used for cleaning the wafer is AMD cleaning. Then the initial parameters are tested and then the wafer goes through the dry oxidation process with O2 flow of 1.548 lpm at 1000 deg calcium for 20 minute to form sio2 layer on both the sides of wafer. Next step is to etch the back side oxide layer. This process is done by applying photo-resist (positive resist – S1813) equal to 1 eye-dropper by spin coating (3000 rpm for 30 seconds) method on front side. After applying photo-resist, wafer is immersed in BOE (buffered oxide etch) for 1 minute. Next step is to make back contact on wafer. This process is done by using Nitride Sputter tool (deposition rate = 14.5 nm/min, pressure = 4e-3 torr, power = 250W, thickness = 150nm). No mask is used during this process. After creating backside contact the only thing which is remaining is the front side contact. These front side contacts are made by depositing aluminum dots on wafer using shadow mask (vacuum < 2e-5 torr, thickness = 150nm). Now last step is to test all parameters like c-v curve, flatband voltage etc.

IV- Results and discussions.

Resistivity of substrate is found out by using 4-point probe method and it came out to be 6.7 Ohm-cm. Table showing different values of resistivity on different voltages and currents is as follows.

Resistivity = $\frac{\Pi * t * V}{In(2) * I}$ …….. Equation (1)

Where

t = substrate thickness = 0.325 nm

V = Voltage

I = current

CURRENT	VOLTAGE	RESISTIVITY
50 uA	2.31 mV	6.8 Ohm-cm
100 uA	4.38mV	6.4 Ohm-cm
200 uA	8.93mV	6.6 Ohm-cm
300 uA	13.35mV	6.5 Ohm-cm

After finishing the entire wafer processing, we found out the C-V curves and oxide thickness.
C-V curves of different regions are as follows.

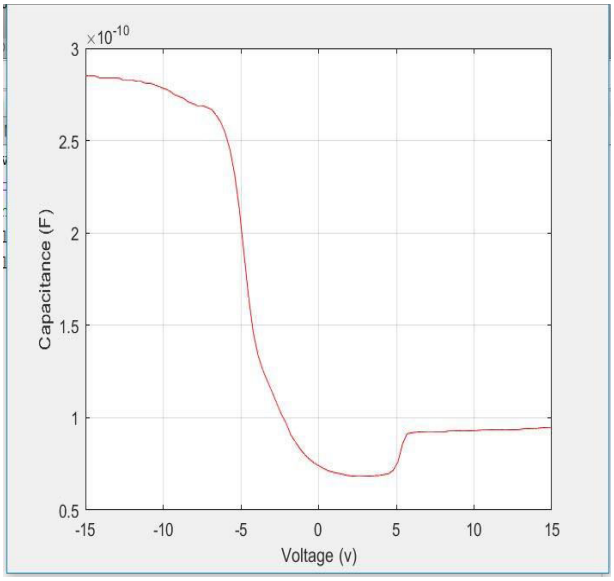

FIG 5 –C-V CURVE OF MOS CAPACITOR AT HF

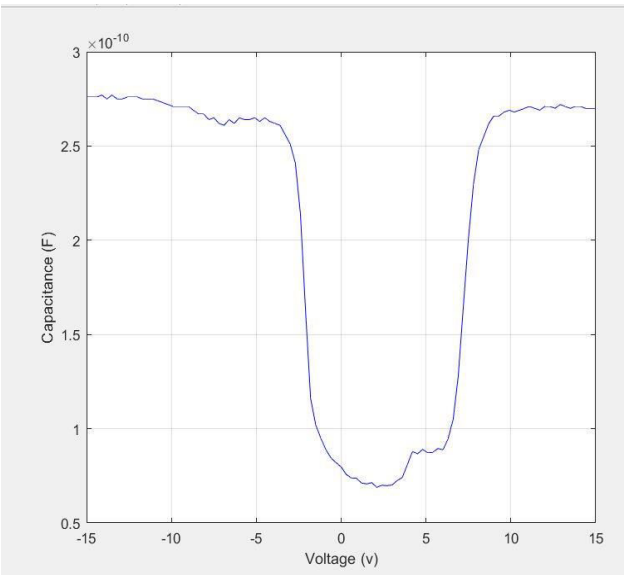

FIG 6 –C-V CURVE OF MOS CAPACITOR AT LF

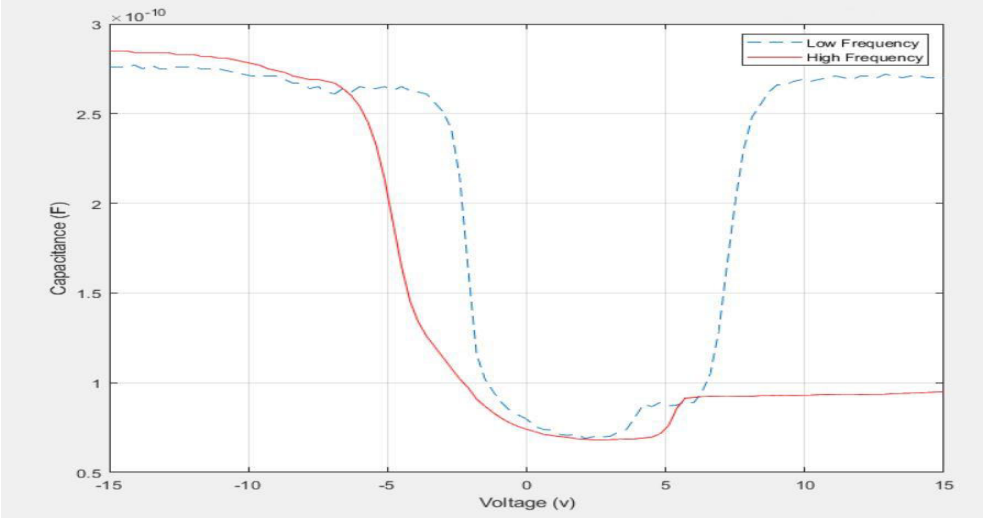

FIG 7 –C-V CURVES OF MOS CAPACITOR

For high frequency graph, total capacitance decreases because there are two capacitors in series, oxide capacitance and depletion capacitance [4]. For low frequency total capacitance increases because there is only one capacitance which is oxide capacitance [4]. We considered low frequency as 500 Hz and high frequency as 1 MHz. Cox from graph is 0.28nF and flatband voltage is approximately equal to -5V.

After dry oxidation method oxide thickness came out to be 624 A.

V- CONCLUSION

Entire process of fabrication MOS capacitor took four steps in total. All the steps were completed successfully. The C-V curve of MOS capacitor shows how its operation is dependent on frequency. The oxide thickness we measured came out to be 624 A which was suppose to be around 700 A and resistivity was suppose to be 6 Ohm-cm and we measured it to be 6.7 Ohm-cm. The measured value of resistivity is bit high as compared to what it was supposed to be.

REFERENCES

[1]- J. Baxi, “Seminar: Fabrication and Characteristics of CMOS,” *LinkedIn SlideShare*, 08-Jan-2014. [Online]. Available: https://www.slideshare.net/jayrbaxi/seminar-fabrication-and-characteristics-of-cmos. [Accessed: 08-May-2019].

[2]- M. Yadav, “Share and discover research,” *ResearchGate*. [Online]. Available: https://www.researchgate.net/post/Can_you_please_elaborate_the_meaning_of_three_different_terms_mentioned_in_LF_region_namely_MOS_transistor_at_any_f_of_attached_C-V_curve_below /. [Accessed: 08-May-2019].

[3] – J.Labram, “Introduction to MOS Capacitors”, April 2019.

[4] – J.Labram, “MOS Capacitors – CV Curves”, April 2019.