Experimental

Four silicon wafers are cleaned off with acetone, then methanol, then distilled (DI) water (AMD clean). The wafers are then dry baked in a Blue M oven at 120°C for 5 minutes. A thick oxide layer is grown by positioning the wafers in the Tempress Lindberg Furnace wet O2 chamber with the wafer tray at the halfway point where it is held at 1100°C with a flow rate of 3.00 liters per minute and water bubbler at 95°C for 49 minutes and 41 seconds until an oxide thickness of ~ 5000Å is achieved. The thickness of the oxide is then measured to be used in future calculations. The wafer is moved into a spin coater and positioned on the chuck. Positive photoresist (S1813) is added until 2/3 of the wafer is covered. The wafer is then spun at 3000 rpm for 30 seconds. A soft bake at 115°C for 2 minutes is performed using a hot plate on the wafer. The intensity of the UV lamp on the Karl Suss MJB3 is measured to be used to calculate the exposure time by taking the exposure of the S1813 and dividing it by the measured intensity. Taking the exposed mask, we develop using MF 321- metal ion free developer for 2 minutes. The wafer is immediately rinsed with DI water and then hard baked at 115°C in the oven for 5 minutes. The wafer is immersed in buffered oxide etch (BOE) for a time calculated using an etch rate of 1112Å/min and the determined oxide thickness. The wafer is rinsed with DI water to stop etching. An AMD clean is performed to remove the leftover photoresist. A dry bake at 120°C for 5 minutes is performed. The wafer is moved to a spin coater and positioned on the chuck where the wafer is covered with SOD. The wafer is then spun at 5000 rpm for 5 seconds. A hard bake is performed at 200°C for 10 minutes using the SOD hotplate. The wafer is then added to doping tube of the Tempress Lindberg Furnace at about three quarters of the length of the furnace where it is held at 1100°C for 30 minutes with an N2 flow at 2 lpm and O2 flow at 0.751 lpm. The wafers are moved to the spin coater and positioned on the chuck. Positive photoresist is used to cover the wafer and the wafer is spun at 3000 rpm for 30 seconds. A soft bake of the wafer is performed using a hot plate at 115°C for 2 minutes. The wafer is then exposed using the Karl Suss MJB3. Using MF321 the wafer is developed for 2 minutes and then rinsed with DI water. A hard bake is performed at 115°C for 5 minutes. The wafer is immersed in BOE using the measured field oxide thickness plus the P-glass thickness divided by the etch rate. The BOE is stopped using DI water and the sheet resistance is obtained. An AMD clean is performed to remove the photoresist. A dry bake is performed in the Blue M oven for 120°C for 5 minutes. The gate oxide is grown using the Tempress Lindberg Furnace dry oxidation chamber by placing the wafer at the halfway position and holding at 1100°C for 20 minutes until an oxide thickness of ~ 700Å is achieved. The oxide thickness is measured to be used in future measurements using an ellipsometer. The wafer is moved to the spin coater where it is positioned on the chuck and covered with photoresist. The wafer is then spun at 3000 rpm for 30 seconds. A soft bake is performed on the wafer using a hot plate at 115°C for 2 minutes. The wafer is then exposed using the Karl Suss MJB3 for the time calculated in previous step. The wafer is then developed using MF321 developer for ~ 2 minutes and rinsed to stop the development. A hard bake is performed in the blue M oven at 115°C for 5 minutes. The wafer is then immersed in BOE to remove the gate oxide, P-glass, and field oxide and DI water is used to stop the etching. An AMD clean is performed to remove the photoresist. The wafer is then dry baked in the Blue M oven at 120°C for 5 minutes. Aluminum contacts are deposited using the Cooke Evaporator at a pressure of <2e-5 Torr until 150 nm thick contacts are achieved.

1st Session

AMD clean/dry bake

Wet oxidation at 1100 Degree Celsius for 49 Min 41s, O2 flow rate of 3lpm, h2o bubbler at 95 Celsius

\*\*\* This may be where our error comes in as the wafers had oxidized greater at the top than the bottom. Measured.



Oxide thickness per wafer measured as ?,?,?,?

CLW - 631.2 nm @ flat cut, 366 nm @ opposite side

SR - 523.9 @ edge, 432.3 @ center

SC - highest 432.2 nm, lowest 359.6 nm

HS - highest 415.1 nm, lowest 163.0 nm

2nd Session

AMD clean -> Spin coat positive photoresist at 3k rpm for 30 sec

Soft bake

Measure lamp intensity (43.7mW/cm^2, 150mJ/cm^2 for PR), cover with mask one and expose to UV for 3.43 seconds

(150mJ/cm^2)/(43.7mW/cm^2) = 3.43 seconds.

Develop in MF 321 developer

Hard bake 115C for 5 minutes.

\*\*\* All wafers were hard baked at the same time so there may be an annealing issue due to the time we waited to put all the wafers onto the hotplate. Also, a piece of aluminum foil was used on the hotplate which raised some of the wafers above the surface results in possible uneven heating.

3rd session

Wafers etched in BOE for 5min 40.8s (thickest wafer oxide/1112A/min etch rate), rinse with DI water to stop etching.

631.2/111.2 = 5.68 = 5 minutes 40.8 seconds.

AMD clean/bake -> spin coat SOD (1ml/cover full wafer, 5000RPM, 5s) -> bake on hot plate 200 Celsius for 10min

Dope in furnace (1100 C, 30 min, N2 flow 2lpm, O2 flow .75 lpm, positioned ¾ way into tube)

4th session

Spin coat photoresist at 3130 rpm for 28 seconds. Covering the whole wafer with S1813.

Soft bake at 115C for 5 minutes. (foil was laid down to protect the hotplate from S1813)

\*\* the foil could cause uneven heating.

Expose with mask with Karl Suss MJB3 for 3.28 seconds (calculation below)

(150mJ/cm^2)/(45.7mW/cm^2)=3.28 seconds

Develop in MF 321 - Metal ion free developer for 2 minutes. Rinse with DI water.

SC - sample fucked at this step (mask alignment wrong)

SR - sample fucked at this step (mask alignment wrong)

CLW - scratched to fuckin’ hell. Hopefully turns out okay. Nope, it’s fucked. (mask alignment)

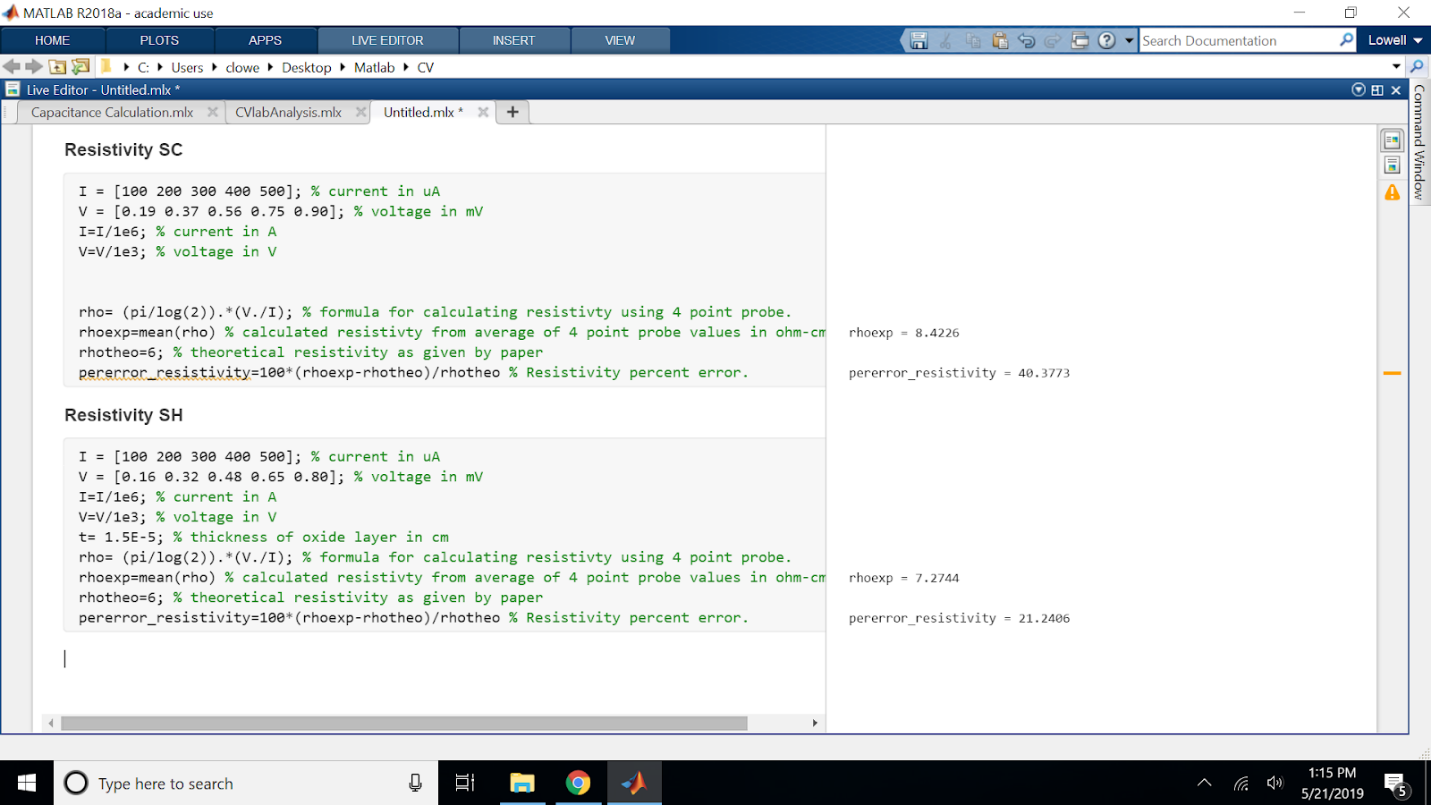
HS - Only one that worked.

5th session

Partha removed the photoresist and metal ion developer and remade them so all samples are good again.

Wafers etched in BOE for 5min 40.8s (thickest wafer oxide/1112A/min etch rate) to remove gate oxide layer, rinse with DI water to stop etching.

After etch sheet resistance is measured.



AMD clean performed.

Dry bake in oven at 120C for 5 minutes.

Tube B, O2 flow at “150” (1.584 lpm), 1100 C for 23 minutes. (was supposed to be 20)

Oxide thicknesses. Flat part is facing right. 1 is top region and 2 is bottom region.

1 2

SC - 780 angstroms 771 angstroms

HS - NA 786

CLW - 778 766

SR - 787 791

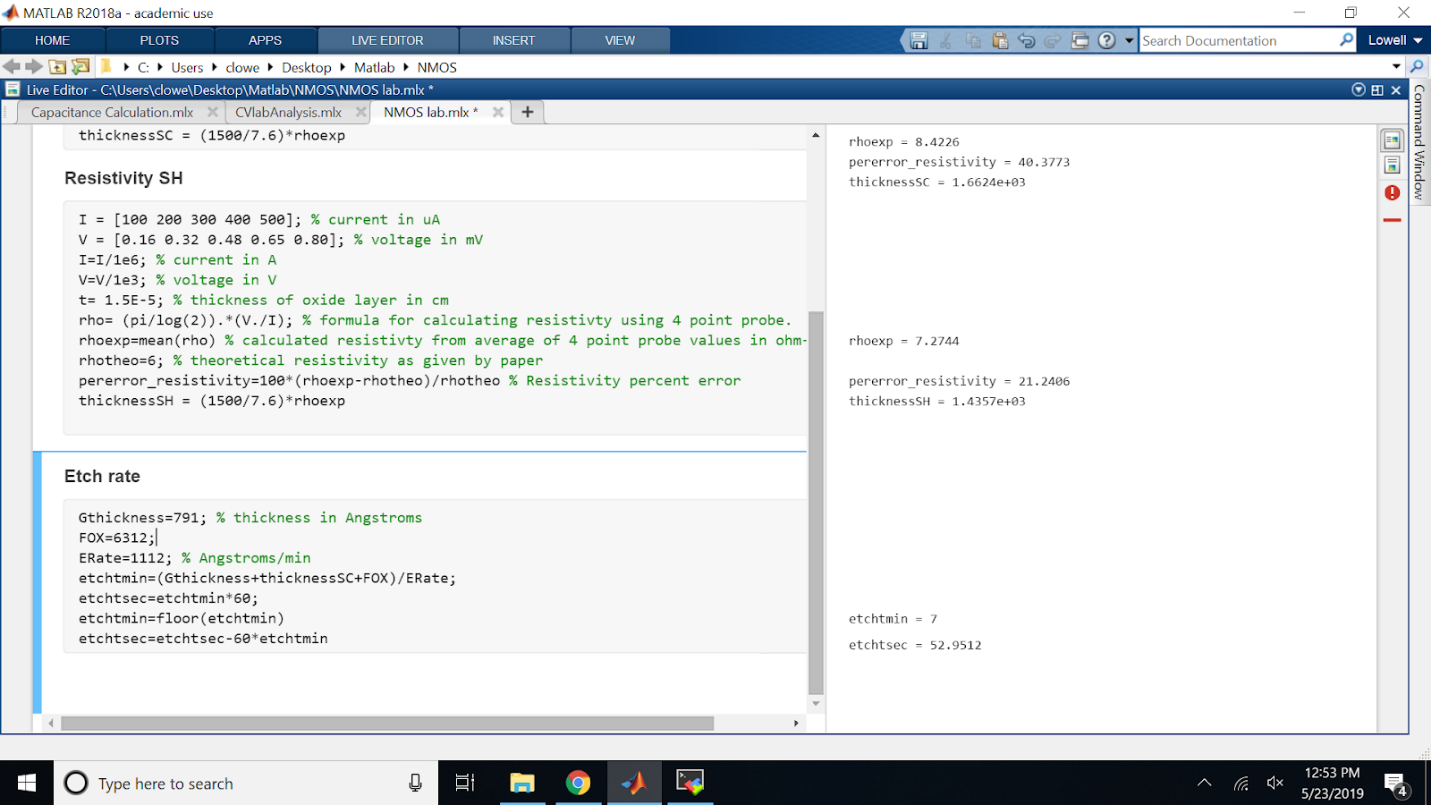
Thickest oxide measured is 791 angstroms.

Wafers then spin coated (3000 rpm for 30 seconds) with positive photoresist (S1813) using 1 eye dropper full to cover ⅔ of the wafer. Soft bake at 115 C for 1 minute (different from procedure which says 2 minutes). Expose with mask 3- MJB3 for 8.5 seconds. Develop with MF321 - metal ion free developer for 2 minutes then rinse immediately with DI water. Hard bake at 115 C for 5 minutes.

6th Session

The wafers are immersed in BOE for 7 minutes 53 seconds.

Calc shown below



After etching, the sample was rinsed with DI water.

AMD clean performed

150 nm Aluminum contacts deposited by sputtering using Cooke Evaporator.

In the spincoater, ⅔ of the wafer is covered in S1813 Positive photoresist and spun at 3000rpm for 30 seconds. The substrate is then soft baked at 115C for 2 minutes

The wafer is exposed using mask 4 - MJB3 for 8.5 seconds.

The wafer is developed in MF 321, metal ion free developer for 2 minutes, and rinsed with DI water.

The wafer is then hard baked at 115C for 5 minutes.

The aluminum is then etched in Al etchant for ? seconds until the greenish discoloration has vanished. To stop the etching, the wafer is rinsed in DI water.

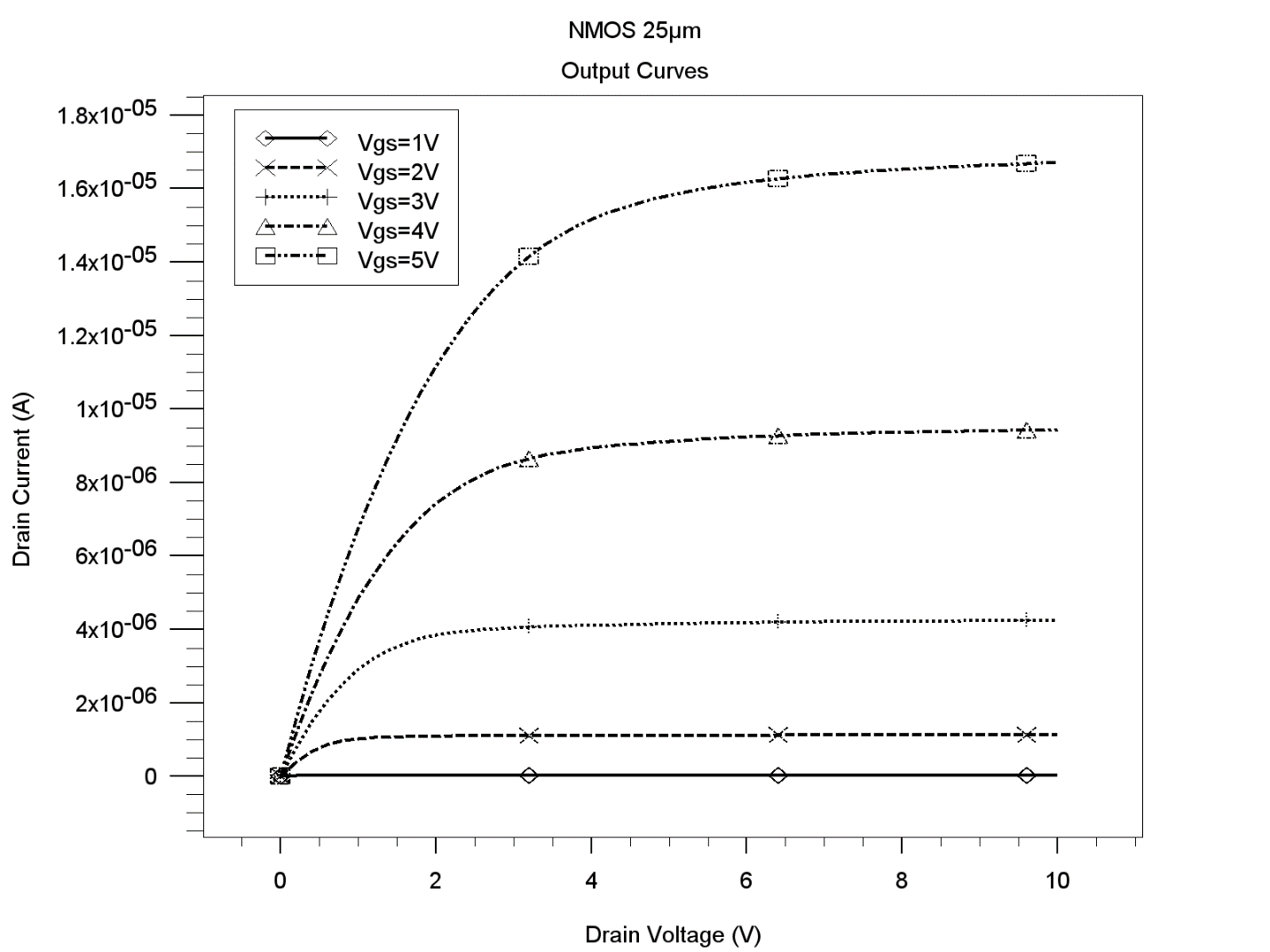
The substrate is then AMD cleaned and dry baked at 120C for 5 minutes.

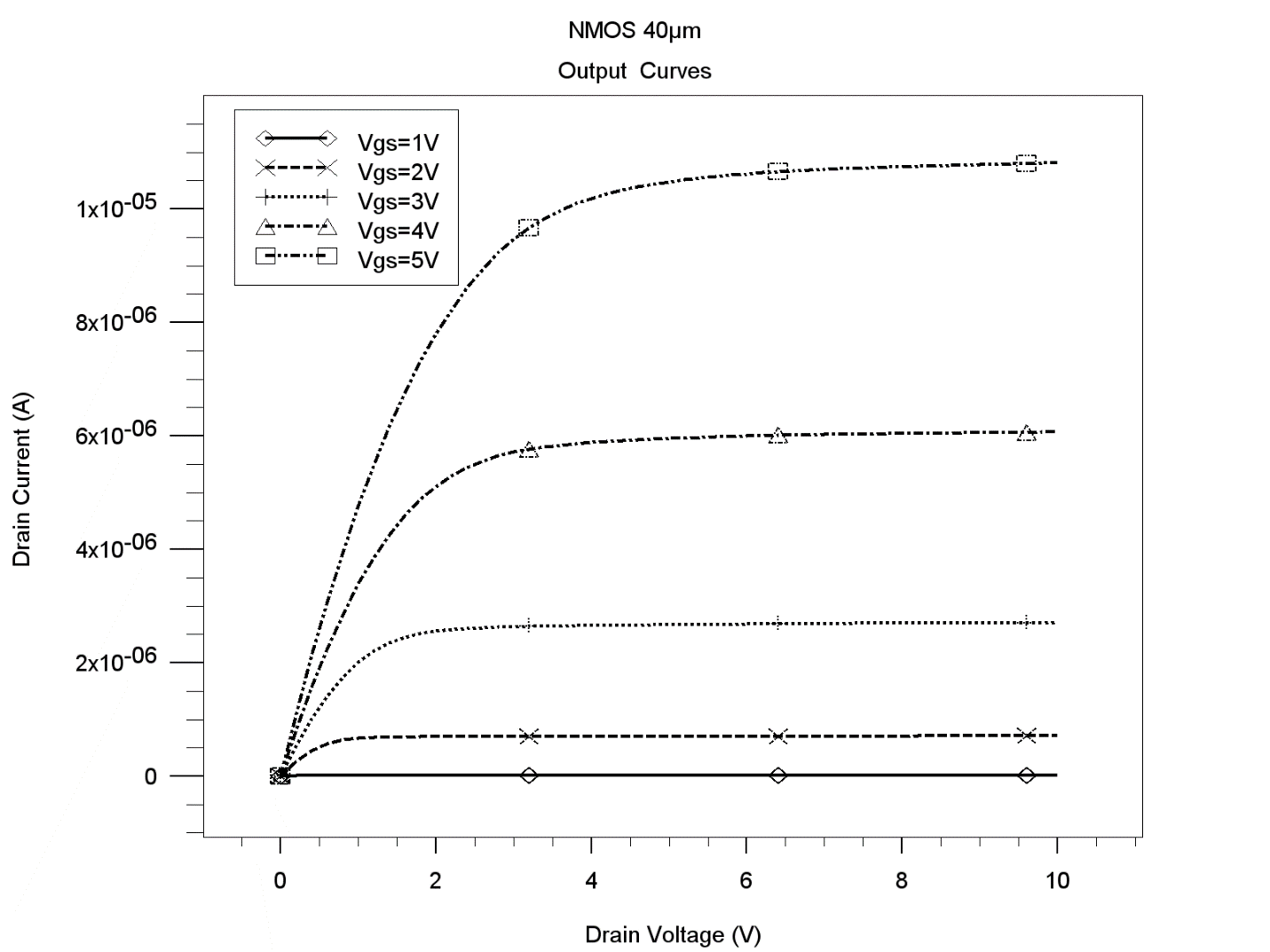
Session 7

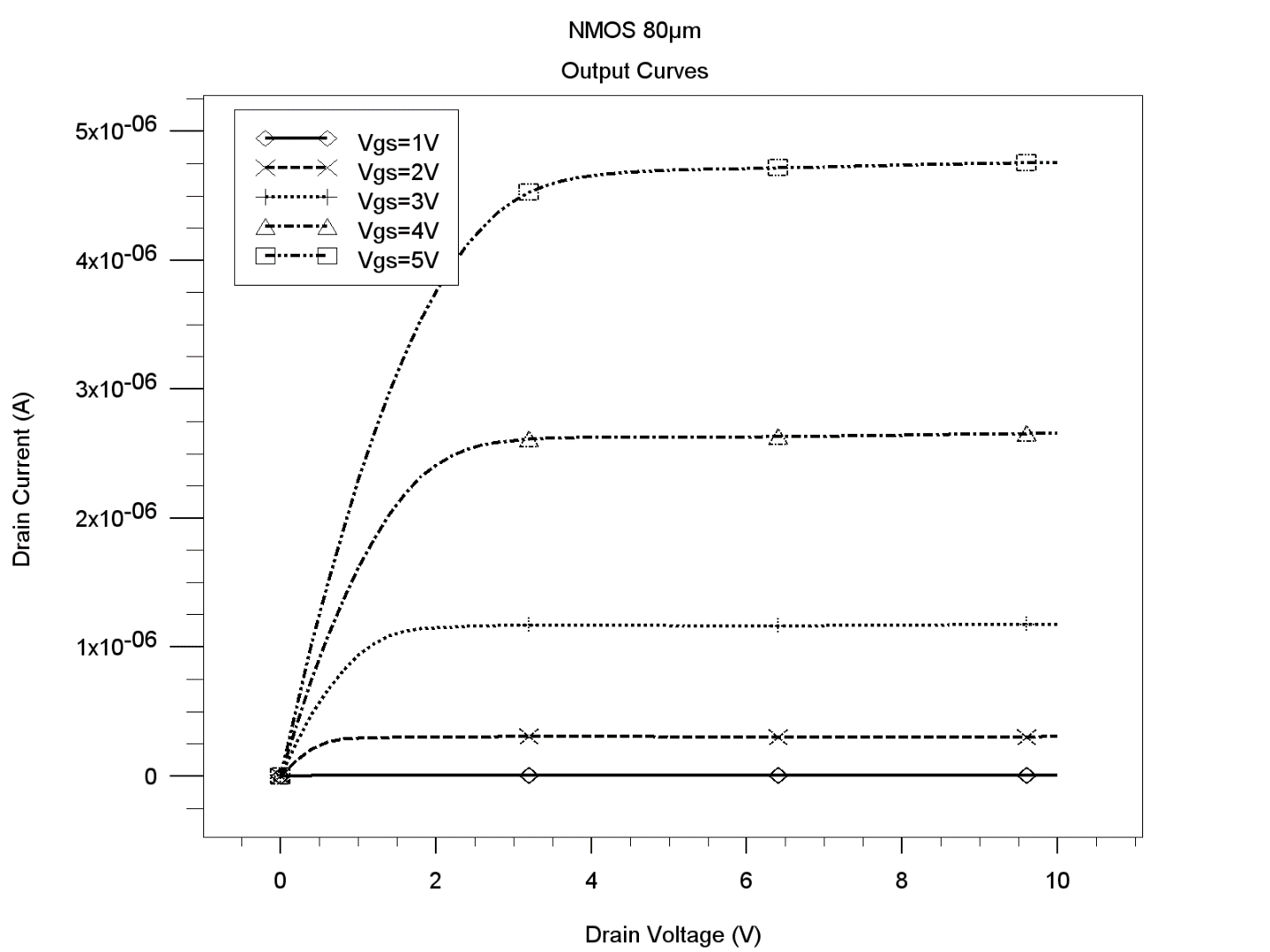
The wafers are each tested for IV characteristics.

**ATHENA/ATLAS Modeling (code at end of document)**

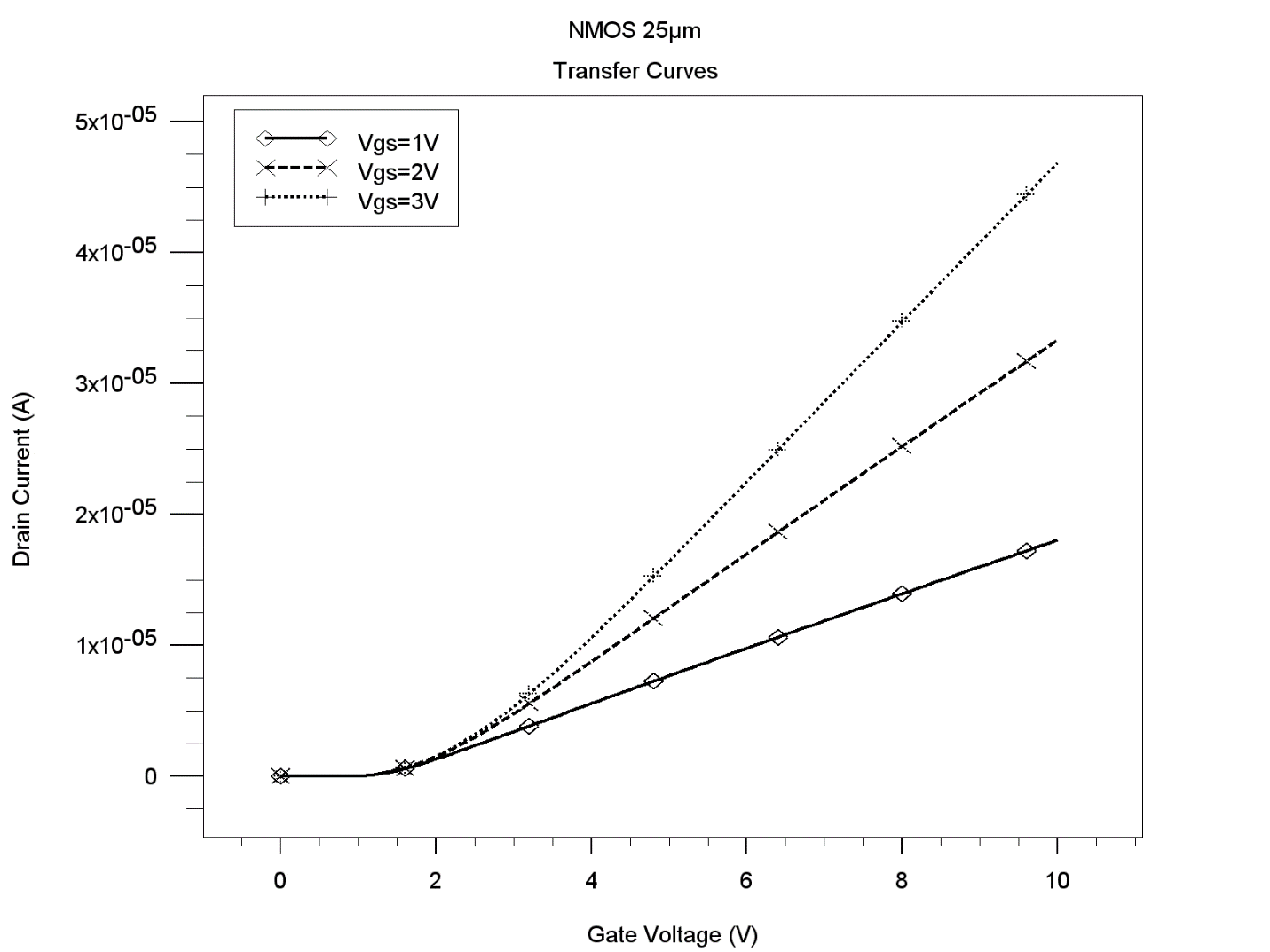
1. **Output Curves**

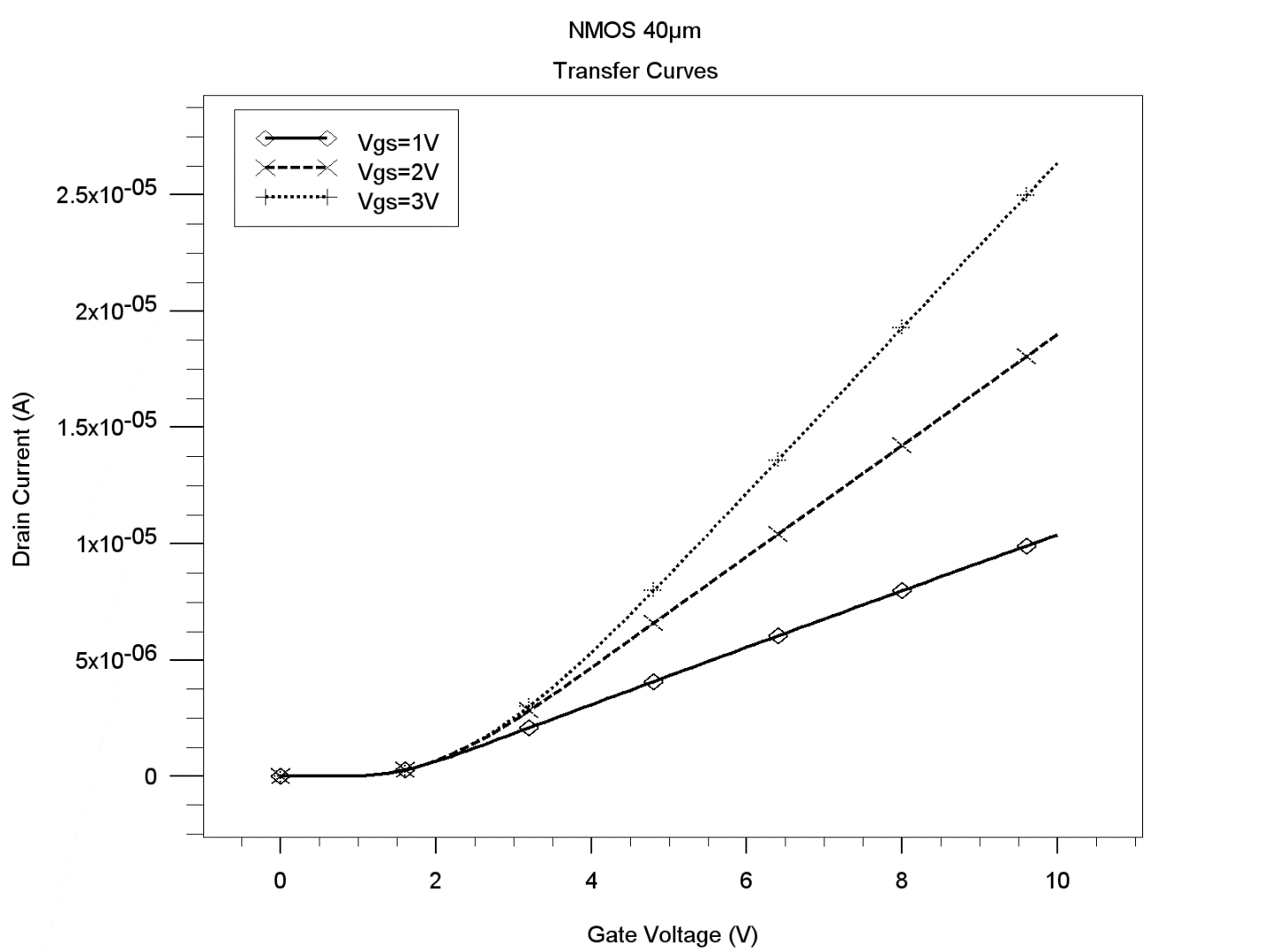
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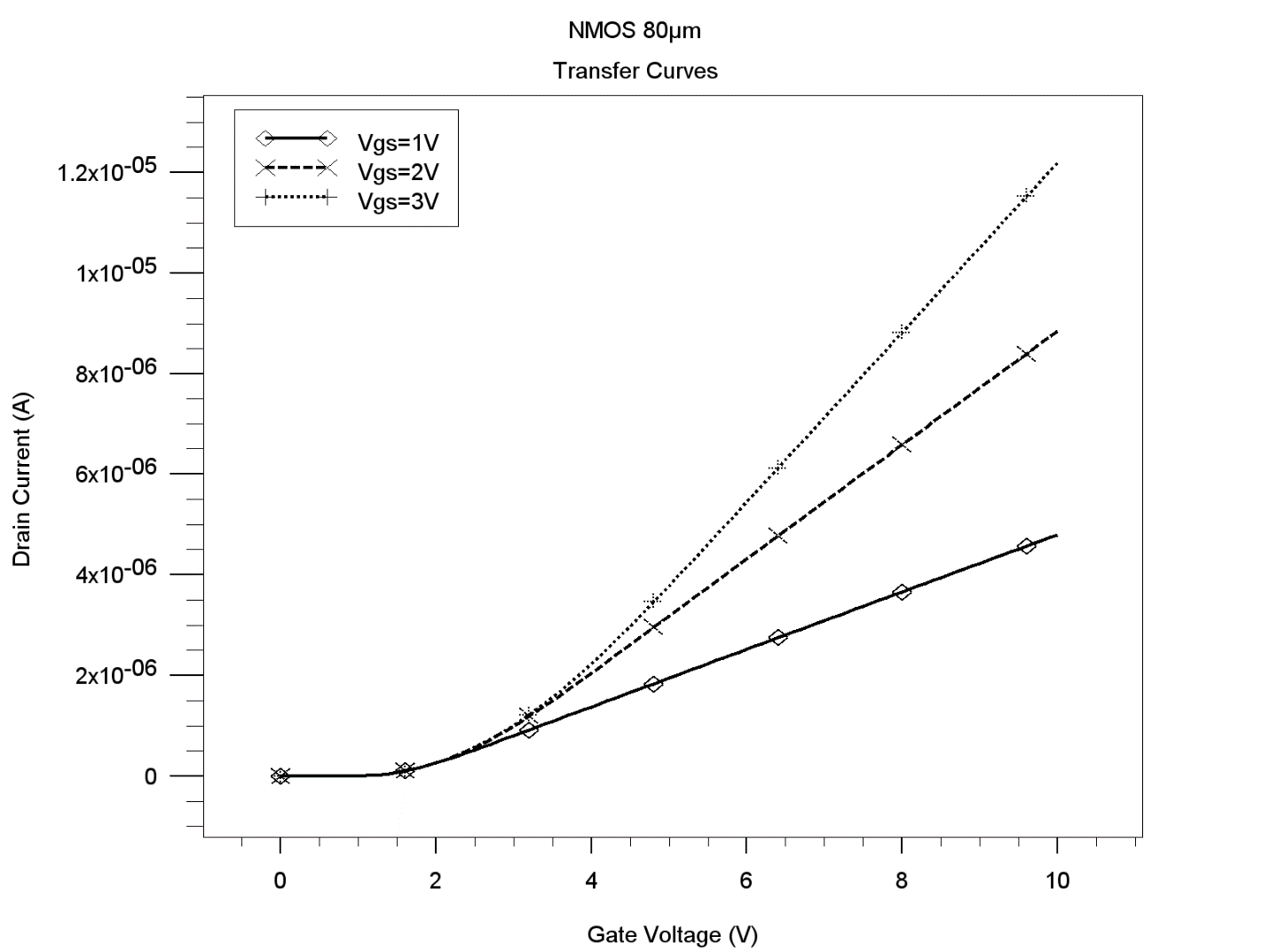
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**2. Transfer Curves**

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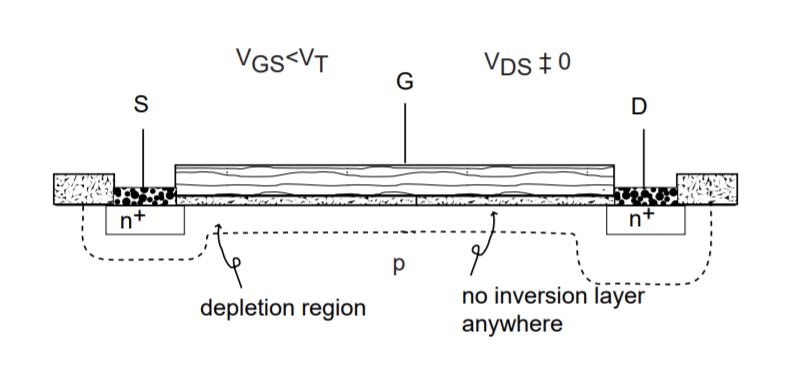
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****

**THEORY**

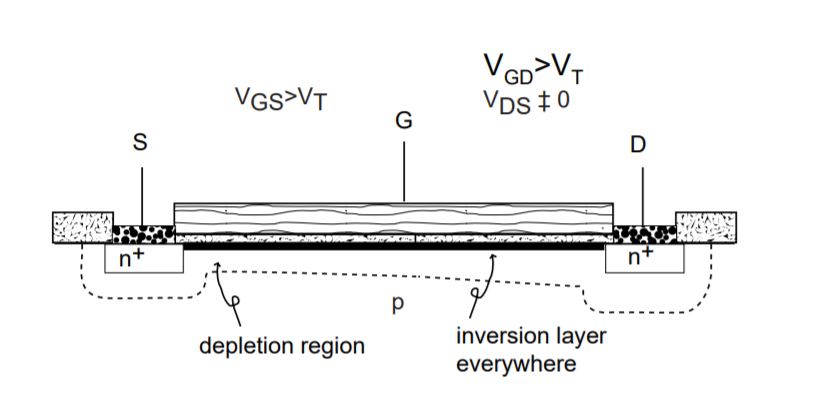
NMOSFET(N-channel metal oxide semiconductor field effect transistor) is a four terminal device including bulk terminal. Out of four terminal bulk/body terminal is usually connected to source. The carriers flow from source to drain, and the rate of flow of carriers is controlled by the gate terminal. If we observe the gate terminal of MOSFET it is similar to MOS capacitor. Therefore MOS capacitor is the control gate of the MOSFET. MOSFET is operated in inversion mode. If the device is NMOS, then the channel between the source and drain is of electrons and electron are transferred from source to drain. The flow of electrons is controlled by gate terminal. Usually the operation of N-MOSFET is divided into three region of operations.

**1 - Cut-off mode**



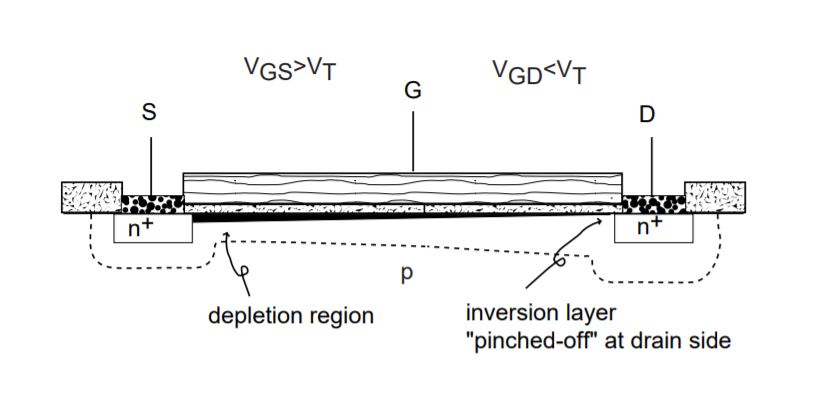
As this is N-MOSFET, we start applying positive voltage at gate to create an inversion layer near the oxide and semiconductor interface.In cutoff region, the gate voltage is less than the threshold voltage. Therefore channel is not formed between the source and drain region. In cutoff region, MOSFET is said to be in off state.

**2 - Linear or triode region**



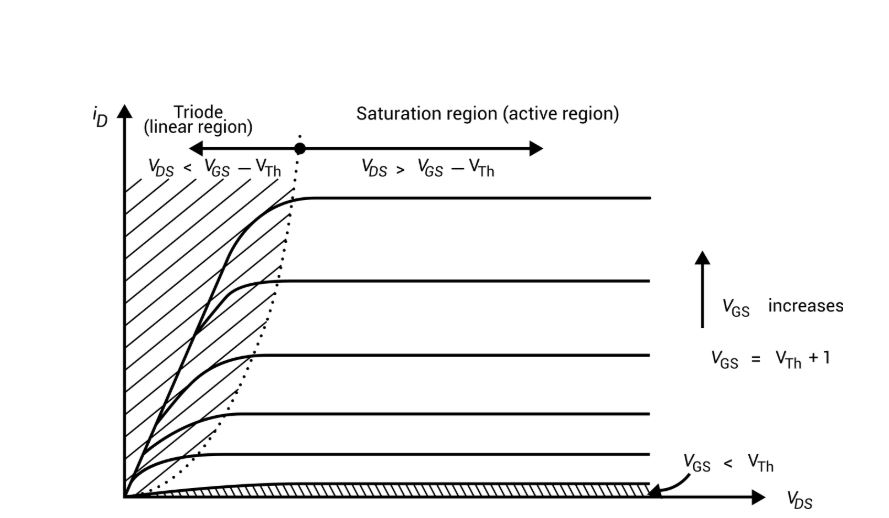
Now we try to increase the gate voltage in positive direction. In linear region, the gate voltage is greater than the threshold voltage and the channel is formed between the source and drain region. In linear or triode mode the channel is uniform across the region.The flow of carriers does not only depend on gate voltage it also depends on drain voltage. Therefore we begin to increase drain voltage as well. The current increases linearly with increase in the drain voltage. Therefore this mode is called as linear mode. In this mode of operation MOSFET works as a resistance.

**3-  Saturation region**



When we try to increase the drain voltage beyond threshold voltage, the depletion region near the drain region increases results in no more presence of channel near the drain region. As a result the channel is pinched off near the drain region. Therefore this mode of operation is also called as pinch off mode. MOSFET is said to be in on state when it is in saturation mode.

**Output characteristics**



As we can observe from the output characteristics, in linear region current increases linearly with increase in drain voltage and acts as a resistor. In saturation region the current saturates no matter how much we increase the drain voltage. When gate voltage is less than the threshold voltage the channel is not formed and there is no current flowing.

**Code**

go athena

#25um

# leftmost position of gate oxide

SET LG=137.5

# rightmost position of gate oxide

SET RG=162.5

#40um

# leftmost position of gate oxide

#SET LG=130

# rightmost position of gate oxide

#SET RG=170

#80um

# leftmost position of gate oxide

#SET LG=110

# rightmost position of gate oxide

#SET RG=190

#Define the mesh

line x loc=0.00 spac=5

line x loc=$"LG" spac=5

line x loc=$"RG" spac=5

line x loc=300 spac=5

line y loc=0.00 spac=0.025

line y loc=2.5 spac=0.25

line y loc=6.75 spac=0.625

line y loc=10 spac=1

#Define the substrate (resistivity in ohm-cm)

init silicon boron resistivity=6 orientation=111 width.str=200.00

#Thermally grown oxide#

diffus time=50 minutes temp=1100 weto2 press=1

#Etch specific region

etch oxide left p1.x=$"LG"

etch oxide right p1.x=$"RG"

#Output Str file and plot

structure outf=before.str

tonyplot before.str

#Deposit dopant

deposit oxide thick=0.5 c.phosphor=1e21 divisions=10

# To drive in our dopants we anneal using command tab -> Process -> Diffuse

diffus time=30 minutes temp=1100 nitro press=1

#Output Str file and plot

structure outf=after.str

tonyplot after.str

#remove oxide layer

etch oxide all

############## ADDING GATE OXIDE ###################

#Adds gate oxide

diffus time=30 minutes temp=1100 dryo2 press=1

#etch

etch oxide left p1.x=$"LG"

etch oxide right p1.x=$"RG"

#output gate structure

structure outf=aftergate.str

tonyplot aftergate.str

############# ADDING ELECTRODES ####################

# Deposit aluminum - command window deposit

deposit aluminum thick=0.2 divisions=10

#output gate structure

structure outf=after\_elec.str

tonyplot after\_elec.str

#Etch using the cmd tab

#Etch to the left of the source

etch aluminum start x=0.00 y=-0.40

etch cont x=0.00 y=0.40

etch cont x=20 y=0.40

etch done x=20 y=-0.40

#Etch between the source and gate

etch aluminum start x=80 y=-0.40

etch cont x=80 y=0.40

etch cont x=$"LG" y=0.40

etch done x=$"LG" y=-0.40

#Etch between the gate and drain

etch aluminum start x=$"RG" y=-0.40

etch cont x=$"RG" y=0.40

etch cont x=220 y=0.40

etch done x=220 y=-0.40

#Etch to the right of the drain

etch aluminum start x=280 y=-0.40

etch cont x=280 y=0.40

etch cont x=300 y=0.40

etch done x=300 y=-0.40

#Define Electrodes using cmd -> str -> electrode

electrode name=gate x=150 y=0.0

electrode name=source x=60 y=0.0

electrode name=drain x=260 y =0.0

#output gate structure

structure outf=FET.str

tonyplot FET.str

####################ATLAS PART################

go atlas

#Previous stuff all on one line.

material material=silicon eg300=1.12 mun=1100

#define gate

contact name=gate

#Define method

method newton

#Initialize solver

solve init

## Create output curves

# Set V\_g to specified vales (BIAS HERE)

solve vgate=1 outf=solve\_C\_4\_tmp1

solve vgate=2 outf=solve\_C\_4\_tmp2

solve vgate=3 outf=solve\_C\_4\_tmp3

solve vgate=4 outf=solve\_C\_4\_tmp4

solve vgate=5 outf=solve\_C\_4\_tmp5

# Now do the V\_d sweeps (BIAS HERE)

load infile=solve\_C\_4\_tmp1

log outf=part\_C\_4\_1.log

solve name=drain vdrain=0 vfinal=10 vstep=0.2

load infile=solve\_C\_4\_tmp2

log outf=part\_C\_4\_2.log

solve name=drain vdrain=0 vfinal=10 vstep=0.2

load infile=solve\_C\_4\_tmp3

log outf=part\_C\_4\_3.log

solve name=drain vdrain=0 vfinal=10 vstep=0.2

load infile=solve\_C\_4\_tmp4

log outf=part\_C\_4\_4.log

solve name=drain vdrain=0 vfinal=10 vstep=0.2

load infile=solve\_C\_4\_tmp5

log outf=part\_C\_4\_5.log

solve name=drain vdrain=0 vfinal=10 vstep=0.2

tonyplot -overlay -st part\_C\_4\_1.log part\_C\_4\_2.log part\_C\_4\_3.log part\_C\_4\_4.log part\_C\_4\_5.log

log off

## Create transfer curves

# Set V\_d to specified values

solve vdrain=1 outf=solve\_C\_5\_tmp1

solve vdrain=2 outf=solve\_C\_5\_tmp2

solve vdrain=3 outf=solve\_C\_5\_tmp3

# Save as separate ATLAS file

mesh\_inf=FET.str

# Now do the V\_g sweeps

load infile=solve\_C\_5\_tmp1

log outf=part\_C\_5\_1.log

solve name=gate vgate=0 vfinal=10 vstep=0.1

load infile=solve\_C\_5\_tmp2

log outf=part\_C\_5\_2.log

solve name=gate vgate=0 vfinal=10 vstep=0.1

load infile=solve\_C\_5\_tmp3

log outf=part\_C\_5\_3.log

solve name=gate vgate=0 vfinal=10 vstep=0.1

tonyplot -overlay -st part\_C\_5\_1.log part\_C\_5\_2.log part\_C\_5\_3.log

quit