FINAL PROJECT REPORT

BY

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&

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ECE 520

DESIGN APPROACH

Closed-loop gain	5 (absolute value)
Load Capacitance	2pF
Settling time	30nS for 0:01% settling

We know that $\beta = \frac{1}{5} = 0.2$

We know the settling time for 0:01% settling. The settling error accounts for static and dynamic error and therefore it will be halved in order to account for dynamic error or static error only.

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$$A_o\omega_o = \frac{\ln 50000}{30nS} * 5$$

$$A_o\omega_o = 348.08 \text{ M Hz}$$

The ideal value of closed loop is $1/\beta$ but the actual value is $\frac{A_o}{1+A_o\beta}$. The difference between these two values will give the error value which will be $error * \beta$

This gives us the following equation,

$$\frac{1}{\beta} - \frac{1}{\beta}\frac{A_o}{1 + A_o\beta} = 0.005\%\frac{1}{\beta}$$

$$5 - 5\frac{A_o}{1 + (5 * A_o)} = 0.005\%\frac{1}{0.2}$$

$$A_o = 99995$$

$$A_o = 100dB$$

It is known that,

$$A_o\omega_o = \frac{g_m}{2\pi C_L}$$

$$100db = \frac{g_m}{2\pi * 2pF}$$

$$\underline{g_m > 4.37mS}$$

Targeted

$$\frac{g_m}{I_d} = 15$$

$$I_d = 291\mu A$$

The design of fully differential folded gain-boosted cascode was implemented to get a high 1st stage gain. The second stage is a fully differential active load common source op-amp. After analyzing the $\frac{g_m}{I_d}$ curves, the length $L = 240\ n$ was set and the respective values of the with were calculated. After implementing the circuit and analyzing the graphs of settling time and phase-margin, lowering the g_m was decided to get a better phase-margin. This was attained by reducing the width. This let the circuit to hit an acceptable value of phase-margin and settling time. This came at the cost of open-loop gain which was reduced from 92 dB to 87 dB. The lowering of gain took care of settling time and lowering g_m reduced the unity-gain bandwidth which improved stability and also the closed loop response.

SCHEMATICS

The topology which we thought of using was the telescopic cascode with 3 PMOS and NMOS. This design was extremely restrictive as the devices demanded precise biasing because of the low V_{DD}. Thus we decided to use folded cascode with gain boosted which can provide high gain. The complete schematic is shown **in figure. In the figure** , the load capacitor C_L is added just for simulation purposes, this capacitor is removed before plugging the op-amp in the testbench.

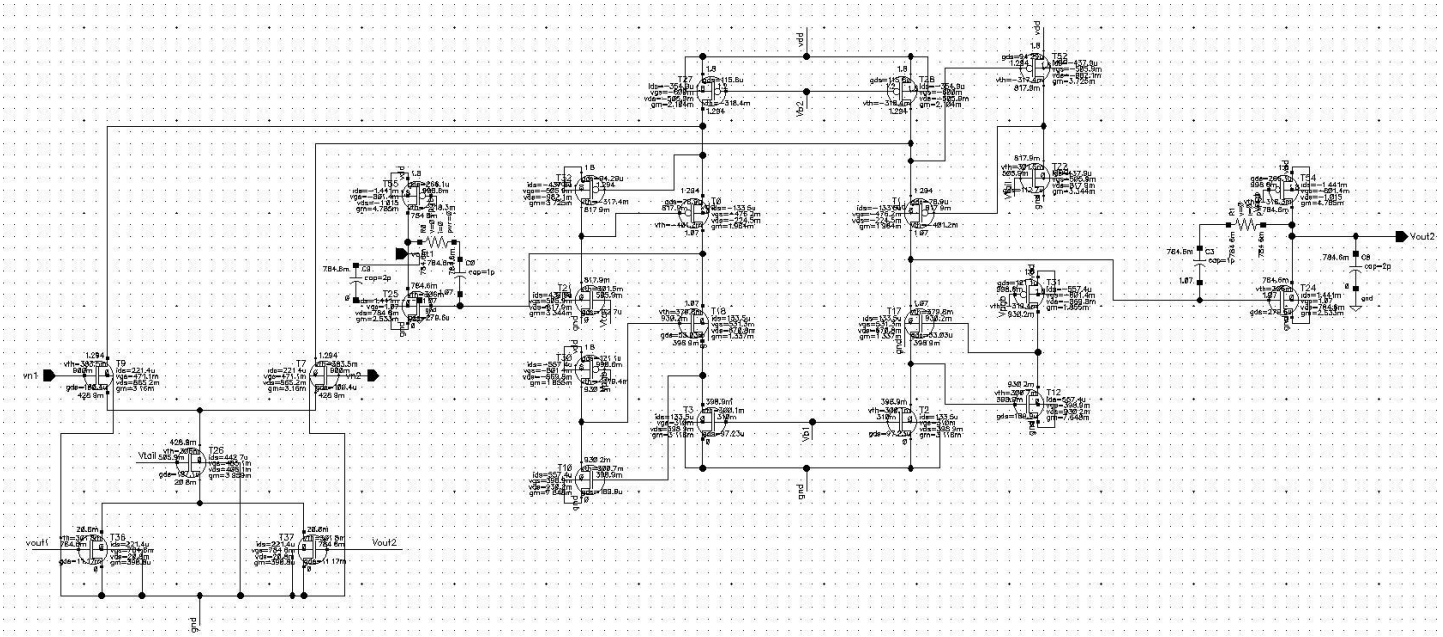


Figure 1: Schematic Topology

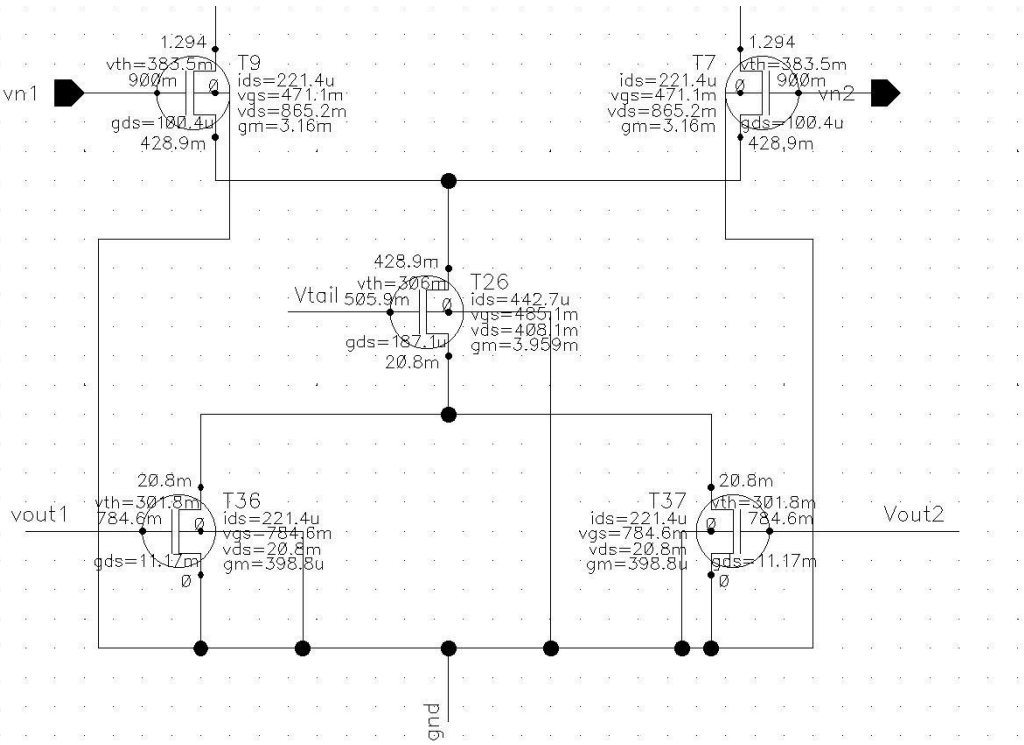


Figure 2: Schematic Topology Input Stage

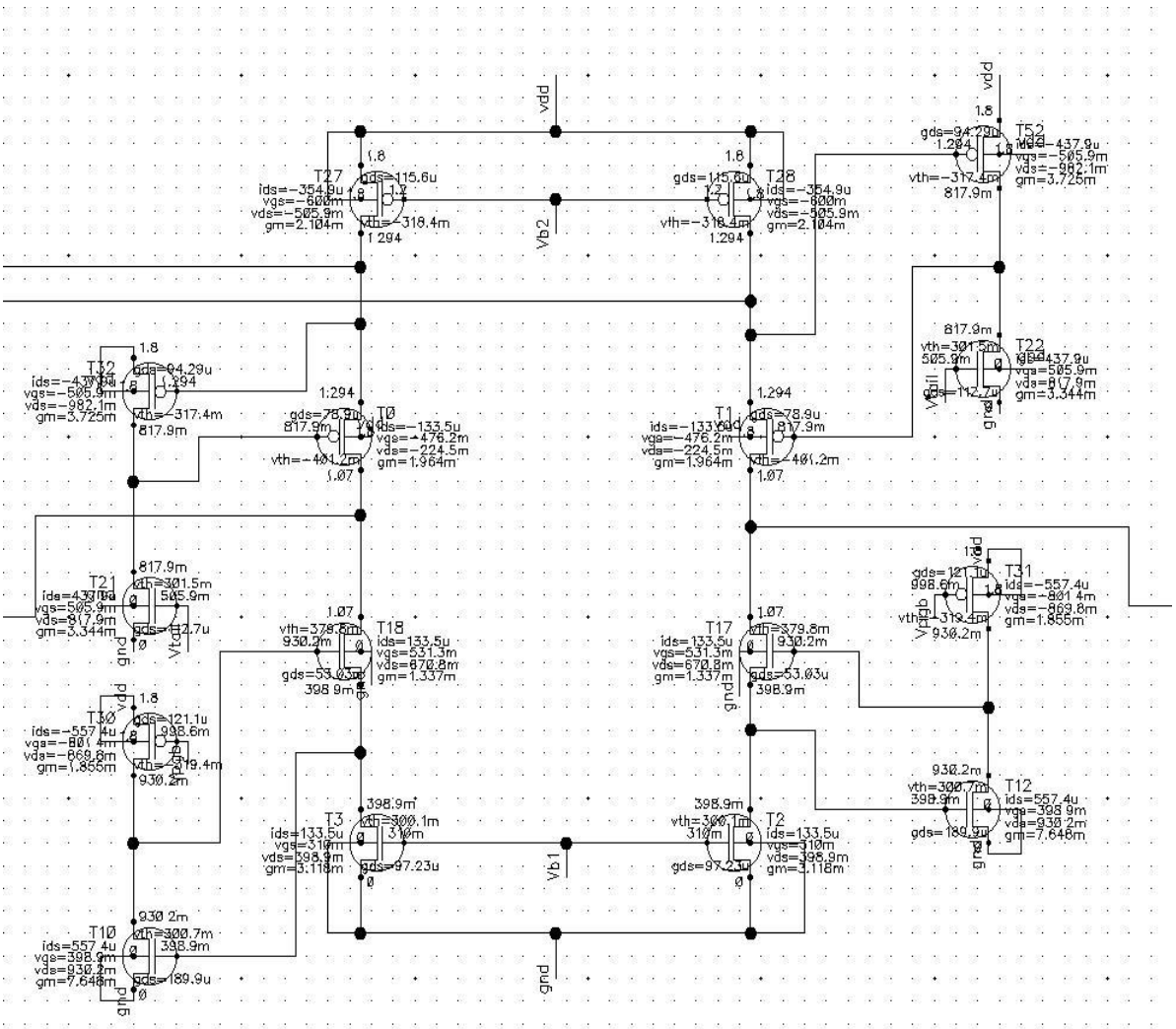


Figure 3: Schematic of Folded cascode gain boosted

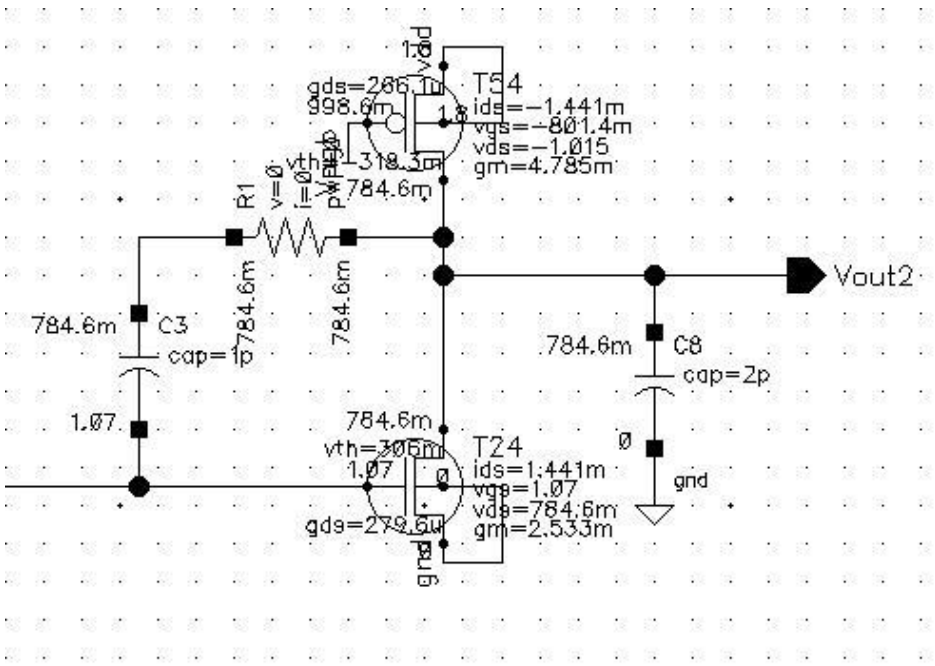


Figure 4:Output Stage

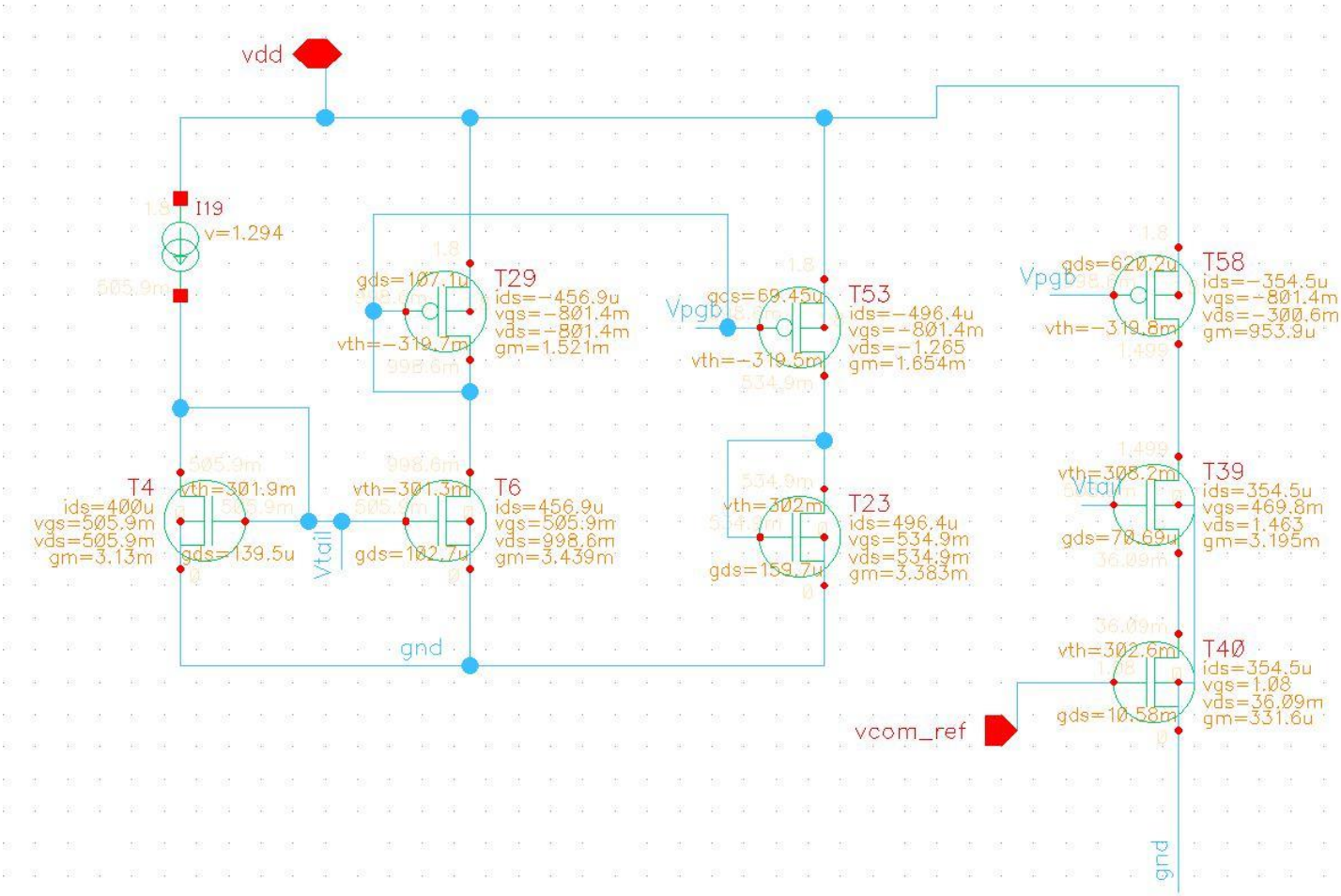


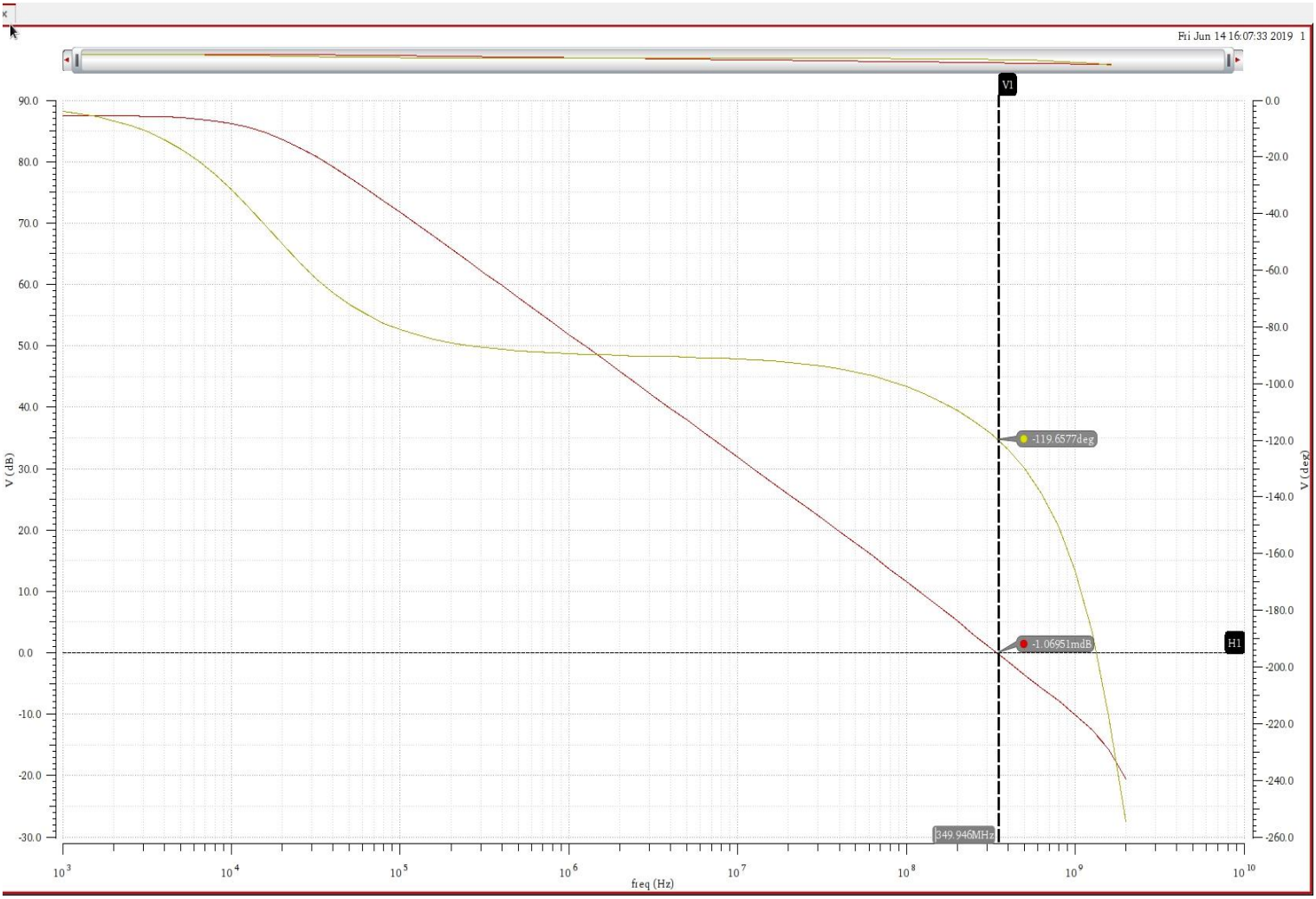
Figure 5:Biasing Circuit

The biasing for the transistors in the cascaded stage is done by the ideal voltage sources as we were unable to replicate the same from the current mirror circuits.

BANDWIDTH AND PHASE MARGIN

Bandwidth = 350 MHz

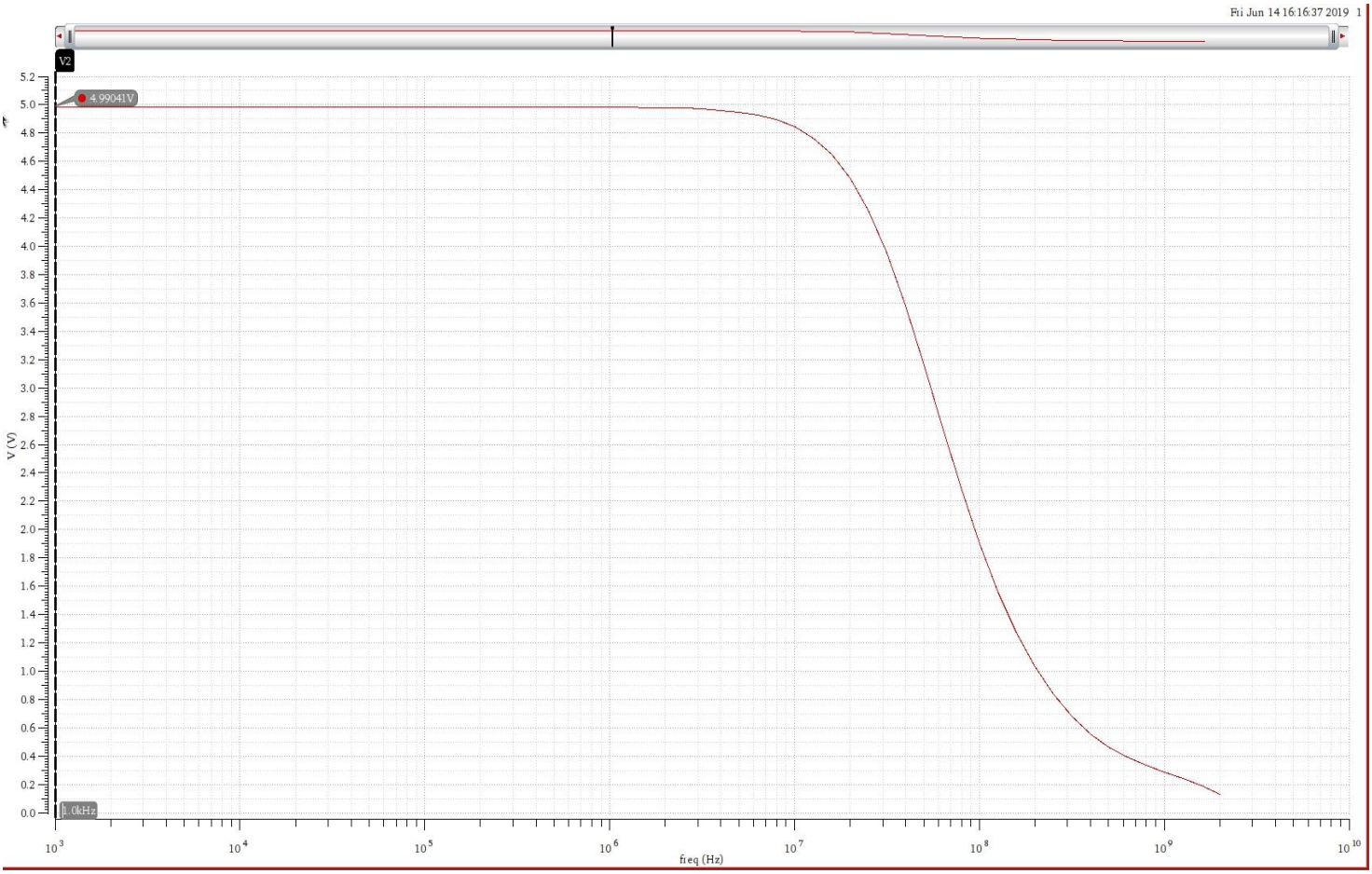
Phase Margin = -119 – (-180) = 61 deg



CLOSE LOOP GAIN

We were supposed to get the close loop gain as 5db. We got that specification accurately.

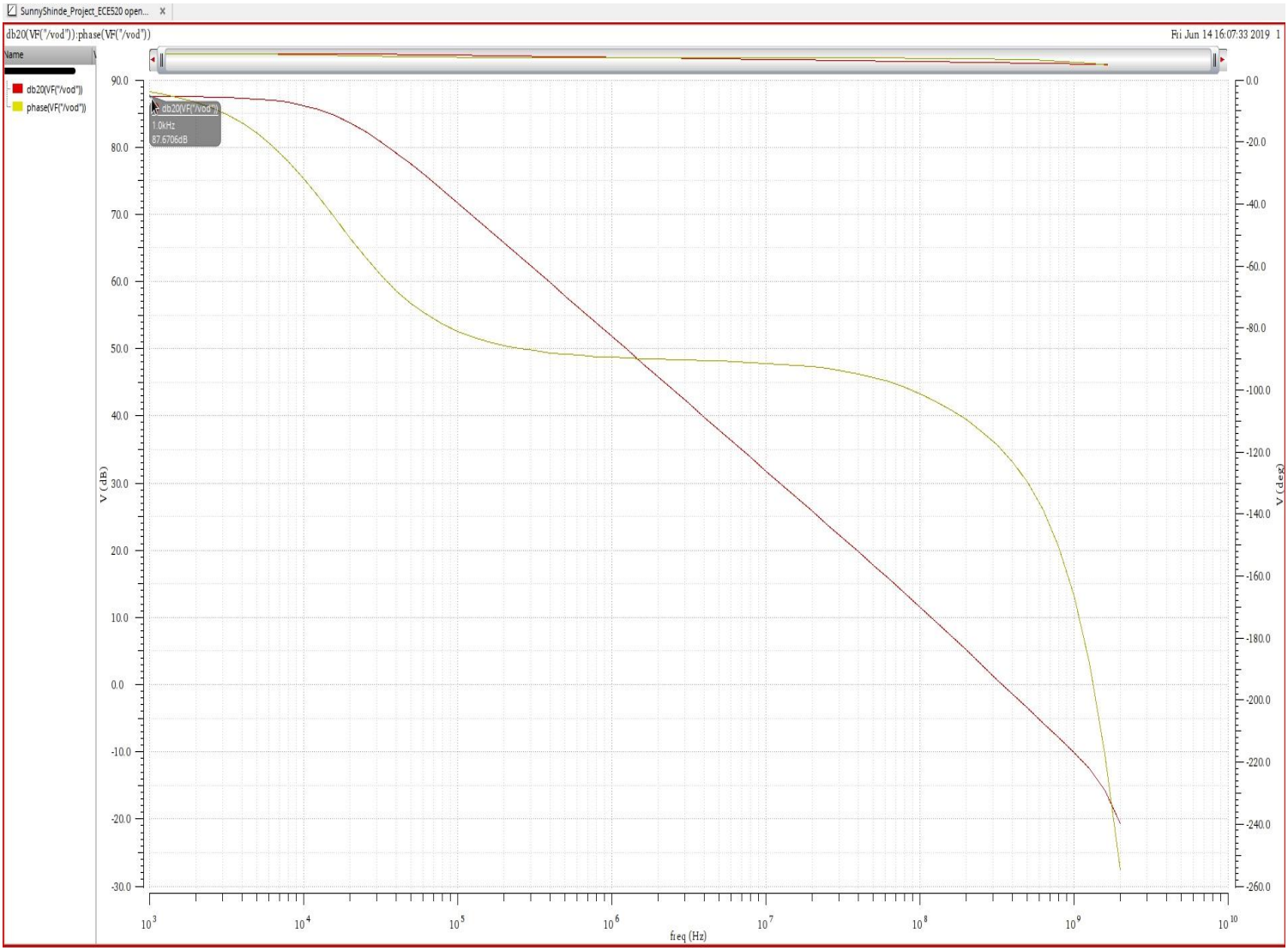
Close loop gain = 4.99 db



According to our calculations we wanted the open loop gain to be of 100db, but due to some trades offs we had to decrease our open loop gain to around 87db. When we were trying to implement the open loop gain of 100db, we found out that our settling time was too high. Settling time to equal to 90ns. When we tried to bring down the open loop gain to 87db our settling time reduced to 68ns. We cannot decrease the open loop gain further because it will be way too far from the requirement. So, we made a tradeoff of settling time. We got open loop gain around 87db and phase margin as 61 degrees. According to calculations we needed bandwidth as 356 MHz and practically we got our bandwidth as 350 MHz.

OPEN LOOP GAIN

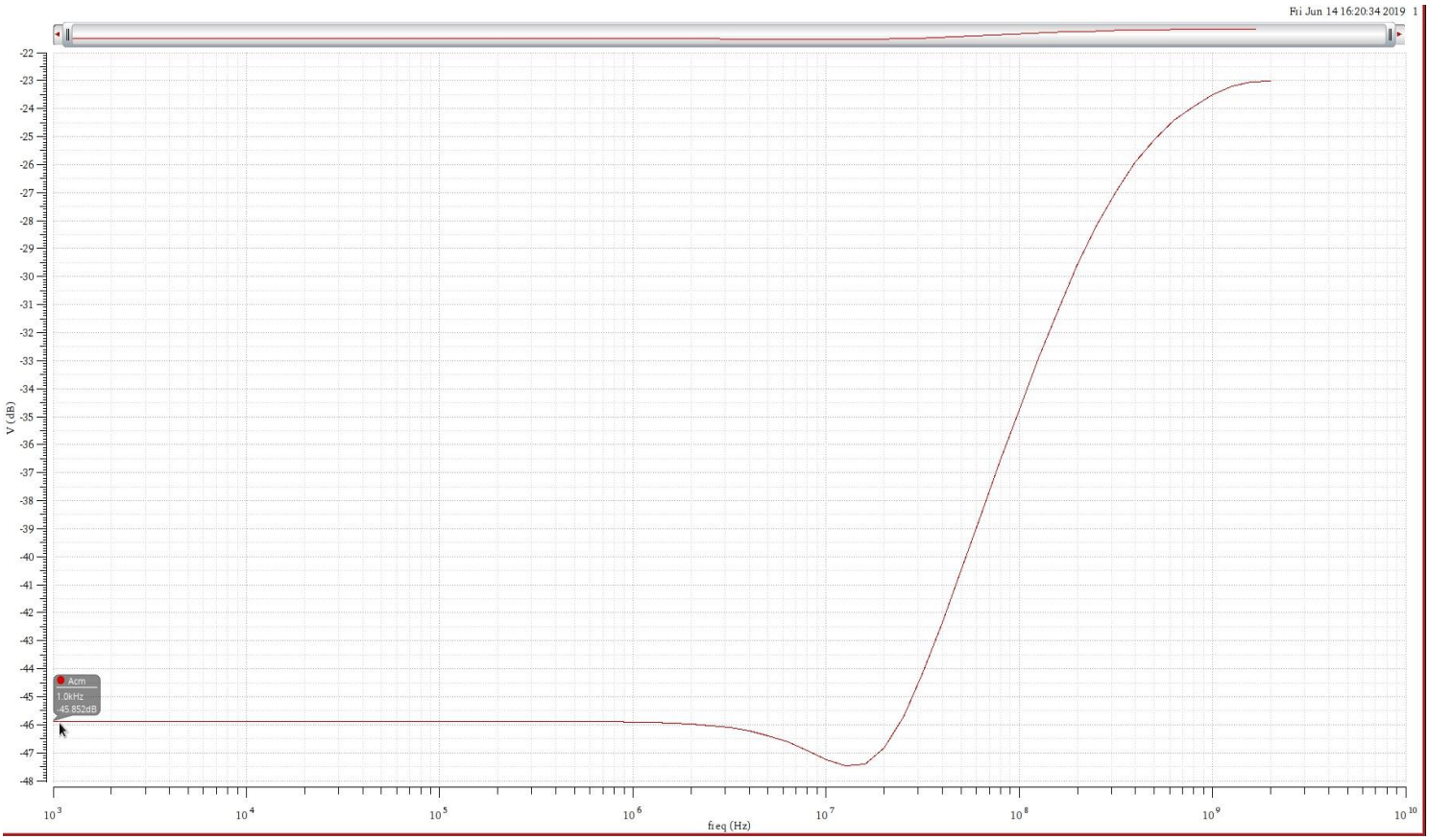
Open loop gain = 87.67 db



COMMON-MODE TO DIFFERENTIAL-MODE REJECTION RATIO

As per our design we got CMRR as 46db.

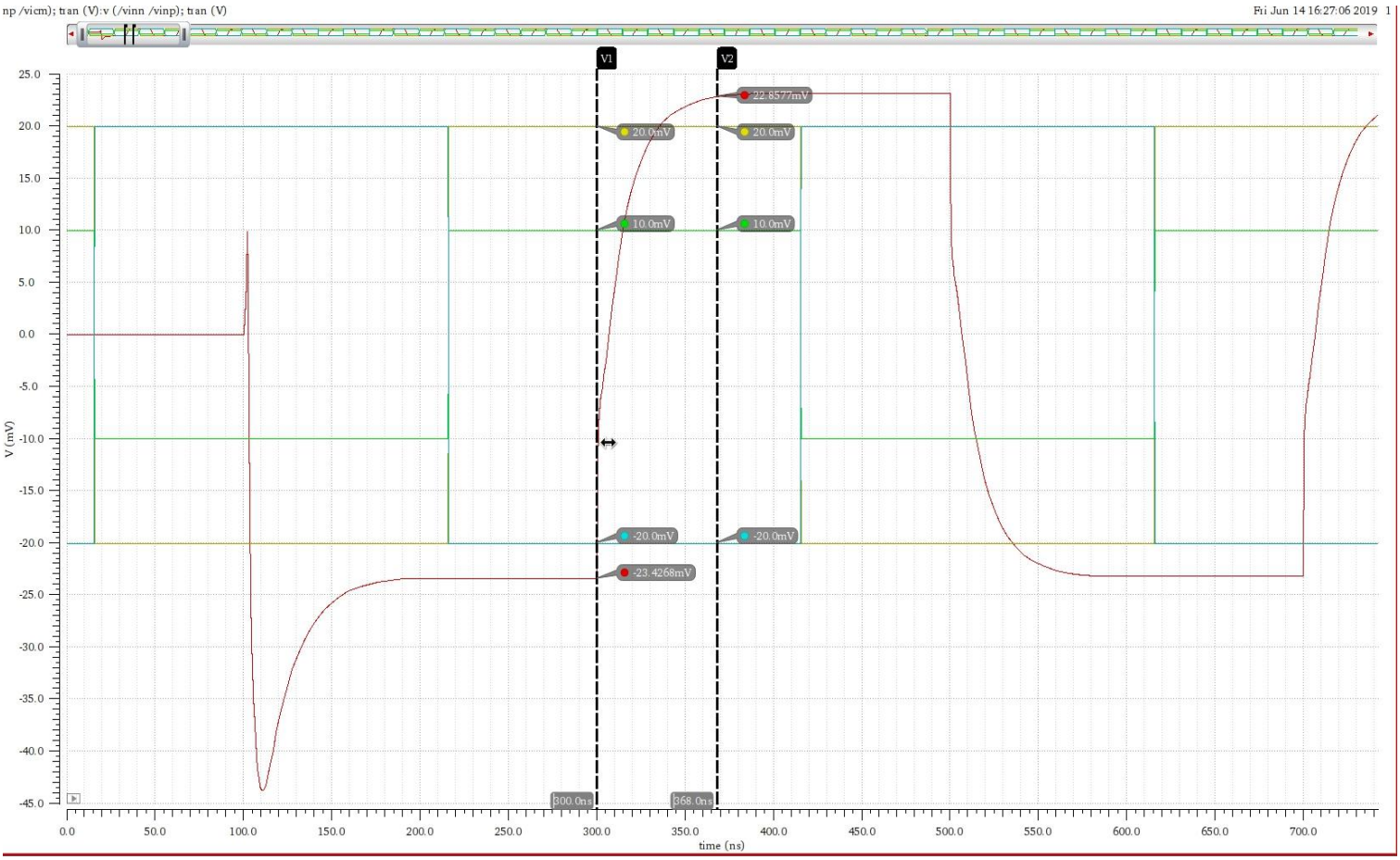
CMRR = -46 db



SETTLING TIME

As already mentioned we got high settling time as compared to what we wanted. We got our settling time as 68ns. I think this is because of high gain.

Settling time = 368ns – 300ns = 68ns



HARMONIC DISTORTION

HD2 will be zero and HD3 for our design came out to be 26db.

Harmonic distortion = -30db – (-4db) = 26db