Clock Application

Description:

The design implements a clock similar to smartphone clock applications.

The design implements four modes; a select mode, a countdown timer mode, a digital clock mode, and a stopwatch mode.
The design utilizes switches and buttons to operate as detailed below.

Design inputs and functions:

*switch 9 and 8 determine the state of the applications

Switch 9 Switch 8	Mode
00	Select time
01	Countdown
10	Clock
11	Stopwatch

- Select time mode: Switches 5 to 0 are used to enter numbers. Switch 7 locks in current time for the clock mode (high lock the time in). Switch 6 locks in the current time for the countdown mode(high lock the time in). Key0 selects a number, Key1 resets the selecting process.
-Countdown mode: Key0 pauses the countdown. Key1 resets the countdown to the time selected in select mode.
-Clock mode: Key0 pauses the countdown. Key1 resets the countdown to the time selected in select mode.
-Stopwatch: Switch 5 pauses and plays the stopwatch (low is pause, high is play). Switches 4 to 0 are used to display the time differences between each lap (the first recorded lap is represented by 5'd1. There is no lap record represented by 5'd0). Key0 is used to record a lap time. Key1 is used to reset the stopwatch (this deletes all recorded lap times).

Resources used:

http://www.myhdl.org/docs/examples/flipflops.html
https://www.youtube.com/watch?v=voi0oZI5Tug&ab_channel=LEPROFESSEUR
https://www.fpgatutorial.com/verilog-operators/
https://www.javatpoint.com/verilog-arrays#:~:text=Verilog%20arrays%20are%20used%20to%20group%20elements%20into,as%20nets%2C%20regs%2C%20and%20other%20Verilog%20variable%20types.
https://www.intel.com/content/www/us/en/programmable/support/support-resources/design-examples/design-software/verilog/ver_statem.html#:~:text=Verilog%20HDL%3A%20Synchronous%20State%20Machine%20This%20is%20a,state%20machine%20and%20the%20conditions%20that%20control%20them.

Video link: https://m.youtube.com/watch?feature=youtu.be&v=baOsriNa2PY