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Assignment 2 CS 3339 – Spring 2019  
Due: Friday, 2/15/19 @ 11:55pm  
40 points (late until noon 2/16 -10 points)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of Ax\_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, I encourage you to work in groups and discuss the problems with your classmates.

Fill in the blank – 1 point each for each blank.

- 1) Every Texas State student has access to an enterprise instance of github as described here:  
<https://cs.txstate.edu/resources/labs/accounts/> The server is https://git.txstate.edu
- 2) In digital computers transistors are used as electronic Switches. Before the invention of transistors and integrated circuits other devices used include electromechanical relays and vacuum tubes.
- 3) For your summer internship you have been tasked to improve the performance of an existing program. You realize that there is a section of code for which a newer math library that is twice as fast is available. You work diligently to incorporate the new library and are planning to wow your bosses. After spending days adapting the code for the new library the program only performs slightly faster. Turns out that the math portion was a small fraction of the original execution time. You have run straight into Amdahl's Law!
- 4) Even though they are available in MIPS assembly, there is no *mov* (move from one register to another) or *blt* (branch less than) operation implemented in "bare metal". For this reason they are known as Pseudo instruction.
- 5) Write the proper prefix for the following e.g  $1 \times 10^{-3}$  seconds = 1 millisecond  
 $1 \times 10^{-9}$  seconds = 1 Nano second       $1 \times 10^{-12}$  seconds = 1 Pico second  
A clock cycle time of  $500 \times 10^{-12}$  seconds corresponds to a clock frequency of 2.0 G Hz  
 $\begin{matrix} 500 \text{ Pico} \\ 5 \text{ Nano} \end{matrix} \quad 2.0 \text{ GHz} \rightarrow \frac{1}{2 \times 10^{-9}} = \frac{1}{2} \times 10^9 \rightarrow 0.5 \times 10^9$
- 6) "SPEC is the Standard Performance Evaluation Corporation, a non-profit organization founded in 1988 to establish standardized performance benchmarks that are objective, meaningful, clearly defined, and readily available. SPEC members include hardware and software vendors, universities, and researchers." "SPEC CPU2017 has 43 benchmarks, organized into 4 suites". The Wide-scale ocean modeling (climate level) SPECspeed 2017 Floating Point benchmark is 628. Pop2-S. [Reference www.spec.org]



7) [4 points] What is the primary advantage of the RISC architecture over the CISC architecture?

RISC has far fewer instructions versus CISC, it's also faster because of the fewer instructions.

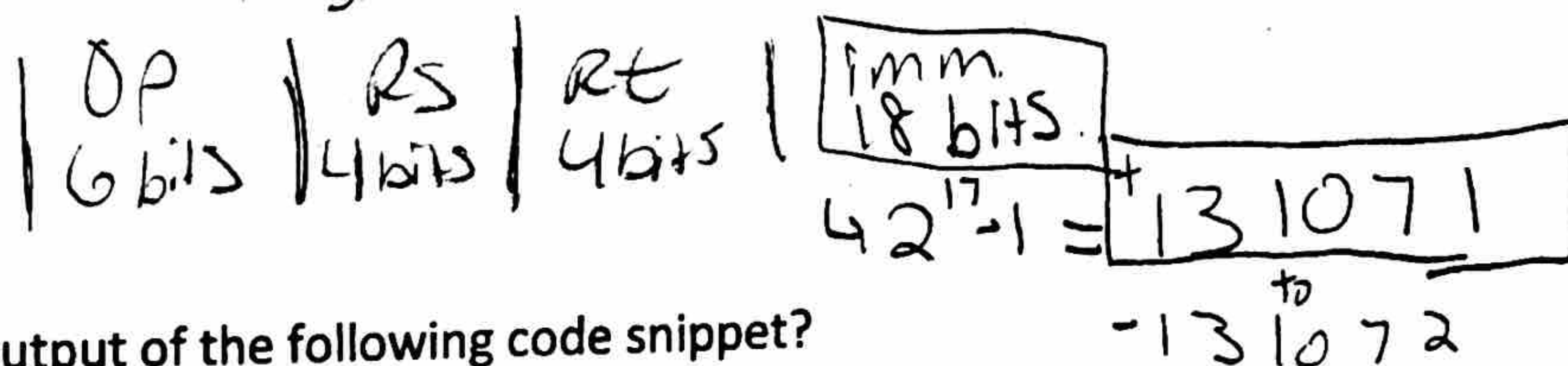
What is the primary advantage that CISC continues to have over RISC?

The flexibility of the code, CISC requires more code, which can quickly be edited/changed without affecting the entire system.

8) [4 points] If you reduced the number of registers from 32 to 16 in the MIPS processor what would be the new maximum signed value you could use as an immediate? Express your number in decimal and explain how you determined your answer. \*assumed bit length is not changed

32 registers . 16 registers

$$2^5 = 32 \quad 2^4 = 16$$



9) [4 points] What will be the output of the following code snippet?

```
uint32_t input = 0xfffc0af;
uint32_t u_field;
int32_t s_field;
u_field = (input >> 4) & 0xff;
cout << hex << setw(8) << u_field << " hex is decimal " << dec << u_field << endl;
s_field = ((signed)input >> 16);
cout << hex << setw(8) << s_field << " hex is decimal " << dec << s_field << endl;
```

11111111 1111 1100 1110 0000 1010 1111  
0 f f f c e 0 a  
0000 1111 1111 1111 1100 1110 0000 1010

$fffc0af \gg 16$   
ffff fffc S field.  
ffff fffc = 0000004

Output  
0000000c hex is decimal 10  
ffff fffc hex is decimal -4

10) [4 points] For project 2 you are provided with a C++ class file ALU.cpp/.h which uses the enum function. Look at the source code and list the possible values that you can use for ALU\_OP.

enum ALU\_OP { Add, And, SHF\_L, SHF\_R, CMP\_Lt, MUL, DIV };  
Value = Add / 0, And / 1, SHF\_L / 2, SHF\_R / 3, CMP\_Lt / 4, MUL / 5, DIV / 6

You don't need it to answer this question but if you want to learn a bit more about the enum function here is a short article <https://docs.microsoft.com/en-us/cpp/c-language/c-enumeration-declarations>

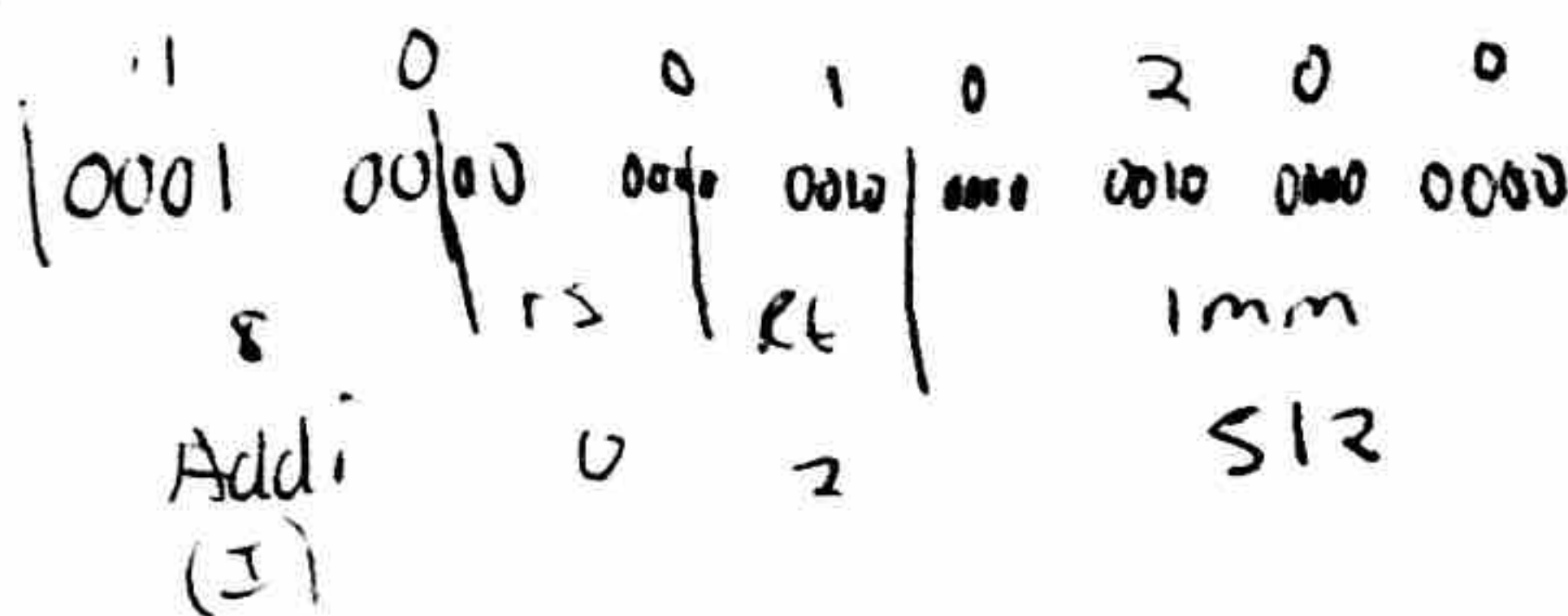
\* Since the instructions aren't specified by default they go from 0 to n.

\* Named ints



- 11) [4 points] A MIPS binary has the following hexadecimal address and instruction data values. Write the assembly code for this instruction. Show your steps and put the answer in the same format as Project 1.

address data  
0x10010200: 0x0085c023

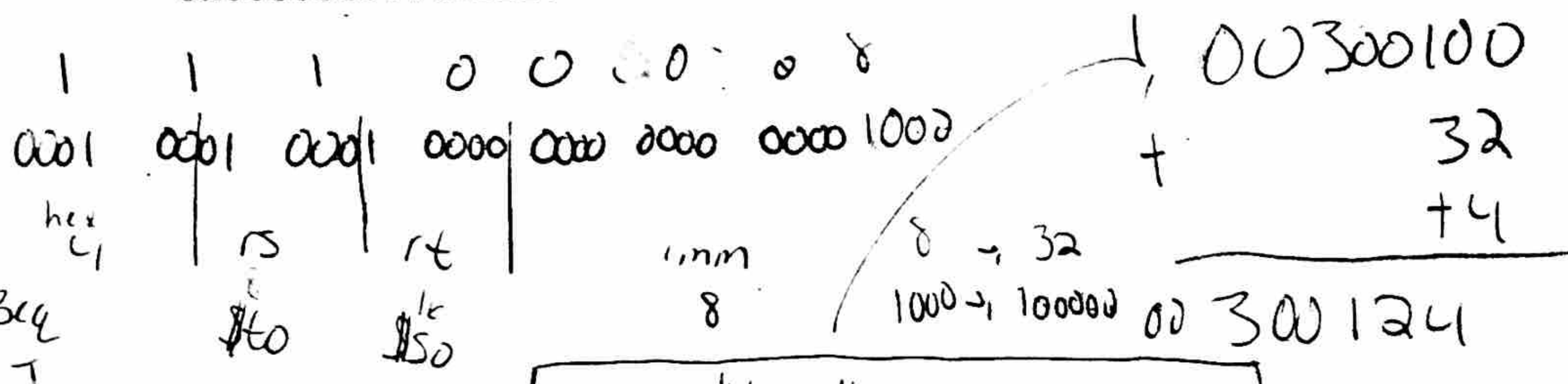


~~Addi \$v0, \$zero, 12~~

Subu \$t8, \$a0, \$a1

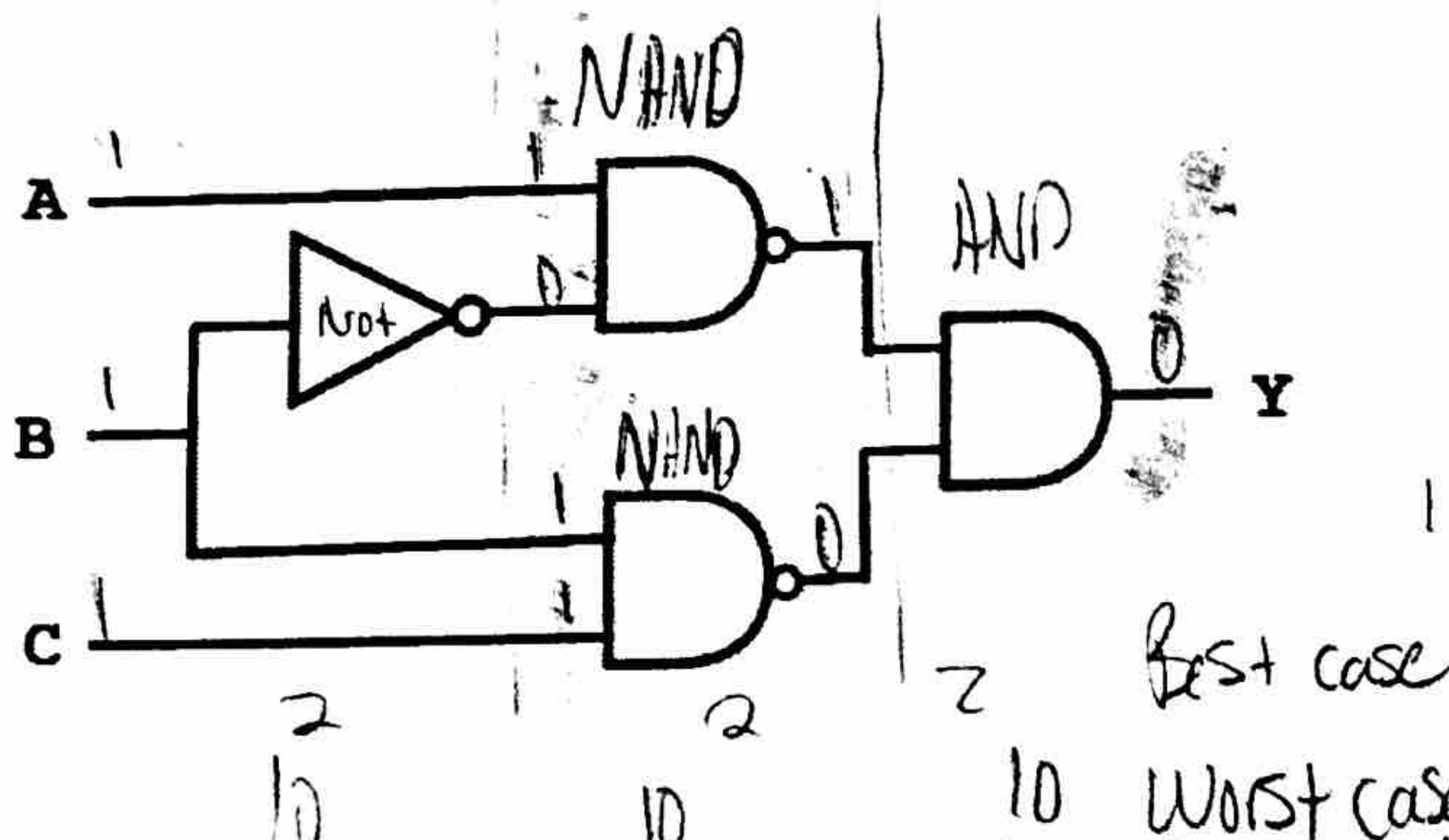
- 12) [4 points] Repeat for this addr:instr pair

0x00300100: 0x11100008



beq \$t0, \$s0, 00300124

- 13) [6 points] Complete the truth table given the combinatorial logic circuit below. Use 0 to represent 0V (FALSE) and 1 to represent 3.3V (TRUE) and put the inputs in binary counting order from 000 to 111 binary.



	A	B	C	Y
000	0	0	0	1
001	0	0	1	1
010	0	1	0	1
011	0	1	1	0
100	1	0	0	0
101	1	0	1	0
110	1	1	0	1
111	1	1	1	0

\* Only 8 instances in truth table, not ten

If the minimum gate delay is 2 ns and the maximum gate delay is 10 ns.

How long would you have to wait after the inputs change to insure all outputs are valid? 30 ns

How long could you wait to sample the original output value after the inputs change? 6 ns

there are 3 levels of switches  $3 \times 10 = 30$   
this is the time to view/sample outputs, not guaranteed to be correct.  $2 \times 3 = 6$  ns