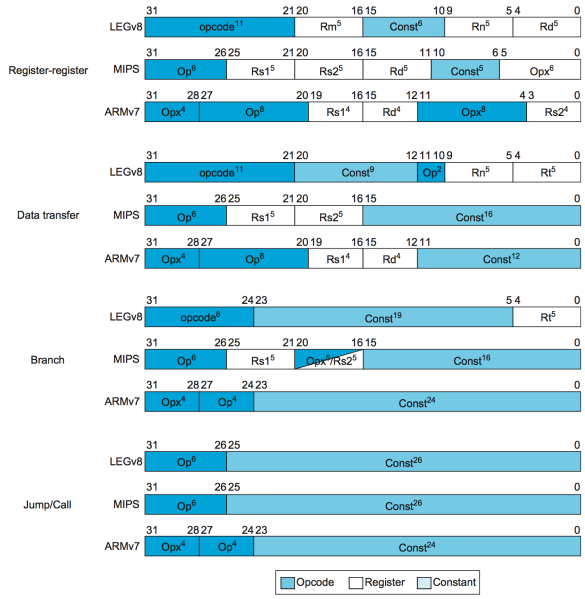
2.17 Real stuff: MIPS instructions

This section has been set as optional by your instructor.

The instruction set closest to ARMv8 comes from another company. MIPS and ARMv8 share the same design philosophy, despite MIPS being 25 years more senior than ARMv8. The good news is that if you know ARMv8, it will be very easy to pick up MIPS. To show their similarity, the figure below compares instruction formats for ARMv8 and MIPS, as well as ARMv7.

Figure 2.17.1: Instruction formats of LEGv8, MIPS, and ARMv7 (COD Figure 2.32).

The differences result in part from whether the architecture has 16 registers (ARMv7) or 32 registers (ARMv8 and MIPS).



The MIPS ISA has both 32-bit address and 64-bit address versions, sensibly called MIPS-32 and MIPS-64. These instruction sets are virtually identical except for the larger address size needing 64-bit registers instead of 32-bit registers. Here are the common features between ARMv8 and MIPS:

- All instructions are 32 bits wide for both architectures.
- Both have 32 general-purpose registers, with one register being hardwired to 0.
- The only way to access memory is via load and store instructions on both architectures.
- Unlike some architectures, there are no instructions that can load or store many registers in MIPS or ARMv8.
- Both have instructions that branch if a register is equal to zero and branch if a register is not equal to zero.
- Both have 32 floating-point registers, as we shall see in COD Chapter 3 (Arithmetic for Computers).
- Both sets of addressing modes work for all word sizes.

One of the main differences between ARMv8 and MIPS is for conditional branches other than equal or not equal. ARMv8 and many other architectures use condition codes. MIPS instead relies on a comparison instruction that sets a register to 0 or 1 depending on whether the comparison is true. Programmers then follow that comparison instruction with a branch on equal to or not equal to zero depending on the desired outcome of the comparison. Keeping with its minimalist philosophy, MIPS only performs less than comparisons, leaving it up to the programmer to switch order of operands or to switch the condition being tested by the branch to get all the desired outcomes. MIPS has both signed and unsigned versions of the set on less than instructions: `SLT` and `SLTU`.

When we look beyond the core instructions that are most commonly used, the other main difference is that the full ARMv8 is a much larger instruction set than the complete MIPS instruction set, as we shall see in COD Section 2.19 (Real stuff: The rest of the ARMv8 instruction set). That size difference means many more instruction formats, many more addressing modes, and many more operations.

PARTICIPATION ACTIVITY 2.17.1: MIPS vs. ARMv8.

1) ARMv8 and MIPS both have 64-bit instructions.
   - True
   - False

2) MIPS uses condition codes for conditional branching.
   - True
   - False

3) ARMv8 and MIPS both have a dedicated register for the value 0.
   - True
   -

False

4) ARMv8 and MIPS have the same number of instructions.

- ○ True
- ○ False

Provide feedback on this section