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Assignment 1 CS 3339 – Spring 2019

Due: Friday, 2/1/19 @ 11:55pm

40 points (late until noon 2/2 -10 points)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of Ax_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, I encourage you to work in groups and discuss the problems with your classmates.

Questions are 4pts each unless otherwise noted – you must show work to support your answers.

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1) Circle RISC or CISC for each of the statements below.

RISC / (CISC) Came first. i.e. was the first technique used for Instruction Set Architectures.
(RISC) / CISC Is easier to implement in hardware.
RISC / (CISC) Would have fewer machine instructions and higher code density.
RISC / (CISC) Is the type of ISA most likely being run on a server in a datacenter.

2) You fell into the hot tub time machine and find yourself back in 1986. Current chips have 140,000 transistors and your boss wants to know how many transistors are likely to be on a chip 10 years from now. Grab a Jolt Cola, pop Peter Gabriel's new 'So' album in the Sony Discman and get calculating. Your answer is? [Assume Gordon Moore said "... every 2 years"]

1986 — 10 years — 1996

140,000 — ? — 4,480,000

$2^5 = 32x \rightarrow 32 \cdot 140.000 =$ 4,480,000

Check $[((((140,000 \cdot 2) \cdot 2) \cdot 2) \cdot 2) \cdot 2] = 4,480,000$

3) Welcome back to 2019. According to https://hothardware.com/reviews/amd-ryzen-threadripper-2950x-and-2990wx-review?page=8 the "beastly" AMD Threadripper 2990WX has 19.2 billion transistors. If you built a giant size model of the die with the transistors arranged in an n x n grid and each transistor was 145mm x 68mm (about the size of the Google Pixel 3 phone) what would be the model's width & length in meters?

mm to m
145mm .145
68mm .068

CPU
x
x 19.2B

$x^2 = 19.2B$

$x = \sqrt{19.2 * 10^9} \approx 138564$

$145mm = .145 * 138564 \approx 20011.78 \rightarrow$ 20012 Meters

$68mm = .068 * 138564 \approx 9422.35 \rightarrow$ 9422 meters

4) Transistor scaling has continued to allow more transistors per CPU die with each new chip generation. Starting in 2004, the additional transistors have been primarily used to:

a) add more pipeline stages
b) increase the precision of floating point calculations
c) add non-volatile (flash) storage
(d) put multiple CPU cores on each chip
e) spread out the heat generated

5) Why did processor clock speeds, which had increased for decades, finally stop increasing around year 2004?

a) Environmental regulations required yearly power reductions
b) The higher frequencies interfered with cellular and WiFi radios
c) Processors were already memory bound so higher frequencies didn't improve performance
(d) The inability to lower voltages further causes the processors to consume too much power
e) Silicon atoms have a fundamental limitation oscillating above 4 GHz

6) The Raspberry Pi 3 B+ runs at a max clock frequency of 1.4 GHz. Calculate the cycle time in picoseconds. For fun reference https://www.raspberrypi.org/products/raspberry-pi-3-model-b-plus/

Cycle time = frequency^{-1} → $(1.4)^{-1} = \frac{1}{1.4} \times 10^{-9} \approx .7142 \times 10^{-9}$

1×10^{9} Ghz = 1×10^{-12} pico

714.2×10^{-12}

714.2 Pico Seconds

7) Your code executes a 4 million instruction sequence with a CPI of 2, followed by a 6 million instruction sequence with a CPI of 4, followed another 4 million instruction sequence with a CPI of 2. What is the CPI of the full code? Express answer to 2 decimal places.

$$CPI = \frac{\text{Cycles}}{\text{Instruct.}} = \frac{[2(4*10^6)] + [4(6\times10^6)] + [2(4*10^6)]}{(4*10^6) + (6*10^6) + [4\times10^6]} = \frac{40*10^6}{14*10^6} \approx 2.86$$

*Cycles = CPI * Instruct

8) Calculate the average CPI of a processor where 35% of the instructions take 1 cycle to execute, 20% take 2 cycles, 20% take 3 cycles, 15% take 4 cycles, and 10% take 5 cycles. Express answer to 2 decimal places.

$$CPI_{AVG} = \frac{[(1*35) + (2*20) + (3*20) + (4*15) + (5*10)]}{100} \approx \frac{35+40+60+60+50}{100}$$

$35+20+20+15+10 = 100\%$

$\approx \frac{245}{100} = 2.45$

9) Processor A has a clock speed of 1.5 GHz and 4 classes of instructions, with CPIs of 1, 2, 3, and 4 respectively. Processor B has a clock speed of 2.0 GHz and the same 4 classes of instructions, with CPIs of 2, 3, 4, and 5. If the number of instructions executed in a program is divided equally among the 4 classes of instructions, which processor is faster and by how much? Express your answer as ratio e.g. 2.1x faster. *Hint: choose a number of instructions so you can use the classic performance equation on L1 slide 24*

CPU Time = $\frac{\text{Cycles}}{\text{Rate}}$ → $\frac{\text{CPI} \cdot \text{Ins}}{\text{Rate}}$

A

Ghz	CPI	
1.5	1 * 1	1
1.5	2 * 1	3
1.5	3 * 1	3
1.5	4 * 1	4
		10

$\frac{10}{1.5} = 6.666$

B

Ghz	CPI	
2.0	2 * 1	2
2.0	3 * 1	3
2.0	4 * 1	4
2.0	5 * 1	5
		14

$\frac{14}{2} = 7$

$\frac{B}{A}$ $\frac{7}{6.667} \approx 1.05$

B is 1.05 x faster

10) Dynamic Voltage and Frequency Scaling (DVFS) is a technique widely used to lower power, especially in large datacenters. In order to conserve electricity both the frequency and voltage of the processor are reduced. If a processor using 200W of power running at 2V and 4 GHz is reduced to 1.5V at 2GHz how much power in Watts will be saved? [Note: Assume 100% of power is dynamic – ignore leakage power]
Hint – see L1 slide 21, the capacitance if a function of the chip and will not change with voltage or freq.

$\frac{1}{2}CV^2f$

200 Watts = $\frac{1}{2}C(2)^2(4)$

$= \frac{1}{2}C(16)$

$200 = 8C$

$25 = C$

$X = \frac{1}{2}(25)(1.5)^2(2)$

$= \frac{1}{2}(25)(2.25)$

$= \frac{1}{2}(112.5)$

≈ 56.25

$200 - 56.25 =$ 143.75 Watts saved