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Assignment 6 CS 3339 – Spring 2018

Due: Friday, 4/26/19 @ 11:55pm

40 points (late until noon 4/27 -10 points)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of Ax_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, you are encouraged to work in groups and discuss the problems with your classmates.

1) [2 points] Caches read data in "chunks" called blocks that usually contain multiple words. Virtual memory systems read data in (larger) "chunks" called Page's.

2) [4 points] A processor executes a *lw* instruction to memory subsystem containing a writeback cache which causes a write cycle to main memory. Explain the two conditions that must occur for this to happen.

dirty

d	m	v	tag

1) tags must match

2) must exist in Memory

3) [6 points] List and briefly describe how the three techniques listed in the textbook/lecture can be used to improve the performance of matrix multiplication operations on large double precision matrices (DGEMM).

Virtual Memory - Sharing main memory as a cache for CPU & OS.

Blocking - max accesses to data before replacement.

Blocking + Unroll + AVX - Combine Blocking and Subword Parrallesim.

4) [2 points] What happens when a page fault occurs? (circle best answer)

a Two reads to memory occur, one to get the page table entry and another to read physical memory. ×

b The system shuts down; page faults are unrecoverable errors. ×

(c) An exception occurs passing control to a handler which loads the requested data from disk into memory.

d The processor will retry the access using a different memory location. ×

e None of the above are true

5) [4 points] What does TLB stand for? Translation look-aside Buffer

What information does it contain? Page table entry (PTE)

How does it improve performance in virtual memory enabled systems?

Reduce the amount of time and accessed in Virtual Memory and Physical Memory

6) [4 points] In a system with 42-bit virtual addresses and 64GB of physical memory what is the size of the virtual address space? How many physical address bits will be needed?

	size	bits
Vm		42 bits
Phy	64gb	

Vm 2^{42} bits → 512GB

Phy 64GB → 2^{36} bits

7) [4 points] A serial program executes in 90 seconds. You modify the program which now runs for 5 seconds serially, then runs on 8 processors in parallel, and finally 5 more seconds serially. Assuming all 8 processors can execute efficiently how long will the new version take to run?

5 seconds + 8 core Parrallel ↳ T_{serial} / cores + 5 seconds → $5 + \left(\frac{90}{8}\right) + 5 \approx 21.25$ = 21 seconds

What is the speedup?

$\frac{T_{serial}}{T_{Parrallel}} = \frac{90}{21} \approx 4.28$ (4x)

What is the efficiency?

$\frac{T_{Serial}}{Core * Parrallel}$ $\frac{90}{8*21} \approx .535$

8) [4 points] Given a system with 32-bit virtual addresses and 4KiB page tables find the physical address. Note that VPN 0 corresponds to the bottom row of the page table.

$2^{32} / 2^{12} \rightarrow 2^{20}$

Virtual address 0x000038F7

0000 0000 0000 0000 0011 1000 1111 0111

translates to 3 1

physical address 0x0 6FE58F7

V	Physical Page Number
1	0x3F34
	⋮
1	0x3FFF
1	0x6FE5
1	0x23FF
1	0x23FE
0	

9) [3 points] Fill in the name of the three methods discussed in class that are used to create parallel programs which best matches the description.

(MPI) Message Passing Interface — Used for computation across very scalable independent nodes. Communications between nodes is relatively slow.

OpenMP — An API whose goal is to simplify parallel programming by enabling such things as executing for loops in parallel with only a few lines of code.

Pthreads — An API for POSIX systems that allows you to more tightly control the execution of multiple threads. Threads are less resource intensive than full processes since they act on shared memory can communicate with each other very quickly.

10) [7 points] Read the article https://www.ibm.com/developerworks/library/iot-lp101-best-hardware-devices-iot-project/index.html and answer the following questions:

IoT devices typically include one or more sensors often connected to the microcontroller through digital or analog GPIO pins. What does GPIO stand for? General Purpose Input/Output

An analog temperature sensor with 10 bits of resolution provides 1024 possible values in total.

The NodeMCU and and AdaFruit Feather Huzzah are boards based on Espressif Systems

Per the article the typical cost of a Raspberry Pi 3 is $35

Also per the article the Raspberry Pi Zero W is a small and very low-cost SBC device (around $10), with ample processing power and memory (1 GHz ARM6 processor and 512 MB RAM)

Circle one: Security ((is) / is not) a critical element within IoT and must be considered at all stages of design and development.