Ho Huy Hung

Becoming a hardware design engineer.

INFORMATION

Birth : **/**/199* (DD/MM/YYYY)
Phone : (+84)-***-***-***
Email : heroh396@gmail.com

EXPERIENCE

Jun 2018 – Sep 2018
Hardware engineer at TSDV (Toshiba Software Development Vietnam)

Having experiences about front-end design (RTL design and verification) of a microprocessor.

Training about IC design tools: Design Compiler, ICC2, PrimeTime.

Sep 2018 – Oct 2018
Studying Japanese at AOTS Center, Japan

Learning about Japanese, the culture, working methodology continuously for 6 weeks.

Nov 2018 – Mar 2019
Trainee at TOSMEC (Toshiba Microelectronics Corporation) (Japan)

Intensive training on the flow of IC design, proficient use of tools of middle-rank and back-end designs.

EDUCATION

2014 - 2018
VNU University of Engineering and Technology (VNU-UET)

Major: Electronics and Telecommunications.

Knowledge of: Microprocessor, Digital Technology, Integrated Circuit Design, Embedded Design, advanced programming (C, SystemC, VHDL, Verilog), Data structures and algorithms, Digital signal processing.

Cumulative GPA: **3.**** / 4.0.

Awards: good student scholarship, 3rd prize in the Faculty-level Student Research Contest. (The academic year 2016-2017)

Attend many workshops, conferences on hardware, integrated circuit design.

AWARD & PUBLICATION

1st Runner-up Award in the 21st LSI 2018 Design Contest in Okinawa, Japan. (2018)

3rd prize in the Student Research Contest in University. (2017)

H. H. Ho et al. "Accurate and low complex cell histogram generation by bypass the gradient of pixel computation," in 2017 4th NAFOSTED Conference on Information and Computer Science, 2017, pp. 201–206.

RESEARCH

Mar 2016 – Jun 2018
Internship at VNU Key Laboratory for Smart Integrated Systems (SISLAB)

Experienced about working environment. (Linux, shell script, server mangagement, redmine, git, svn)

Participating in IC design projects:

- **May 2016 – Aug 2016**
IOT application in collecting sensors signal measurements use Arduino kit project.

- **Nov 2016 – Aug 2017**
Hardware implementation of Human detection by Histogram of Oriented Gradient (HOG) project.

- **Aug 2017 – Feb 2018**
Low-power optimization in NOC based on Multi-core Embedded System project.

- **Nov 2017 – Mar 2018**
Hardware implementation of Neural Network with Backpropagation Algorithm project.

SKILLS

FRONT-END DESIGN
● ● ● ● ● ● ○ ○

ENGLISH
● ● ● ● ● ○ ○

BACK-END DESIGN
● ● ● ○ ○ ○ ○

JAPANESE
● ● ● ○ ○ ○ ○