Huy-Hung Ho

Becoming a digital design engineer.

INFORMATION

Birth : **/**/1996 (DD/MM/YYYY)
Phone : (+84)-1642-792-***
Email : hhhung96@gmail.com

PUBLICATION & AWARD

H. H. Ho et al. "Accurate and low complex cell histogram generation by bypass the gradient of pixel computation," in 2017 4th **NAFOSTED Conference on Information and Computer Science**, 2017, pp. 201–206.

1st Runner-up Award in the 21st LSI 2018 Design Contest in Okinawa.

3rd prize in the Faculty-level Student Research Contest in University. (2017)

EDUCATION

2014 - 2018

VNU University of Engineering and Technology (VNU-UET)

The senior student in Faculty of Electronics and Telecommunications. Key objects: Digital Signal Processing, Data Structures & Algorithms, Advanced programming, Digital Design, Real-time Embedded System, Integrated Circuit Design...

Awards: good student scholarship, 3rd prize in the Faculty-level Student Research Contest. (The academic year 2016-2017)

RESEARCH

Mar 2016 - Present

Internship at VNU Key Laboratory for Smart Integrated Systems (SISLAB)

Experienced in working environment. (Linux, shell script, server working, redmine, git, svn)

Attended training course of Synopsys and practice using tools: VCS, Design Compiler, IC Compiler, UPF and Verification.

Reference

Associate Professor Xuan-Tu Tran

Email: ***@vnu.edu.vn

PROJECT

May 2016 – Aug 2016

IOT application in collecting sensors signal measurements use Arduino kit

Nov 2016 – Aug 2017

Hardware implementation of Human detection by Histogram of Oriented Gradient (HOG)

Learning HOG algorithm and simulating in Matlab, C++ (not OpenCV lib). Designing a basic hardware architecture and simulation using VHDL language.

Optimization of Cell Histogram Generation (CHG) module, simulation in Questasim and synthesis on Synopsys tools. (Use for Student research contest and NAFOSTED conference paper)

Nov 2017 – Mar 2018

Hardware implementation of Neural Network use Backpropagation Algorithm

Learning neural network algorithm and its optimizations. Software simulation uses Matlab. Designing a parameterized neural network architecture from reference architecture uses VHDL, synthesis on FPGA use Vivado tool.

Low area cost optimization by a Simplified sigmoid function and Stochastic Computing method. (Use for LSI 2018 Design Contest)

Aug 2017 – Feb 2018

Low-power optimization in NOC based on Multi-core Embedded System

Read, analyze and present articles on multi-core systems using Network-on-chip (NOC) and power gating technique for low-power optimization.

SKILLS

VHDL ●●●●●●○

C, C++, MATLAB ●●●●●○○

LINUX ●●●●●○○

ENGLISH ●●●●○○○