



# HUY-HUNG HO

My objective becomes a digital design engineer.



## INFORMATION

Sex : Male  
Birth: 12-09-1996



## CONTACT ME

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## MY WEBSITE

<https://voloh3.github.io>

## WORK EXPERIMENT

March 2016 – Present

### SISLAB MEMBER – DIGITAL DESIGN

SISLAB is VNU Key Laboratory of Smart Integrated System. I made an IOT application product using ARDUINO KIT (get sensor data and control via the internet).

November 2016 – August 2017

### HARDWARE IMPLEMENTATION - HUMAN DETECTION

This project from LSI Design Contest 2017: Human detection by HOG. I got the prize in the student research contest. A part of the project has used to write a paper.

July 2017 – Present

### SISLAB-TOSHIBA PROJECT – LOW POWER

I am a student member of this project. We have research about a low power approach for multi-core hardware.

## SKILLS

LINUX – SHELL



VHDL



C/C++



ENGLISH



## EDUCATION

2014 - 2018

### VNU University of Engineering and Technology (VNU-UET)

My major is Electronic and Telecommunication. Key objects: C/C++ programming, Digital Signal Processing, Digital Design, Embedded System...

GPA: **3.11** / 4.0. I got the prize in student research contest.

## INTERESTS

