HUY HUNG HO

My objective becomes a digital design engineer.

INFORMATION
Sex : Male
Birth: 12-09-1996

CONTACT
Call : +84-1642-792-422
Email: hhhung96@gmail.com

ADDRESS
201 E4, Xuan Thuy Street, Hanoi 100000
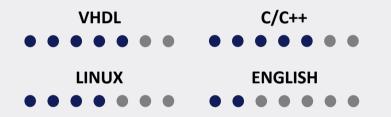Online: https://yoloh3.github.io

WORK EXPERIMENT

March 2016 – Present

Internship at VNU Key Laboratory of Smart Integrated Systems (SISLAB)

Researching about the low power for multi-core chip.

SKILLS

VHDL
● ● ● ● ● ● ○ ○

C/C++
● ● ● ● ● ○ ○

LINUX
● ● ● ● ● ○ ○ ○

ENGLISH
● ● ● ● ○ ○ ○ ○

EDUCATION

2014 - 2018

VNU University of Engineering and Technology (VNU-UET)

The senior student in Faculty of Electronics and Telecommunication. Key objects: Digital Signal Processing, C/C++ programming, Digital Design, Real-time Embedded System, Integrated Circuit Design...

Prizes: good student scholarship, 3rd prize in the Faculty-level Student Research Contest. (The academic year 2016-2017)

Cumulative GPA: **3.11** / 4.0

PROJECTS

May 2016 – August 2016

IOT application in collecting sensors signal measurements

Using Arduino KIT for (collect sensor data, monitor, feedback control) over the internet using the ThingSpeak server. (have finished products)

November 2016 – August 2017

Human detection by Histogram of Oriented Gradient

Objectives: performing a hardware design of the operation unit as a theme of "human detection by HOG".

- HOG software simulation in Matlab, C/C++ (not OpenCV).
- Designing a HOG hardware architecture and simulating a part in VHDL.
- My partner and I wrote a paper about improving HOG algorithm performance.

INTERESTS