

EXPERIMENT - 8

AIM:

To analyse the circuit and truth table of 4-bit SIPO (serial input parallel output) shift register by using IC 7474 (D flip flop).

THEORY:

Introduction

In Serial In Parallel Out (SIPO) shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 1 shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D1 of FF1). It is also seen that the inputs of all other flip-flops (except the first flip-flop FF1) are driven by the outputs of the preceding ones like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q1 to Qn).

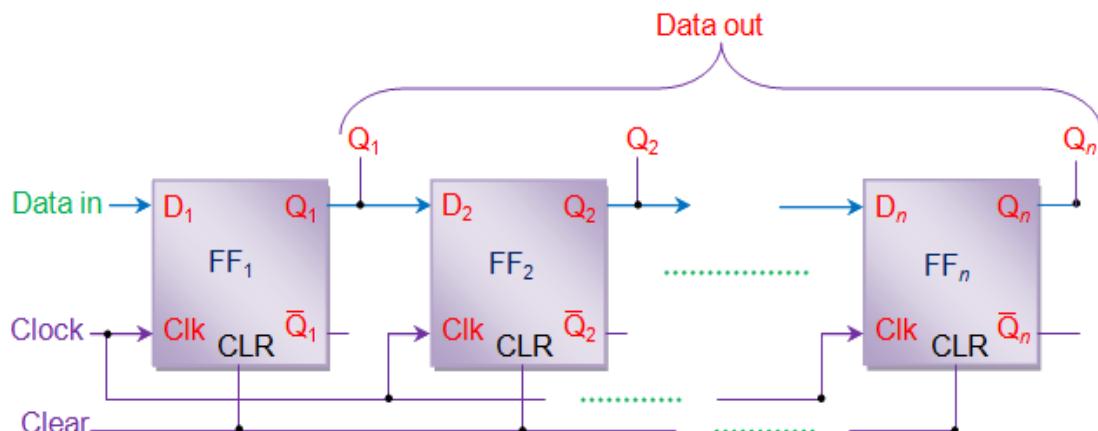


Figure 1 n-bit Serial-In Parallel-Out Right-Shift Shift Register

In general, the register contents are cleared by applying high on the clear pins of all the flip-flops at the initial stage. After this, the first bit, B1 of the input data word is fed at the D1 pin of FF1. This bit (B1) will enter into FF1, get stored and thereby appears at its output Q1 on the appearance of first leading edge of the clock. Further at the second clock pulse, the bit B1 right-shifts and gets stored into FF2 while appearing at its output pin Q2 while a new bit, B2 enters into FF1. Similarly at each clock pulse the data within the register moves towards right by a single bit while a new bit of the input word enters into the register. Meanwhile one can extract the bits stored within the register in parallel-fashion at the individual flip-flop outputs.

Analyzing on the same grounds, one can note that the n-bit input data word is obtained as an n-bit output data word from the shift register at the rising edge of the nth clock pulse. This

working of the shift-register can be summarized as in Table I and the corresponding waveforms are given by figure 2.

Table I Data Movement in Right-Shift SIPO Shift Register

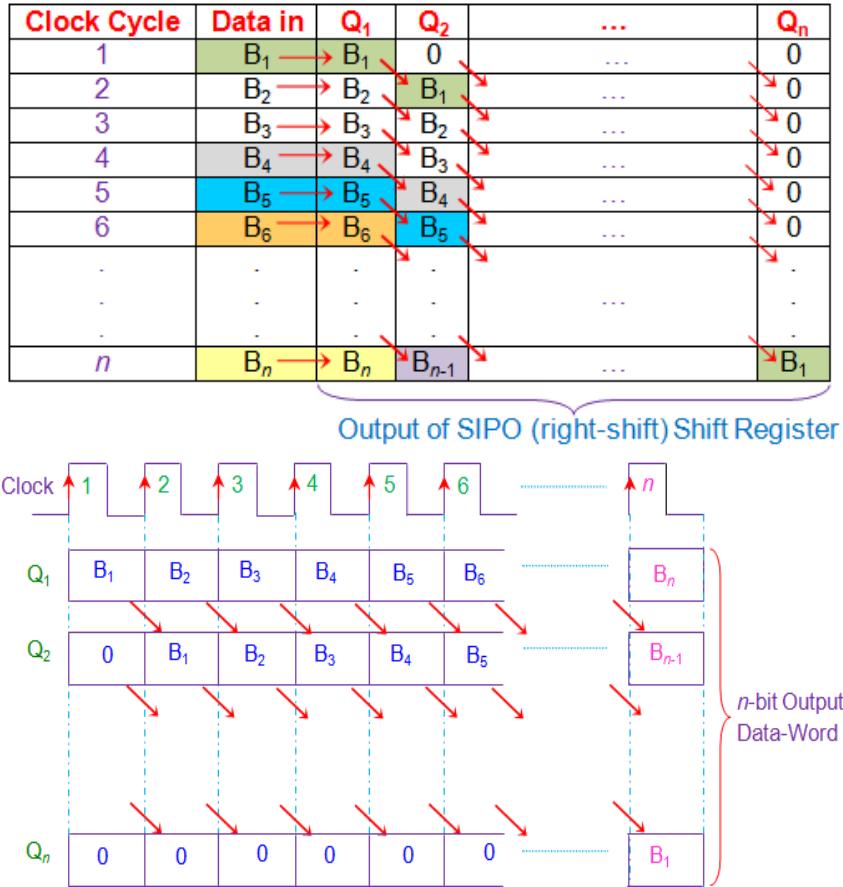


Figure 2 Output Waveform of n -bit Right-Shift SIPO Shift Register

In the right-shift SIPO shift-register, data bits shift from left to right for each clock pulse. However if the data bits are made to shift from right to left in the same design, one gets a left-shift SIPO shift-register as shown by figure 3. Nevertheless the basic working principle remains the same except the fact that now B_n down to B_1 is stored in Q_n down to Q_1 i.e. $Q_1 = B_1$, $Q_2 = B_2$... $Q_n = B_n$ at the nth clock pulse.

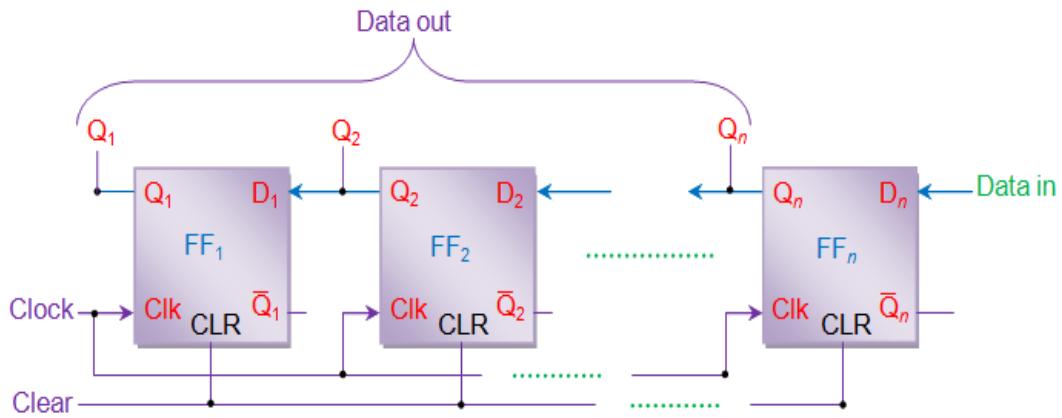


Figure 3 *n*-bit Serial-In Parallel-Out Left-Shift Shift Register

PRETEST:

Aim
Design and Verify the 4-Bit Serial In - Parallel Out Shift Registers.

Theory	<p>A register that can be used to provide data movements _____</p> <p><input type="radio"/> a: Parallel Register</p> <p><input type="radio"/> b: Simple Register</p> <p><input checked="" type="radio"/> c: Serial Register</p> <p><input checked="" type="radio"/> d: Shift Register</p>
Procedure	<p>A n-bit register has a group of _____ flip-flops and some logic gates.</p> <p><input checked="" type="radio"/> a: n</p> <p><input type="radio"/> b: p</p> <p><input type="radio"/> c: 10</p> <p><input type="radio"/> d: 01</p>
Posttest	<p>Shifting a register content to left by one position is equivalent to _____</p> <p><input type="radio"/> a: division by 2</p>
References	
Feedback	

Shifting a register content to left by one position is equivalent to _____

- a: division by 2
- b: addition by 2
- c: multiplication by 2
- d: subtraction by 2

To serially shift a nibble(4 bits) of data into a shift register, there must be _____

- a: 1 clock pulse
- b: 8 clock pulses
- c: 4 clock pulses
- d: 1 clock pulse for each 1 in the data

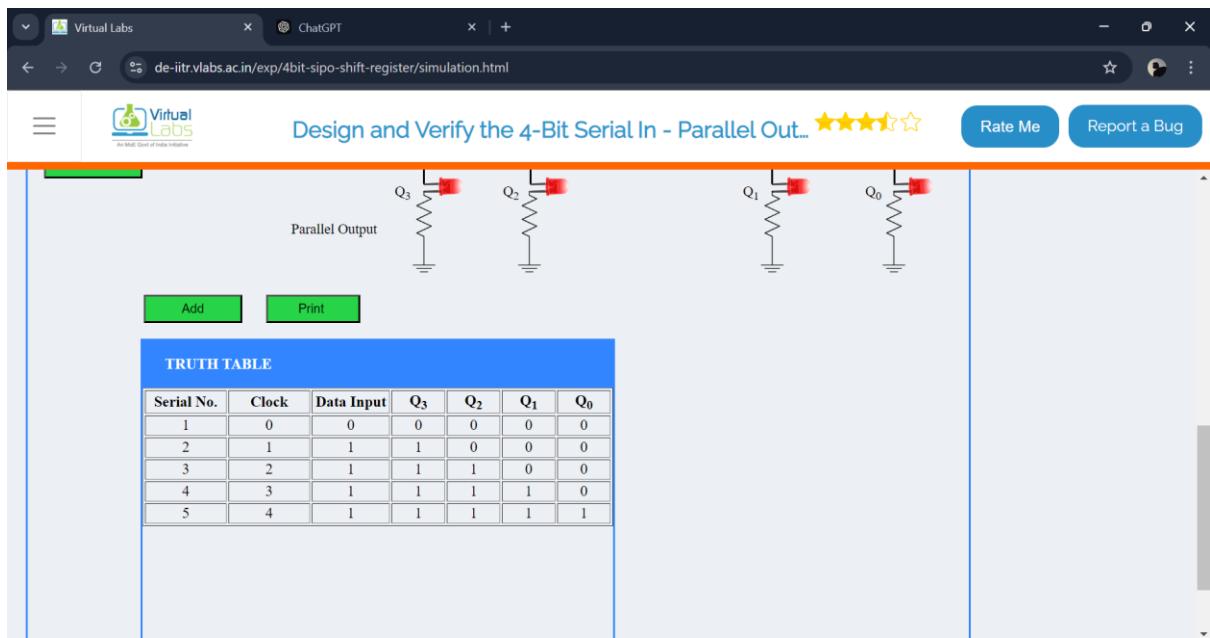
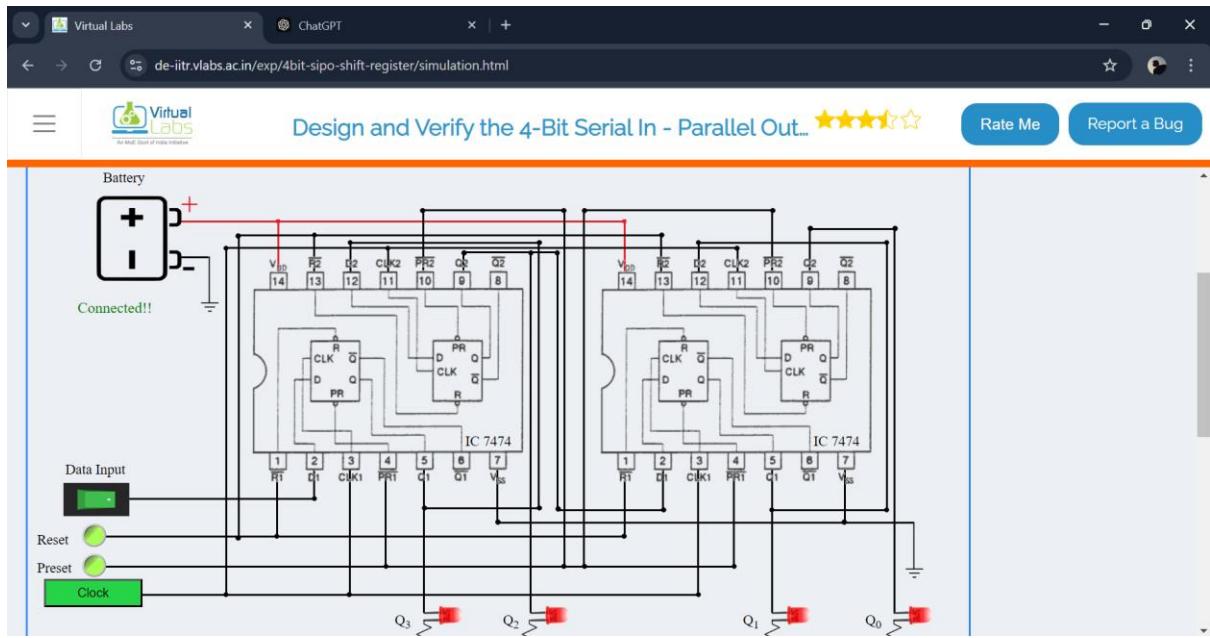
What is meant by parallel load of a shift register?

- a: Parallel shifting of data
- b: Each flip-flop is loaded with data one at a time
- c: All flip-flops are preset with data

PROCEDURE:

- Step-1) Connect the supply(+5V)  to the circuit.
- Step-2) Keep the Reset and Preset as active-high signals .
- Step-3) Apply the data at data input
- Step-4) Press clock pulse and observe this data at LED Q₃.
- Step-5) Then press "ADD" button to add data in the given truth table.
- Step-6) Apply the next data at data input.
- Step-7) Press clock pulse and observe that the data at LED Q₃ will shift to LED Q₂ and the new data applied will appear at Q₃.
- Step-8) Repeat steps 3 to 5 till all the 4 bits appear at the output of shift register.
- Step-9) Press the "Print" button after completing your simulation to get your results.

SIMULATION:



POSTEST:

Screenshot of a web browser showing a posttest page from de-iitr.vlabs.ac.in. The page is titled "Posttest" and includes sections for Pretest, Procedure, Simulation, Posttest, References, and Feedback. The Posttest section contains several questions with multiple-choice answers.

Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.

- a: 2
- b: 3
- c: 4
- d: 5

How can parallel data be taken out of a shift register simultaneously?

- a: Use the Q output of the first FF
- b: Use the Q output of the last FF
- c: Tie all of the Q outputs together
- d: Use the Q output of each FF

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

- a: 01110
- b: 00001

Screenshot of a web browser showing a posttest page from de-iitr.vlabs.ac.in. The page is titled "Posttest" and includes sections for Pretest, Procedure, Simulation, Posttest, References, and Feedback. The Posttest section contains several questions with multiple-choice answers.

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

- a: 01110
- b: 00001
- c: 00101
- d: 00101

The full form of SIPO is _____

- a: Serial-in Parallel-out
- b: Parallel-in Serial-out
- c: Serial-in Serial-out
- d: Serial-In Peripheral-Out

A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?

- a: Tristate
- b: End around
- c: Universal

CONCLUSION:

The 4-bit SIPO shift register using IC 7474 (D flip-flop) effectively captures serial input data and provides parallel output, demonstrating the versatility of flip-flops in digital circuits. This design highlights the functionality of sequential logic in processing and storing binary information.

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