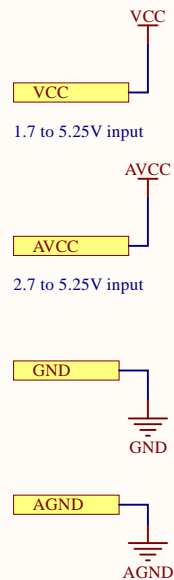
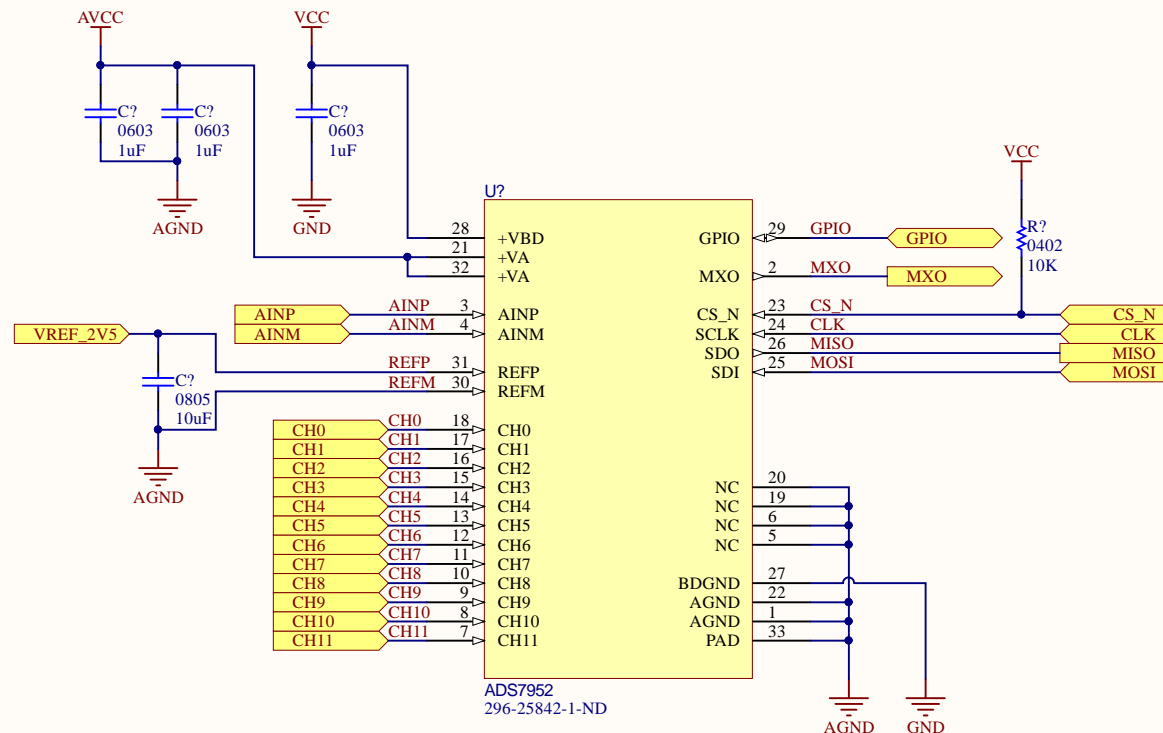


POWER INPUTS  
AVCC >= VCC (pg 51)



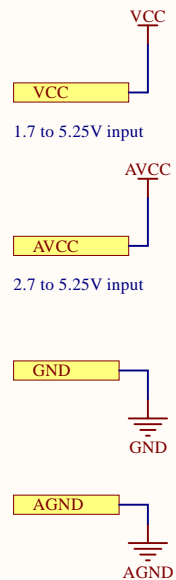
See pg 53, each +VA pin should have it's own 1uF



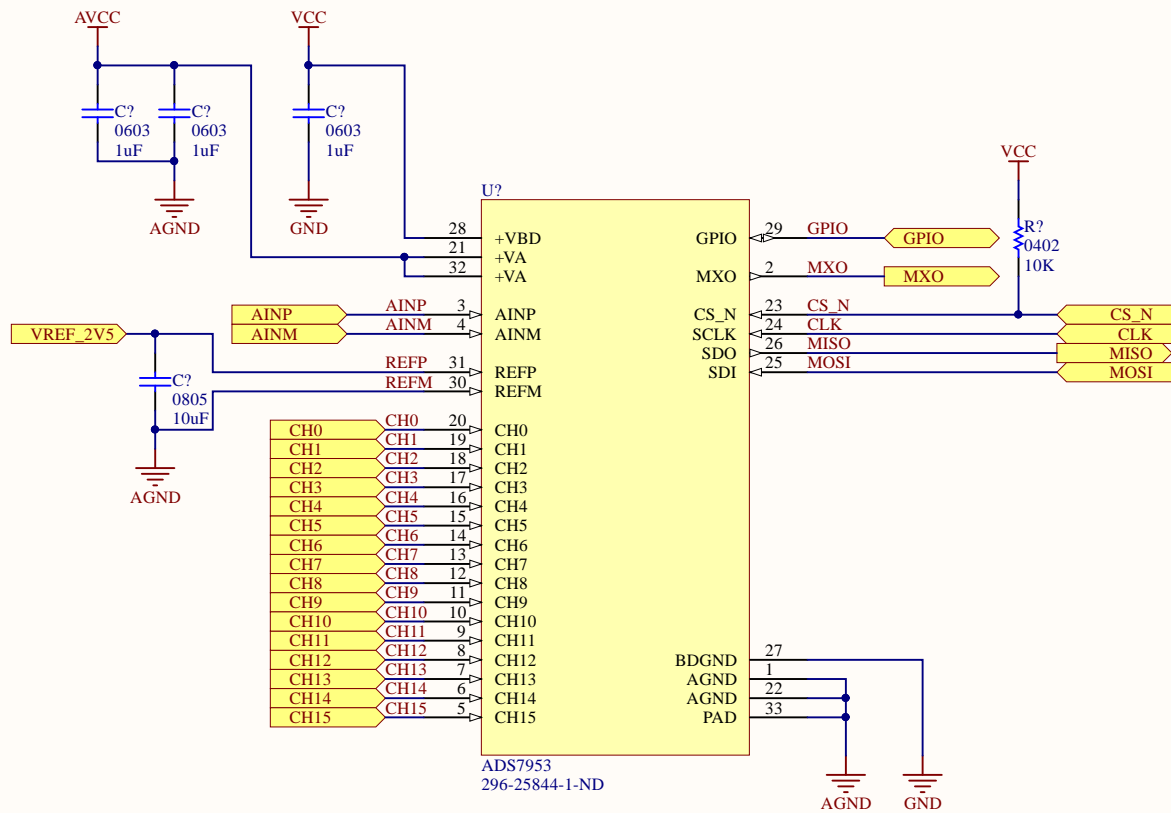
12 CHANNEL ADC

Title		
adc-ADS7952.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\adc-ADS7952.SchDoc	Drawn By: Dylan Vogel

POWER INPUTS  
AVCC >= VCC (pg 51)



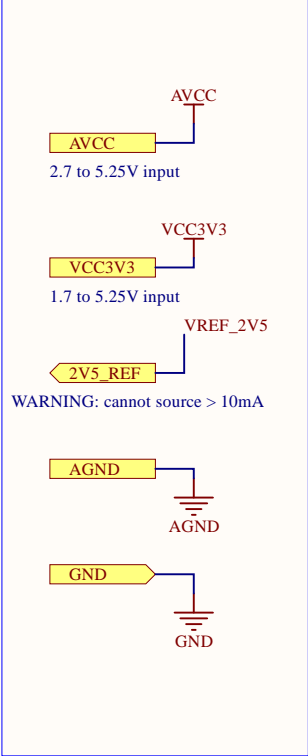
See pg 53, each +VA pin should have it's own 1uF



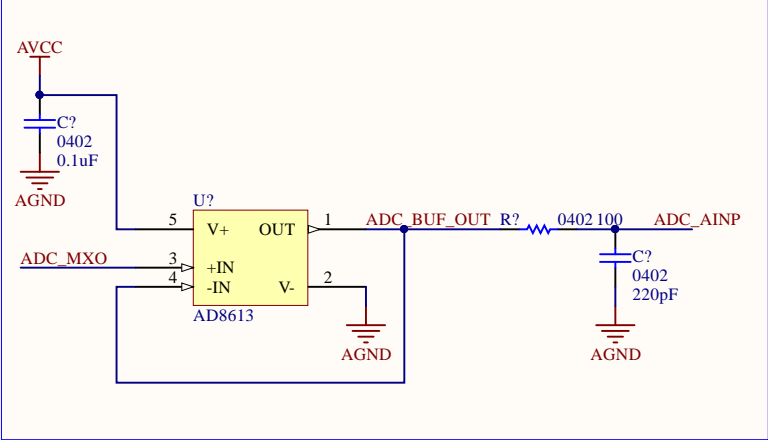
16 CHANNEL ADC

Title			
adc-ADS7953.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-07-14	Sheet * of *	
File:	C:\Users\...\adc-ADS7953.SchDoc	Drawn By:	Dylan Vogel

POWER PORTS  
AVCC >= VCC (pg 51)



ADC INPUT BUFFER  
See pg. 50 for discussion of unity buffer design procedure



2V5 REFERENCE  
Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)

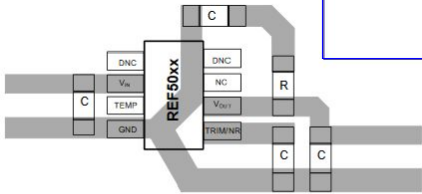
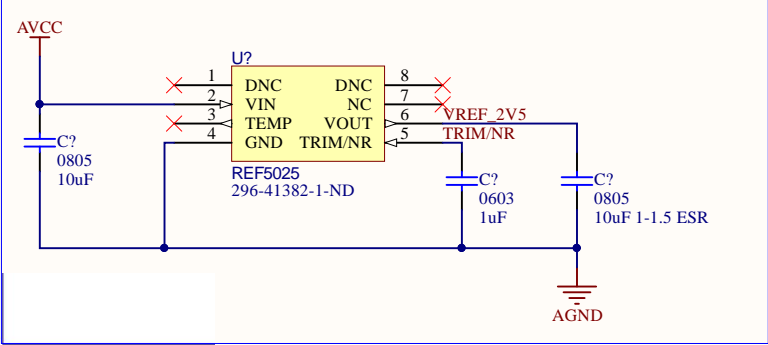


Figure 44. Layout Example

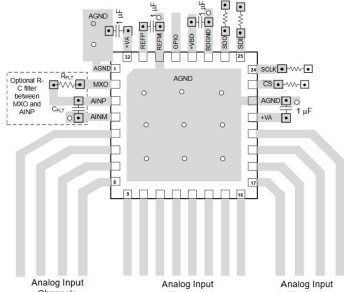
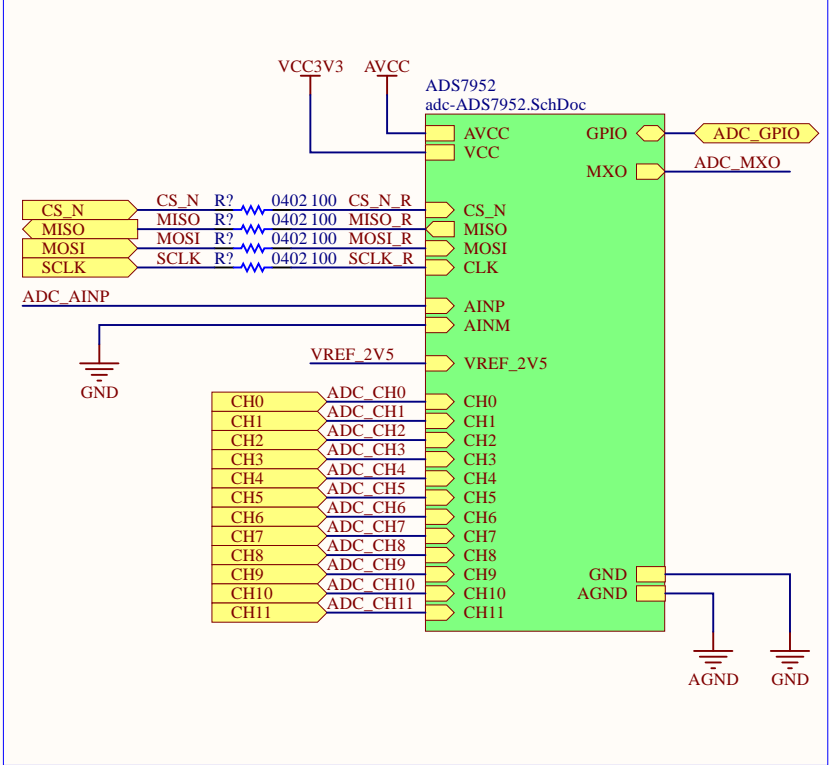


Figure 70. Recommended Layout for the VQFN Packaged Device

ADC

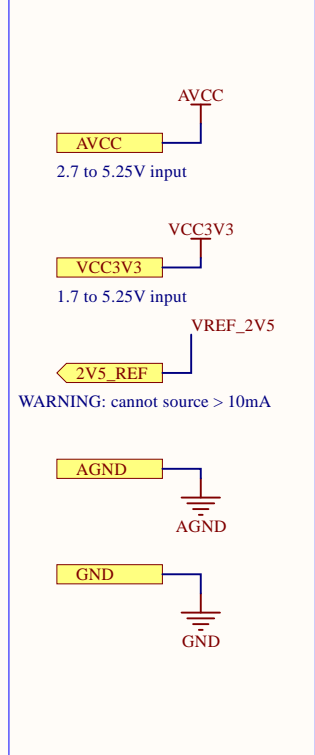


This schematic implements the ADS7952 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.

- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7952 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

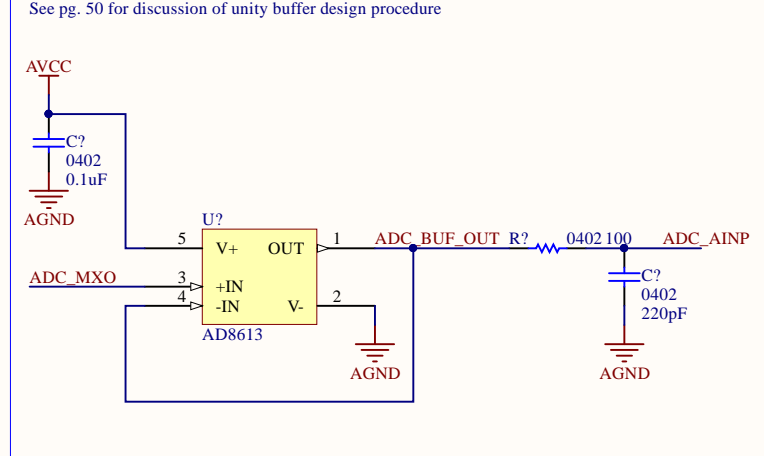
Title		
adc-circuit-ADS7952.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\adc-circuit-ADS7952.SchDoc	Drawn By: Dylan Vogel

POWER PORTS  
AVCC >= VCC (pg 51)



ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure



2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)

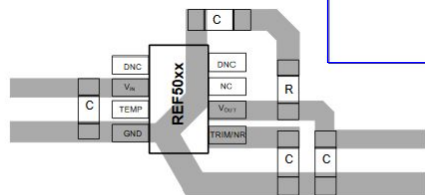
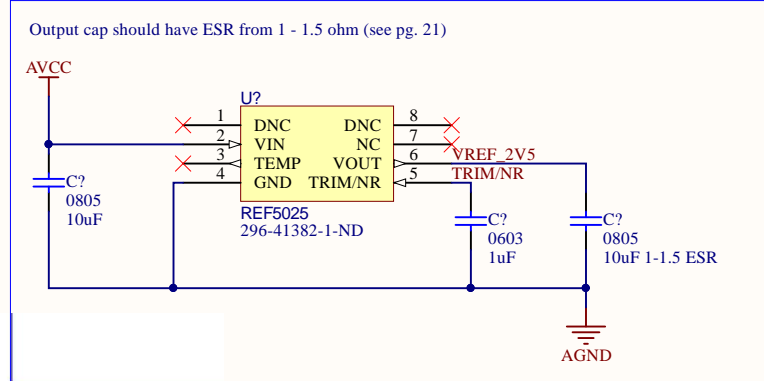


Figure 44. Layout Example

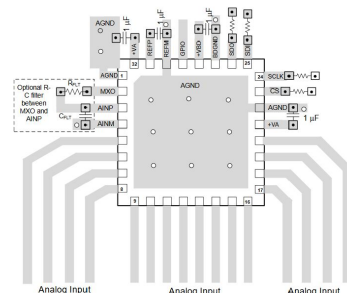
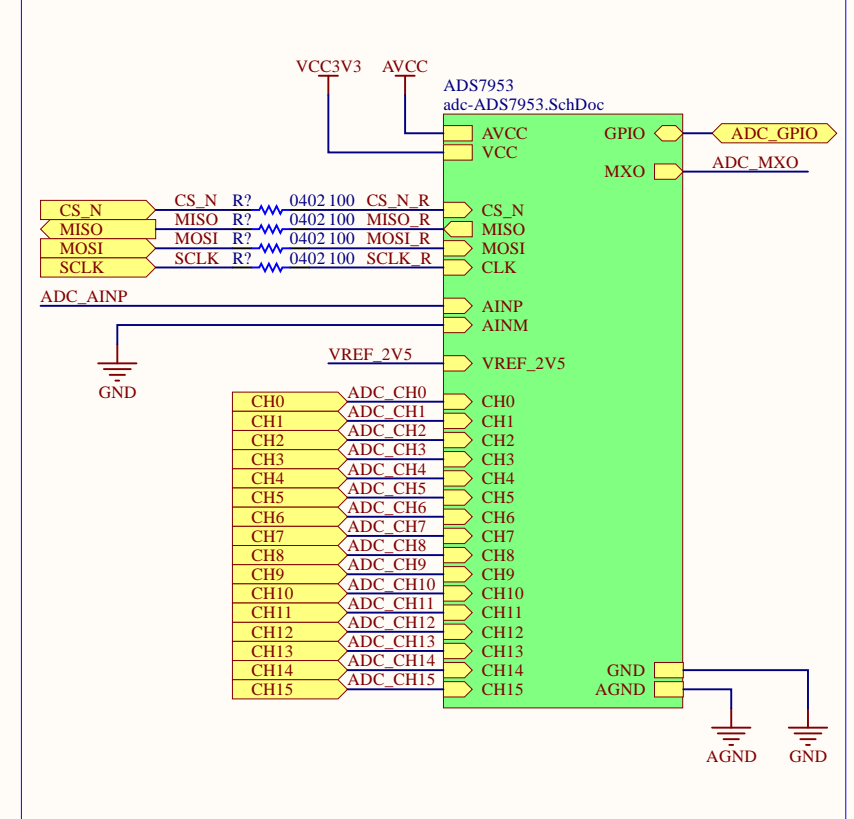


Figure 70. Recommended Layout for the VQFN Packaged Device

ADC



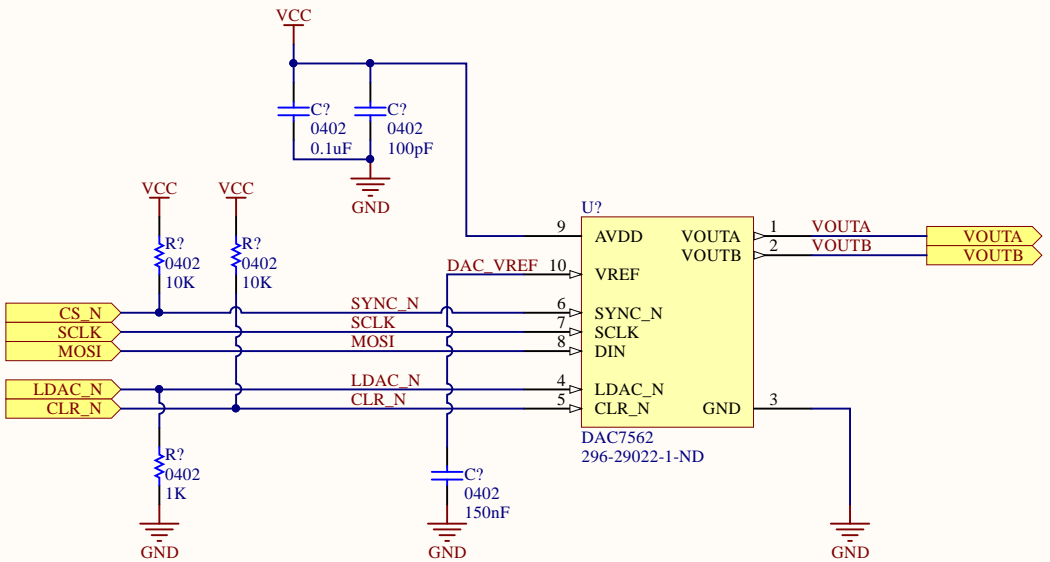
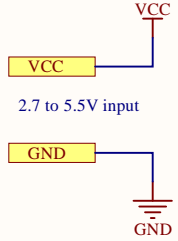
This schematic implements the ADS7953 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.

- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7953 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

Title		
adc-circuit-ADS7953.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\adc-circuit-ADS7953.SchDoc	Drawn By: Dylan Vogel



POWER INPUTS



This schematic implements the DAC7562 16-bit digital-to-analog converter. The device has two configurable outputs, VOUTA and VOUTB, which can be digitally written through the 3-wire SPI interface. This particular device is set to zero scale (0V) both outputs upon power-on/reset. Toggling CLRn to LOW via an external GPIO will also zero both outputs.

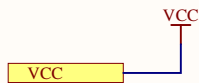
The device is connected in synchronous mode, where LDAC\_N is connected to GND through a strong pull-down. This means that output VOUTA/VOUTB will be updated at the end of the SPI communication frame. The alternative would be to connect LDAC\_N to a microcontroller GPIO and toggle it low manually to set all outputs at the same time. This is referred to as asynchronous mode in the datasheet.

Title		
dac-DAC7562.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\dac-DAC7562.SchDoc	Drawn By: Dylan Vogel

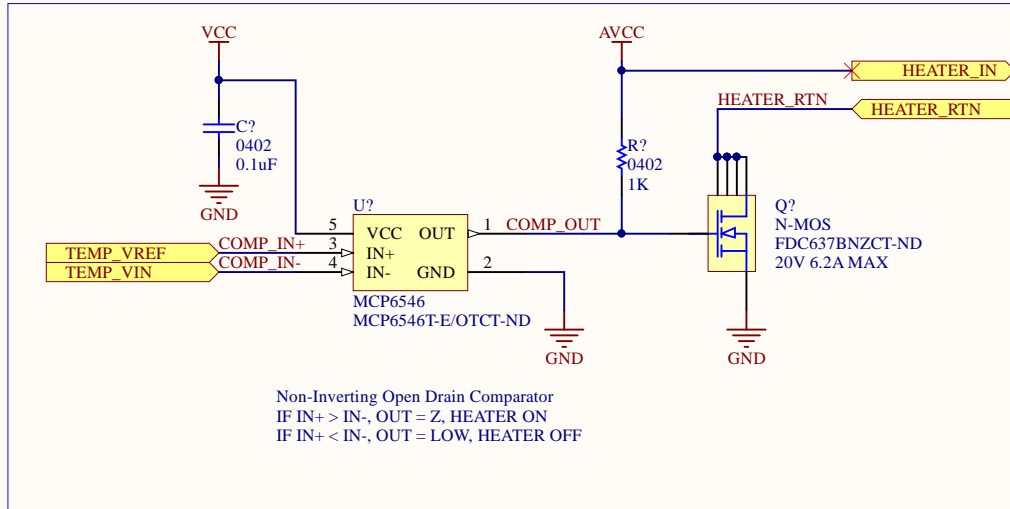
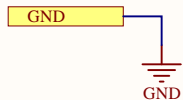
# POWER INPUTS



Designed for +5V, see note below

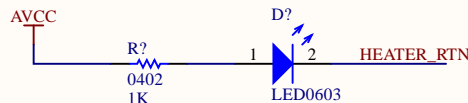


1.6 to 5.5V input



Non-Inverting Open Drain Comparator  
IF IN+ > IN-, OUT = Z, HEATER ON  
IF IN+ < IN-, OUT = LOW, HEATER OFF

## LED HEATER STATUS INDICATION



Might need to be changed based on your AVCC level. Designed for 5V

This schematic implements a single heater control circuit, relying on an open-drain comparator and NMOS switch for completely analog operation.

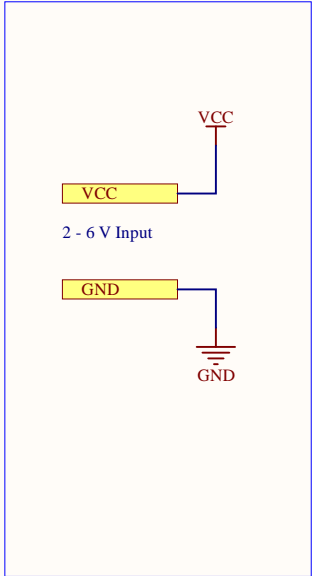
The temperature setpoint is set via the voltage on the TEMP\_VREF pin, which is compared against the voltage on the TEMP\_VIN pin. If the voltage on TEMP\_VREF is higher, the output of the comparator will go high-impedance and drive the gate of the NMOS to 5V through the 1K pull-up resistor. This should be enough to switch the MOSFET in triode with a relatively low VDS at our target current (128mA).

Conversely, when TEMP\_VIN is above TEMP\_VREF, the output is switched to GND and the MOSFET turns off. How you decide to set TEMP\_VREF and TEMP\_VIN is entirely up to you.

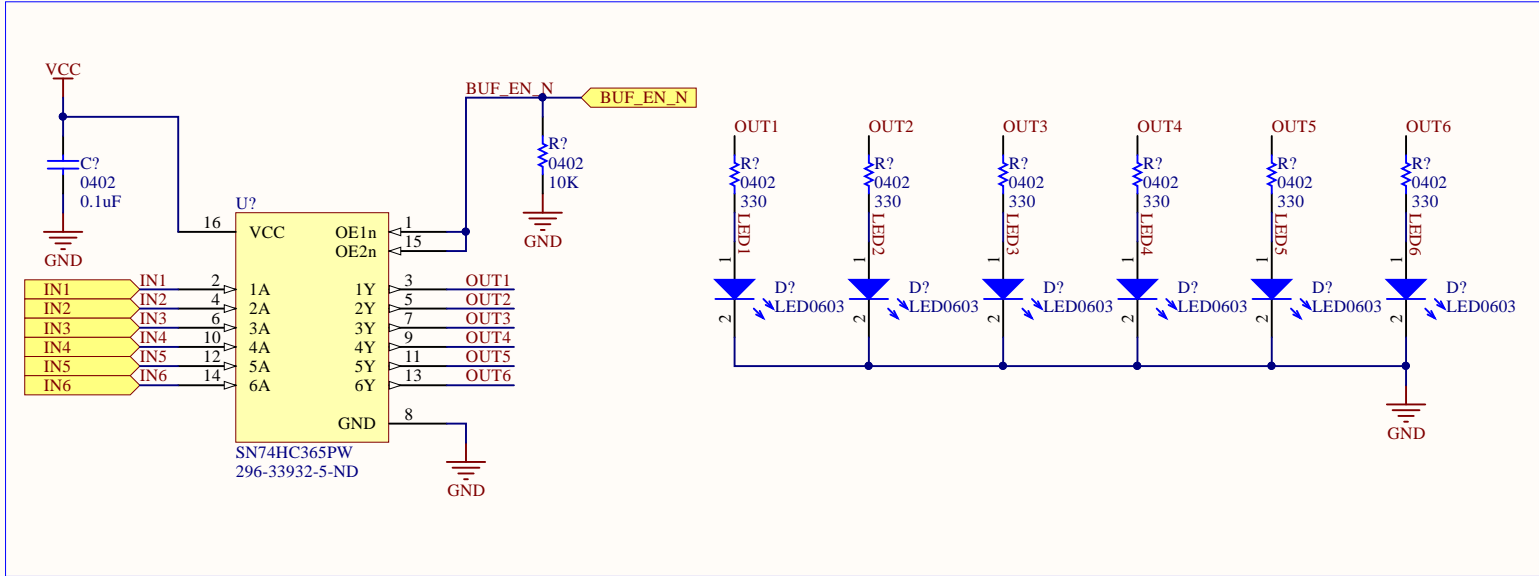
The circuit is designed to work at 5V. To operate at different voltages, just be sure to check the relevant ratings on the different components.

Title		
heater-control-comparator.SchDoc		
Size	Number	Revision
A	PCBS-COMMON	1.0
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\heater-control-comparator.SchDoc	Downloaded By: B. Almeida, D. Vogel

INPUT POWER



LED BUFFER



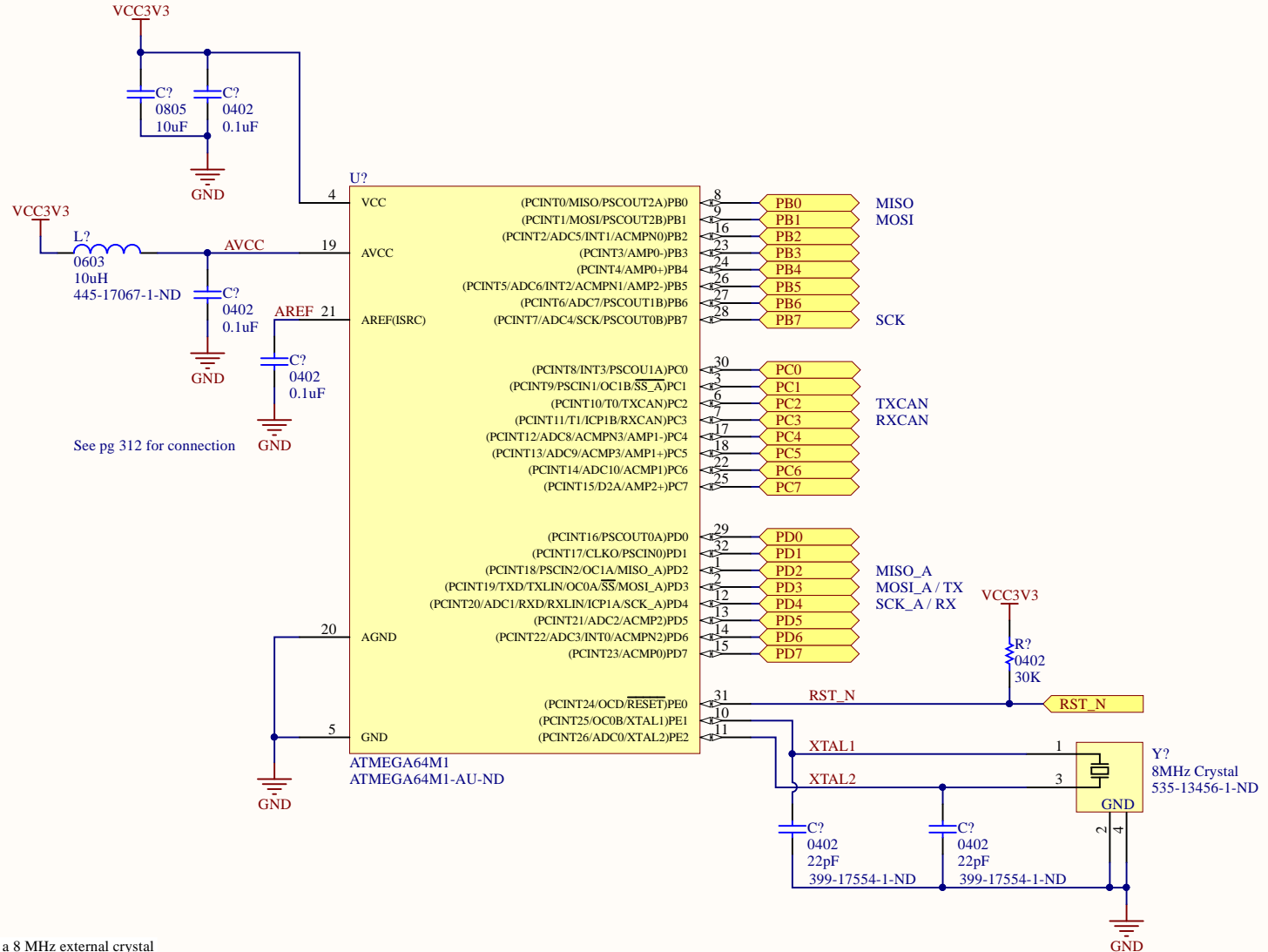
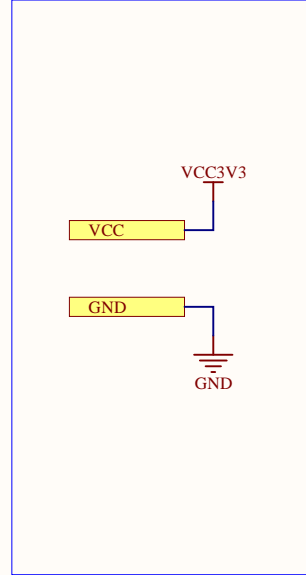
This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF\_EN\_N input can be connected to a microcontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title			
led-monitoring-SN74HC365PW.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-07-14	Sheet *	of *
File:	C:\Users\...led-monitoring-SN74HC365PW.SchDoc	Drawn By:	Dylan Vogel



# POWER INPUT



This schematic implements the ATMEGA64M1 microcontroller with a 8 MHz external crystal and necessary power connections.

- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
- I would read through 18.5.2 and 18.6.2 of the complete 64M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
- If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be selected in software as the reference voltage.

Title		
micro-ATMEGA64M1.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\micro-ATMEGA64M1.SchDoc	Drawn By: Dylan Vogel

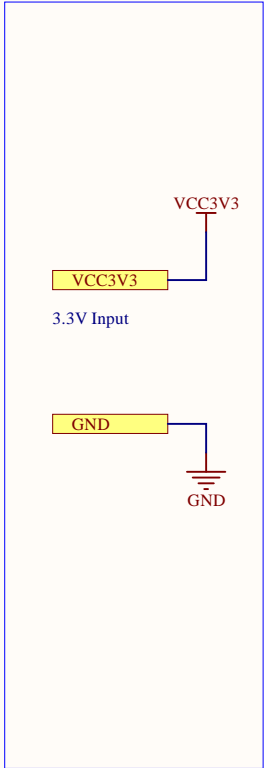
A

B

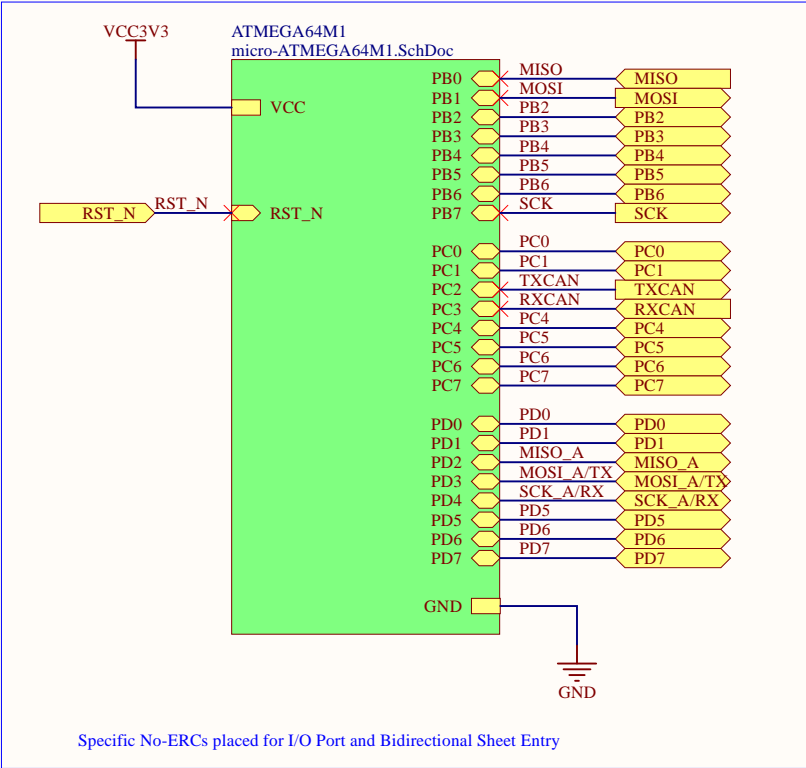
C

D

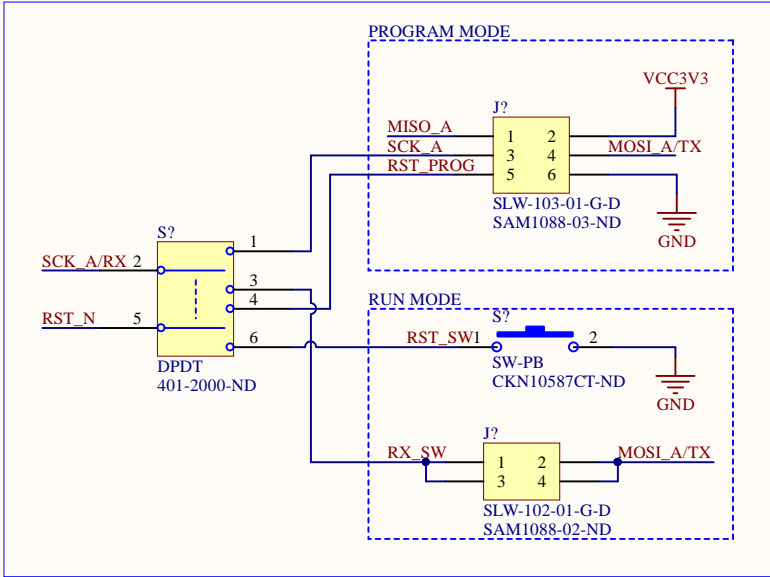
POWER INPUTS



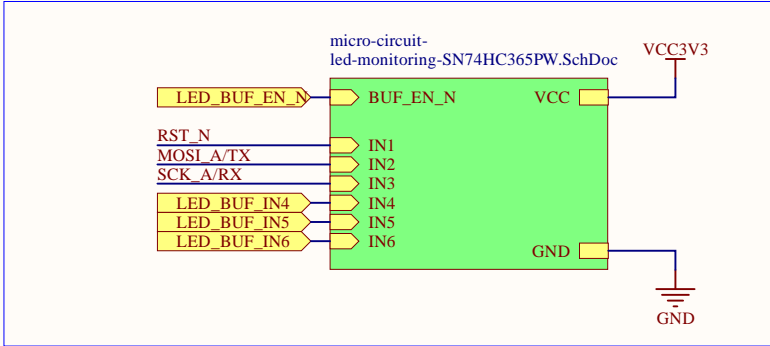
ATMEGA32M1



MODE SELECT CIRCUITRY



LED MONITORING

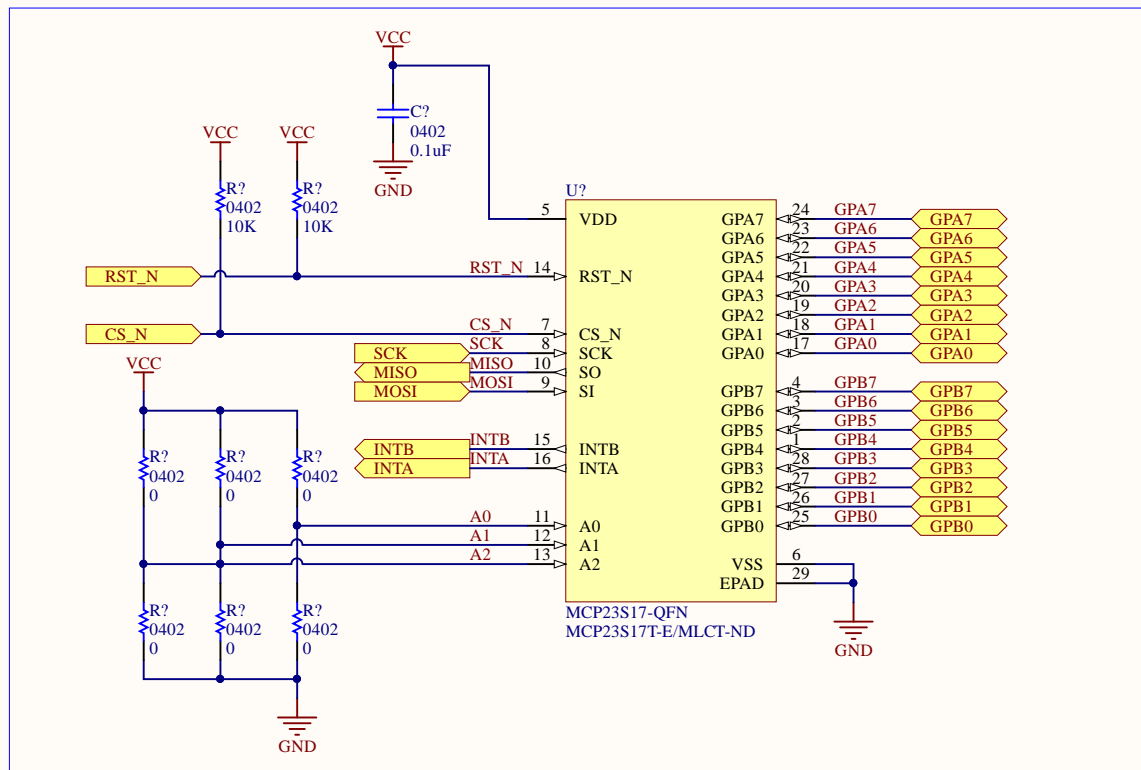
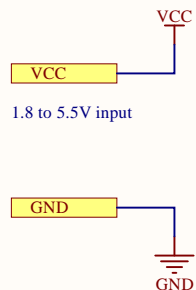


This schematic extends the functionality already included in the micro-ATMEGA32M1 schematic, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED\_BUF\_IN[4:6]. They can be connected in the schematic which includes this sheet up to an additional 3 lines. Highly recommend more blinking lights.

Title		
micro-circuit-ATMEGA64M1.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\micro-circuit-ATMEGA64M1.SchDoc	By: Dylan Vogel

## POWER INPUTS



## ADDRESS:

### CHANNEL SELECTION

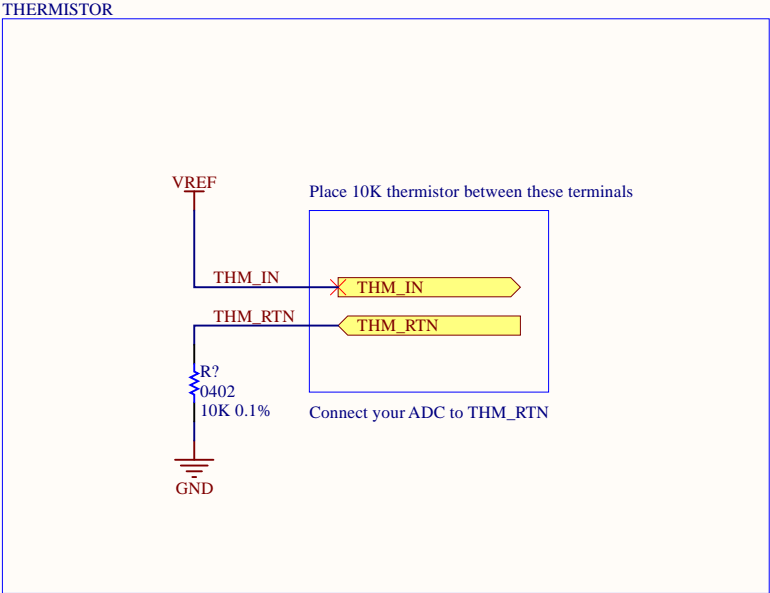
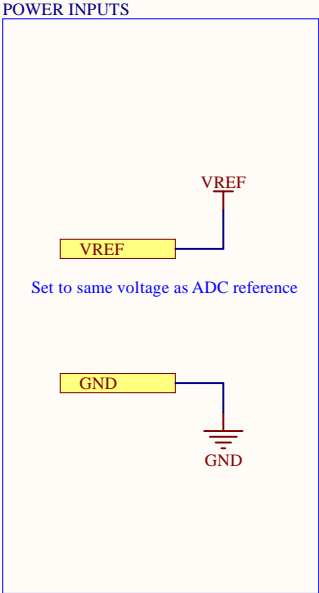
ONLY SOLDER ONE 0 OHM FROM EACH PAIR  
 PEX ADDRESS = A2 A1 A0  
 VCC == 1 GND == 0

This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST\_N and CS\_N.

Multiple port expanders can be connected to the same CS\_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

Title		
pex-MCP23S17.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\pex-MCP23S17.SchDoc	Drawn By: Dylan Vogel

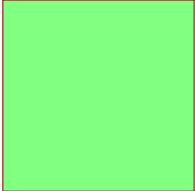


Title		
thermistor-input-10k.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-14	Sheet * of *
File:	C:\Users\...\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

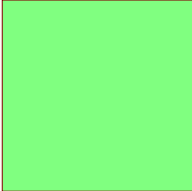
A

A

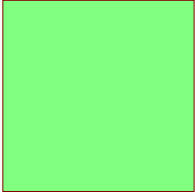
ADS7952  
adc-circuit-ADS7952.SchDoc



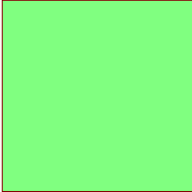
ATMEGA64M1  
micro-circuit-ATMEGA64M1.SchDoc



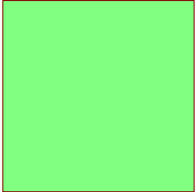
ADS7953  
adc-circuit-ADS7953.SchDoc



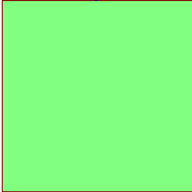
PEX  
pex-MCP23S17.SchDoc



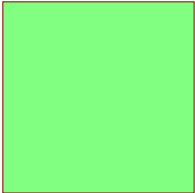
CAN  
can-SN65HVD233.SchDoc



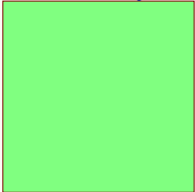
THM\_INPUT  
thermistor-input-10k.SchDoc



DAC  
dac-DAC7562.SchDoc



HEATER\_CTRL\_COMP  
heater-control-comparator.SchDoc



B

B

C

C

D

D

"TABLE OF CONTENTS" PAGE SO THAT ALTIUM COMPILES THE PROJECT CORRECTLY

Title			
TOC.SchDoc			
Size	Number		Revision
A4	PCBS-COMMON		*
Date:	2019-07-14	Sheet * of *	
File:	C:\Users\...\TOC.SchDoc	Drawn By:	*