Course Name: EMBEDDED SYSTEMS I / III

Course Number and Section: **14:332:493:03 / 16:332:579:05**

Year: Spring 2024

Lab Report #: 1

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Student Name and RUID: Ruben Alias 207005068

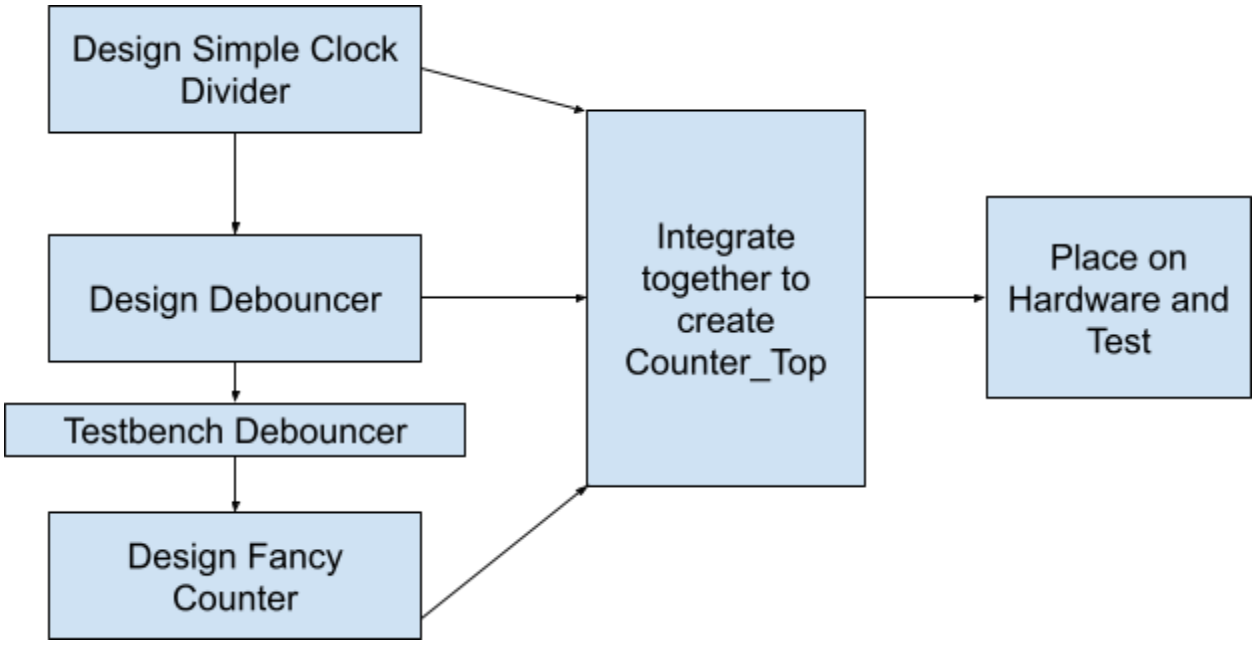
Date Submitted: 02/23/2024

GitHub Link:

https://github.com/embedded-systems-1-spring-2024-labs/lab-1-Herxity

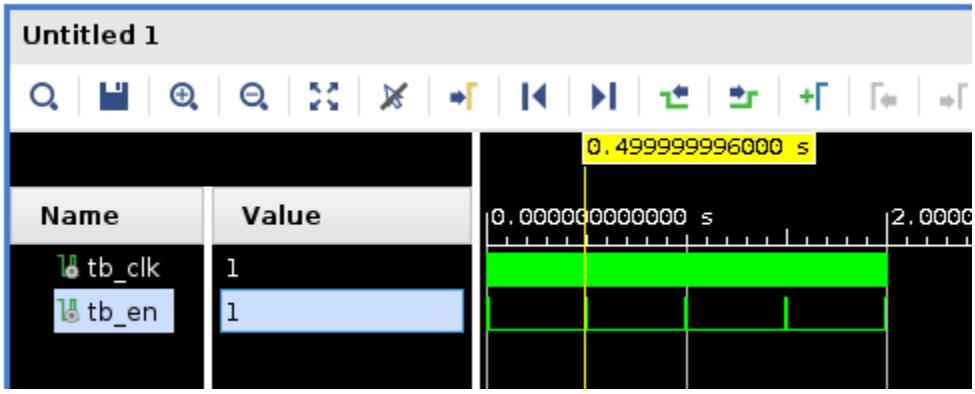
Purpose/Objective: The purpose of this lab was to design simple controllable counter, able to take button inputs which were debounced to ensure input stability, all synced up to a stead 2Hz clock

Theory of Operation:

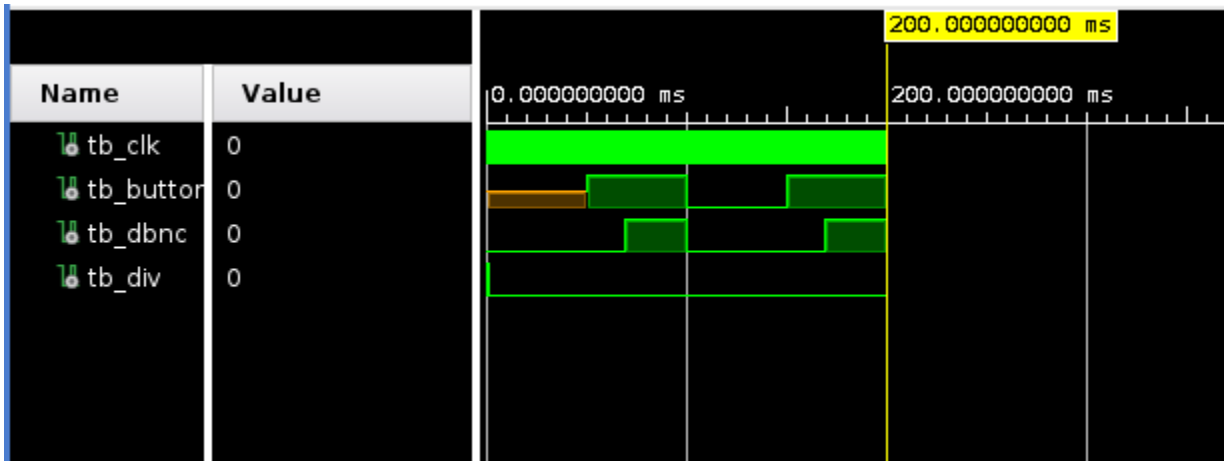


Simulation Waveforms:

Clock Div



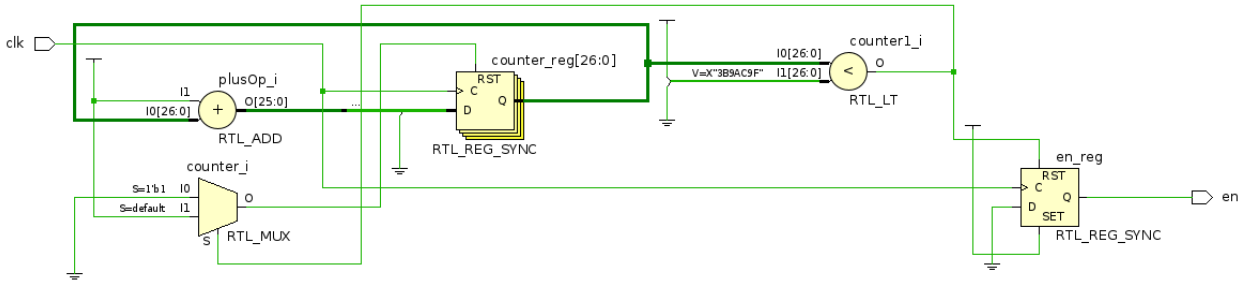
Debouncer Simulation



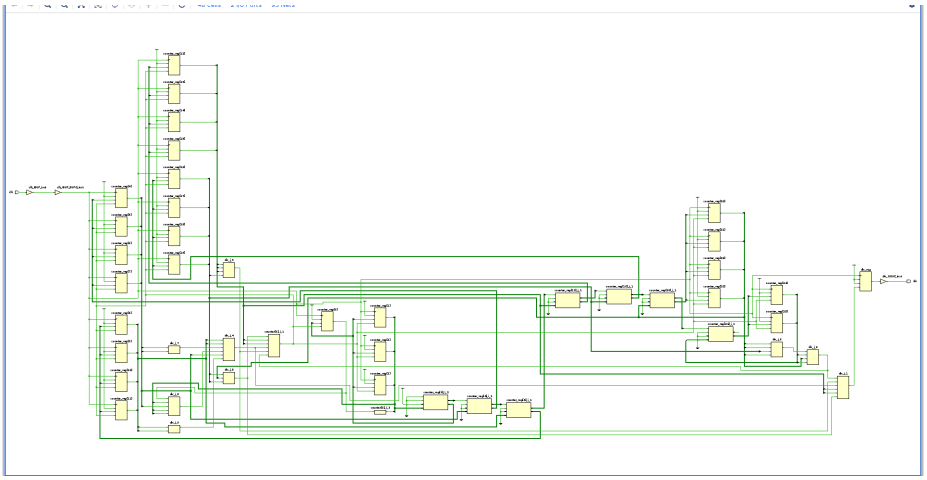
Vivado Schematics:

CLOCK DIV

Elaboration

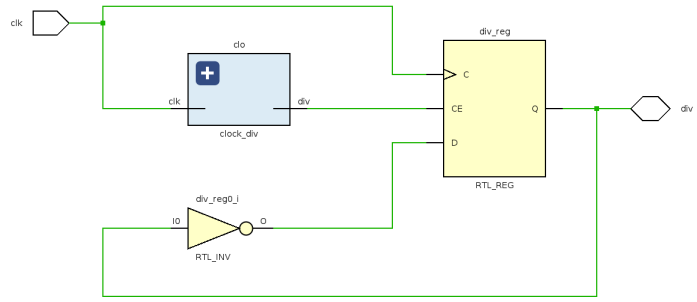


Synthesis Schematic

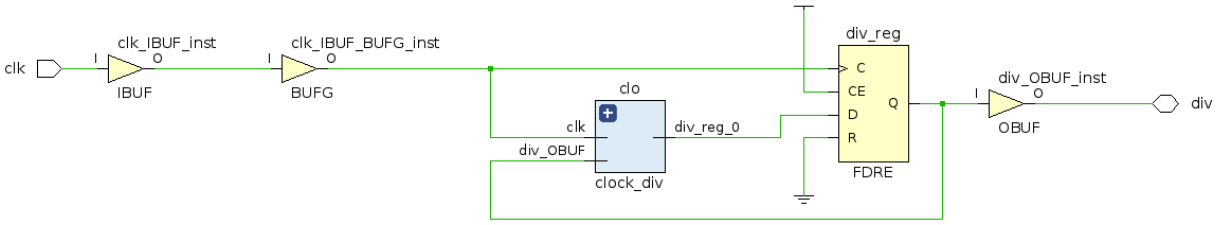


Div_top

RTL SCHEMATIC



Div Top Synthesis

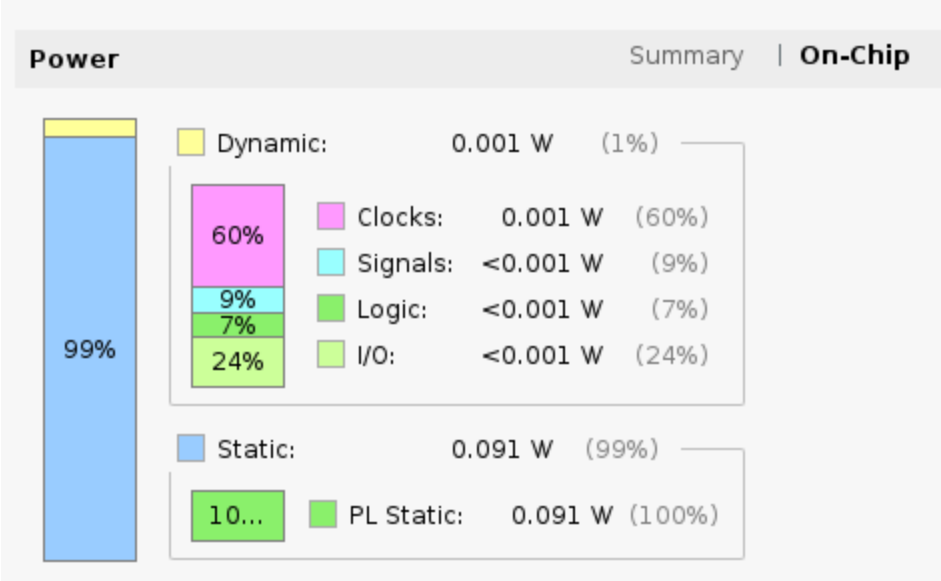


Div top utilization table

Graph | **Table**

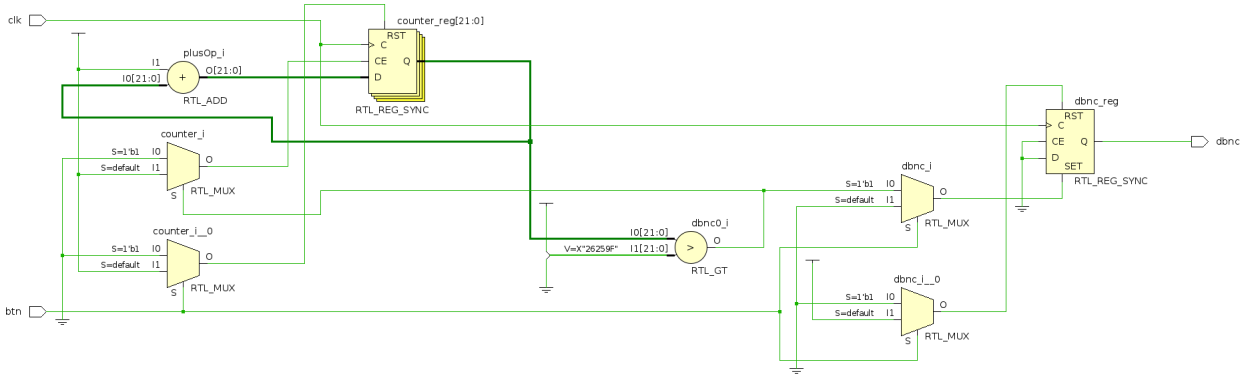
Resource	Estimation	Available	Utilization %
LUT	7	17600	0.04
FF	28	35200	0.08
IO	2	100	2.00
BUFG	1	32	3.13

Div Top power usage

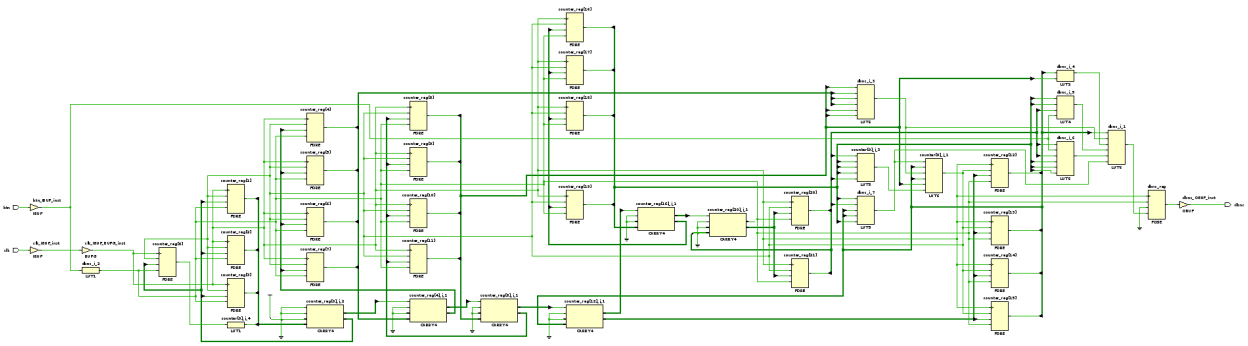


DEBOUNCER

Debouncer RTL Schematic



Debouncer Synthesis Schematic



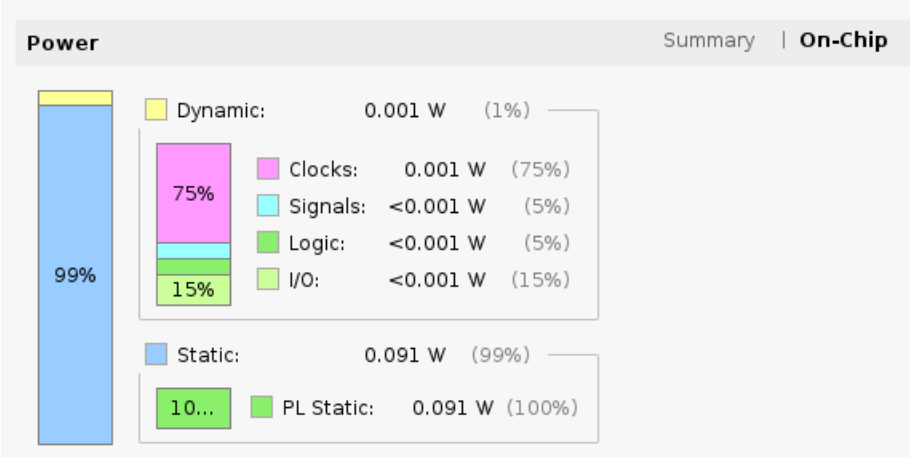
Debouncer Utilization Table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

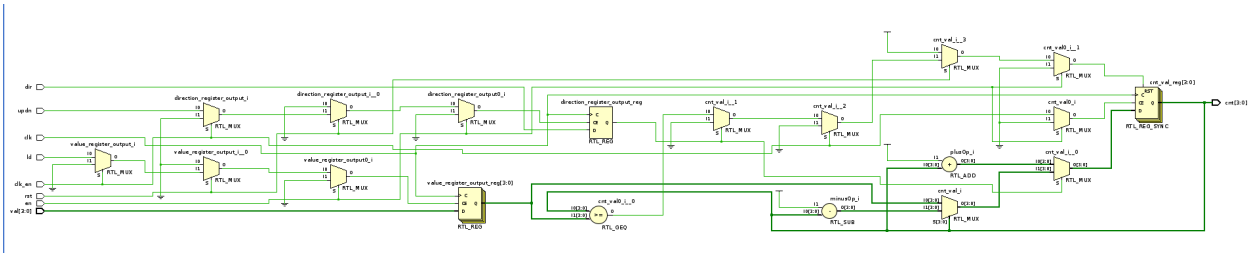
Resource	Estimation	Available	Utilization %
LUT	10	17600	0.06
FF	23	35200	0.07
IO	3	100	3.00
BUFG	1	32	3.13

Debouncer On-Chip Power Graph

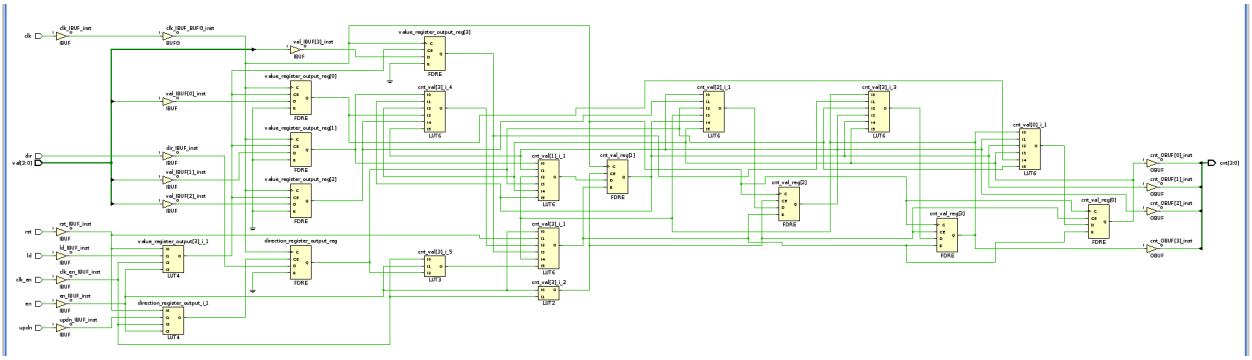


Part 3 Actually Using a Counter to Count

RTL Schematic



Synthesis schematic



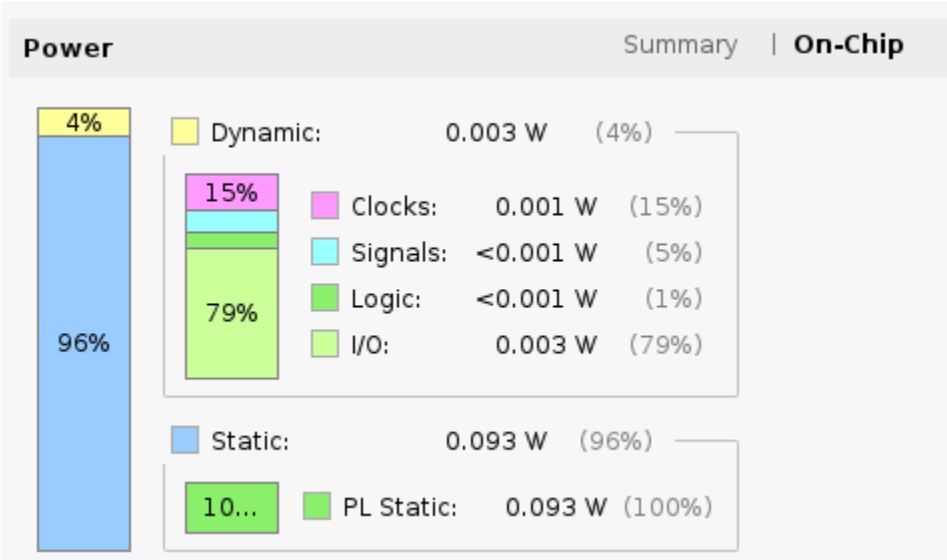
Utilization Table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

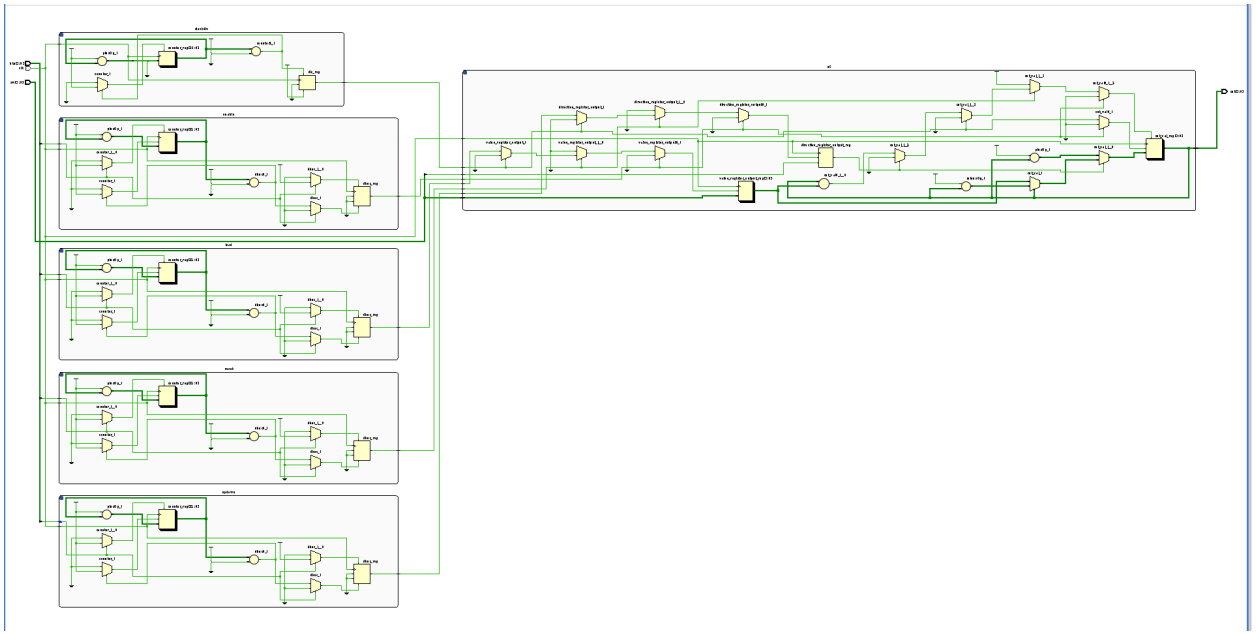
Resource	Estimation	Available	Utilization %
LUT	10	17600	0.06
FF	9	35200	0.03
IO	15	100	15.00
BUFG	1	32	3.13

Power Graph

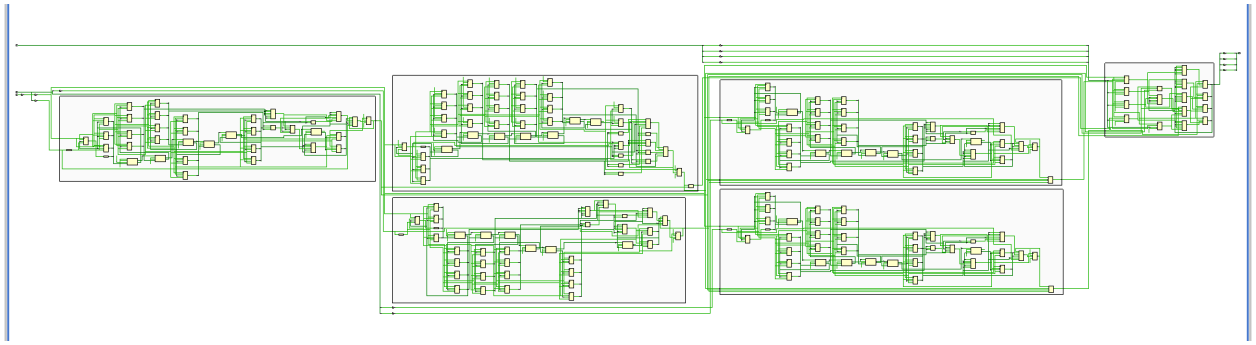


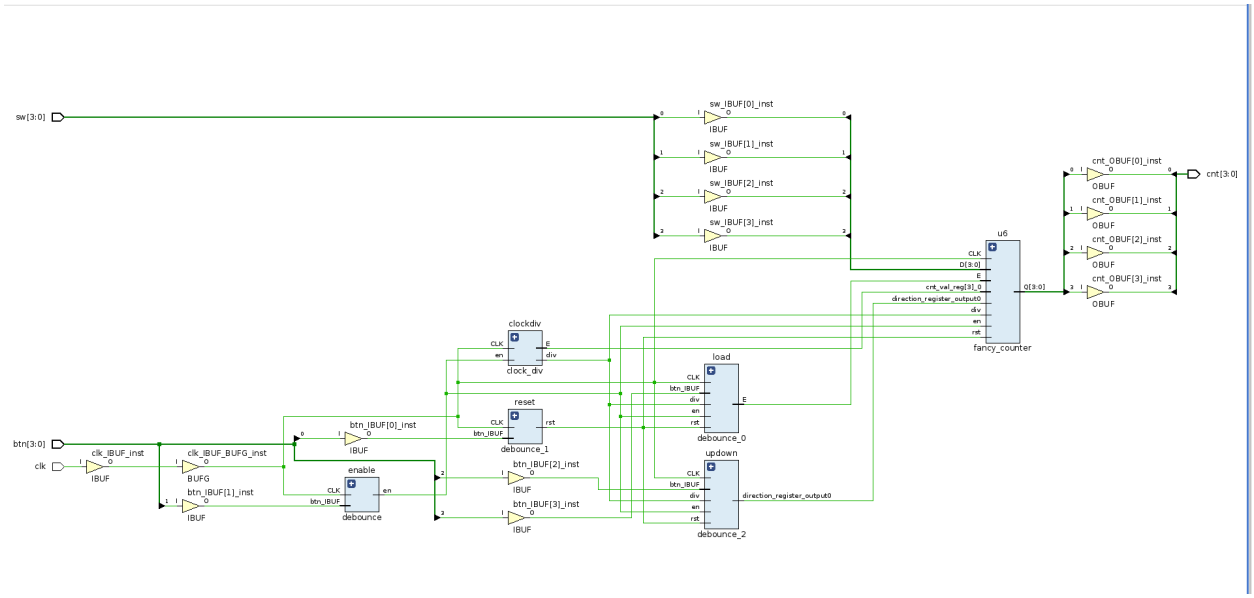
Part 4 - Bringing it All Together

RTL Schematic



Synthesis Schematic





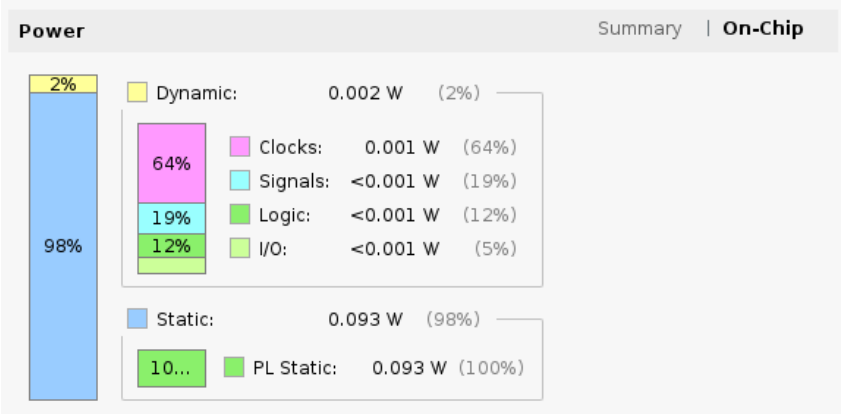
Utilization table

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	53	17600	0.30
FF	128	35200	0.36
IO	13	100	13.00
BUFG	1	32	3.13

Power Graph



XDC File:

I needed to uncomment the switches and buttons and clock, keeping their names the same. I needed to rename the LEDs array to *cnt* as that was my output variable for counter_top.

Answers to Additional Questions and Extra Credit:

Part I

Question 1.1: How much do we need to divide our input by to get from 125 MHz to 2 Hz?

125Mhz => 125 * 10^6 Oscillations/second
2Hz => 2 Oscillations/second
(125*10^6)/62500000 = 2
Divide by 62500000.

Question 1.2: How many bits are required to store a counter that can count up to the value obtained in Q1.1?

27 Bits are required.

Part II

2.1 What is the value of the button when it is pressed for Zybo?

The button value is 1

2.3: If we want our debounce time to be 20 ms, and our system clock is 125 MHz, how many ticks do we need a steady '1' to be read for it to count as a '1'?)

2.5 million

2.4: How many bits are required for a counter that can go that high?

ceil(log_2 (2.5mil)) = 22 bits

Conclusion: In this Lab I learned the importance of syncing up processes to the clock to prevent any unseen errors in Synthesis and Implementation, as well as practical applications of a clock divider and the importance of debouncing inputs.

Follow Up: I feel like I completely understand structural modeling and the basics of VHDL's basic types and their interactions.