Course Name: EMBEDDED SYSTEMS I / III

Course Number and Section: **14:332:493:03 / 16:332:579:05**

Year: Spring 2024

Lab Report #: 5

Lab Instructor: Milton Diaz

Student Name and RUID: Ruben Alias 207005068

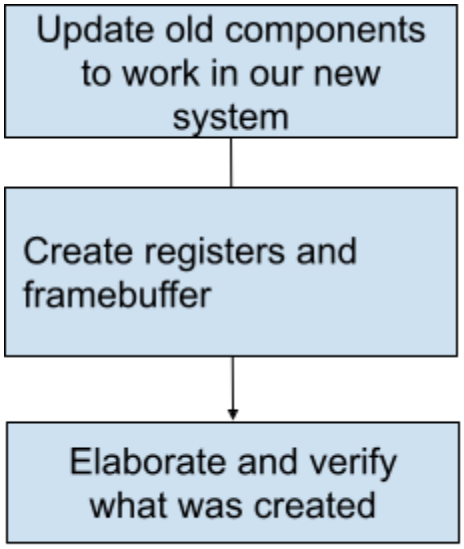
Date Submitted: 04/19/2024

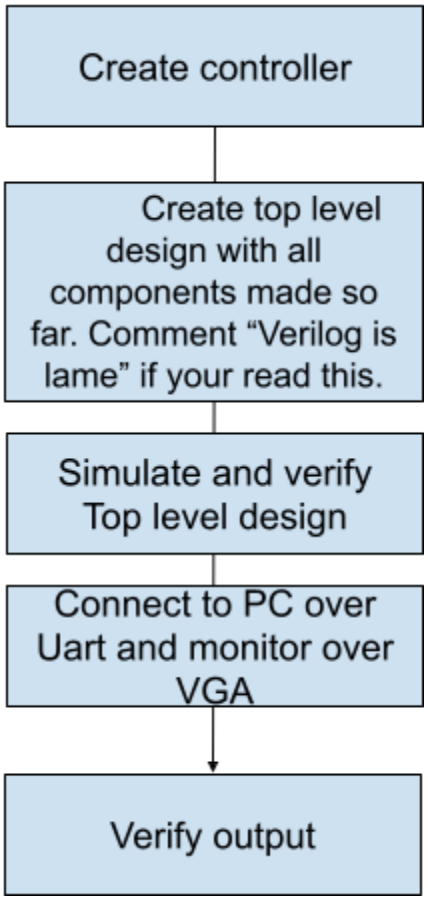
GitHub Link:
https://github.com/embedded-systems-1-spring-2024-labs/lab-5-Herxity/tree/main

Purpose/Objective:

The purpose of this lab is to learn to compile multiple large VHDL and Xilinx IP components together into a larger top level design, maintaining proper timing and state management. The exact project was to create a simple microprocessor running GRISC assembly instructions.

Theory of Operation:

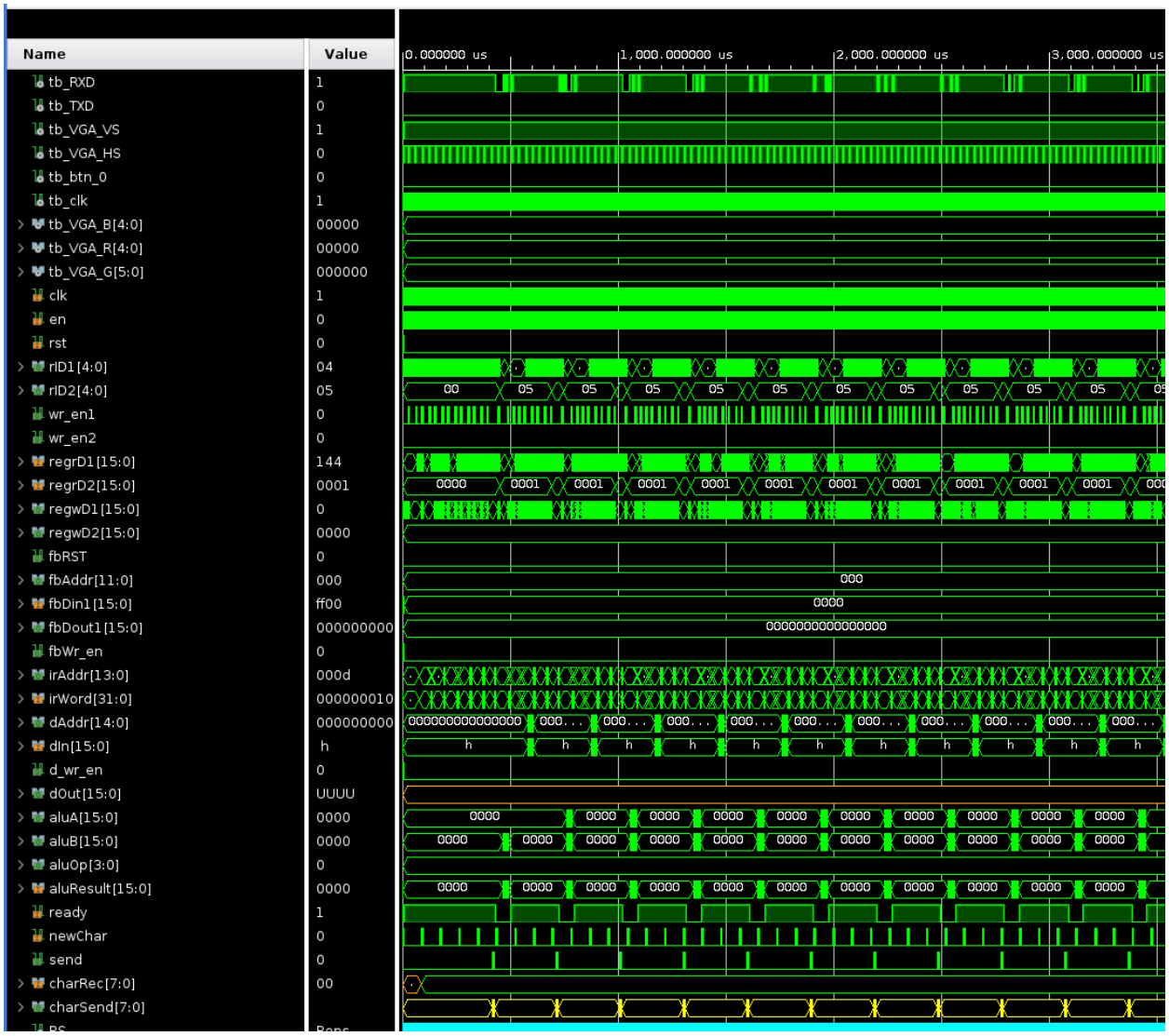




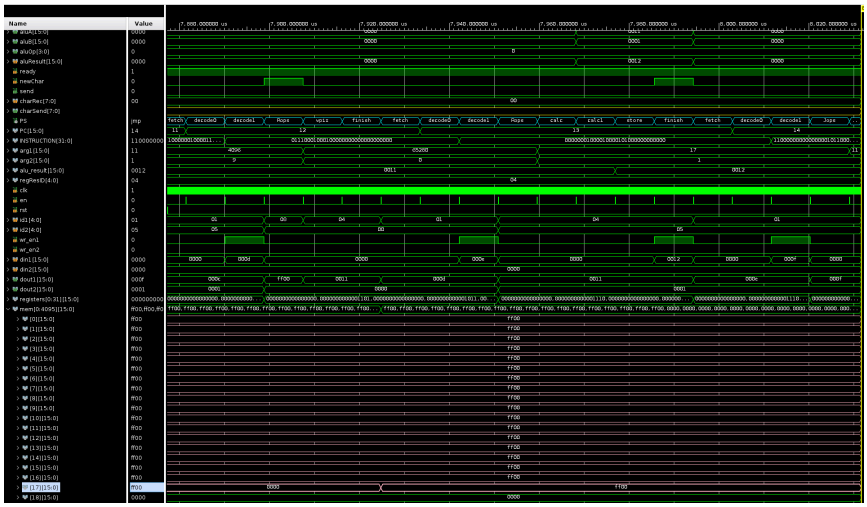
Simulation Waveforms:

Top Level

Sending HELLO WORLD



Framebuffer Filling up

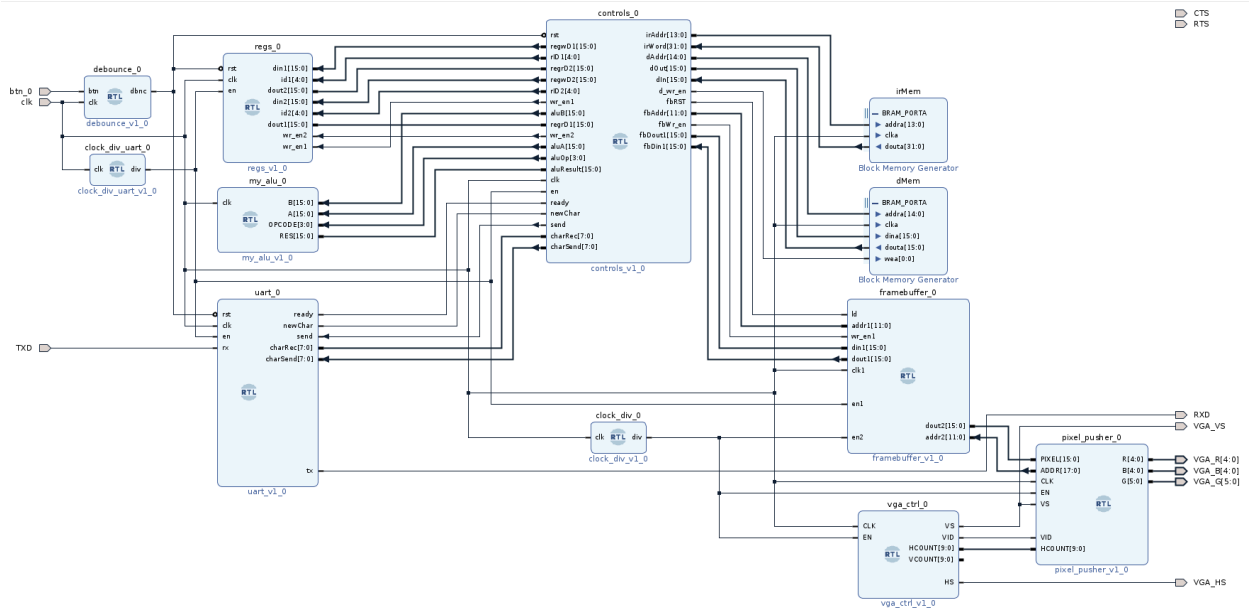


VGA Displaying

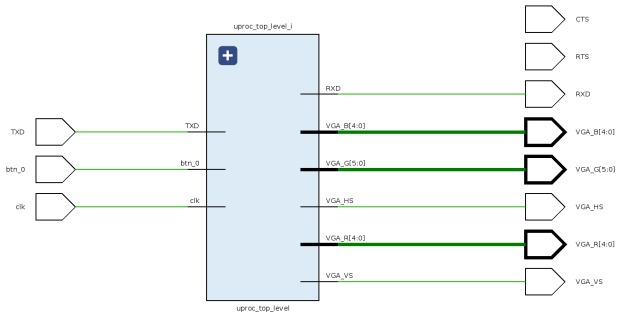
Vivado Schematics, Power Diagrams, and Utilization

Top level

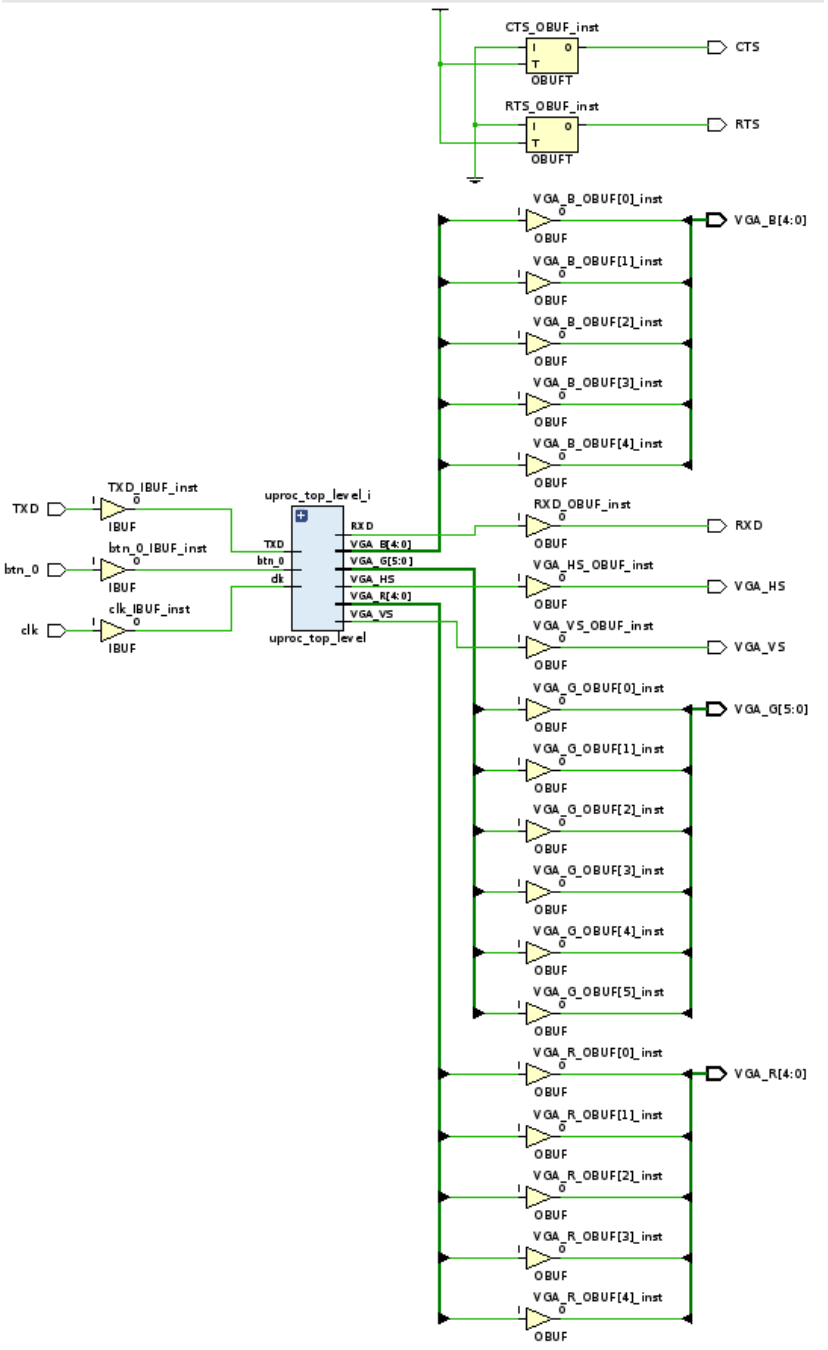
Block Diagram



Elaboration Schematic



Synthesis Schematic



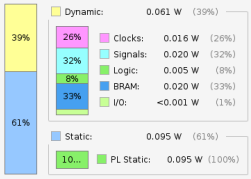
Tables and Graphs

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

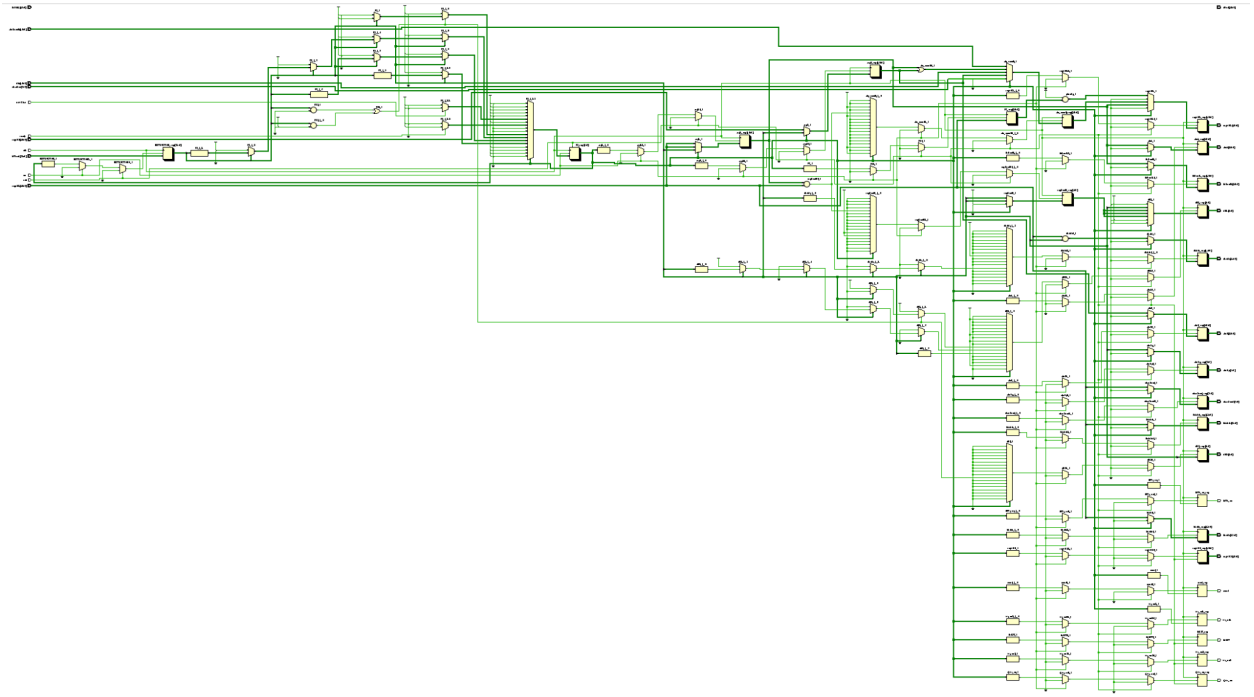
Resource	Utilization	Available	Utilization %
LUT	6516	17600	37.02
LUTRAM	4224	6000	70.40
FF	1128	35200	3.20
BRAM	29	60	48.33
IO	24	100	24.00
BUFG	1	32	3.13

Power — Summary | **On-Chip**

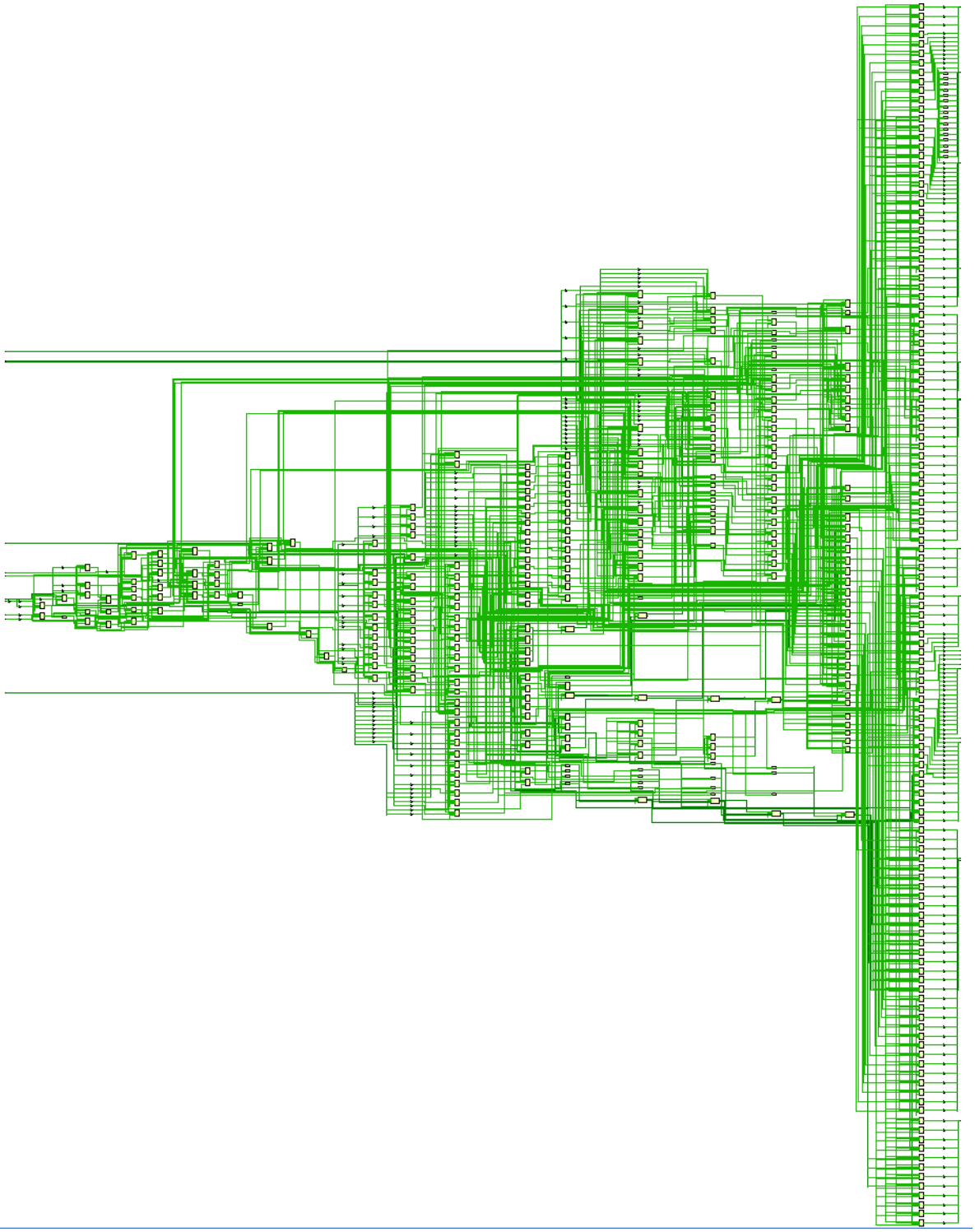


Control

Elaborate



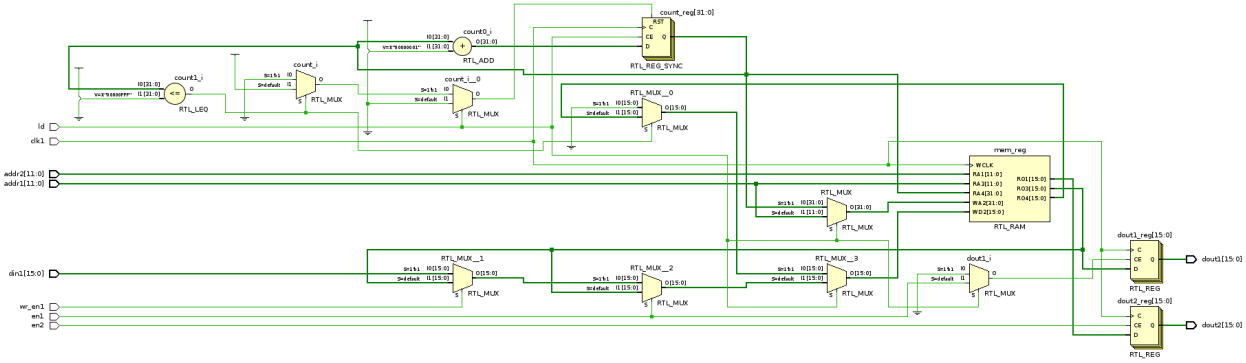
Synthesis Schematic



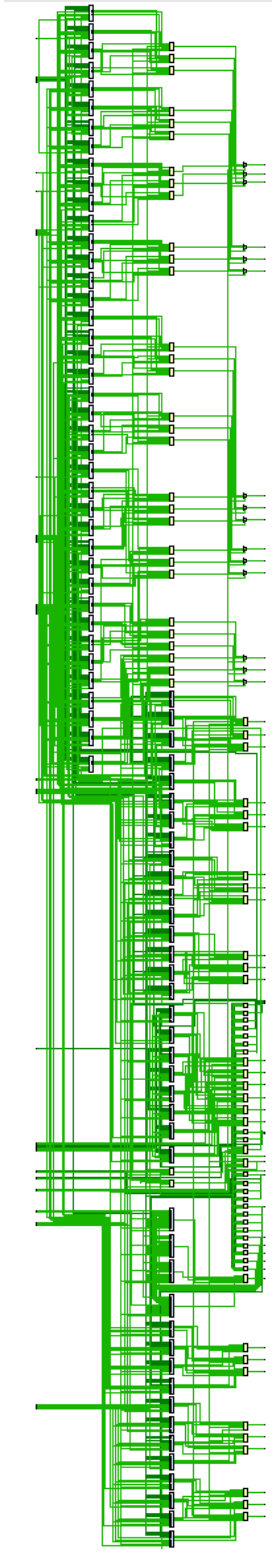
Graphs and Tables:
Implementation Fails due to IO issues

Framebuffer

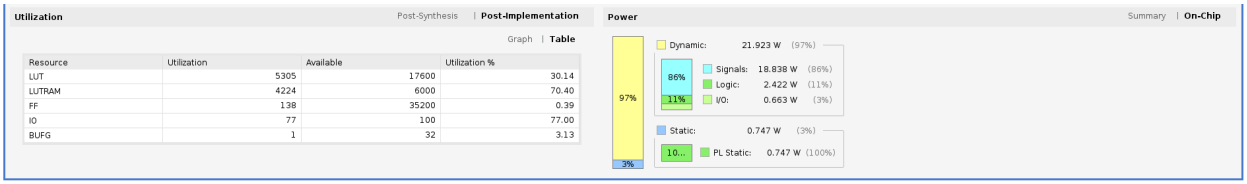
Elaborate



Synthesis

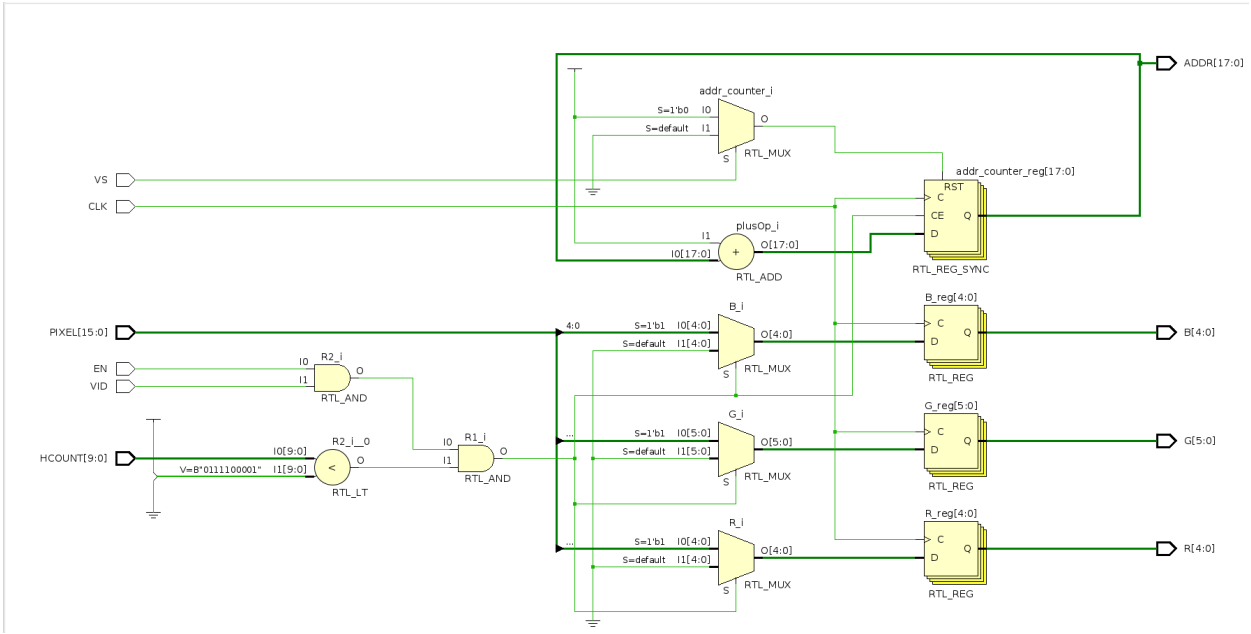


Graphs & Tables

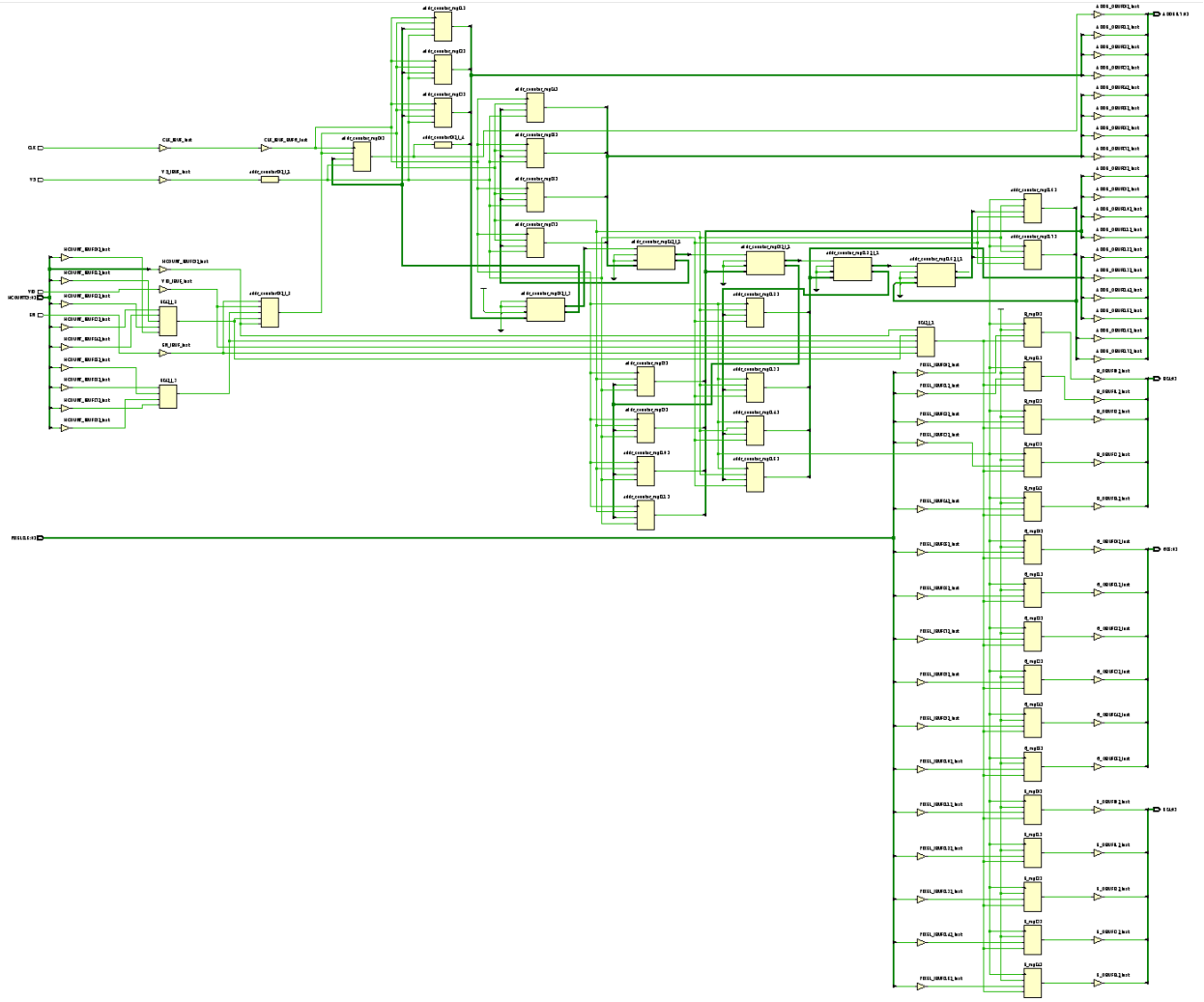


Pixel Pusher

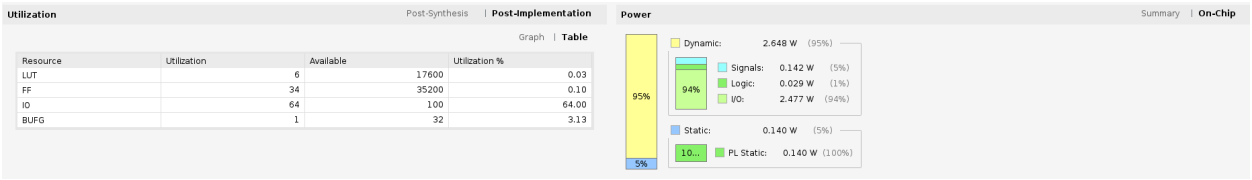
RTL



Synthesis



Graphs and Table



Utilization — Post-Synthesis | **Post-Implementation** — Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	6	17600	0.03
FF	34	35200	0.10
IO	64	100	64.00
BUFG	1	32	3.13

Power — Summary | **On-Chip**

95% / 5%

Dynamic: 2.648 W (95%)

94%

Signals: 0.142 W (5%)

Logic: 0.029 W (1%)

I/O: 2.477 W (94%)

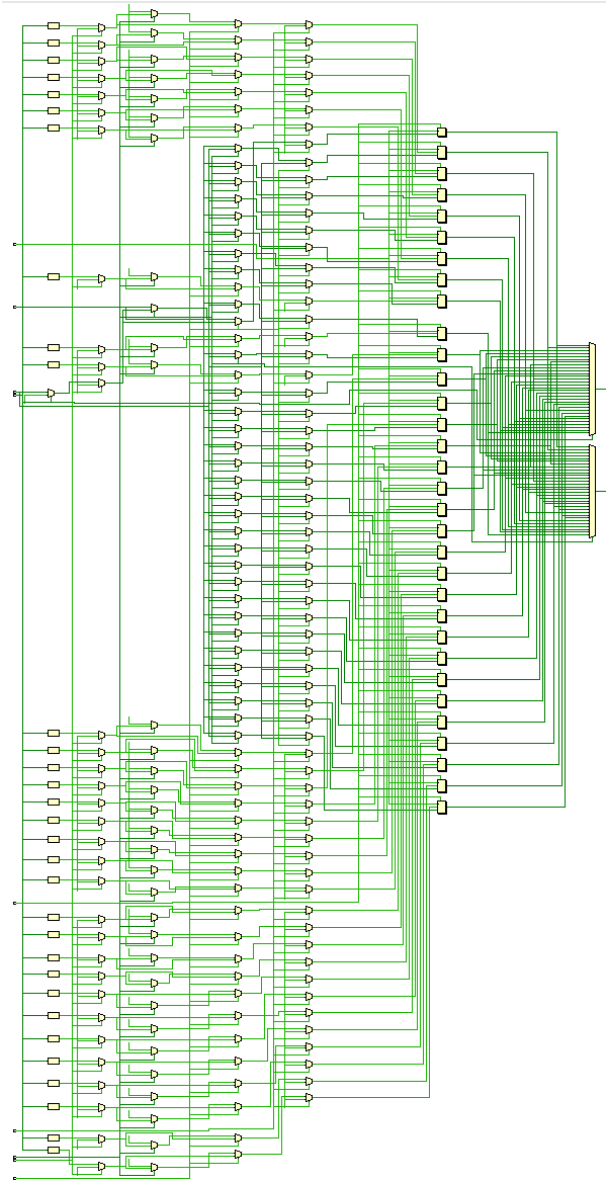
Static: 0.140 W (5%)

10...

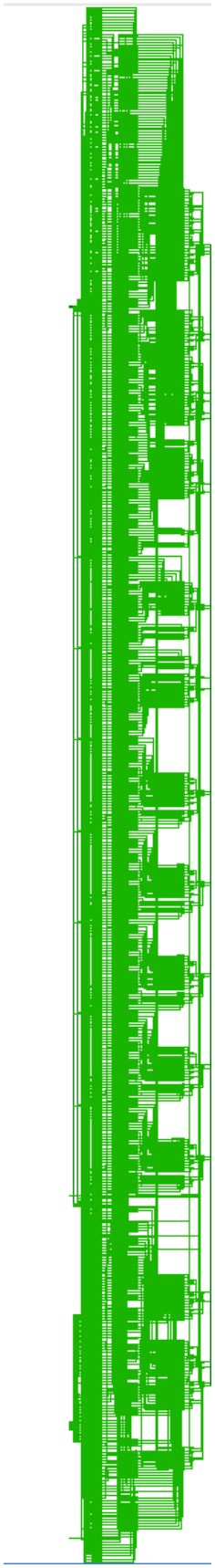
PL Static: 0.140 W (100%)

Regs

RTL



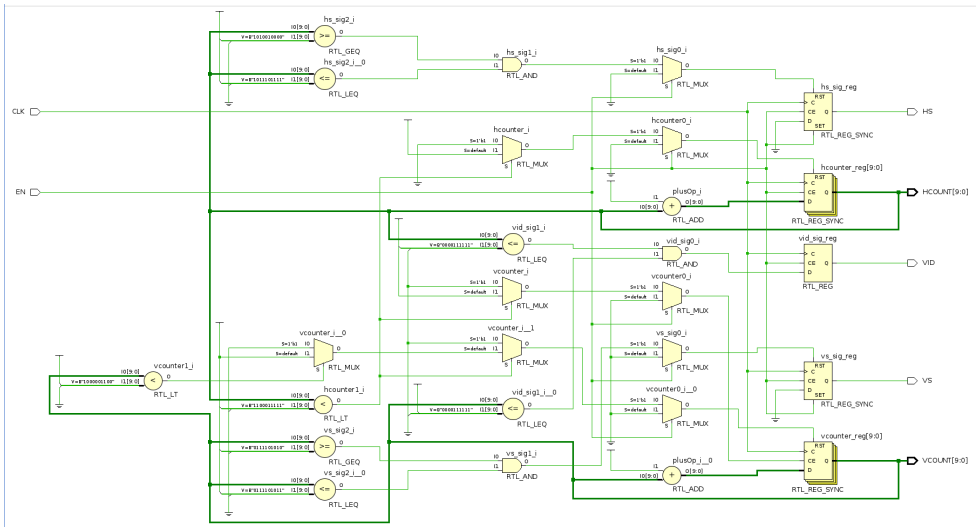
Synthesis



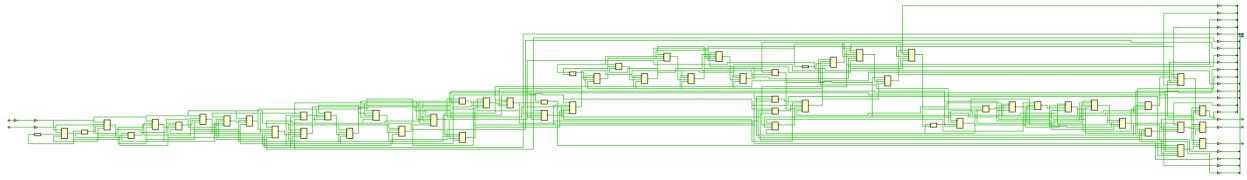
Graphs and Tables
Failed to standalone implement.

VGA CTRL

RTL



Synthesis



Graphs and Table