Course Name: EMBEDDED SYSTEMS I / III

Course Number and Section: **14:332:493:03 / 16:332:579:05**

Year: Spring 2024

Lab Report #: 4

Lab Instructor: Milton Diaz

Student Name and RUID: Ruben Alias 207005068

Date Submitted: 04/05/2024

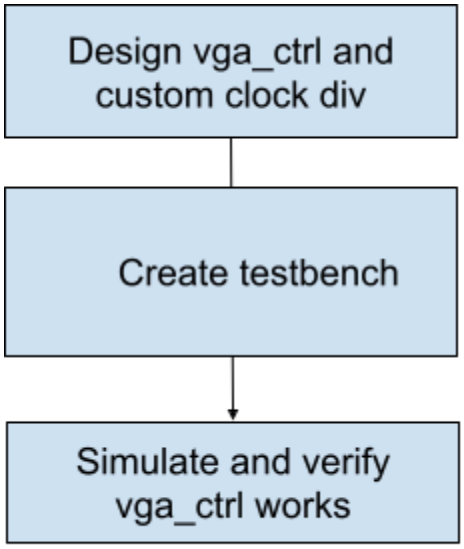
GitHub Link:

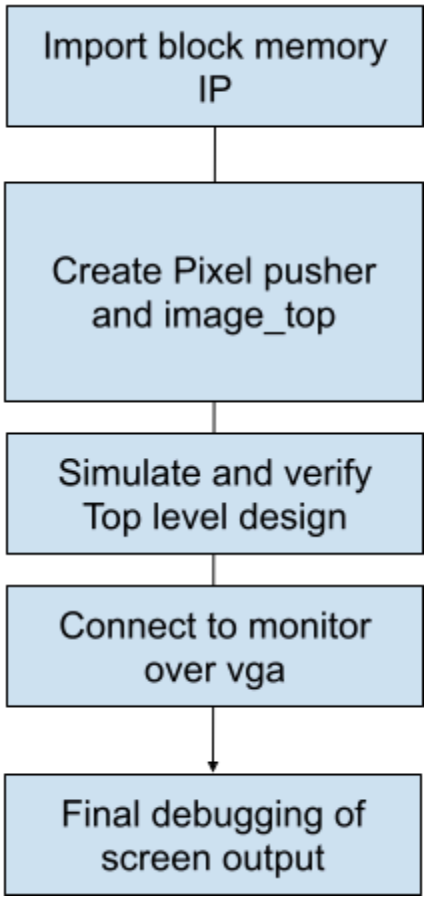
https://github.com/embedded-systems-1-spring-2024-labs/lab-4-Herxity

Purpose/Objective:

The purpose of this lab is to learn to use the VGA protocol in VHDL in order to display an image on a monitor from a Zybo. This lab further enforced the importance of timing when dealing with more complex designs which interface with the outside world.

Theory of Operation:

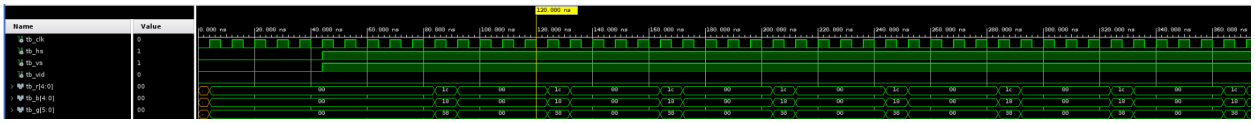




Simulation Waveforms:

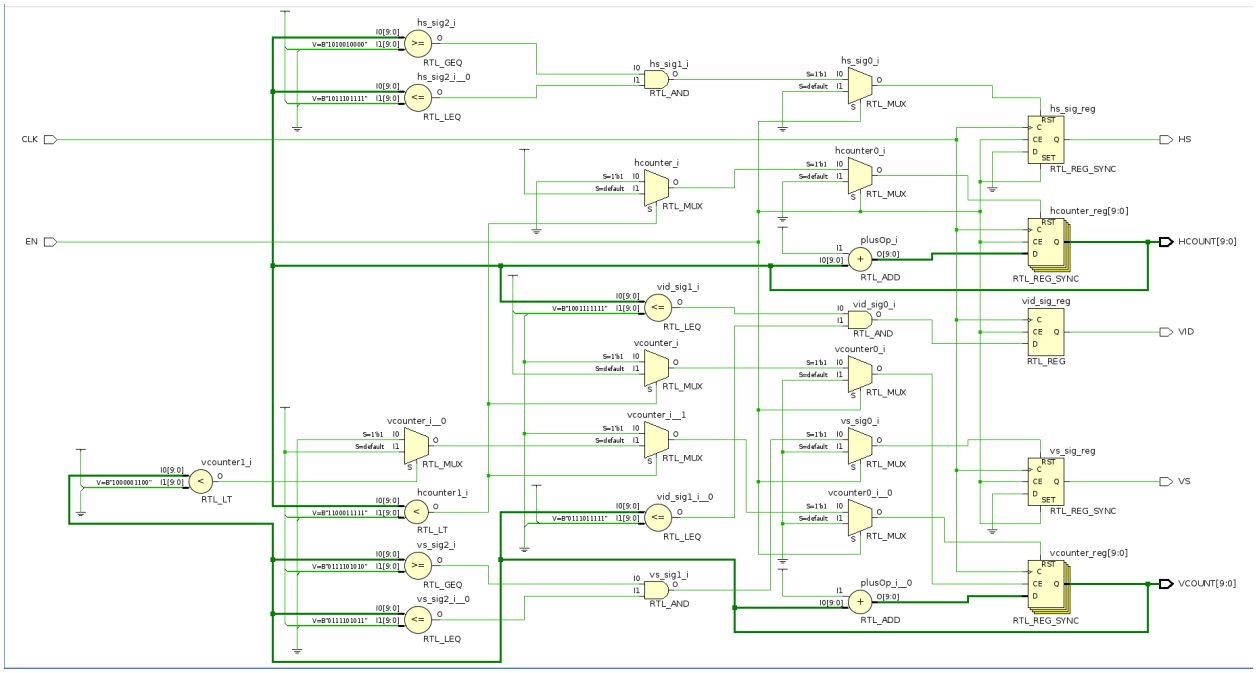
VGA_CTRL_TB

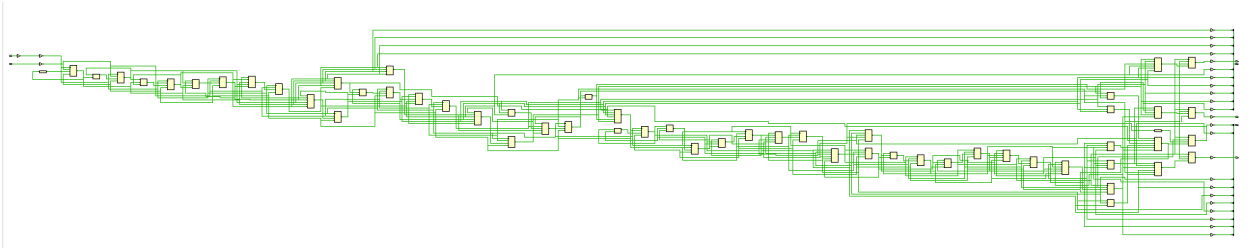
IMAGE_TOP_TB



Vivado Schematics, Power Diagrams, and Utilization:

VGA_CTRL

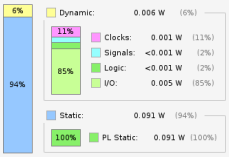




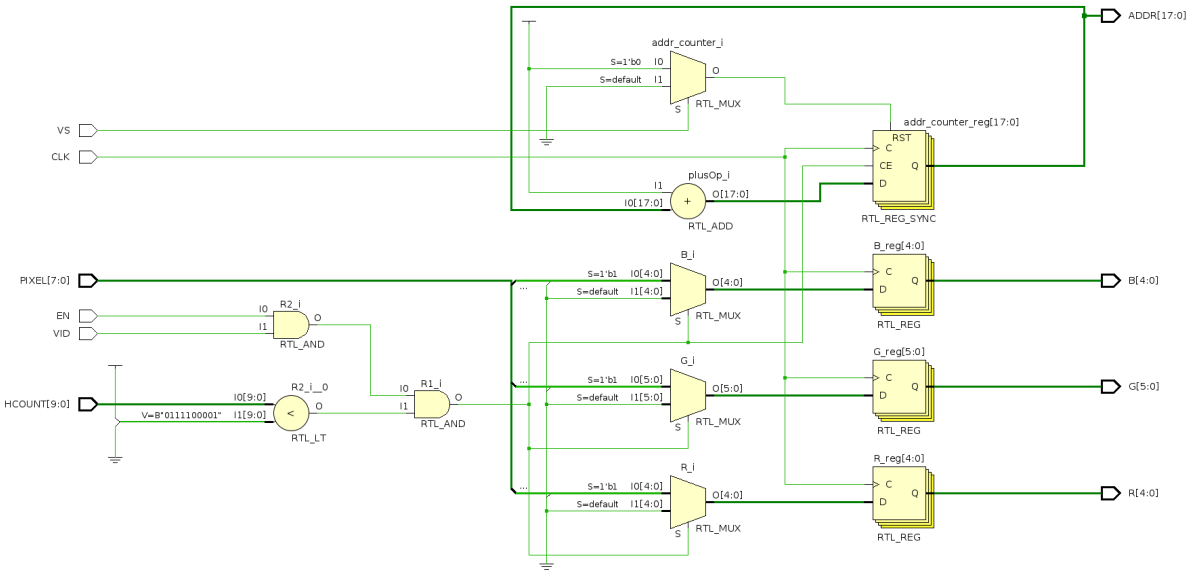
Utilization — Post-Synthesis | Post-Implementation — Graph | Table

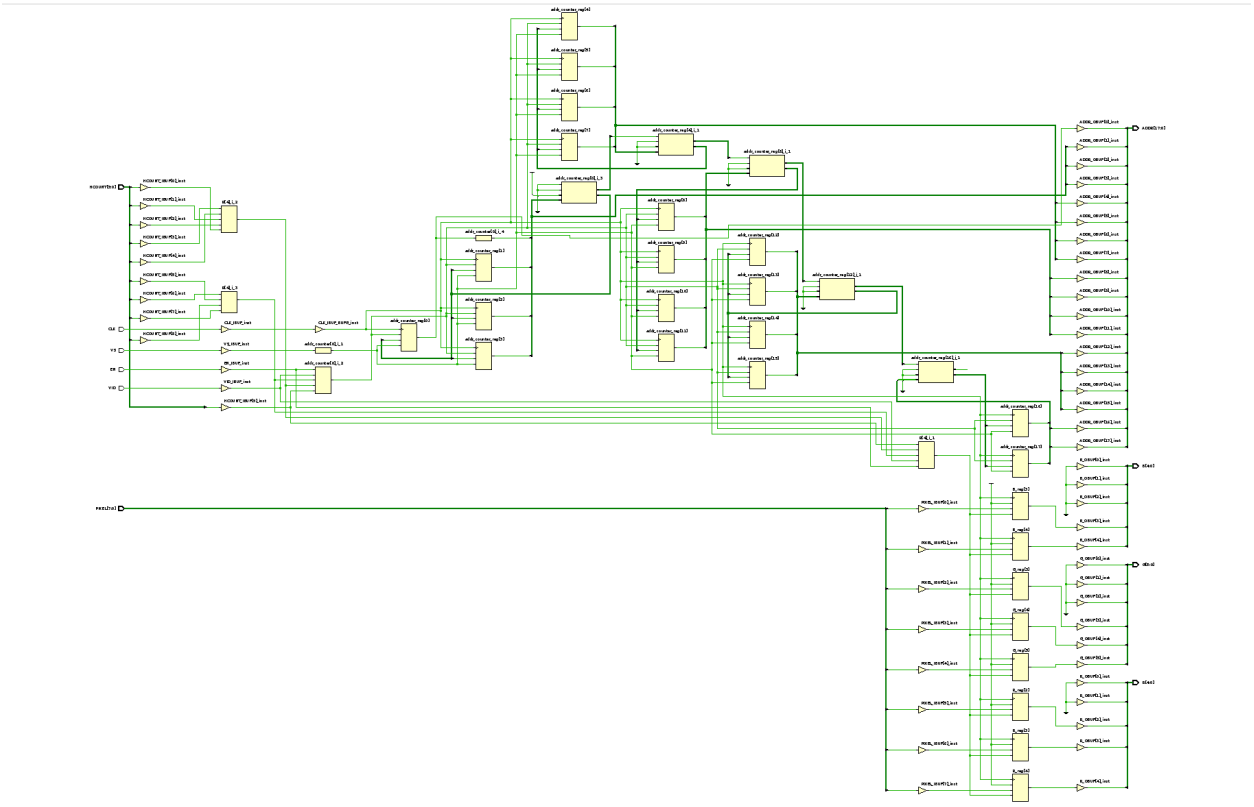
Resource	Estimation	Available	Utilization %
LUT	24	17600	0.14
FF	23	35200	0.07
IO	25	100	25.00
BUFG	1	32	3.13

Power — Summary | On-Chip



Pixel_Pusher



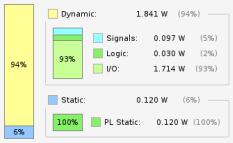


Utilization — Post-Synthesis | **Post-Implementation**

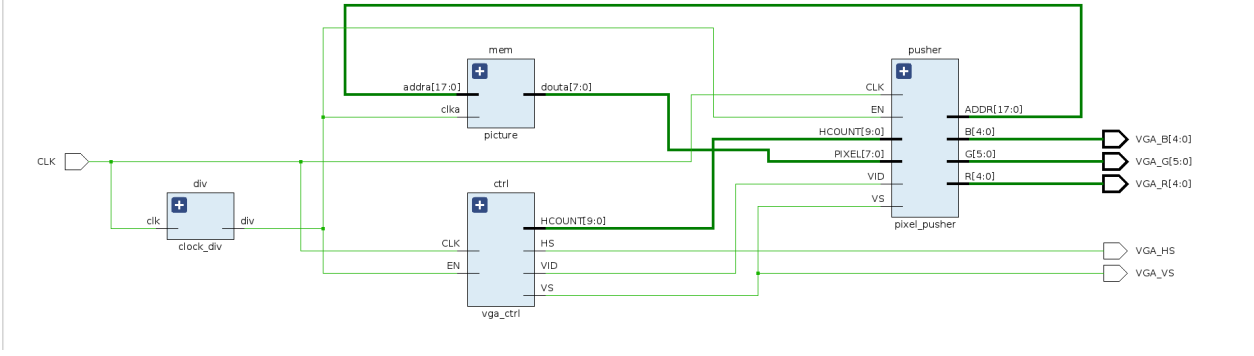
Graph | **Table**

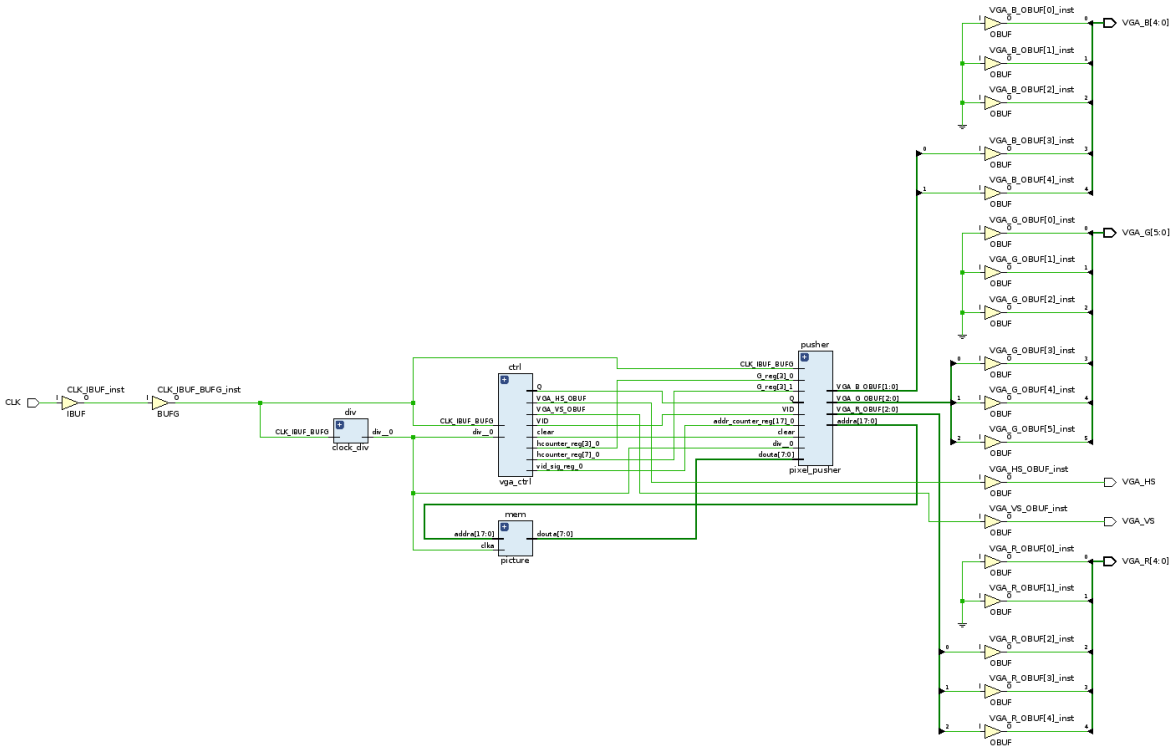
Resource	Utilization	Available	Utilization %
LUT	6	17600	0.03
FF	26	35200	0.07
IO	56	100	56.00
BUFG	1	32	3.13

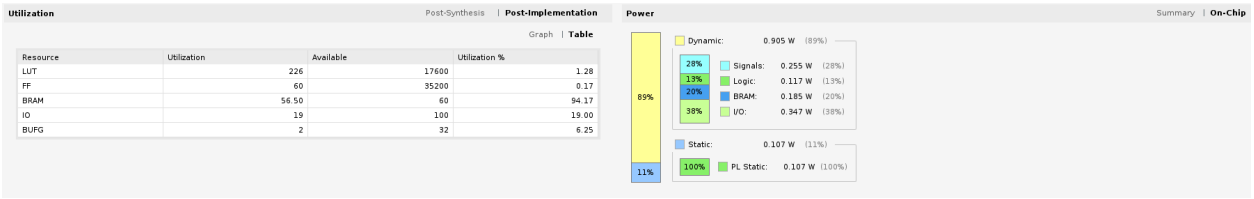
Power — Summary | **On-Chip**



IMAGE_TOP







Answers to Additional Questions and Extra Credit:

NONE

Conclusion

In this lab I learned how to implement the VGA Protocol. I noticed an interesting behavior of how the pixel clock and the VGA controller's clock interact when they don't match. It gave very visible consequences to timing issues.

Follow up

I feel like I understand better how timing issues are debugged as well as working with Datasheets since we were asked to read into those for the HDMI portion. I didn't understand how to complete the implementation for HDMI however.