Date:

# EXPERIMENT NO. 5

#### AIM: Implement a common bus system with ALU, 8 registers and 1 memory unit

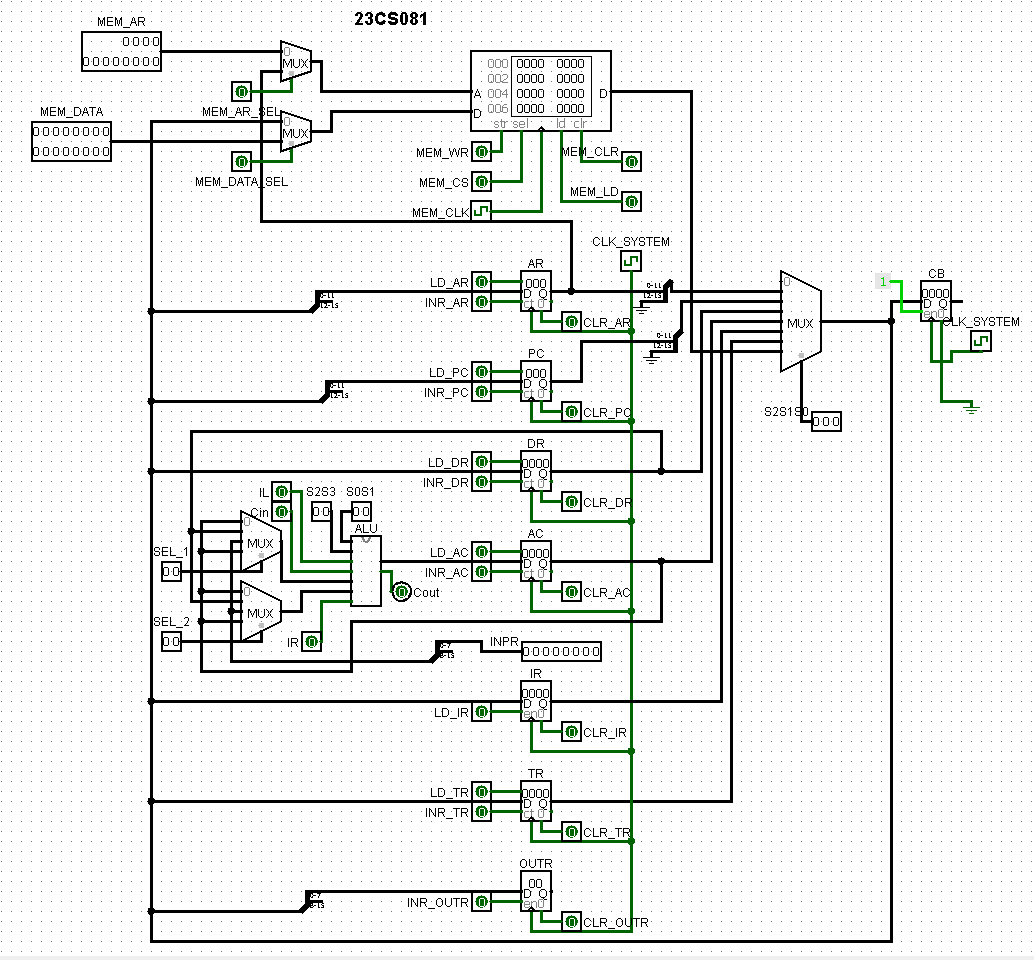
#### with necessary control signals.

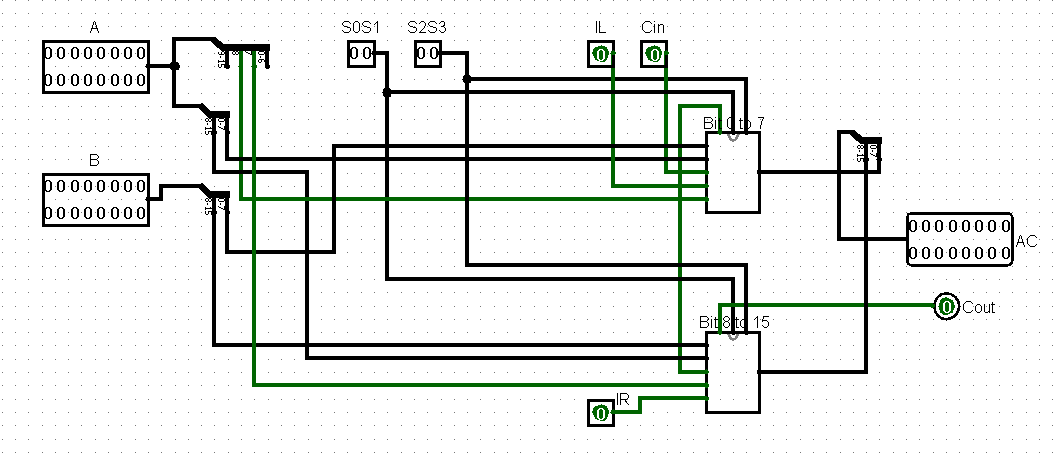
#### OBJECTIVES:

#### Implement 16-bit ALU that is suitable for common bus system

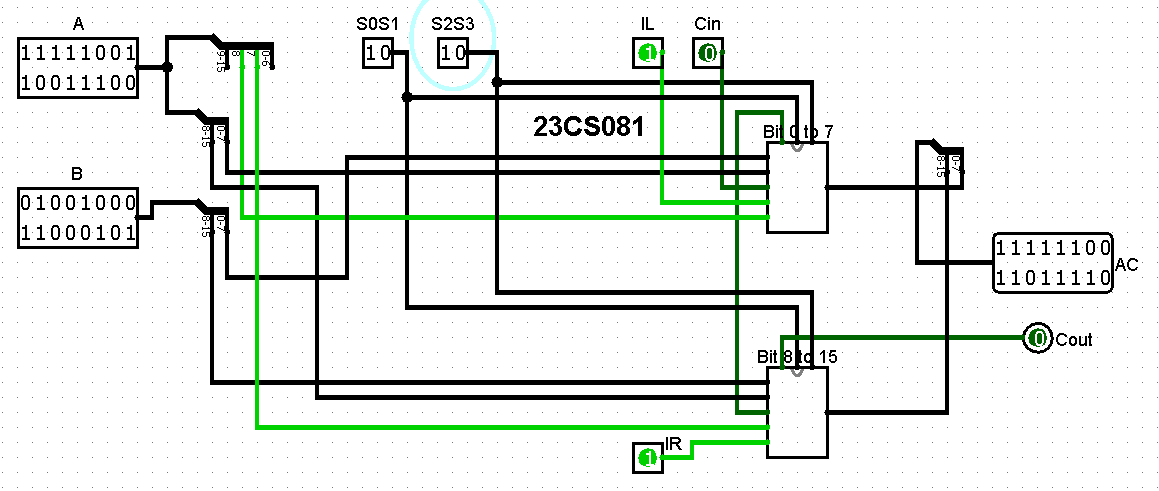
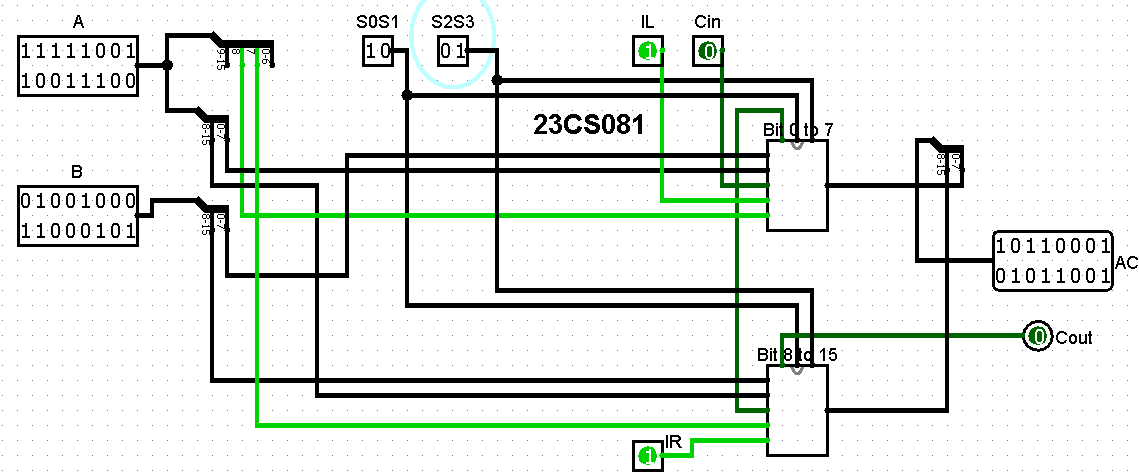
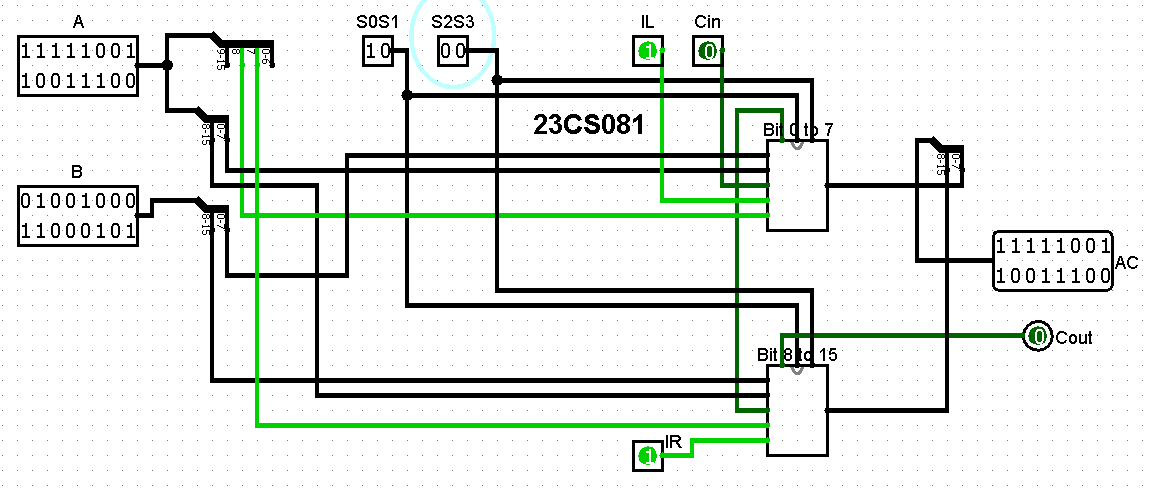
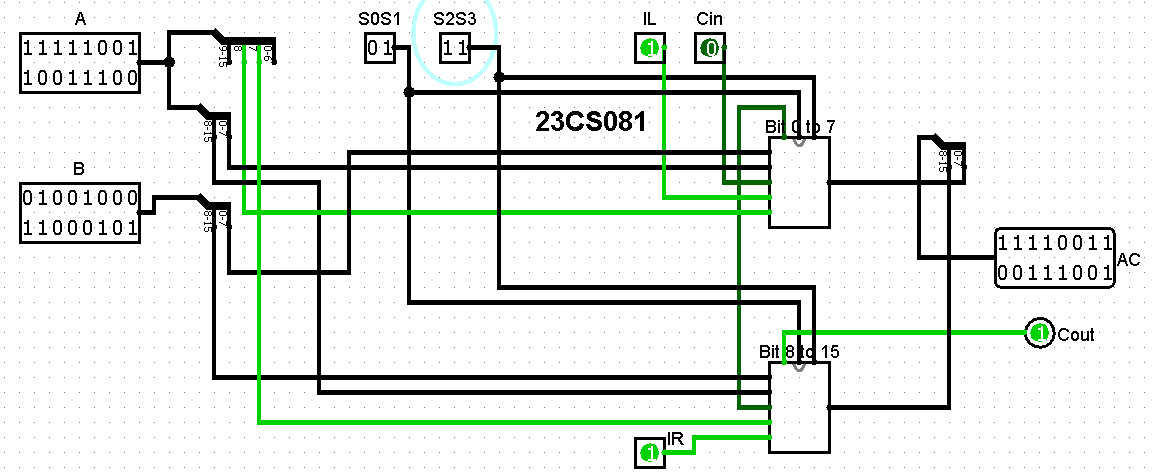
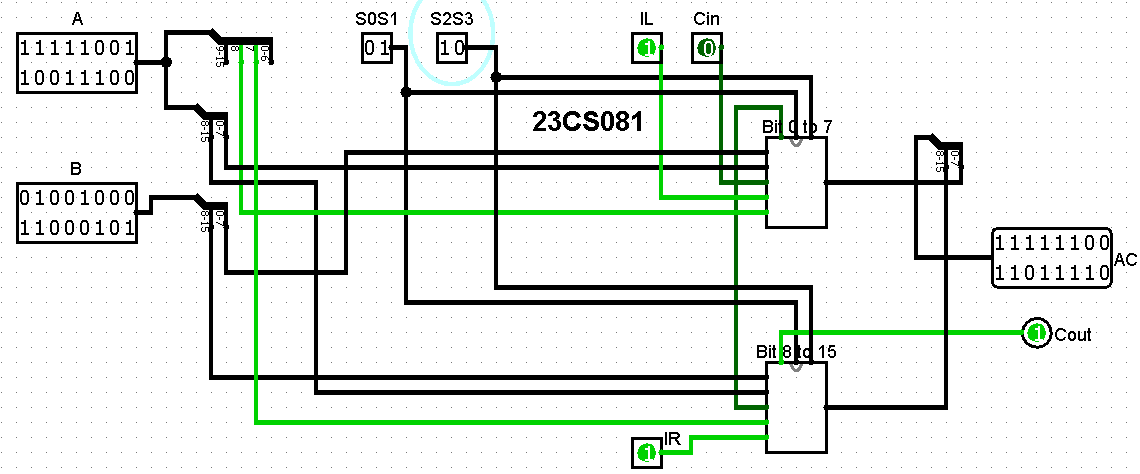
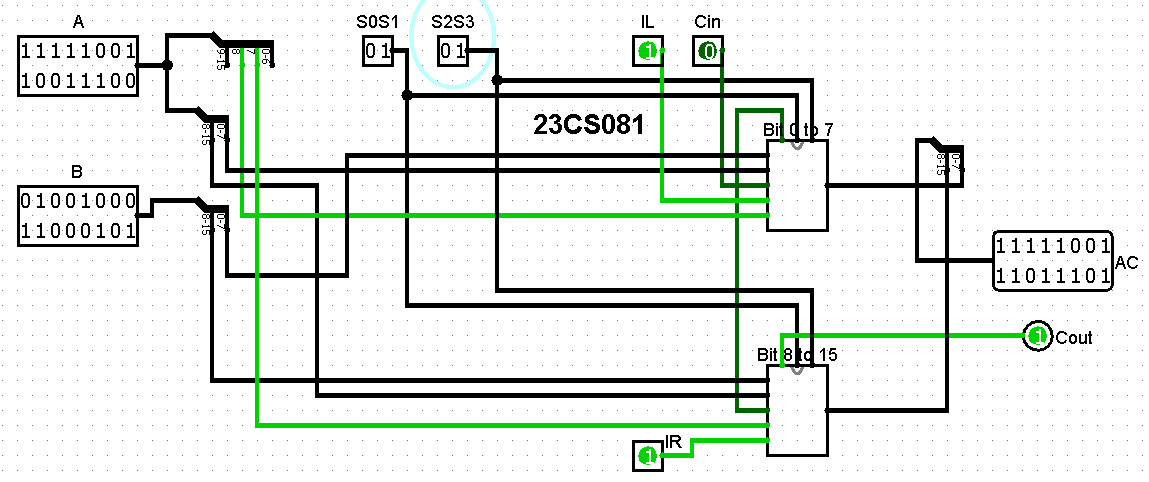
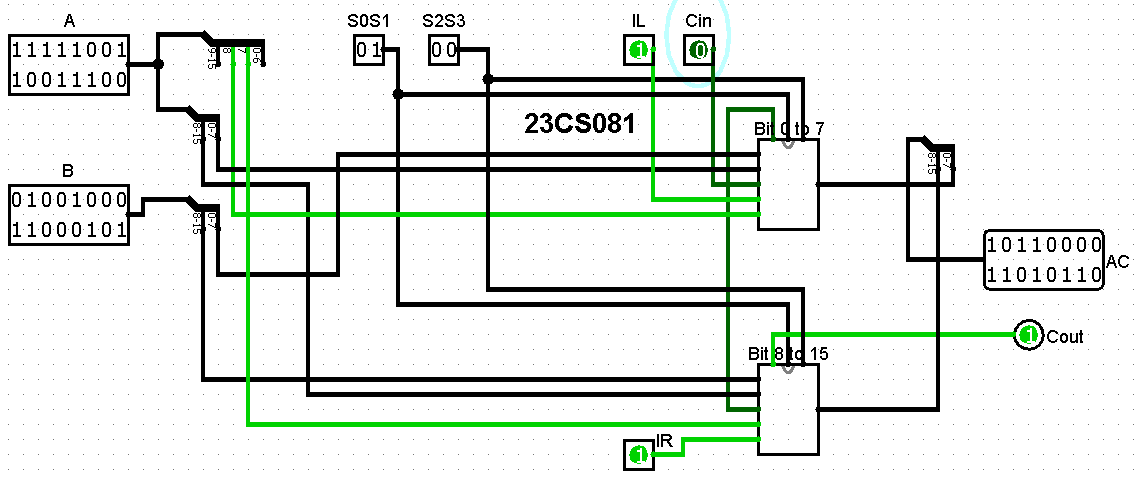
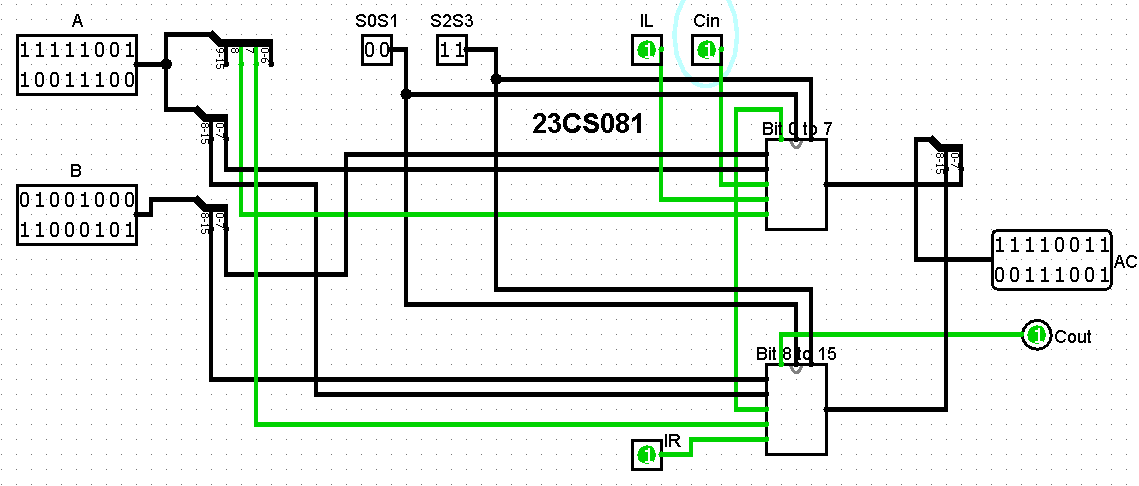
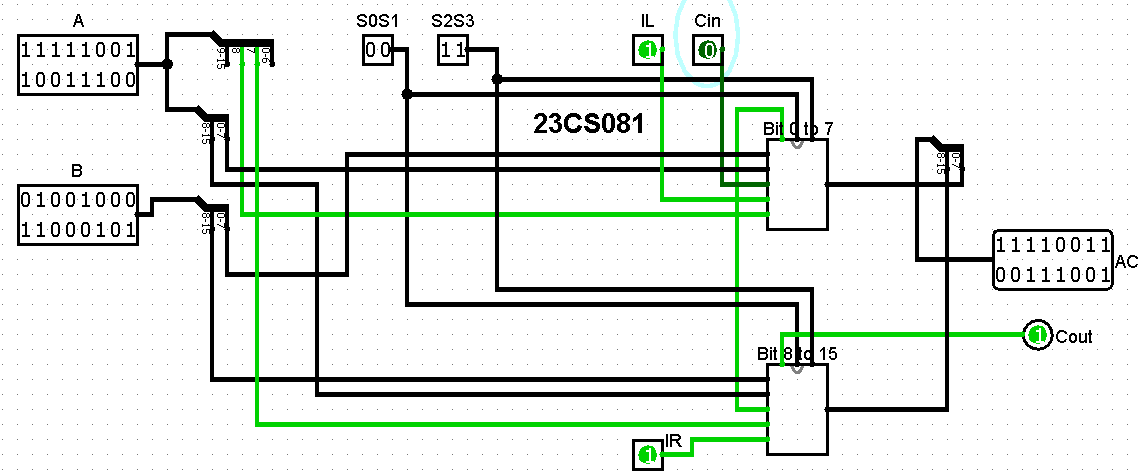
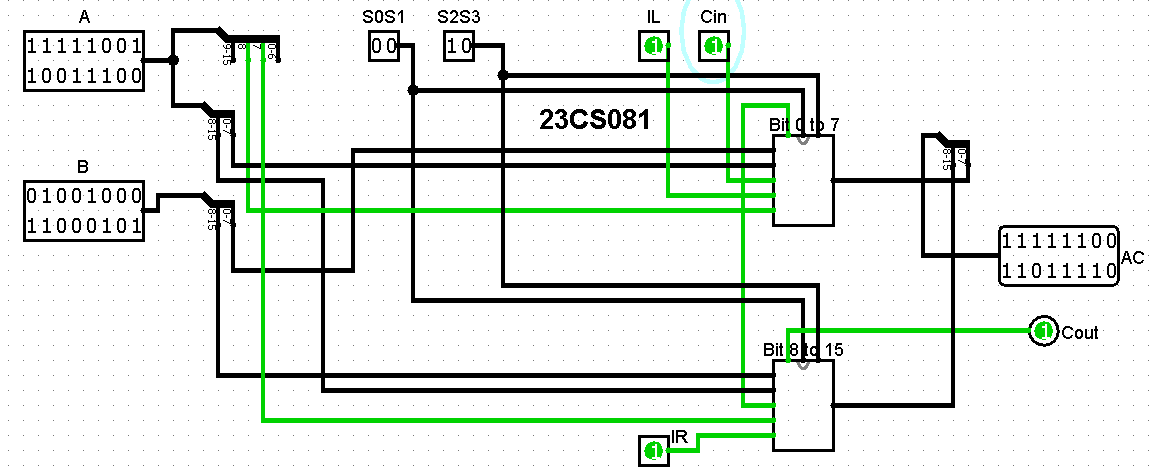
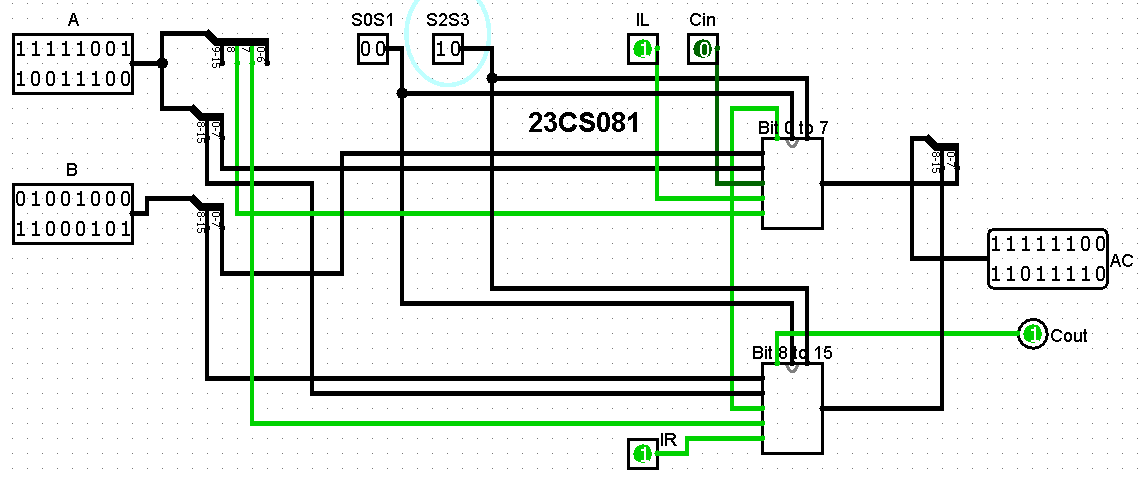
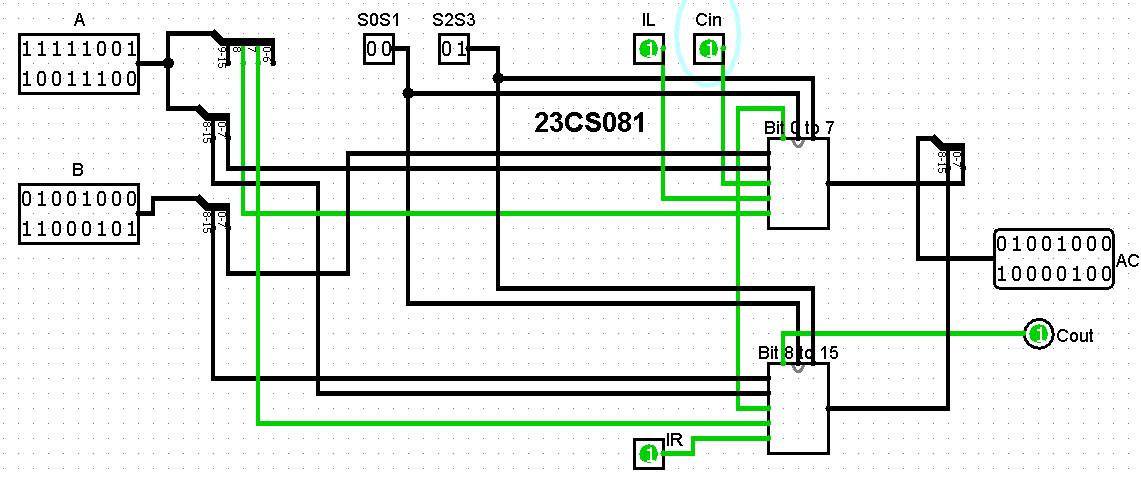
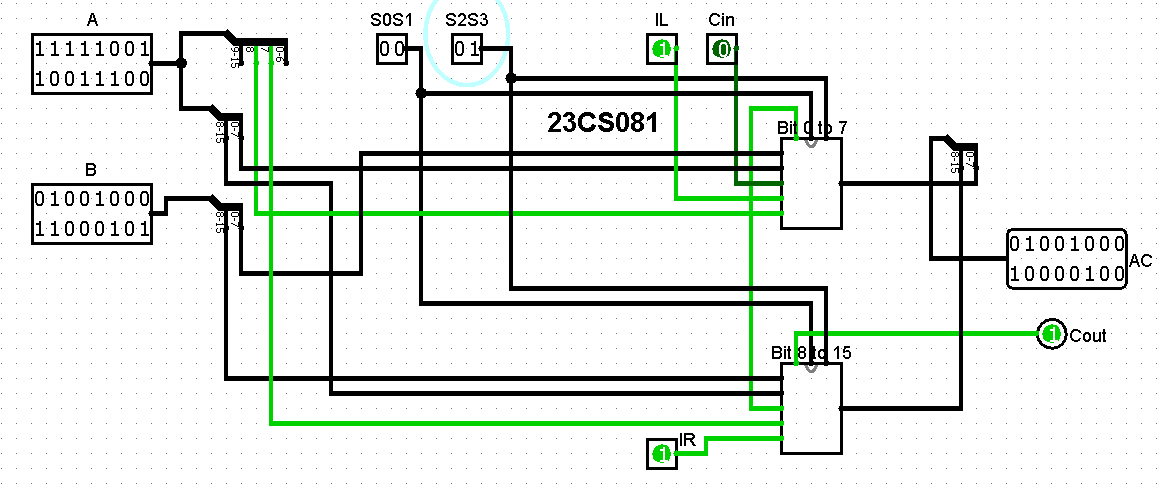
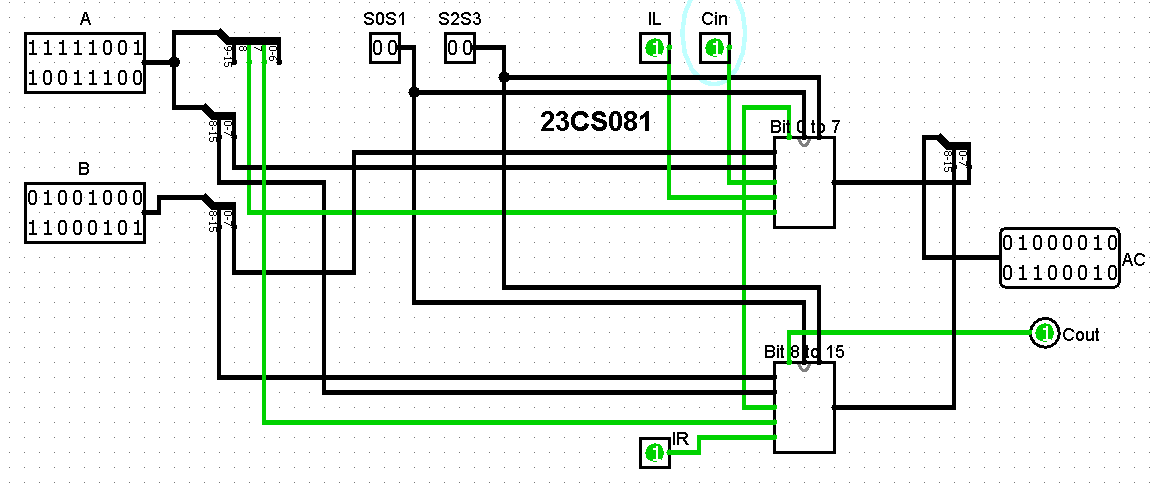
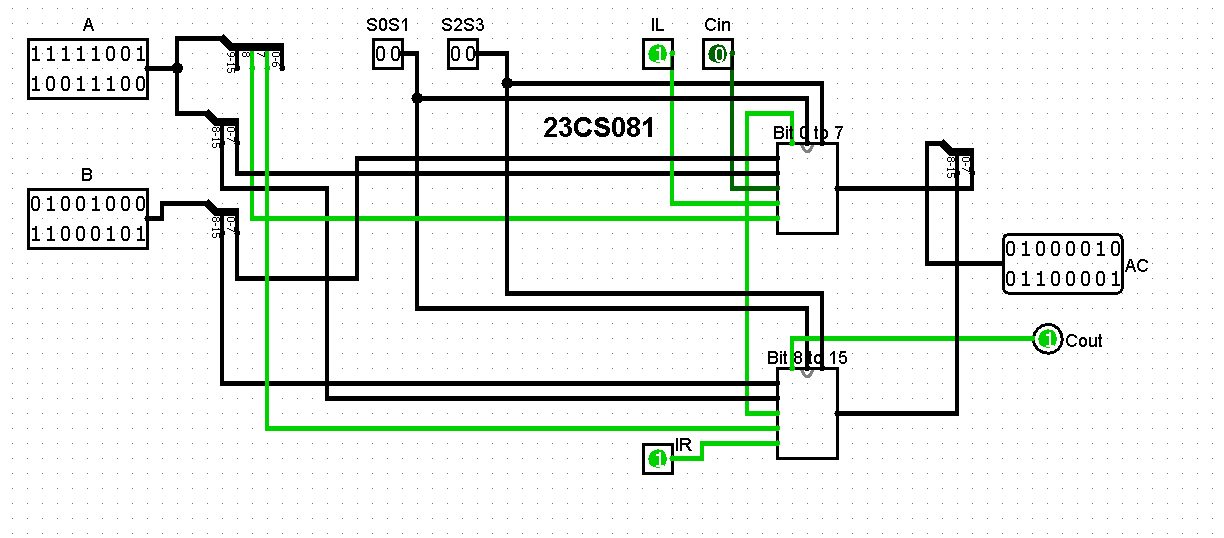
#### Implement 16-bit common bus system with ALU, 8 registers and 1 memory unit

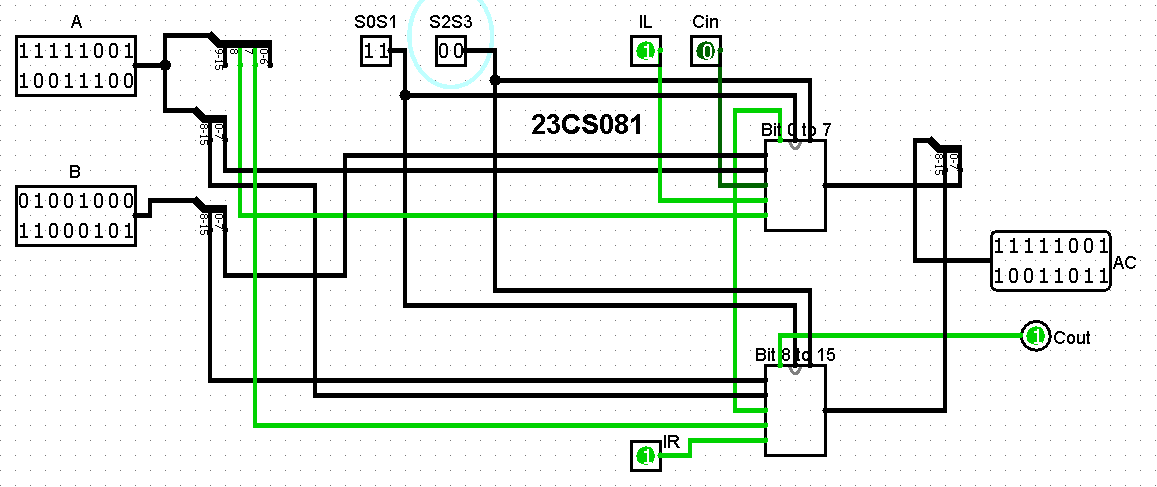
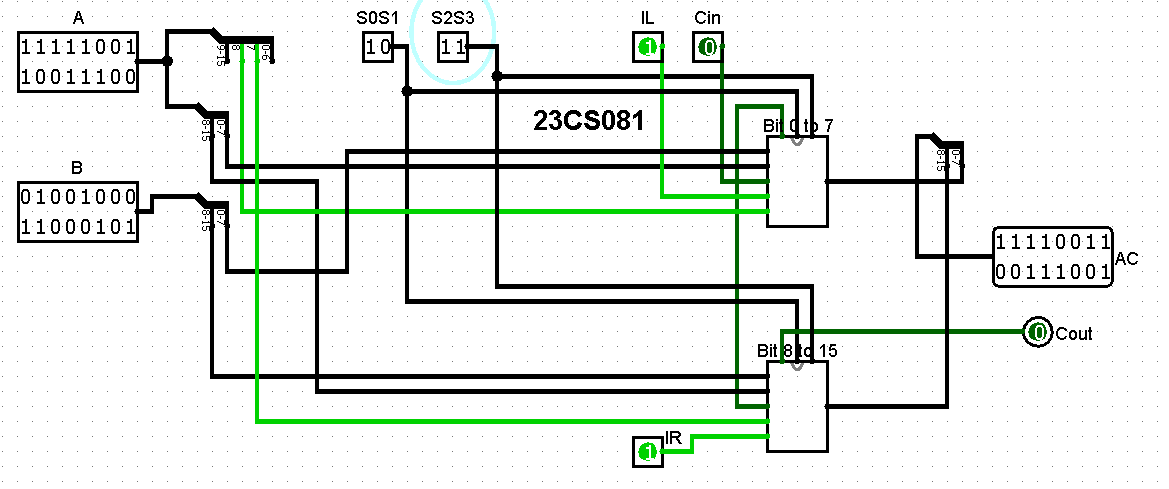
**CIRCUITS:**

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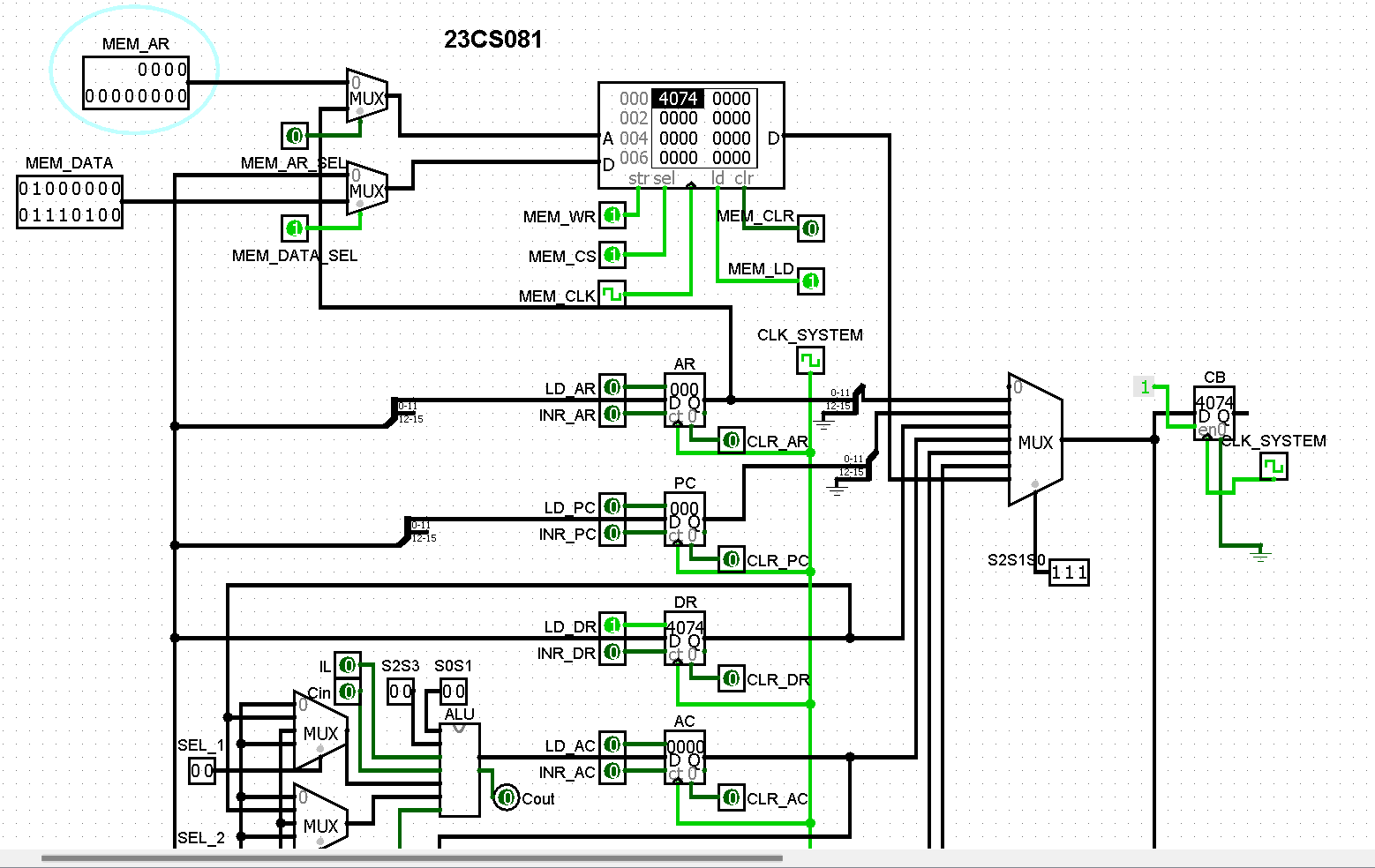
**OUTPUTS:**

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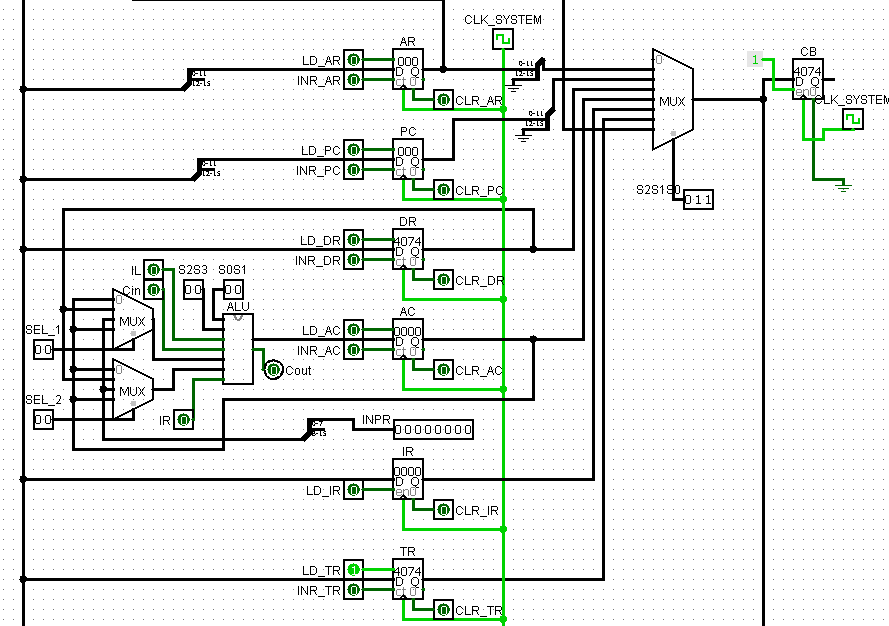
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**Outputs for common bus system:**

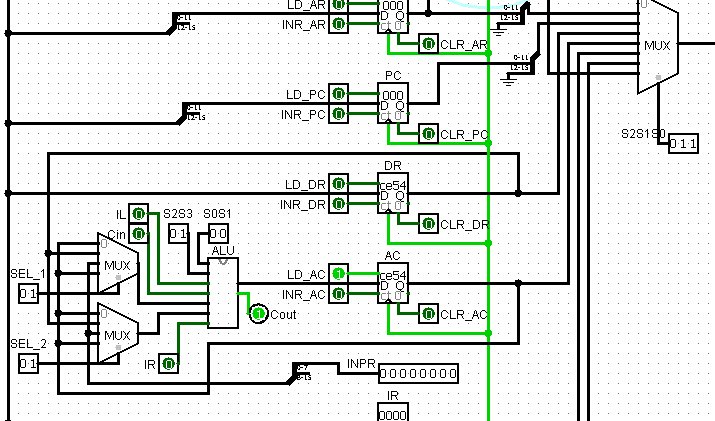
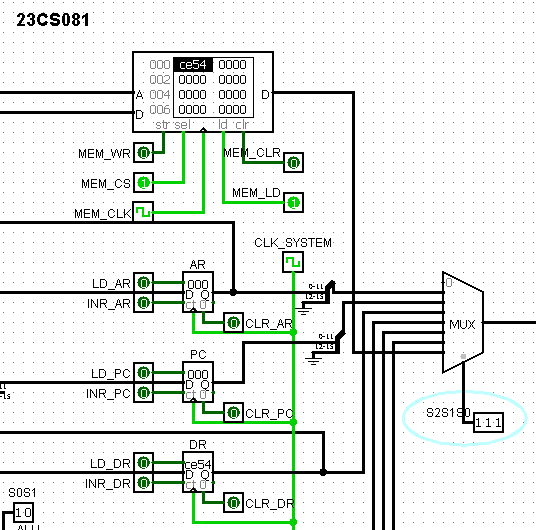
**DR<-MEM[AR]**

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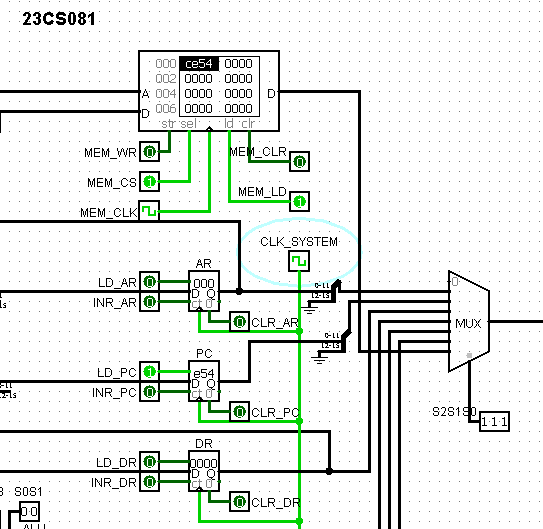
**TR<-DR**

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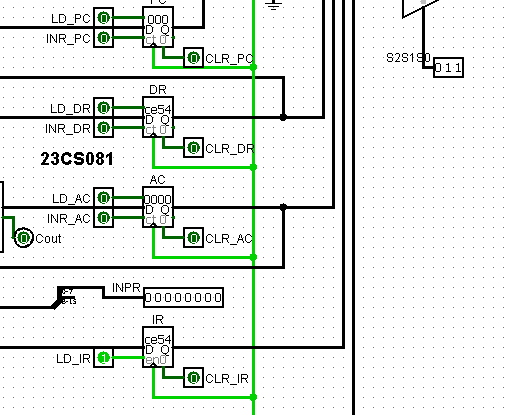
**AC<-DR**

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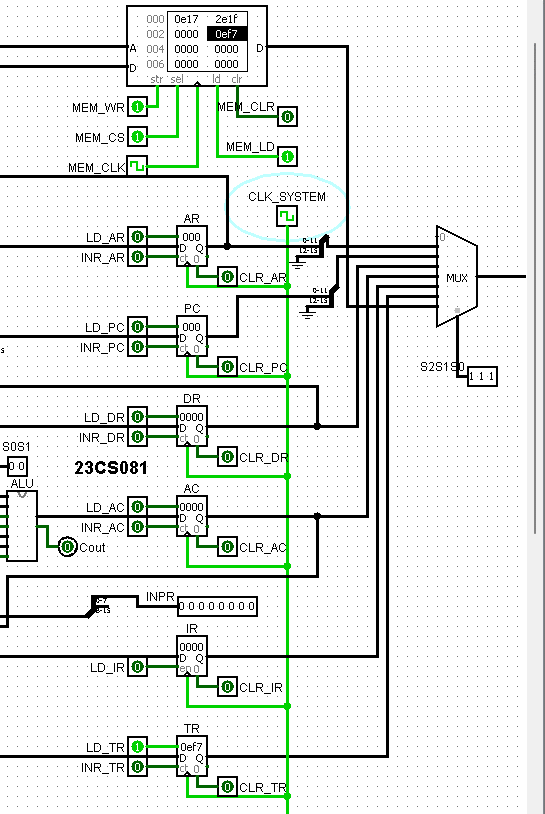
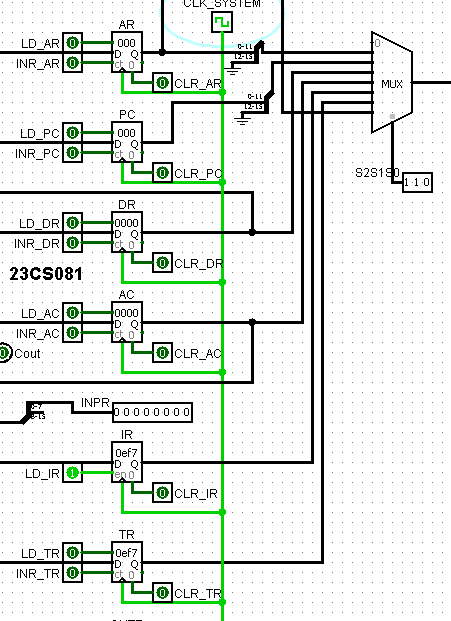
**PC<-MEM[AR]**

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**IR<-DR**

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**IR<-TR**

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**CONCLUSION:**