

## Green sheet ISA Pipeline CPU

### Stall

31:0

00000000000000000000000000000000

### Data register-register

Id				Registers			Null
Type	Op	I		RD	RA	RB	Null
31:30	29:27	26		25:22	21:18	17:14	13:0
ADD	01	000	0	Destino	Operando 1	Operando 2	00000000000000
SUB	01	001	0	Destino	Operando 1	Operando 2	00000000000000
AND	01	010	0	Destino	Operando 1	Operando 2	00000000000000
OR	01	011	0	Destino	Operando 1	Operando 2	00000000000000
MOV	01	100	0	Destino	0000	Operando 2	00000000000000
MOD	01	101	0	Destino	Operando 1	Operando 2	00000000000000
EXP	01	110	0	Destino	Operando 1	Operando 2	00000000000000
CMP	01	111	0	0000	Operando 1	Operando 2	00000000000000

### Data register-immediate

Id				Registers			
Tipo	Op	I		RD	RA	Immediate	
31:30	29:27	26		25:22	21:18	17:0	
ADDI	01	000	1	Destino	Operando 1	Imm = Operando 2	
SUBI	01	001	1	Destino	Operando 1	Imm = Operando 2	
ANDI	01	010	1	Destino	Operando 1	Imm = Operando 2	
ORI	01	011	1	Destino	Operando 1	Imm = Operando 2	
MOV	01	100	1	Destino	0000	Imm = Operando 1	
MOD	01	101	1	Destino	Operando 1	Imm = Operando 2	
EXP	01	110	1	Destino	Operando 1	Imm = Operando 2	
CMPI	01	111	1	0000	Operando 1	Imm = Operando 2	

### Memoria

Id				Addressing			
Type	Op	Null		RD	RA	Immediate	
31:30	29	28:26		25:22	21:18	17:0	
LDR	10	0	000	RD = MEM[RA + IMM]	RA = Mem dir	Imm = offset	
STR	10	1	000	MEM[RA + Imm] = RD	RA = Mem dir	Imm = offset	

### Control

Id				Null	Instruction number		
Type	Op	Null		Null	Immediate		
31:30	29:28	27:26		25:18	17:0		
JMP	11	00	00	00000000			
JEQ	11	01	00	00000000			
JNE	11	10	00	00000000			