ECE 564
Digital ASIC and FPGA Design
Project Demonstration

Please follow the following instructions for the project demonstration:-

- Log in to the linux machine.
- In the Home directory, create a folder called 564_Project_Demo.
- Wait for a TA to come to you before you proceed further.
- Download the following files from moodle.
    - Submitted project- place in the directory created above.
    - Constraints.tcl and CompileAnalyze.tcl files provided for the demo.- replace your files with these files for the purpose of demo.
    - Updated Testbench. - replace your testbench with this.

NOTE: If caught using any other version of the project or working in any other directory, the project grade will be given as 0.

NO CHANGES can be made to the downloaded project.

- In the presence of a TA, simulate your MyDesign.v. Show results for given test cases after which you will be asked to simulate the DUT for a different set of test cases.
- Once finished with simulation, and after the TA has completed logging that required data, move forward to synthesizing the design.
- Change clock period to 50 in setup.tcl and synthesize the design using the following commands. (This step is to check for warnings and errors in design)
    - source setup.tcl
    - source read.tcl > read_synth.txt
    - source Constraints.tcl > Constraints_synth.txt
    - source CompileAnalyze.tcl > CompileAnalyze_synth.txt
- After all the required data are recorded by a TA, logout of the terminal and you're done!