A Broadband High-Efficiency RF Rectifier for Ambient RF Energy Harvesting

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***Abstract*—In this letter, a compact broadband high-efficiency RF rectifier is presented for ambient RF energy harvesting (EH). A novel impedance matching network with an additional quarter-wavelength short-circuited stub was designed to achieve broadband impedance matching. After the branch was added, the parallel resonance point on track S_{11} did not move, and the remaining points were compressed. The measurement results show that the proposed topology could realize a broadband high-efficiency rectifier for ambient RF EH, and the measured results were basically consistent with the simulation results. The measured efficiency is as high as 71.5% for an input power level of 8 dBm. A 1–2.4 GHz wide frequency band with an efficiency above 50% is achieved for an input power level of 5 dBm with a terminal load of 1.6 kΩ. Moreover, the circuit had wide dynamic input power characteristics, whose measured values remained above 50% with an input power of 3–14 dBm.**

***Index Terms*—Ambient RF energy harvesting (EH), broadband, high efficiency, parallel resonance, wide dynamic input power.**

I. Introduction

WIRELESS power transmission (WPT) and energy harvesting (EH) are two popular topics in microwave research. WPT is mainly used for high-power long-distance efficient power transmission, while EH mainly focuses on low-power ambient RF EH. With the development of Internet of Things technology, ambient RF EH can provide energy for low-power devices to avoid the use of batteries. From an RF survey, digital television (DTV), GSM900, GSM1800, 3G, and Wi-Fi were identified as potentially useful ambient RF EH sources [1].

The design of a rectifying circuit should consider such factors as the low input power level and more frequency distribution. Low-power rectifiers have been studied in different literature [2]–[6]. Due to the nonlinear characteristics of the diode, the input impedance varies with the frequency, input power, and dc load. Therefore, the design of multiband and broadband rectifiers is very challenging. Until now, only few studies have been reported on multiband [7]–[10] and broadband rectifier circuits. A wideband rectifier operating at 0.57–0.90 GHz with an input power of 12.8 dBm is implemented by the three steps illustrated in [11]. A high-efficiency rectifier with a one octave bandwidth is proposed by using a diode array with a frequency selective topology [12]. In [13], a rectifier based on a coplanar waveguide transmission line was proposed. Its efficiency frequency range is 0.1–2.5 GHz and the efficiency can exceed 45% at 10-dBm input power. A novel rectifier based on a branch-line coupler was proposed [14] to operate within a wide range of input powers, operating frequencies, and output loads. The measured efficiency remains over 70% with an operating frequency of 2.08–2.58 GHz. A matching network based on nonuniform transmission lines was used to achieve greater bandwidth in [15], which has a measured efficiency above 5% from 470 to 990 MHz at −20 dBm input power. However, this matching method has the disadvantages of large physical size. A matching circuit based on two L-section stages is proposed in [16] for impedance matching. The conversion efficiency from 870 MHz to 2.5 GHz is over 30% at 0-dBm input power. The conversion efficiency from 870 MHz to 2.5 GHz is over 30% at 0-dBm input power. A broadband rectifier with a wide dynamic range of input power is designed using three segments of microstrip lines as impedance matching network; the proposed rectifier shows a bandwidth of 44.4% for an efficiency over 70% at an input power of 14 dBm [17].

In this letter, a novel broadband rectifier using a quarter-wavelength short-circuited stub as a parallel resonant compression topology is proposed to achieve broadband impedance matching for EH. To minimize the size of the rectifier, the microstrip line is bent to make the structure more compact. A rectifier retaining an operating bandwidth of 1–2.4 GHz with an efficiency above 50% is achieved for an input power level of 5 dBm.

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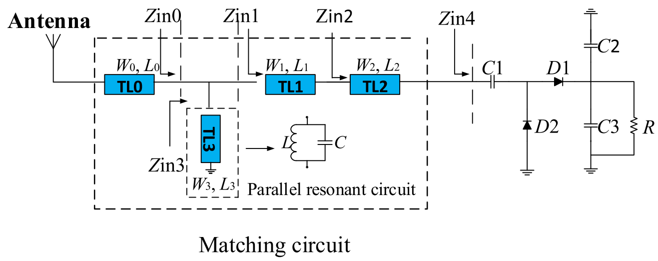


Fig. 1. Topology of the proposed rectifier with the parts of the microstrip.

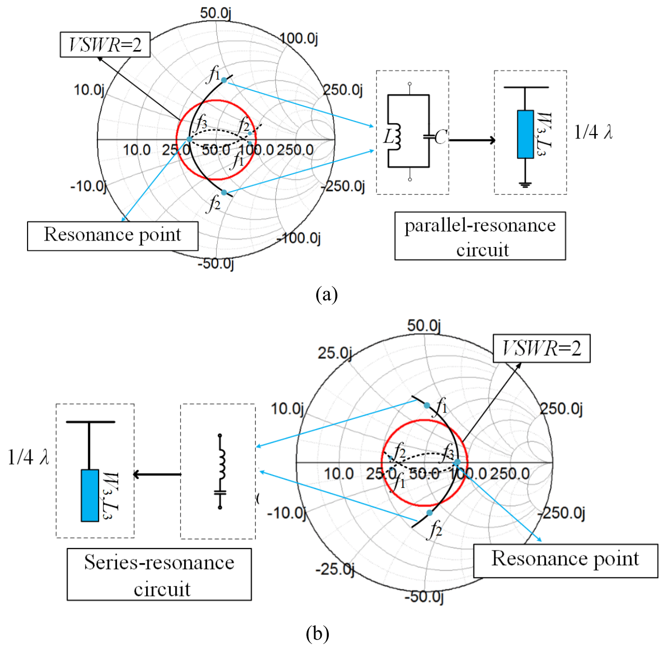


Fig. 2. Two different resonant compression methods. (a) Parallel resonance compression method. (b) Series resonance compression method.

II. Broadband Rectifier Design

For low power, a diode series form can achieve the highest rectifier efficiency, but the output voltage is not high. To increase the output voltage, we select the single-stage voltage double configuration [18]. A series pair of Schottky diodes (SMS7630-005LF) is suitable for low-power RF EH in this work [19]. Fig. 1 shows the topology of the proposed rectifier with the parts of the microstrip. It consists of three main parts: a broadband-matching network, a single-stage Schottky diode, and a dc pass filter.

A. Principle Analysis

Broadband matching requires moving or compressing the entire S_{11} track in the required frequency band into a circle, where the VSWR is equal to 2. For different S_{11} trajectories, there are two different compression methods, as shown in Fig. 2. The resonance points on the track are fixed and the remaining points move to compress the curve.

When track S_{11} is located in Fig. 2(a), as the parallel inductance has little influence on the high-frequency part, and the parallel capacitance has little influence on the low-frequency part, the high-frequency part of the S_{11} curve compresses downward, and the low-frequency part drags upward. Finally, the entire curve is compressed in the circle of VSWR $= 2$. When track S_{11} is located in Fig. 2(b), as the series inductance

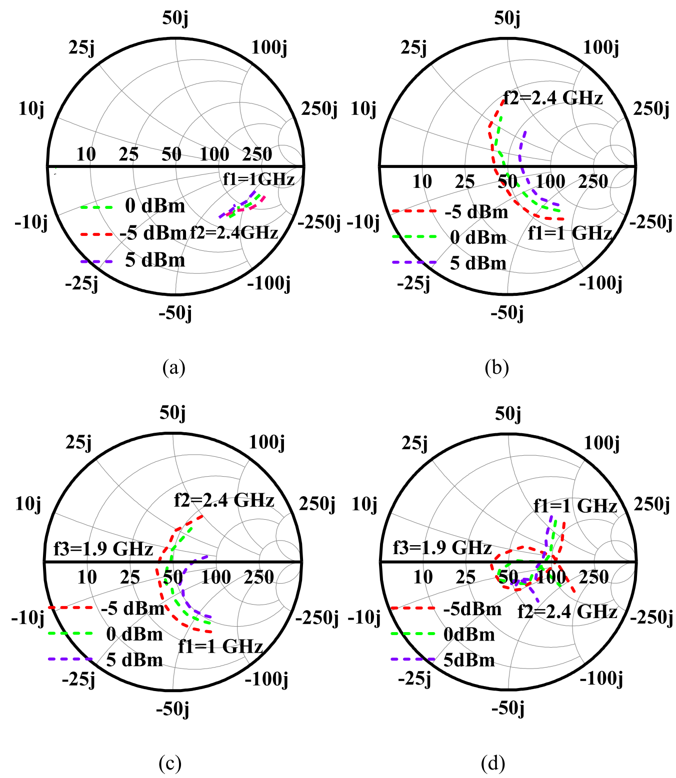
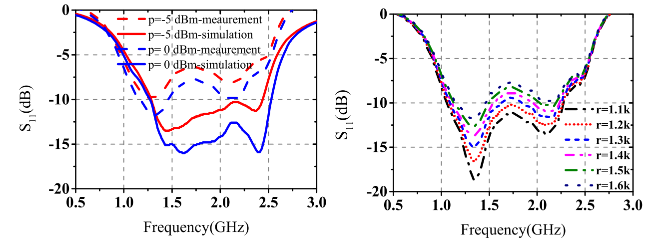


Fig. 3. Trace of S_{11} on the Smith chart. (a) Trace of the S_{11} of the single-voltage circuit. (b) Adding transmission line TL1. (c) Adding transmission line TL2. (d) Adding transmission line TL3 as a parallel resonance circuit. f_3 is the resonance point.

has less influence on the low-frequency part, and the series capacitance has less influence on the high-frequency part, the high-frequency part of curve S_{11} compresses downward, and the low-frequency part drags upward. Finally, the entire curve is compressed in the circle of VSWR $= 2$.

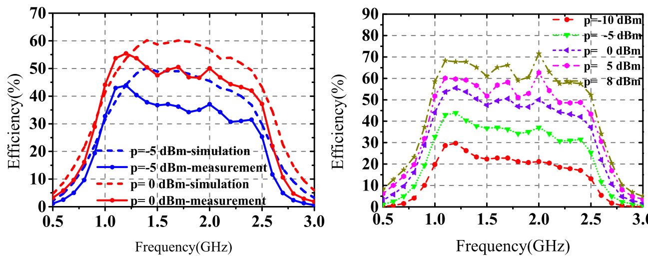
B. Parallel Resonant Compression Based on Microstrip Lines

Track S_{11} of the single-voltage circuit on the Smith chart is shown in Fig. 3(a). The track of S_{11} must move clockwise; after we moved transmission line TL1 clockwise, we added transmission line TL2 to compress the S_{11} track of the high-frequency band, as shown in Fig. 3(b) and (c). Z_{in4} can be transformed into Z_{in2} through transmission line TL2. Similarly, Z_{in2} can be transformed into Z_{in1} through TL1. It is necessary to move the high-frequency point f_2 clockwise along the conductance circle and low-frequency point f_1 counterclockwise along the conductance circle. A parallel resonant circuit is required. When the parallel resonance circuit is added, the impedance does not change at the resonance point; that is, the trajectory at the resonance frequency point does not change. The trajectory is compressed at the nonresonant frequency. Frequencies f_1 and f_2 were set to be 1 and 2.4 GHz, respectively. The resonant frequency of the resonant circuit is f_3. A quarter-wavelength short-circuited transmission line can be equivalent to a parallel resonant circuit. According to the transmission line theory, the input impedance of Z_{in3} can be written as $Z_{in3} = jZ_3 \tan(\beta l_3)$. It replaces the lumped parameter to realize broadband compression, as shown in Fig. 3(d). According to the Smith chart, the resonant point $f_3 = 1.9$ GHz was calculated. Using mathematical formulas,



(a) (b)

Fig. 4. (a) Measured and simulated S_{11} of the rectifier for two power levels. (b) Measured S_{11} of the proposed rectifier at six different load values.



(a) (b)

Fig. 5. RF-to-DC conversion efficiency versus frequency at different power levels. (a) Measured and simulated RF-to-DC conversion efficiency versus frequency at two power levels. (b) Measured RF-to-DC conversion efficiency versus frequency at five power levels.

we can conclude the following:

$$Z_{\text{in}0} = \frac{Z_{\text{in}1} \times Z_{\text{in}3} tg(\beta l_3)}{Z_{\text{in}3} tg(\beta l_3) - jZ_{\text{in}1}}. \quad (1)$$

The optimized size of the entire circuit is as follows: $W_1 = 3.5$ mm; $L_1 = 3.9$ mm; $W_2 = 0.3$ mm; $L_2 = 11.5$ mm; $W_3 = 1.8$ mm; and $L_3 = 21.5$ mm. The capacitor adopts the Murata GRM18 series, where $C_1 = C_2 = C_3 = 100$ pF. The proposed rectifier is designed and optimized by using an electromagnetic (EM) simulation. The fabricated rectifier is shown in Fig. 6.

III. Fabrication and Measurement Results

A prototype circuit has been realized on the substrate with the dielectric constant $\epsilon_r = 2.55$ and thickness $h = 0.8$ mm. The total size of the rectifier circuit is 40×25 mm^2. To make the rectifying circuit more compact, the microstrip line is bent. The measured RF–DC conversion efficiency is obtained through a measurement setup. The microwave power is provided by a microwave source (E8267C; Agilent). A digital multimeter (VC890D) measures the dc voltage by a standard resistance box. The measured and simulated S_{11} are shown in Fig. 4(a). The measured results are slightly frequency shifted due to manufacturing tolerances and inaccurate diode modeling. Reflection coefficient S_{11} was experimentally measured under different loads, as shown in Fig. 4(b). Resistors of 1.1–1.6 kΩ were selected for the investigation. The observed efficiency of the rectifier varies with the resistance. The measured and simulated RF-to-DC conversion efficiency versus frequency at two power levels is shown in Fig. 5(a). The RF–DC efficiency of the rectifier is over 45% from 1.1 to 2.1 GHz and 50% from 1 to 2.4 GHz at the power levels of 0 and 5 dBm, respectively, as shown in Fig. 5(b). The maximum rectifier conversion efficiency is 71.5% for an input power level of 8 dBm. The rectifier conversion efficiency and output

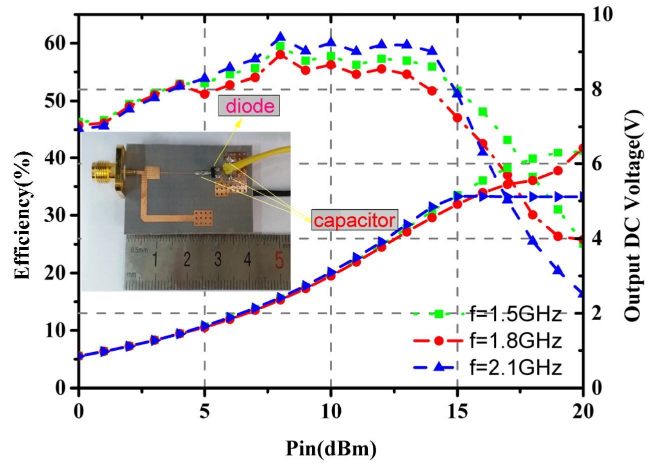


Fig. 6. Measured RF–DC conversion efficiency and output dc voltage of the rectifier circuit versus input power at three frequencies.

TABLE I
Comparison of the Proposed Rectifier and Related Designs

Ref.	BW (GHz)	Frequency (GHz)	Max-PCE	Circuit area (mm×mm)/ ($\lambda_0 \times \lambda_0$)
[13]	1.84	0.1-2.5>45% @10 dBm	74.8% @10 dBm	22.5×31/ $0.1\lambda_0 \times 0.13\lambda_0$
[14]	0.21	2.08-2.58>70% @17.2 dBm	80.8% @17.2 dBm	126×68/ $0.98\lambda_0 \times 0.53\lambda_0$
[15]	0.59	0.47-0.86>60% @10 dBm	60% @10 dBm	N.A.
[16]	0.8	0.87-2>40% @0 dBm	63% @0 dBm	17.8×6.4/ $0.09\lambda_0 \times 0.03\lambda_0$
This work	0.82	1-2.4 >50% @5 dBm	71.5% @8 dBm	40×25/ $0.22\lambda_0 \times 0.14\lambda_0$

dc voltage at different input power levels are shown in Fig. 6. The circuit has wide dynamic input power characteristics and the measured value remains above 50% with an input power of 3–14 dBm. Moreover, a high dc output voltage is obtained by selecting the voltage-doubling structure. Our proposed rectifier was compared with prior works, as shown in Table I. It is obvious that the proposed rectifier circuit performs well in terms of circuit size, bandwidth, and maximum conversion efficiency relative to different input power densities. The size of the circuit with respect to the respective wavelengths of the central frequency is only $0.22\lambda_0 \times 0.14\lambda_0$ (λ_0 is the central frequency of the broadband circuit). Compared with that of other designs, the efficiency of the proposed circuit is greater than 50% at an input power of 5 dBm from 1 to 2.4 GHz.

IV. Conclusion

This letter has presented a broadband high-efficiency RF rectifier with a wide power range for ambient RF EH. The impedance matching network is realized using a parallel resonant compression topology. The proposed topology has been theoretically analyzed and realized. Compared with the previous work, the circuit is uncomplicated in structure since it uses a quarter-wavelength short-circuited stub to achieve efficient broadband matching. The measured results show that the conversion efficiency exceeds 50% from 1 to 2.4 GHz at low power levels of 5 dBm. The measured efficiency remains above 50% for an input power range of 3–14 dBm.

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