ECE 404 - Project 2

RF Detector

Fall 2021
Design Due (for fabrication): 11/12/2020 (By Noon)

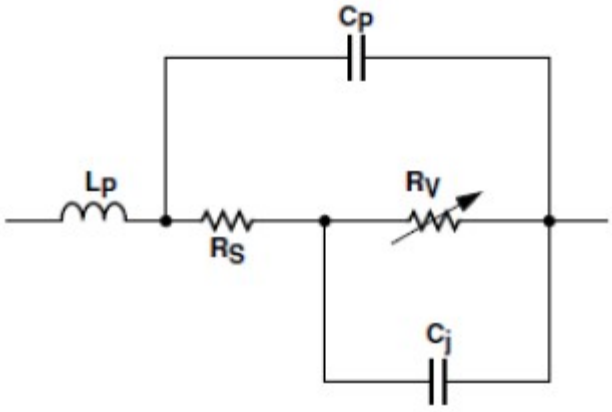
Introduction

For this project, working in groups of two students, you are required to design a lumped element based matching circuit for a zero bias Schottky detector diode. The impedance matching circuit will have to match the impedance of the diode to a 50 Ω transmission line. The impedance matching circuit must be designed at the operating frequency of 0.915 GHz (FCC regulated RFID frequency) with 3dB bandwidth of >20 MHz (i.e., S_{11} < -3dB over this bandwidth). Note, goal is to achieve S_{11} below -10dBm at the design frequency.

The substrate that you will be using is:

- Type: Rogers 4350
- Thickness: 1.524 mm
- Dielectric Constant: 3.55 (Note: the dielectric constant of RO4350 is frequency dependent, see data sheet on D2L)
- Dielectric Loss, tanδ = 0.003
- **Special thanks to Rogers Corporation for donating the high frequency substrates**

The equivalent circuit for a single zero bias diode (Skyworks SMS7630-079LF) is:

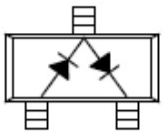


Where,

Cp = 0.6 pF
Lp = 0.1 nH
Cj = 0.26 pF
Rs = 11.6 k
Rv = 7.8 k

Note: The given values are a rough approximation, and further tuning may be performed if deemed necessary.

You may use the chip with a single diode or a chip with two diodes, see figures below.

	
Single	Series Pair
SC-79 Green™	SOT-23
♦ **SMS7621-079LF** Marking: Cathode and SA	♦ **SMS7621-005LF** Green™ Marking: XH2
♦ **SMS7630-079LF** Marking: Anode and SC	**SMS7630-005LF** Green™ Marking: XD2
L_S = 0.7 nH	L_S = 1.5 nH

After design completion, upload your design layout file to the D2L dropbox in the **dxf file format (mm units)**.

Once the circuit is fabricated, solder all the components and necessary shorting pins, and edge mount a connector for testing. To test your final fabricated impedance matching circuit, measure its S_{11} using the VNA. Note, reduce the power setting on the VNA below -10dBm to minimize effect of self-biasing.

Is the result what you expect? (S_{11} magnitude less than -10 dB at the design frequency)

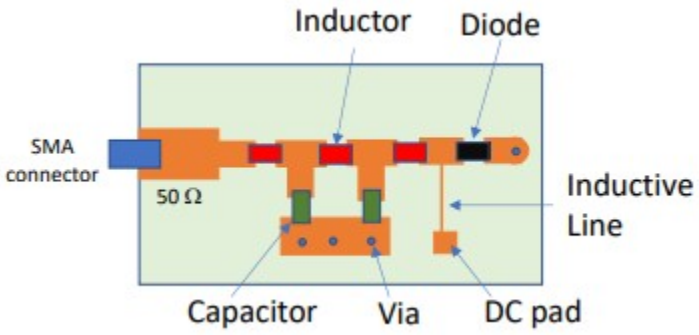
Design Process

- Use Smith Chart tool on ADS to design the impedance matching circuit
- 1-port and 2-port S-parameter data of the diode is available on D2L
  - Note, components can be placed on both sides of the diode
- Use ADS to optimize the circuit and generate a rough layout
  - You may use the S-parameter file of the diode that is posted on D2L
- Use the equivalent model (or S-parameters) of all the components
- Generate a layout that will be used in the fabrication of your boards
  - Check the layout with the TA before submission. Errors are difficult, if not impossible, to fix after fabrication.

Brian Wright will help us to fabricate the designs. Make sure to submit your design by the due date, as Brian will fabricate all circuits from your section at the same time. No late submission will be accepted.

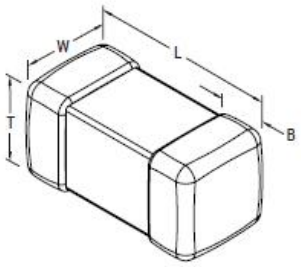
Project Practical Requirements

The figure below is an illustration of a layout of a circuit using lumped elements.



- Please pay attention to the DC path, and we do not want to DC short the diode
- Add a 50 Ω transmission line (> 6 mm long) at the input to accommodate the soldering of an edge mount SMA connector.
- Do not use any dimension less than 0.3 mm in the design (due to fabrication tolerances)
- The minimum allowed spacing between the component's edges must be >4 mm for ease of mounting/soldering.
- Use narrow inductive bias lines (or an inductor) along with a DC pad. This will allow for ease of measurement of the output signal.
- You are limited to using inductor and capacitor values present in the inductor and capacitor kits. The datasheet for these and the diode are available on D2L.
- Pay attention to the dimensions of the components for the design layout. The figure below shows the dimensions of the surface mount chip-inductors and -capacitors.

Dimensions – Millimeters (Inches)



Case Size (in.)	Case Size (mm)	L Length	W Width	T Thickness	B Bandwidth	Mounting Technique
0603	1608	1.60±0.10 (0.063±0.004)	0.80±0.10 (0.031±0.004)	0.80±0.07 (0.031±0.003)	0.40±0.15 (0.016±0.006)	Solder Wave or Solder Reflow

Project Grading Factors (ordered by importance)

- Completion of work

- Is the S_{11} at the design frequency less than -10dB at the design frequency? If not, how close is it to -10dB?
    - Hint: Try to design a relatively wideband matching circuit. This will give you some wiggle room.
- How compact (surface area of the circuit) is your design?
- The number of components used, the fewer the better.

Report

Document your calculation design process followed by the simulation validation and the experimental evaluation. Include the following information in the report:

1. Measured and simulated S_{11} over 0.75 – 1.25 GHz.
2. Measure rectified voltage as a function of frequency (200 MHz around the design frequency at fixed power -10dBm) and power (-20 dBm to -5 dBm at fixed center frequency).
3. Layout and picture of fabricated circuit.
4. Comment on any discrepancies.
5. Discuss approaches to improve your design.