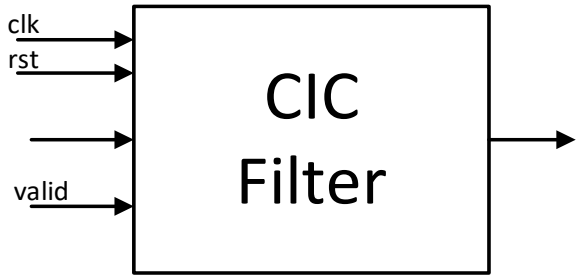
Filtro CIC Interpolatore

In digital signal processing, a Cascaded Integrator–Comb (CIC) is an optimized class of finite impulse response (FIR) digital filter combined with an interpolator or decimator. It is required to design a digital circuit for implementing a 16-bit interpolating low-pass CIC filter with the following characteristics:

- Interpolation factor R = 4
- Delay of Comb stages M = 1
- Number of filter stages N = 4
- Zero-Insertion of R-1 zeros between Comb and Integrator stages

$$y[n] = \sum_{k=0}^{RM-1} x[n-k]$$

The interface of the circuit to be designed is as follows:



New input (x) must be evaluated only when the valid signal = 1, otherwise the circuit state must be retained. You are requested to deal with the various possible error situations, documenting the choices made. In particular, it is necessary to take into consideration:

- Valid set and reset continuously

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions