SC3050
Advanced Computer Architecture

Lab 1
General Introduction

College of Computing and Data Science

Nanyang Technological University

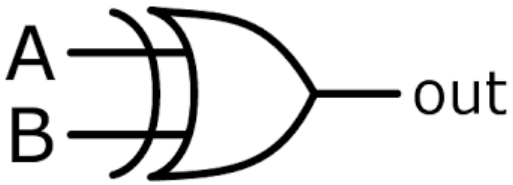
Objective

To design a 64-bit processor based on ARMv8 (LEGv8)ISA in 4 labs

- In lab 1, we will see the functionality of ALU along with the area and delay parameters.
- In lab 2-4, we will build this to a fully pipelined 64-bit LEGv8 **alike processor**.
- Note contents of lab 1 (ALU) will be reused as we are building up the architecture.

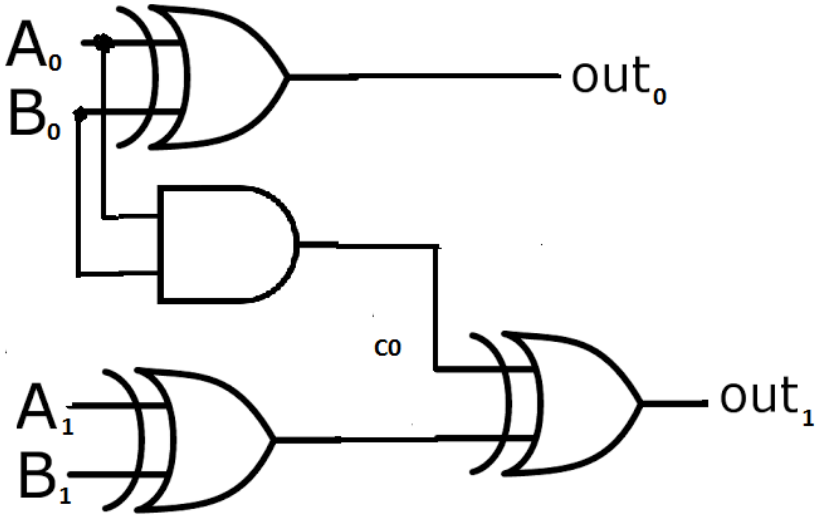
Single-bit adder

out=A (XOR) B



A	B	out
0	0	0
0	1	1
1	0	1
1	1	0

Two-bit adder



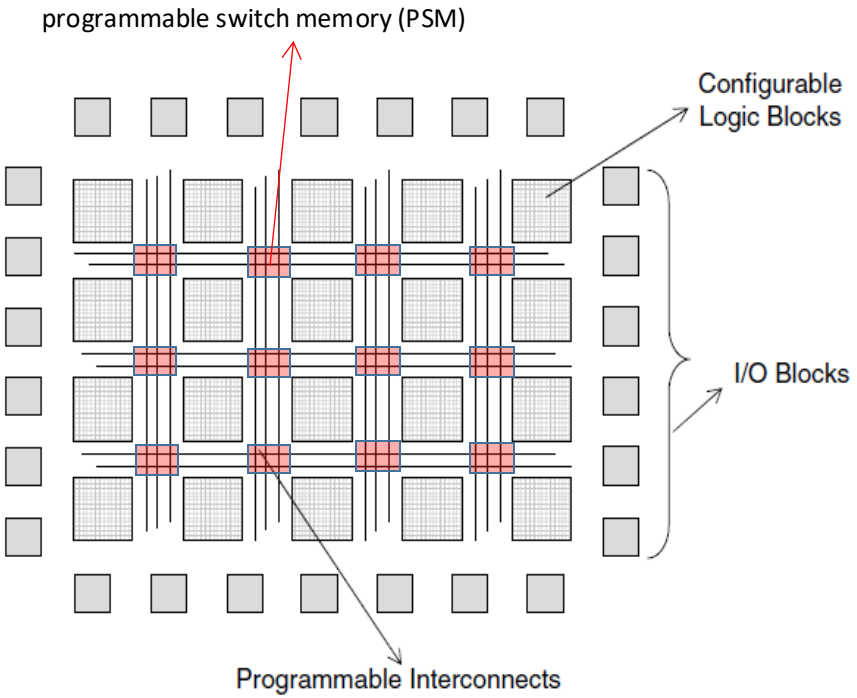
Field Programmable Gate Array(FPGA)

Core architecture of FPGA consists of three main components:

- Array of configurable/programmable logic blocks (CLBs): the combinational units
- A sea of programmable interconnects
- Memories and specialized I/O blocks

Other components in modern FPGAs are

- DSP blocks,
- Hardwired IP cores
- Soft cores

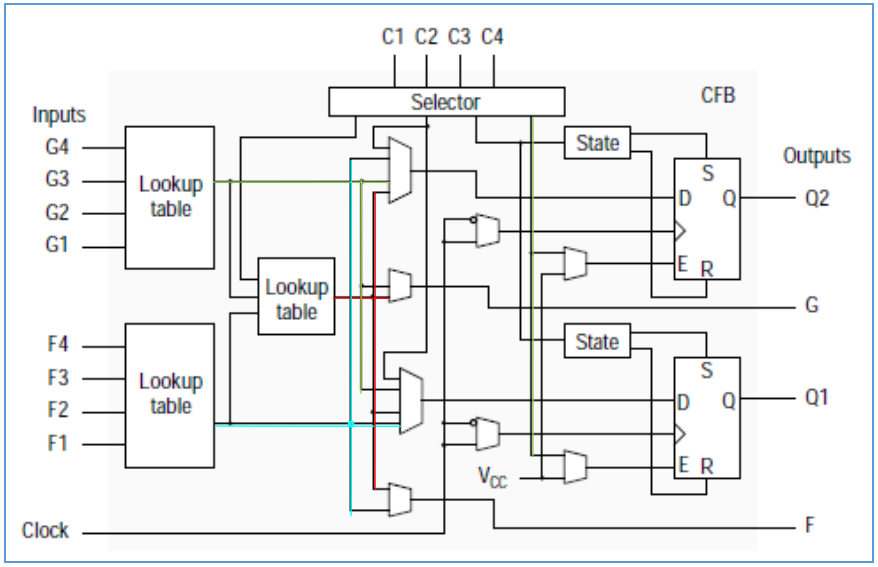


Source: S. Brown and J. Rose, "FPGA and CPLD Architectures: A Tutorial", IEEE Design & Test of Computers, Summer 1996, pp. 42-57

Field Programmable Gate Array(FPGA)

- Configurable Logic Block : Contains 2 four-input LUTs and a third LUT (3-input) fed by the output of other two.
  - CLB can implement logic functions
  - function with more than 4 inputs or two separate 4-input functions

- each LUT is 1-bit-wide memory array
- address lines are CLB inputs
- any desired K-input logic function can be realized with this LUT by writing the truth table for the function directly into the memory.

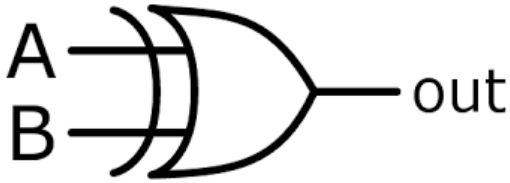


Configurable Logic Block- XC4000 family

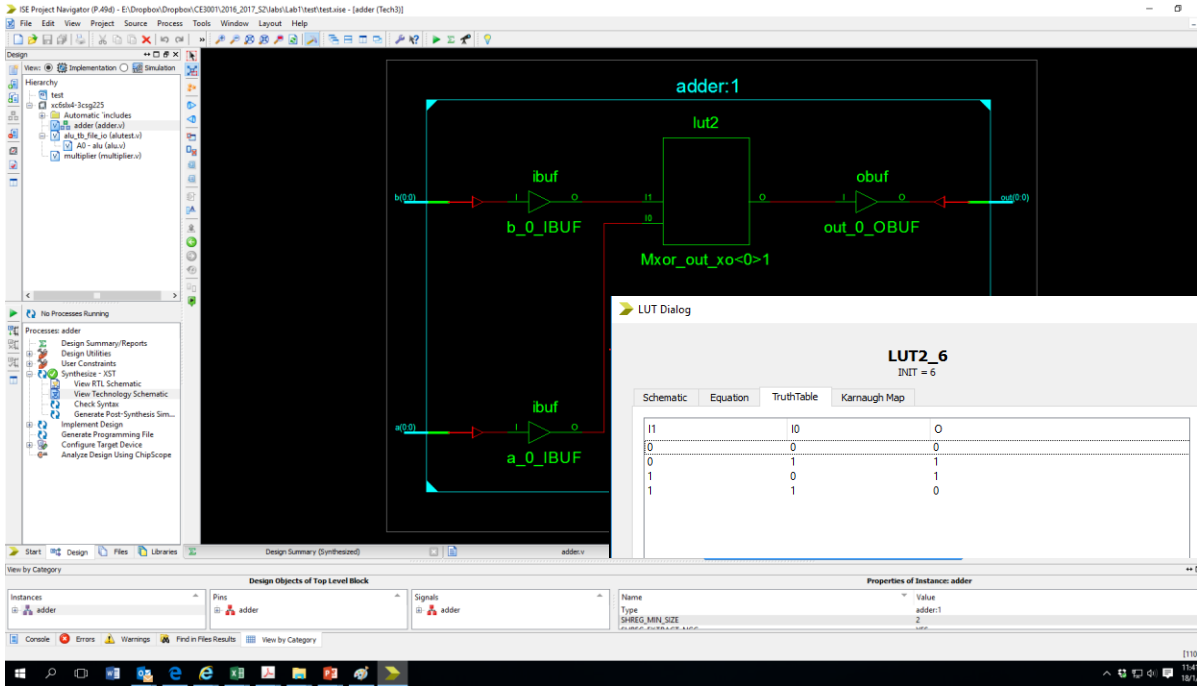
Source: S. Brown and J. Rose, "FPGA and CPLD Architectures: A Tutorial", IEEE Design & Test of Computers, Summer 1996, pp. 42-57

Single bit adder

out=A (XOR) B



A	B	S
0	0	0
0	1	1
1	0	1
1	1	0



Two bit adder