

National University of Computer & Emerging Sciences, Karachi Fall -2020 CS-Department Activity 01



Memory Management

Course Code: CS220	Course Name: Operating System	
Instructor Name: Anaum Hamid		Deadline: 15/12/2020
Marks: 20		Section No: C/E

Consider a system using multilevel paging scheme. The page size is 16 KB. The memory is byte addressable and virtual address is 48 bits long. The page table entry size is 4 bytes.

Find-

- 1. How many levels of page table will be required?
- 2. What will be the size of inner page table?
- 3. What will be the size of outer page table?
- 4. Give the divided physical address and virtual address illustrated by a diagram of address translation.