Teaching Plan

FAKULTI TEKNOLOGI MAKLUMAT DAN KOMUNIKASI
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

COMPUTER ORGANIZATION AND ARCHITECTURE		
DITS1133	**SEMESTER 1**	**SESSION 2020/2021**

DITS1133 COMPUTER ORGANIZATION AND ARCHITECTURE (3, 2, 2)
TYPE OF COURSE: C
UPDATED: 23-08-2019

1.0 LEARNING OUTCOMES

Upon completion this course, students will be able to:

CLO 1: Explain the principles and techniques used in implementing a computer architecture and organization concept (C2).
CLO 2: Identify the concept of functional computer components and the detail interactions in computer systems (CTPS1).
CLO3: Assemble basic computer components and its architectural attributes, including instruction set and technique for addressing memory (P3).

2.0 SYNOPSIS

This subject provides a detail of computer system's functional components, their characteristics, their performance and their interactions including system bus, different types of memory and Input/Output and CPU, as well as practical implementations of the components. Besides, the architectural issues, such as instruction set design and data types, are covered. In addition to this, students are introduced to the increasingly important area of parallel organization.

3.0 PRE-REQUISITE

None

4.0 PRACTICAL

Students will be introduced to number representation and basic digital logic circuit. The knowledge will be used when students learned the programming technique of assembly language. In addition to this, students will be

introduced to computer system's component and then assembling the PC components.

5.0 REFERENCES

[1] William Stallings, (2017). Computer Organization & Architecture, 10th Edition. Prentice Hall.

[2] David A. Patterson and John L. Hennessy (2016). Computer Organization and Design: The Hardware / Software Interface, 5rd Edition. Morgan Kauffman.

[3] Syarulnaziah, Zakiah, Marliza., Aslinda. *Lab Module: Computer Organization and Architecture With MIPS Programming.*

[4] Linda Null and Julia Lobur (2016). The Essential of Computer Organization and Architecture, 4nd Edition. Jones & Bartletts Pub.

[5] Carl Hamacher, Zvonko Vranesic, Safwat Zaky, (2016). Computer Organization, 6th Ed. McGraw Hill.

[6] Irv Englander, (2016). The Architecture of Computer Hardware and System Software: An Information Technology Approach., 5rd Edition. John Wiley & Sons.

6.0 COURSE IMPLEMENTATION

i. Lecture
- 2 hours per week for 14 weeks (Total = 28 hours)

ii. Laboratory Activities
- 2 hours per week for 14 weeks (Total = 28 hours)

6.0 COURSE EVALUATION

Assessment Method	**CLO 1** (C2)	**CLO 2** (CTPS1)	**CLO 3** (P3)
Lab exercise (5) = 25%		LA1-3 (15%) CTPS1,PLO5	LA2-LA5 (10%) P3, PLO:3
Lab Test = 10%			LT1 (10%) P3, PLO:3
Quiz (4) = 20%	Q1-Q2 (10%) C2, PLO:1	Q3-Q4 (10%) CTPS1, PLO:5	
Mid Term = 15%	MT1 (15%) C2, PLO:1		
Final assessment = 30%	FA (30%) C2, PLO:1		
Total	55%	25%	20%

7.0 STUDENT LEARNING TIME (SLT)

		Guided Learning Time				Independant Learning								Assessment Time				
Week	CLO	L	T	P	O	L	T	P	O	F	T	A	O	F	T	A	O	SLT
W1	3	2		2		2	0	1		0	0	0	0					7
W2	1	2		2		2	0	1		0	0	0	0					7
W3	1	2		2		2	0	1		0	0	0	1				0.25	8.25
W4	1	2		2		2	0	1		0	0	0	0					7
W5	3	2		2		2	0	1		0	0	0	0					7
W6	2	2		2		2	0	1		0	4	0	1		1		0.25	13.25
W7	3	2		2		2	0	1		0	0	0	0					7
W8	2	2		2		2	0	1		0	0	0	0					7
W9	2	2		2		2	0	1		0	0	0	0					7
W10	1	2		2		2	0	1		0	0	0	1				0.25	8.25
W11	1	2		2		2	0	1		0	0	0	0					7
W12	1	2		2		2	0	1		0	0	0	0					7
W13	1	2		2		2	0	1		0	0	0	1				0.25	8.25
W14	1	2		2		2	0	1		0	4	0	0		1			12
>W14										0	6	0	0		1.5			7.5
Overall		28	0	28	0	28	0	14	0	0	14	0	4	0	3.5	0	1	120.5
															SLT Credit Equivalent			3.0125

9.0 DETAILED SYLLABUS AND TEACHING PLAN

Week	Contents	References	Delivery Methods
1	**Lecture 1: Introduction to Computer, Introduction to Basic Electronics** **Lab 1: Assembling PC**	[2] Chapter 1 Online source https:www.openlearning/courses/OSK [3] Lab 1	Online
2	**Lecture 2: Arithmetic for Computers** Number System Base, Number conversion (decimal, binary and hexadecimal) **Lab 2: Disk formatting and partitioning**	[1] Chapter 3 [3] Lab 1	Online
3	**Lecture 3: Arithmetic for Computers (Cont)** Binary number operation (add, sub, multiply and divide), Hexadecimal number operation (add and sub). **Lab 3: Number Systems & Operations (Cont)** Negative number representation and conversion	[1] Chapter 3 [3] Lab 2	Online
4	**Lecture 4: The Basics of Logic Design**	[1] Appendix C	Online

	Basic logic gates, combinational circuit, Boolean equation forms, Laws of Boolean Algebra **Lab 4: Digital Logic – Combinational Circuit** 2's complement number operation (add and sub for positive and negative number)	[3] Lab 3	
5	**Lecture 5: The Basics of Logic Design (Cont)** Karnaugh Map, Simplification of combinational circuit **Lab 5: Digital Logic – Combinational Circuit (Cont)** Introduction of multimedia logic; Introduction to adder, multiplexer, decoder and SR flip flop.	[1] Appendix C [3] Lab 4 [3] Lab 5, 6	Online
6	**Lecture 6: Language of the Computers** Instruction Sets, Type of operands (register, memory, immediate) **Lab 6: Introduction to Microprocessor** Introduction to assembly language and simulations tool	[1] Chapter 2 [3] Lab 7	Online
7	**Lecture 7: Language of the Computers** Assembly language Addressing modes (Register, Immediate, PC-relative, Base, Pseudo-direct) ; Addressing formats (R, I and J-Type) **Lab 7: Introduction to Microprocessor** Implementation of assembly language addressing	[1] Chapter 2 [3] Lab 8	Online
8	**Lecture 8: The Processor** CPU overview; Control unit; Intro to Datapath **Lab 8: Assembly Language 1** Load and store operations	[1] Chapter 4 [3] Lab 9	Online
9	**Lecture 9: The Processor** Building Datapath (R and I-type) **Lab 9: Assembly Language 2**	[1] Chapter 4 [3] Lab 10	Online

	Arithmetic operations (add, sub, mult)		
10	**Lecture 10: Exploiting Memory Hierarchy** Memory type; Principle of locality; Intro to cache mapping technique(direct, associative, set-associative); cache mapping example (direct mapping) **Lab 10: Assembly Language 3** Logical operation (sll, ori, and)	[1] Chapter 4 [3] Lab 11	Online
11	**Lecture 11: Exploiting Memory Hierarchy** RAM, Memory Module, SRAM, DRAM, Introduction to ROM **Lab 11: Assembly Language 4** Translating HLL code to assembly language (Syscall and if-else statement)	[1] Chapter 5 [3] Lab 11	Online
12	**Lecture 12: Exploiting Memory Hierarchy** Magnetic disc; Magnetic disc access, **Lab 11: Assembly Language 5** Translating HLL code to assembly language (loop statement)	[1] Chapter 5 [3] Lab 11	Online
13	**Lecture 13: Exploiting Memory Hierarchy** Intro to I/O; Bus type and example; I/O management; RAID **Lab 11: Assembly Language 6** Translating HLL code to assembly language (array statement)	[4,5] Chapter 5 [3] Lab 11	Online
14	**Lecture 14: Discussion** **Lab Test**		
15	**Revision Week**		

10.0 MATRIX OF LEARNING OUTCOMES

SUBJECT vs PROGRAM OUTCOME (PO)

Subject	PROGRAM OUTCOME (PO)								
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	
DITS 1133	X		X		X				

LEARNING OUTCOME (CLO)

CLO1	Explain the principles and techniques used in implementing a computer architecture and organization concept (C2).
CLO2	Identify the concept of functional computer components and the detail interactions in computer systems (CTPS1).
CLO3	Assemble basic computer components and its architectural attributes, including instruction set and technique for addressing memory (P3).

LEARNING OUTCOME (LO) vs PROGRAM OUTCOME (PO)

CLO	PROGRAM OUTCOME (PO)								
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	
CLO1	X								
CLO2					X				
CLO3			X						

Subject	SOFT SKILLS																							
	communication skill					critical thinking & problem solving					team work			lifelong learning			entrepreneurship skills			ethics&moral professionalism			leadership skills		
	CS1	CS2	CS3	CS4	CS5	CTPS1	CTPS2	CTPS3	CTPS4	CTPS5	TS1	TS2	TS3	LL1	LL2	LL3	ES1	ES2	ES3	EM1	EM2	EM3	LS1	LS2	LS3
DITS 1133						X																			

LEARNING OUTCOME (LO) vs SOFT SKILLS

CLO	SOFT SKILLS																							
	communication skill					critical thinking & problem solving					team work			lifelong learning			entrepreneurship skills			ethics & moral professionalism			leadership skills		
	CS1	CS2	CS3	CS4	CS5	CTPS1	CTPS2	CTPS3	CTPS4	CTPS5	TS1	TS2	TS3	LL1	LL2	LL3	ES1	ES2	ES3	EM1	EM2	EM3	LS1	LS2	LS3
CLO1																									
CLO2						X																			
CLO3																									

SUBJECT vs TAXONOMY

Subject	Taxonomy																
	Affective					Cognitive						Psychomotor					
	A1	A2	A3	A4	A5	C1	C2	C3	C4	C5	C6	P1	P2	P3	P4	P5	P6	P7
DITS 1133						X	X					X	X	X				

LEARNING OUTCOME (LO) vs TAXONOMY

CLO	Taxonomy																
	Affective					Cognitive						Psychomotor					
	A1	A2	A3	A4	A5	C1	C2	C3	C4	C5	C6	P1	P2	P3	P4	P5	P6	P7
CLO1						X	X											
CLO2																		
CLO3												X	X	X				

TEACHING PLAN APPROVAL

Prepared by;

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Name: DR NURUL AZMA ZAKARIA

Stamp:

Date: 9 October 2020

Approved by;

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Dean/Deputy Dean (Academic)/HOD

Stamp:

Date: 9 October 2020

TEACHING PLAN IMPLEMENTATION (MID SEMESTER BREAK)

Comment :

Checked by;

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Dean/Deputy Dean (Academic)/HOD

Stamp: Date: _____

TEACHING PLAN IMPLEMENTATION (WEEK 16)

Comment :

Checked by;

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Dean/Deputy Dean (Academic)/HOD

Stamp: Date: _____