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Experiment 2

**Verification of Basic Logic Gates & their Truth tables**

**Objective**

* To demonstrate the input and output relationship of 2 input AND, OR, NOT, NAND, NOR, XOR gates using EWB and Logic Trainers.

**Tools/Equipment Requirement**

* ICs 7408, 7432, 7404, 7400, 7402, 7486
* Analog and Digital Trainer
* Connecting wires

**Procedure**

* Patch the circuit on the trainer.
* Connect the inputs to the input switches and output to the LEDs given on the trainer.
* Make connections of input, output, Vcc and GND according to pin configurations of each IC.
* Verify the truth table for all the combinations.
* Repeat steps 1 and get it checked by the instructor.

**Theoretical Explanation**

1. **AND gate**

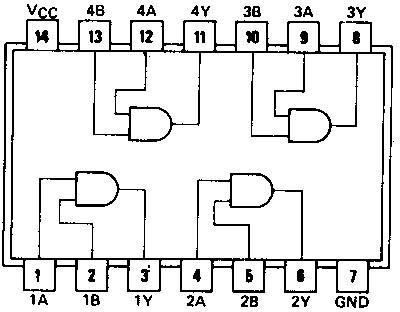
TTL stands for Transistor Transistor logic. The TTL IC used for a 2 input AND gate is **7408** (Quad 2 input AND gate)

**Logic Equation**

Y = AB

**Logic Symbol**

**Diagram  Description automatically generated**

**Pin configuration**

Pin Configuration of AND Gate

1. **OR gate**

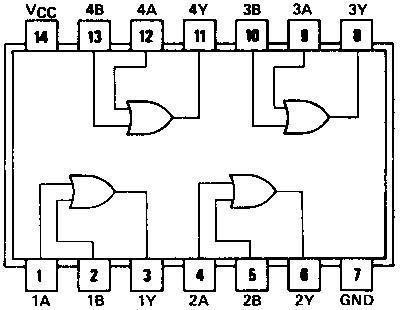
The TTL IC for an OR gate is **7432** (Quad 2 input OR gate) which has four 2- input OR gate.

**Logic Equation**

Y= A + B

**Logic Symbol**

**Pin Configuration**

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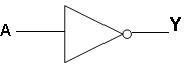
1. **NOT GATE**

The TTL IC for NOT gate (also known as an inverter) is **7404** (Hex 1 input NOT gate) which has six 1-input NOT gate. The output of an inverter is opposite to an input.

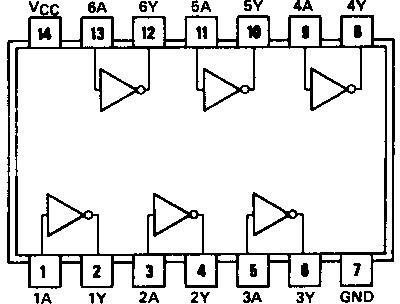
**Logic equation**

**Y= ~A or ** (inverted output)

**Logic Symbol**

****

**Pin configuration**

****

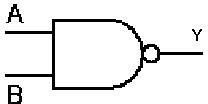
1. **NAND gate**

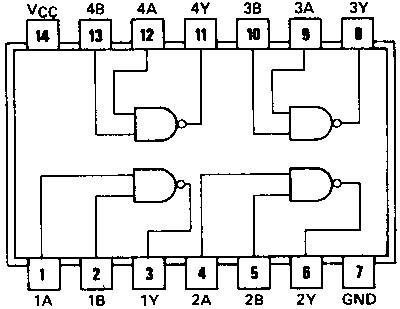
The TTL IC for four 2-inputs NAND gate is **7400**. The operation of NAND gate is opposite to that of an AND gate.

**Logic equation:**

Y =  (AB)

**Logic Symbol**

****

**Pin configuration**

1. **NOR gate**

The TTL IC used for four 2-input NOR gate is **7402** (Quad 2-input NOR gate). The operation of NOR gate is opposite to that of an OR gate.

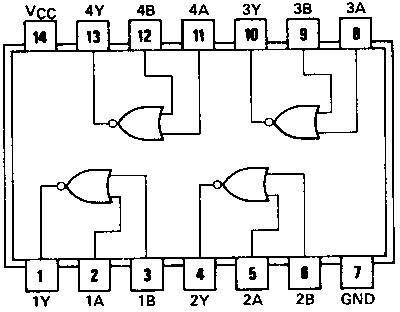
**Logic Equation**

Y=  (A+B)

**Logic Symbol**

**Diagram  Description automatically generated**

**Pin configuration**

****

1. **XOR gate**

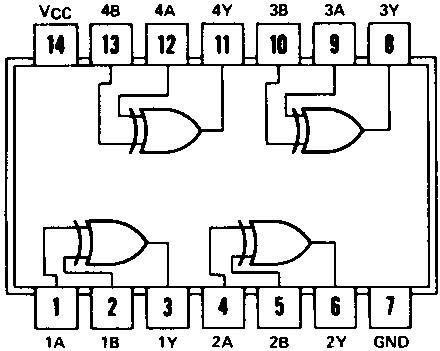
The TTL IC for an XOR gate is **7486** which has four 2-input XOR gates.

**Logic Equation**

Y= AB=A’B +AB’

**Logic symbol**

**Diagram  Description automatically generated**

**Pin configuration**

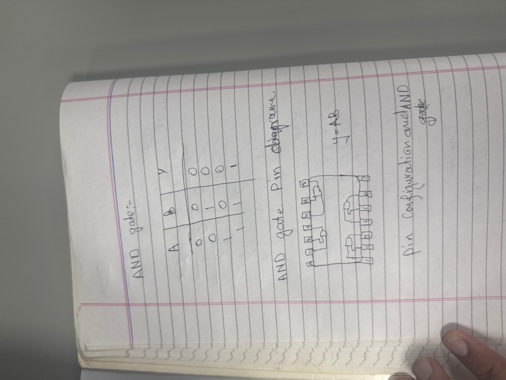
**Task 1**

Draw the circuit diagrams of the above-mentioned Gates using the IC’s and logic gates in EWB and Trainer and fill the tables below.

**AND Gate:**

**Circuit Diagrams:**

**Observations/Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y=A.B** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**OR Gate:**

**Circuit Diagrams:**

A blue electronic device with wires

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.

A blue electronic device with wires

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.A notebook with writing on it

AI-generated content may be incorrect.

**Observations/Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y=A+B** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**NOT Gate:**

**Circuit Diagrams:**

A blue electronic device with wires

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.A hand writing on a notebook

AI-generated content may be incorrect.

**Observations/Truth Table**

|  |  |
| --- | --- |
| **A** | **Y=A’** |
| 0 | 1 |
| 0 | 1 |
| 1 | 0 |
| 1 | 0 |

**NAND Gate:**

**Circuit Diagrams:**

A blue electronic device with wires and switches

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.

A blue electronic device with wires

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.

A hand holding a piece of paper

AI-generated content may be incorrect.

**Observations/Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y=(AB)’** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NOR Gate: Circuit Diagrams:**

A blue electronic device with wires

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.A blue electronic device with wires

AI-generated content may be incorrect.

A notebook with writing on it

AI-generated content may be incorrect.

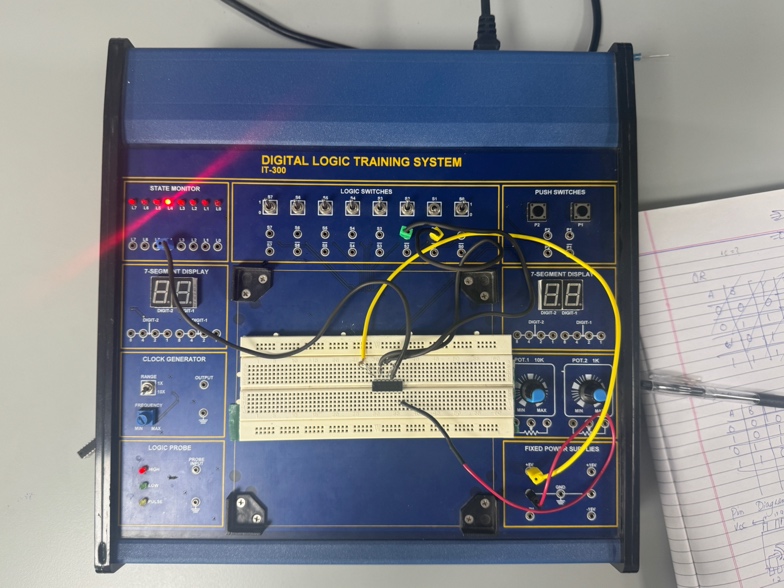
**Observations/Truth Table**

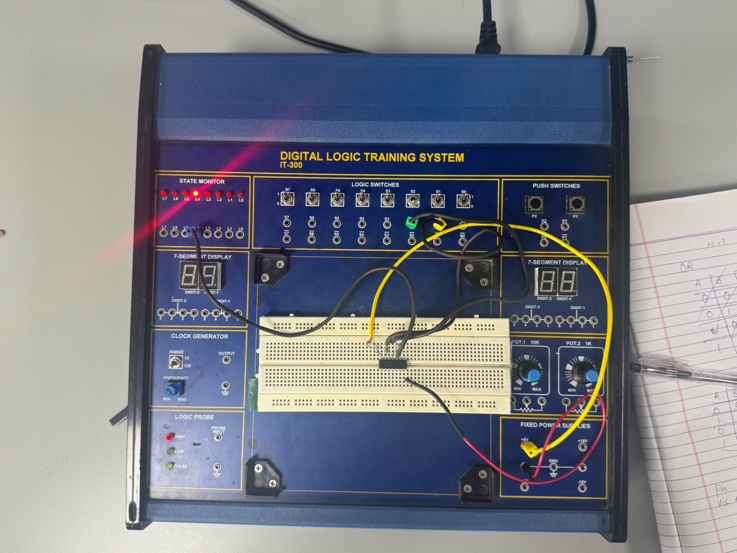
|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y=(A+B)’** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**XOR Gate:**

**Circuit Diagrams:**

A blue electronic device with wires and wires

AI-generated content may be incorrect.



**Observations/Truth Table**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y=**AB |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Conclusion**

In this experiment I learn how logic gates work. I see the truth table is same like theory. AND give output 1 only when both input 1, OR give 1 when any input is 1, NOT change 0 to 1 and 1 to 0. NAND and NOR work opposite of AND and OR. XOR give 1 when inputs are different. So my practical result match with theory and I understand gates more good.