Haoyang Zhang

Undergraduate / Computer Engineering
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EDUCATION

University of Michigan, Ann Arbor, US Sep. 2020 – May. 2022 (Expected)

B.SE. Computer Engineering (Dual Degree)

- Cumulative GPA: 4.000/4.000
- Course Works: Computer Architecture (A), Compiler Construction (A+), Intro. Computer Organization (A), Digital Integrated Circuit (A), Data Structure & Algorithms (A), Linear Spaces and Matrix Theory (A)

Shanghai Jiao Tong University (UM-SJTU JI), Shanghai, China Sep. 2018 – Aug. 2022 (Expected)

B.S. Electrical and Computer Engineering (Dual Degree)

- Cumulative GPA: 3.718/4.000, with rank 38/245
- Course Works: Programming & Data Structures(A+), Intro. Logic Design(A), Intro. Circuits(A), Honors Physics(A, A+)

RESEARCH EXPERIENCE

Efeslab – University of Michigan Ann Arbor, US

Undergraduate Research Intern (Advisor: Dr. Baris Kasikci) Apr. 2021 – Present

- **Project: Reconfigurable Hardware Debugging.**
  - **Description:** Study bugs in existing FPGA designs and produce a testbed to reliably reproduce each bug. Build a novel collection of hybrid static/dynamic program analysis and monitoring tools for debugging FPGA designs.
  - **Responsibility:** Implement the simulator for SignalCat, a recorder and printer on actual hardware deployments, study Intel/Xilinx platforms and Interfaces, implement special building blocks to help reproduce hardware bugs. Search and find more opensource buggy examples, reproduce can debug them, update our bug study and further improve our tools.

EECS573 – University of Michigan Ann Arbor, US

Undergraduate Researcher (Advisor: Dr. Todd Austin) Sept. 2021 – Present

- **Project: A Penetrating Spectre/Meltdown Attack Targeting Compiler-based Protections.**
  - **Description:** Find a way to subvert compiler-based Spectre protections by identifying and jumping over the speculation barrier code inserted by the compiler using a special partially-tagged BTB.

Emerging Computing Technology Laboratory – Shanghai Jiao Tong University Shanghai, China

Research Assistant (Advisor: Dr. Weikang Qian) Jan. 2021 – Present

- **Project: MiniHLS: A Simple High-Level Synthesis Tool.**
  - **Description:** An HLS tool based on LLVM, which can compile C functions to Verilog modules, having multiple features including loop optimization, support for structs and classes, tcl file parsing, etc.
  - **Responsibility:** Study the start-of-art array partition algorithms for HLS and the Polyhedral Compilation Model, and try to implement our own memory partition algorithm using Polly. Test the HLS output on FPGA, do post-synthesis debugging/on-board verification and hence modify the source code of our Mini-HLS.

Trusted Cloud Group – Shanghai Jiao Tong University Shanghai, China

Undergraduate Researcher (Advisor: Dr. Zhengwei Qi) Nov. 2020 – Jul. 2021

- **Project: FPGA-based Accelerator Design for Neural Network Algorithms in Image Compression**
  - **Description:** An end-to-end exploration of hardware acceleration for learning-based image compression, which used an optimized systolic array architecture and the winograd accelerating algorithm.

- **Responsibility:** Study and be proficient in Xilinx Vivado HLS, implement the winograd transformation for our convolution data flow, implement part of the accelerator, conduct simulations and tests.

INTENSHIP EXPERIENCE

T-head Division, Alibaba Cloud Hangzhou, China

Software Research & Development Intern (Mentor: Yunhai Shang) Jul. 2021 – Aug. 2021

Study the latest vector ISA extension of RISC-V. Implement part of the optimization for the jpeg library for RISC-V vector processors.

SELECTED PROJECT EXPERIENCE

A 3-Way Superscalar R10K-Style Out-of-Order Processor Core Feb. 2021 - April. 2021

Final project of EECS 470: Computer Architecture

Project: Build a 3-way Superscalar R10K-Style Processor with a few advanced features: Non-blocking L1 Data cache, Dynamic branch prediction, Instruction prefetching, etc.

- Implement Data Cache, Memory Controller, Retire Stage, Map Table/Arch. Map Table, Branch FU, and do debugging.
- Analysis and optimize the performance of our processor.

An Optimized Compiler for Decaf Language Jan. 2021 - April. 2021

Final project of EECS 483: Compiler Construction

Project: Implemented a working compiler with source language Decaf and target language MIPS using flex (lexical analysis), yacc/bison (syntax analysis), and C/C++ (other parts).

- Build and optimize the compiler by gradually implementing scanner, parser, IR generator and Mips generator.
- Chose Chaitin's Algorithm for register allocating and implemented a few IR optimization including Dead Code Elimination, Common Subexpression Elimination and Constant Propagation.

TEACHING EXPERIENCE

Honors Physics I (VP160), Teaching Assistant, Shanghai Jiao Tong University May 2020

SELECTED AWARDS

Roger King Scholarship, University of Michigan Aug. 2021
University Honors, University of Michigan Apr. 2021
Dean's Honors List, University of Michigan Jan. 2021, Apr. 2021
Silver Medal, University Physics Competition 2019 Jan. 2020
Student Development Scholarship of SJTU 2019-2020 Jun. 2020
Honorable Mention, Mathematical Contest of Modeling 2019 Apr. 2019

SKILLS

- **Programming Language:** C/C++, Verilog/System Verilog, CUDA, Python, MATLAB
- **Electronic Circuit Simulation:** Synopsys VCS, Verilator, Xilinx Vivado, Cadence Virtuoso