Haoyang Zhang

Seinor student, Computer Engineering, University of Michigan

+1 734-882-9526 | haoyoung@umich.edu | hieronzhang.github.io | HieronZhang | @HaoyangZhang19

Education

University of Michigan *Ann Arbor, U.S.*

B.S.E. Computer Science (Summa Cum Laude, Dual Degree) *Aug. 2020 - May. 2022(Expected)*

- GPA: 4.00/4.00
- Course Highlights: Computer Architecture *(grad, A)*, Compiler Construction *(grad, A+)*

Shanghai Jiao Tong University *Shanghai, China*

B.S.E. Electrical and Computer Engineering (Dual Degree) *Sep. 2018 - Aug. 2022(Expected)*

- GPA: 3.72/4.00

Mcgill University *Montreal, Canada*

Winter Exchange Program *Jan. 2020 - Feb. 2020*

Course Works: Intro. to Data Modeling/Project Management

Publications

Debugging in the Brave New World of Reconfigurable Hardware.
Jiacheng Ma, Gefei Zuo, Kevin Loughlin, **Haoyang Zhang**, Andrew Quinn, Baris Kasikci. (ASPLOS 2022). *To Appear*.

Research

Efeslab - University of Michigan *Ann Arbor, U.S.*

Advisor: Baris Kasikci *Apr.2021 - Present*

- **Project: Reconfigurable Hardware Debugging**
  - **Objectives:** Study bugs in existing FPGA designs and produce a testbed to reliably reproduce each bug. Build a novel collection of hybrid static/dynamic program analysis and monitoring tools for debugging FPGA designs.
  - **Responsibility:** Implement the simulator for SignalCat, a recorder and printer on actual hardware deployments. Study Intel/Xilinx platforms and Interfaces, implement special building blocks to help reproduce hardware bugs. Search and find more opensource buggy examples, reproduce can debug them, update our bug study and further improve our tools.

EECS573 (Also Course Project) - University of Michigan *Ann Arbor, U.S.*

Advisor: Todd Austin *Sept. 2021 – Present*

- **Project: A Penetrating Spectre/Meltdown Attack Targeting Compiler-based Protections.**
  - **Objectives:** Find a way to subvert compiler-based Spectre protections by identifying and jumping over the speculation barrier code inserted by the compiler using the special partially-tagged BTB.
  - **Responsibility:** Secret for now.

Emerging Computing Technology Laboratory – Shanghai Jiao Tong University *Shanghai, China*

Advisor: Weikang Qian *Jan. 2021 – Present*

- **Project: MiniHLS: A Simple High-Level Synthesis Tool**
  - **Objectives:** An HLS tool based on LLVM, which can compile C functions to Verilog modules, having multiple features including loop optimization, support for structs and classes, tcl file parsing, etc.
  - **Responsibility:** Study the start-of-art array partition algorithms for HLS and the Polyhedral Compilation Model, and try to implement our own memory partition algorithm using Polly. Test the HLS output on FPGA, do post-synthesis debugging/on-board verification and hence modify the source code of our Mini-HLS.

Trusted Cloud Group - Shanghai Jiao Tong University *Shanghai, China*

Advisor: Prof. Zhengwei Qi *Nov. 2020 – Jul. 2021*

- **Project: FPGA-based Accelerator Design for Neural Network Algorithms in Image Compression**
  - **Objectives:** An end-to-end exploration of hardware acceleration for learning-based image compression, which used an optimized systolic array architecture and the winograd accelerating algorithm.
  - **Responsibility:** Study and be proficient in Xilinx Vivado HLS, implement the winograd transformation for our convolution data flow, implement part of the accelerator, conduct simulations and tests.

Selected Projects

3-Way Superscalar R10K-Style Out-of-Order Processor Core *Ann Arbor, U.S.*

Advisor: Jon Beaumont *Feb. 2021 - April. 2021*

- **Description:** Build a 3-way Superscalar R10K-Style Processor with a few advanced features: Non-blocking L1 Data cache, Dynamic branch prediction, Instruction prefetching, etc.
- **Responsibility:** Implement Data Cache, Memory Controller, Retire Stage, Map Table/Arch. Map Table, Branch FU, and do debugging. Analysis and optimize the performance of our processor.

An Optimized Compiler for Decaf Language *Ann Arbor, U.S.*

Advisor: Lingjia Tang *Jan. 2021 - April. 2021*

- **Objectives:** Implement a working compiler with source language Decaf and target language MIPS using flex (lexical analysis), yacc/bison (syntax analysis), and C/C++ (other parts).
- **Responsibility:** Build and optimize the compiler by gradually implementing scanner, parser, IR generator and Mips generator. Chose Chaitin's Algorithm for register allocating and implemented a few IR optimization including Dead Code Elimination, Common Subexpression Elimination and Constant Propagation.

Teaching

Shanghai Jiao Tong University

SU. 2020 **Honors Physics (VP160)**, Teaching Assistant

Selected Awards and Honors

2021 **Roger King Scholarship**, University of Michigan

2021 **Univerisity Honors**, University of Michigan

2021,2020 **Dean's List**, University of Michigan

2020, 2019 **Undergraduate Academic Excellence Scholarship**, Shanghai Jiao Tong University

2020 **Student Development Scholarship**, Shanghai Jiao Tong University

2019 **Silver Medal**, University Physics Competition

2019 **Honorable Mention**, Mathematical Contest of Modeling

Service and Activities

Service

2021 **UM Mhardware**, Active Member

2019 **SJTU Student Science and Technology Innovation Association**, Consultant

2019 **JI Young Volunteers Association**, Minister

Volunteering

2019 **Yunnan San He Junior High School Volunteer Teaching Team**, Team leader

Skills

Language **C/C++, Verilog/SystemVerilog, CUDA, Python, MATLAB, TeX**

ISAs **RISC-V, X86, LEGv8, MIPS, LC2K**

EDA Tools **Synopsys VCS, Verilator, Xilinx Vivado, Cadence Virtuoso**