Haoyang Zhang

Undergraduate / Computer Engineering
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EDUCATION

University of Michigan, Ann Arbor, US Sep. 2020 – May. 2022 (Expected)
B.SE. Computer Engineering (Dual Degree)

- Cumulative GPA: 4.000/4.000
- Course Works: Computer Architecture (A), Compiler Construction (A+), Intro. Computer Organization (A), Digital Integrated Circuit (A), Data Structure & Algorithms (A), Linear Spaces and Matrix Theory (A)

Shanghai Jiao Tong University (UM-SJTU JI), Shanghai, China Sep. 2018 – Aug. 2022 (Expected)
B.S. Electrical and Computer Engineering (Dual Degree)

- Cumulative GPA: 3.718/4.000, with rank 38/245
- Course Works: Programming & Data Structures(A+), Intro. Logic Design(A), Intro. Circuits(A), Honors Physics(A, A+)

RESEARCH EXPERIENCE

Efeslab – University of Michigan Ann Arbor, US (Remote)
Undergraduate Researcher (Advisor: Dr. Baris Kasikci) Apri. 2021 – Present

Trusted Cloud Group – Shanghai Jiao Tong University Shanghai, China
Undergraduate Researcher (Advisor: Dr. Zhengwei Qi) Dec. 2020 – Present

- **Project: Optimizing FPGA-based Accelerator Design for Neural Network Algorithms.**
  - **Description:** Various accelerators for CNN have been proposed based on FPGA platform because it has advantages of high performance, reconfigurability, and fast development round. The goal of this project is to build an FPGA-based accelerator for some specific neural network algorithms.
  - **Responsibility:** Study and be proficient in Xilinx Vivado HLS design, build part of the accelerator (architectural support of Fast Fourier Transformation), conduct simulations and tests.

Emerging Computing Technology Laboratory – Shanghai Jiao Tong University Shanghai, China
Research Assistant (Advisor: Dr. Weikang Qian) Jan. 2021 – Present

- **Project: MiniHLS: A Simple High-Level Synthesis Tool.**
  - **Description:** An HLS tool based on LLVM, which can compile C functions to Verilog modules, having multiple features including loop optimization, support for structs and classes, tcl file parsing, etc.
  - **Responsibility:** Implement array partitions, test the HLS output on FPGA, do post-synthesis debugging and hence modify the source code of our Mini-HLS.

SELECTED PROJECT EXPERIENCE

A 3-Way Superscalar R10K-Style Out-of-Order Processor Feb. 2021 - April. 2021
Final project of EECS 470: Computer Architecture

Project: Build a 3-way Superscalar R10K-Style Processor with a few advanced features: Non-blocking L1 Data cache, Dynamic branch prediction, Instruction prefetching.

- Implement Data Cache, Memory Controller, Retire Stage, Map Table/Arch. Map Table, Branch FU, and do debugging.
- Analysis and optimize the performance of our processor.

An Optimized Compiler for Decaf Language Jan. 2021 - April. 2021
Final project of EECS 483: Compiler Construction

Project: Implemented a working compiler with source language Decaf and target language MIPS using flex (lexical analysis), yacc/bison (syntax analysis), and C/C++ (other parts).

- Build and optimize the compiler by gradually implemented scanner, parser, IR generator and Mips generator.
- Chose Chaitin's Algorithm for register allocating and implemented a few IR optimization including Dead Code Elimination, Common Subexpression Elimination and Constant Propagation.

TEACHING EXPERIENCE

Honors Physics I (VP160), Teaching Assistant, Shanghai Jiao Tong University — May 2020

SELECTED AWARDS

Dean's Honors List, University of Michigan — Jan. 2021
Silver Model, University Physics Competition 2019 — Jan. 2020
Student Development Scholarship of SJTU 2019-2020 — Jun. 2020
Honorable Mention, Mathematical Contest of Modeling 2019 — Apr. 2019

SKILLS

- **Programming Language:** C/C++, Verilog/System Verilog, Python, MATLAB, Bash, yacc, bison
- **Electronic Circuit Simulation:** Xilinx Vivado, Cadence Virtuoso, Pspice, Proteus, NI Multisim