

Haoyang Zhang

FIRST-YEAR PH.D. STUDENT, COMPUTER SCIENCE, UNIVERSITY OF ILLINOIS URBANA-CHAMPAIGN

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Education

University of Illinois Urbana-Champaign

Urbana, IL, U.S.

PH.D. COMPUTER SCIENCE

Aug. 2022 - Present

- Advisor: prof. Jian Huang
- Research Interest: Computer Architecture, Algorithm/Hardware co-design, Heterogeneous Memory/Storage Systems

University of Michigan

Ann Arbor, MI, U.S.

B.S.E. COMPUTER SCIENCE (DUAL DEGREE)

Aug. 2020 - Apr. 2022

- Advisor: prof. Baris Kasikci

Shanghai Jiao Tong University

Shanghai, China

B.S.E. ELECTRICAL AND COMPUTER ENGINEERING (DUAL DEGREE)

Sep. 2018 - Aug. 2022

- Advisor: prof. Weikang Qian

Publications

Debugging in the Brave New World of Reconfigurable Hardware.

Jiacheng Ma, Gefei Zuo, Kevin Loughlin, **Haoyang Zhang**, Andrew Quinn, Baris Kasikci. (ASPLOS 2022).

Scheduling Information-Guided Efficient High-Level Synthesis Design Space Exploration.

Xingyue Qian, Jian Shi, Li Shi, **Haoyang Zhang**, Lijian Bian, Weikang Qian. (ICCD 2022).

Teaching

SHANGHAI JIAO TONG UNIVERSITY

SU. 2022 **Computer Architecture (VE470)**, Teaching Assistant

SU. 2020 **Honors Physics (VP160)**, Teaching Assistant

Selected Awards and Honors

2021 **Roger King Scholarship**, University of Michigan

2021 **University Honors**, University of Michigan

2021, 2020 **Dean's List**, University of Michigan

2020, 2019 **Undergraduate Academic Excellence Scholarship**, Shanghai Jiao Tong University

2020 **Student Development Scholarship**, Shanghai Jiao Tong University

2019 **Silver Medal**, University Physics Competition

Research Experience

PlatformX Group - University of Illinois Urbana-Champaign

Urbana, IL, U.S.

ADVISOR: JIAN HUANG

Aug. 2022 - Present

• Project: Break the GPU Memory Wall with Smart Data Migrations

Design a novel GPU-CPU-SSD unified memory system with smart data migrations to break the memory wall for large-scale DNN models training on GPU, with high performance and good programmability.

Efeslab - University of Michigan

Ann Arbor, U.S.

ADVISOR: BARIS KASIKCI

Apr. 2021 - Apr. 2022

• Project: Reconfigurable Hardware Debugging

Studied bugs in existing FPGA designs and produced a testbed to reliably reproduce each bug. Helped build a novel collection of hybrid static/dynamic program analysis and monitoring tools for debugging FPGA designs. Implemented the simulator for SignalCat, a recorder and printer on actual hardware deployments.

CELAB - University of Michigan

Ann Arbor, U.S.

ADVISOR: TODD AUSTIN

Sept. 2021 - Dec. 2021

• Project: A Spectre Attack Targeting Compiler-based Protections. (Also EECS573 Course Project)

Found a way to subvert compiler-based LFENCE Spectre protections by identifying and jumping over the speculation barrier code inserted by the compiler, basically by exploiting the partial-tagged and partial-data BTB to conduct a special kind of intra-process, out-of-place Spectre attack.

Emerging Computing Technology Laboratory – Shanghai Jiao Tong University

ADVISOR: WEIKANG QIAN

Shanghai, China

Jan. 2021 – Aug. 2022

- **Project: MiniHLS: A Simple High-Level Synthesis Tool**

Helped to build an HLS tool based on LLVM, which can compile C functions to Verilog modules, having multiple features including loop optimization, tcl file parsing, etc. Test the HLS output on FPGA, do post-synthesis debugging/on-board verification, and hence modify the source code.

Industry Experience

T-head Division, Alibaba Cloud

MENTOR: YUNHAI SHANG

Hangzhou, China

Jul. 2021 - Aug. 2021

- **Position: Software Research & Development Intern**

- **Project:** Implement the optimization for the jpeg library for RISC-V vector processors.

Skills

Language C/C++, Verilog/SystemVerilog, CUDA, Yacc, Murphi, Python, MATLAB, TeX

ISAs RISC-V, X86, LEGv8, MIPS, LC2K

EDA Tools Synopsys VCS, Verilator, Xilinx Vivado

Community Services

SERVICE

2019 SJTU Student Science and Technology Innovation Association, Consultant

2019 JI Young Volunteers Association, Minister

VOLUNTEERING

2019 Yunnan San He Junior High School Volunteer Teaching Team, Team leader