Haoyang Zhang

Undergraduate / Computer Engineering
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EDUCATION

University of Michigan, Ann Arbor, US   Sep. 2020 – May. 2022 (Expected)

B.SE. Computer Engineering (Dual Degree)
- Cumulative GPA: 4.000/4.000
- Course Works: Intro. Computer Organization (A), Digital Integrated Circuit (A), Data Structure & Algorithms (A)

Shanghai Jiao Tong University (UM-SJTU JI), Shanghai, China   Sep. 2018 – Aug. 2022 (Expected)

B.S. Electrical and Computer Engineering (Dual Degree)
- Cumulative GPA: 3.718/4.000, with rank 38/245
- Course Works: Programming & Data Structures(A+), Intro. Logic Design(A), Intro. Circuits(A), Honors Physics(A, A+)

RESEARCH EXPERIENCE

Trusted Cloud Group – Shanghai Jiao Tong University   Shanghai, China

Undergraduate Researcher (Advisor: Dr. Zhengwei Qi)   Dec. 2020 – Present
- **Project: Optimizing FPGA-based Accelerator Design for Neural Network Algorithms.**
  - **Objectives:** Various accelerators for CNN have been proposed based on FPGA platform because it has advantages of high performance, reconfigurability, and fast development round. The goal of this project is to build an FPGA-based Accelerator for some specific neural network algorithms.
  - **Responsibility:** Study and be proficient in Xilinx Vivado HLS design, build part of the accelerator (architectural support of Fast Fourier Transformation), conduct simulations and tests.

Emerging Computing Technology Laboratory – Shanghai Jiao Tong University   Shanghai, China

Undergraduate Researcher (Advisor: Dr. Weikang Qian)   Jan. 2021 – Present
- **Project: MiniHLS: A Simple High-Level Synthesis Tool.**
  - **Objectives:** High-level synthesis raises the design abstraction level and allows rapid generation of optimized RTL hardware. The goal of this project is to build a simple HLS tool based on LLVM, which can compile C functions to Verilog modules, and automatically conduct some optimization.
  - **Responsibility:** Test the HLS output on FPGA, do post-synthesis debugging and hence modify the source code of our Mini-HLS.

SELECTED PROJECT EXPERIENCE

"Trailblazer": Mars Explorer Robotic Dog, Shanghai, China   Mar. 2019 - Aug. 2019

Team Leader

   Project: Built a robotic dog with paper main structure, which has several moving functions.
- Assigned the tasks, design the main structure and the electronic control system, set progress checks.
- Designed and manufacture the circuit using Arduino to implement sound tracking function.

TEACHING EXPERIENCE

Honors Physics I (VP160), Teaching Assistant, Shanghai Jiao Tong University   May 2020

SELECTED AWARDS

Dean's List, University of Michigan   Jan. 2021

Silver Model, University Physics Competition 2019   Jan. 2020

Student Development Scholarship of SJTU 2019-2020   Jun. 2020

SKILLS

- **Programming Language:** C/C++, Verilog/System Verilog, Python, MATLAB, Bash
- **Electronic Circuit Simulation:** Xilinx Vivado, Cadence Virtuoso, Pspice, Proteus, NI Multisim