Haoyang Zhang

third-year Ph.D. student, Computer Science, University of Illinois Urbana-Champaign

zhang402@illinois.edu | hieronzhang.github.io | HieronZhang | @HaoyangZhang19

Education

University of Illinois Urbana-Champaign *Urbana, IL, U.S.*

PH.D. Computer Science *Aug. 2022 - Present*

- Advisor: prof. Jian Huang
- Research Interest: computer architecture and system software, with a focus on building memory/storage systems and architecture for hardware accelerators and AI systems.

University of Michigan *Ann Arbor, MI, U.S.*

B.S.E. Computer Science (Dual Degree) *Aug. 2020 - Apr. 2022*

- Advisor: prof. Baris Kasikci

Shanghai Jiao Tong University *Shanghai, China*

B.S.E. Electrical and Computer Engineering (Dual Degree) *Sep. 2018 - Aug. 2022*

- Advisor: prof. Weikang Qian

Publications

SkyByte: Architecting An Efficient Memory-Semantic CXL-based SSD with OS and Hardware Co-design.
Haoyang Zhang*, Yuqi Xue*, Shaobo Li, Yirui Eric Zhou, Jian Huang. (HPCA 2025).

G10: Enabling An Efficient Unified GPU Memory and Storage Architecture with Smart Tensor Migrations.
Haoyang Zhang*, Yirui Eric Zhou*, Yuqi Xue, Yiqi Liu, Jian Huang. (MICRO 2023).

Debugging in the Brave New World of Reconfigurable Hardware.
Jiacheng Ma, Gefei Zuo, Kevin Loughlin, **Haoyang Zhang**, Andrew Quinn, Baris Kasikci. (ASPLOS 2022).

Scheduling Information-Guided Efficient High-Level Synthesis Design Space Exploration.
Xingyue Qian, Jian Shi, Li Shi, **Haoyang Zhang**, Lijian Bian, Weikang Qian. (ICCD 2022).

Research Experience

PlatformX Group - University of Illinois Urbana-Champaign *Urbana, IL, U.S.*

Advisor: Jian Huang *Aug.2022 - Present*

- **Project: SkyByte: Architecting An Efficient Memory-Semantic CXL-based SSD with OS and Hardware Co-design (Published in HPCA'25)**
  The CXL-based solid-state drive (CXL-SSD) provides a promising approach towards scaling the main memory capacity at low cost. However, the CXL-based SSD has faced performance challenges due to the long flash access latency and unpredictable events such as garbage collection in the SSD device, stalling the host processor and wasting compute cycles. In this work, we present SkyByte, an efficient CXL-based SSD that employs a holistic approach to address the aforementioned challenges by co-designing the host operating system (OS) and CXL-SSD controller.
- **Project: G10: Enabling An Efficient Unified GPU Memory and Storage Architecture with Smart Tensor Migrations (Published in MICRO'23)**
  We present a unified GPU memory and storage architecture driven by the fact that DNN workloads are highly predictable. G10 integrates the host memory, GPU memory, and flash memory into a unified memory space, to scale the GPU memory capacity while enabling transparent data migrations. G10 utilizes compiler techniques to characterize the tensor behaviors in DNN workloads to schedule data migrations in advance by considering the available bandwidth of flash memory, host memory, and interconnections.

Efeslab - University of Michigan *Ann Arbor, MI, U.S.*

Advisor: Baris Kasikci *Apr.2021 - Apr.2022*

- **Project: Reconfigurable Hardware Debugging (Published in ASPLOS'22)**
  Studied bugs in existing FPGA designs and produced a testbed to reliably reproduce each bug. Helped build a novel collection of hybrid static/dynamic program analysis and monitoring tools for debugging FPGA designs. Implemented the simulator for SignalCat, a recorder and printer on actual hardware deployments.

Emerging Computing Technology Laboratory – Shanghai Jiao Tong University *Shanghai, China*

Advisor: Weikang Qian *Jan. 2021 – Aug. 2022*

- **Project: MiniHLS: A Simple High-Level Synthesis Tool (Published in ICCD'22)**
  Helped to build an HLS tool based on LLVM, which can compile C functions to Verilog modules, having multiple features including loop optimization, tcl file parsing, etc. Test the HLS output on FPGA, do post-synthesis debugging/on-board verification, and hence modify the source code.

Industry Experience

T-head Division, Alibaba Cloud *Hangzhou, China*

Mentor: Yunhai Shang *Jul. 2021 - Aug. 2021*

- **Position: Software Research & Development Intern**
  - **Project:** Implement the optimization for the jpeg library for RISC-V vector processors.

Teaching

University of Illinois Urbana Champaign

SP. 2025, FA. 2024 **Computer Architecture (CS233)**, Teaching Assistant

Shanghai Jiao Tong University

SU. 2022 **Computer Architecture (ECE4700J)**, Teaching Assistant

SU. 2020 **Honors Physics (VP160)**, Teaching Assistant

Selected Awards and Honors

2021 **Roger King Scholarship**, University of Michigan

2021 **Univerisity Honors**, University of Michigan

2021, 2020 **Dean's List**, University of Michigan

2020, 2019 **Undergraduate Academic Excellence Scholarship**, Shanghai Jiao Tong University

2020 **Student Development Scholarship**, Shanghai Jiao Tong University

2019 **Silver Medal**, University Physics Competition

Selected Projects

3-Way Superscalar R10K-Style Out-of-Order Processor Core *Ann Arbor, U.S.*

Capstone. Advisor: Jon Beaumont *Feb. 2021 - April. 2021*

- Build a 3-way Superscalar R10K-Style Processor with a few advanced features: Non-blocking L1 Data cache, Dynamic branch prediction, Instruction prefetching, etc.
- Implement our processor using SystemVerilog. Analysis and optimize the performance of our processor.

An Optimized Compiler for Decaf Language *Ann Arbor, U.S.*

Advisor: Lingjia Tang *Jan. 2021 - April. 2021*

- Implement a compiler with source language Decaf and target language MIPS using flex (lexical analysis), yacc/bison (syntax analysis), and C/C++ (other parts).
- Implemented a few IR optimizations including Dead Code Elimination, Common Subexpression Elimination, etc.

Skills

Language **C/C++, HLS, Verilog/SystemVerilog, CUDA, Yacc, Murphi, Python, MATLAB, TeX**

ISAs **RISC-V, X86, LEGv8, MIPS, LC2K**

EDA Tools **Synopsys VCS, Verilator, Xilinx Vivado**

Community Services

Leadership

2019 **JI Young Volunteers Association**, Minister

Volunteering

2019 **Yunnan San He Junior High School Volunteer Teaching Team**, Team leader

Academic Services

Artifact Evaluation Committee

2024 **HPCA 2025** , Artifact Reviewer