Implementation of High Performance Hardware Architecture of Face Recognition Algorithm Based on Local Binary Pattern on FPGA

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Abstract

This paper presents a high performance hardware architecture of face recognition algorithm based on local binary pattern. Through the software implementation of the algorithm, the optimization of the data's widths and block size can be obtained. Then a hardware structure based on the algorithm is proposed. The histogram statistic and recognition can be handled concurrently with a ping-pang memory and the data throughput can be increased with the pipeline and parallel processing units. The proposed architecture is implemented in the Xilinx Virtext-7 FPGA VC707 evaluation board and is verified with a large number of training pictures. The design costs 5975 LUTs and the clock frequency can be up to 233MHz. For a library with one hundred thousand faces, the proposed design can recognize 1.7 faces per second and its recognition speed is 74 times faster than the software's in the general CPU platform.

Keywords-FPGA; Face recognition; Local Binary Pattern; Hardware architecture;

1. Introduction

As a research hotspot in recent years, face recognition has been widely used in the area of identification and verification, information security and so on and quantities of commercial face recognition systems have also been produced [1]. Nowadays, the number of face library picture utilized in the face recognition system becomes increasingly large, which may reach tens of thousands, or even hundreds of thousands. In order to meet the real-time requirement with such a large amount of data, this paper implements the algorithm by designing a high performance hardware architecture.

The face recognition algorithm proposed in this paper is based on local binary pattern (LBP) which is proposed by Timo Ojala [2]. LBP operator is widely applied in many image analysis algorithms to describe the texture information of picture. LBP operator is able to distinguish pictures of different textures effectively with gray-scale invariance [3]. The recognition rate can reach 95% according to some related experimental results [4].

Some related work has been done to realize the face recognition algorithm based on LBP. However most of them [4-9] focus on the recognition accuracy and a few mentions the recognition speed in the CPU platform. In paper [4], the system recognizes around one picture per second on 1800MHz AMD Athlon running Linux from FERET database. The results mentioned in paper [7] draw the similar conclusion. It should be mentioned that the number of train library picture is no more than 5000 in experiment above. And the papers that mention the implementation of face recognition based on LBP are even fewer. In paper [6], the application of LBP algorithm based on AccelDSP in face recognition is presented. However, both of them don't research on the recognition speed on condition of tens of thousands of train pictures.

A high performance hardware structure of face recognition algorithm based on local binary pattern is presented in this paper and then realized in FPGA. Compared with the implementation in the CPU platform, our contributions are:

1) Pipeline architecture is proposed. When calculating the LBP values, it is doing the histogram statistic as well.
2) Parallel arithmetic units are used to calculate the Chi square statistic distance and make the identification, which greatly increases the degree of parallel.
3) Compared with the implementation in CPU platform, the recognition speed with our hardware architecture is greatly increased when the number of face library picture is huge.

The rest of this paper is organized as follows: Section 2 introduces the face recognition algorithm based on local binary pattern briefly and presents the design of hardware architecture at length. Then, the experience results of hardware architecture realized on the Xilinx Virtex7 FPGA device are showed in section 3. And section 4 makes the conclusion.

2. Proposed hardware architecture

In this section, a proposed hardware architecture is presented. Before the design of architecture the related algorithm is introduced. Besides, the accuracy test and fixed-pointed test are made to optimize the architecture design.

2.1 Algorithm for architecture

The theory of face recognition algorithm based on local binary pattern is demonstrated in this part, which can be referred from paper [4] [5].

The whole face recognition process can be divided into four steps: LBP value calculation, region division, histogram statistic and prediction, which is shown in

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figure 1.

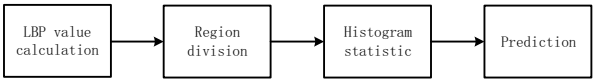

Figure 1. Face recognition process based on LBP

First, every pixel of the picture is translated into LBP code, which describes the variations of gray in the neighborhood, by using the LBP operator when a gray picture is input. In this paper, the neighborhood used in LBP operator is a circle of radius of 1 with 8 sampling points.

Then, the LBP picture which is produced in step one can be divided into several blocks with the same size in a certain way, which means the character of whole picture is divided and described with many local characters. The different region on the LBP picture contains different information, according to which a weight can be set with different regions.

After finishing the region division, LBP code histogram statistic is done for every region and the results are stored into a vector. Then combine the characteristic vectors of all regions and the characteristic vector of the whole face picture is produced which labels the identity of face picture. The general mathematical expression is

$$H_{i,j} = \sum_{x,y} I\{f_l(x,y) = i\} I\{(x,y) \in R_j\}$$
$$i = 0, \dots, n-1, j = 0, \dots, m-1 \quad (1)$$

in which $H_{i,j}$ means the size of bin_i of j-th region, m means the number of regions and $f_l(x,y)$ means the LBP code of the pixel with the coordinate of (x,y).

After the operation above, the characteristic vector of the test face picture is generated. Similarly, the characteristic vectors of face pictures in train library can be calculated and correspondingly put with identity labels.

After that comes the face identification. With the nearest-neighbour classifier, the train picture that has nearest distance from test picture will be found and the label of the train picture will be output as the identity label of test picture. Chi square statistic distance shown bellow is used in this paper.

$$\chi^2(S,M) = \sum_i \frac{(S_i - M_i)^2}{S_i + M_i} \quad (2)$$

2.2 Related work before the design of architecture

Before the design of hardware architecture, a recognition accuracy test in software platform is made to find the suitable way to divide the picture. And then a fixed-point test of the algorithm is done to fix the data width used in each module in order to guarantee the accuracy and recognition at the same time.

The picture database used in this test is the ORL database of face. This database contains 40 persons' face and everybody has 10 face pictures in different environment.

2.2.1 Recognition accuracy test

Table 1. Recognition accuracy test of algorithm

train picture / block size	1/person	3/person	5/person
2*2	72%	85%	92%
6*6	65%	88%	96%
8*8	63%	85%	94%
10*10	64%	82%	93%
12*12	58%	80%	89%

The recognition accuracy test result shows that the highest recognition rate reaches 96% when the train picture number is 5 per person. Besides, it's found that the block size has something to with the recognition rate and it reaches highest when block size is 6*6. It should be mentioned that the test result may be different with other database.

2.2.2 Fixed-point test

Table 2. Fixed-point test of algorithm

bit-width	recognition rate
32	91%
26	91%
24	89%
22	88%
20	88%
18	84%
16	77%

As the prediction module is the fateful part that influence the recognition rate, the fixed-point test of prediction data is done. We find that the recognition rate is highest when the data bit-width is 32.

2.3 Hardware architecture

This part mainly proposes the hardware architecture based on the algorithm mentioned above. As is shown in figure 2, the whole architecture can be briefly divided into three parts: LBP picture calculation, histogram statistic and prediction. The function of the architecture is to get the identity label of test picture input.

As mentioned before, the increasing number of train picture leads to the long recognition time. So characteristic vectors of five test pictures is produced when doing the LBP value calculation and histogram statistic and also the five test pictures are compared with

train pictures at the same time when making the prediction in order to save recognition time. Besides, the data bit-width of prediction module is 256 while the statistic data is 32, which improves the degree of parallelism. And when LBP value calculation is processing, the histogram statistic is doing simultaneously.

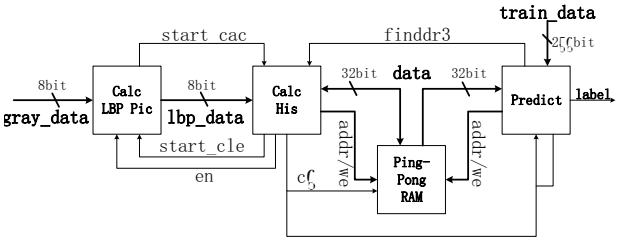

Figure 2. Overall architecture of algorithm

2.3.1 LBP value calculation module

The gray data input from external interface is first stored into line buffer that consists of three lines whose register number is as same as horizontal pixels of picture. As is shown in figure 3, the LBP code of every pixel can be produced by comparing R5 with the registers from R1 to R9. Every time one gray data input, the line buffer moves forward one, which means moving the calculation window to the right one columns in the original picture.

Then the LBP code produced will be sent to the next module. It is mentioned that when to input the gray data and when to make the calculation should be controlled by these control signals related.

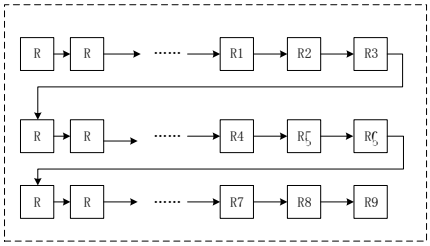

Figure 3. Line buffer of LBP value calculation module

2.3.2 Histogram statistic module

The brief architecture of this module is shown in figure 4, whose function is to do the histogram statistic by region and then save into the ping-pang RAM. When the LBP value is input from previous module, first address the ping-pong RAM according to the LBP value and its location in the picture. Then bring the statistic data out from RAM to add one and store back.

The ping-pong RAM composed of RAM1 and RAM2 in which one is for doing histogram statistic and the other is for prediction is used for storing the statistic data of five pictures. Both RAM1 and RAM2 consist of eight rams because the data bit-width is 256 in prediction while the statistic data is 32.

Besides, zeroing the rams after prediction is necessary because statistic data should be zero when starting doing the histogram statistic.

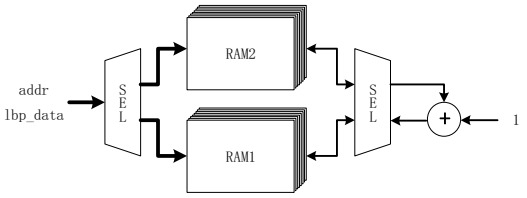

Figure 4. Architecure of ping-pang RAM

2.3.3 Prediction module

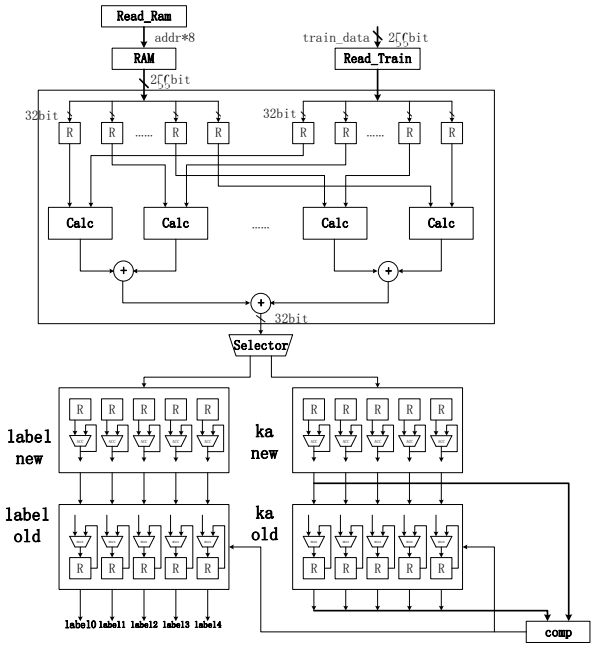

Figure 5. Architeture of prediction module

The architecture of prediction module is shown above. In this module, the characteristic vector data of five test pictures is input from ping-pong RAM while the train picture data from external interface. Then comes the Chi square statistic distance calculation of test pictures and train pictures by eight sets of summing units. After that compare test pictures with every train picture in face library according to the distance calculated.

The label-new registers are designed to store the identity label of train pictures temporarily while the label-old registers store the label of test picture and the ka registers store the Chi square statistic distance calculated. After finishing the comparison between five test pictures and one train picture, the label of test pictures will be updated according to comparison result. And when comparison between five test pictures and all the train pictures is finished, the label of test pictures is finally got.

3. Experimental result

This experiment focusses on how the number of train library pictures influence the speed of recognition. First we implement the algorithm in a server which is integrated with a core i7-3370 processor (3.4GHz) and evaluate the performance as well. Then we implement the designed architecture with the VC707 development board that contains a Xilinx XC7VX485T-2FFG1761C FPGA. The board provides a good development platform for high performance ASIC design with 1030 BRAMs, 303600 LUTs, and 607200 registers. The utilization of resource can be seen in table 3, which shows that the FPGA resource is enough for our design. Besides, the highest clock frequency can be up to 233.372MHz.

Table 3. Resource utilization of FPGA

	Used	Total	Utilization
LUT	5975	303600	1.96%
Registers	2263	607200	0.372%
DSPs	24	2800	0.857%
BRAM	128	1030	12.4%

The resolution of experiment picture is 60*60 and the experimental results in the case of 1000, 10000, 10000 pictures respectively is shown in table 4. It can be analyzed from the result that the recognition speed in the FPGA is 74 times faster than in CPU when the picture number is same. And the recognition speed gradually double down with the increase of number of face images. When the number reaches hundreds of thousands, the speed in CPU has dropped to 0.02 per second, which cannot meet the real-time requirement. The speed in FPGA has also dropped to about 1.7 per second, which is able to meet the requirement in the face recognition system.

Table 4. Comparison with sever in recognition speed

picture number	speed（/sec）		speed-up
	FPGA	CPU	
1,000	174	2.33	74.7
10,000	17.4	0.234	74.4
100,000	1.74	0.0235	74.0

In paper [6], the experimental results show the system is able to process about 100 pictures per second when the train picture number is about 1200 pictures with the resolution of 116 * 116. However, their work is concerned more about the feature extraction not the recognition speed. So it's necessary to evaluate the recognition speed performance of hardware architecture on condition of numerous train pictures.

4. Conclusion

In this paper, we first do some research on the face recognition algorithm based on local binary pattern and the procedure is summarized. Then we propose a high performance hardware architecture based on the algorithm in order to speed up the recognition. The number of train library picture is one of the fateful factor that restrict the recognition speed. We propose some specific designs to solve it. First, we calculate the characteristic vector of five test pictures when doing the histogram statistic and compare five test pictures with train pictures when doing prediction. Then, we utilize eight operation units when calculating the Chi square statistic distance to improve the degree of parallel. Besides, pipeline is designed for doing the LBP value calculation and histogram statistic at the same time. Finally, we proposed ping-pong RAM to respectively store the statistic data and make the prediction.

The hardware architecture is implemented on Vertex-7 FPGA and the performance experimental result proves that the recognition speed in FPGA is about 74 times faster than in CPU platform.

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