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Upgrade of the ATLAS Level-1 Trigger with event topology information

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Abstract. The Large Hadron Collider (LHC) in 2015 will collide proton beams with increased luminosity from 10^{34} up to $3 \times 10^{34} cm^{-2} s^{-1}$. ATLAS is an LHC experiment designed to measure decay properties of high energetic particles produced in the protons collisions. The higher luminosity places stringent operational and physical requirements on the ATLAS Trigger in order to reduce the 40MHz collision rate to a manageable event storage rate of 1kHz while at the same time, selecting those events with valuable physics meaning. The Level-1 Trigger is the first rate-reducing step in the ATLAS Trigger, with an output rate of 100kHz and decision latency of less than $2.5\mu s$. It is composed of the Calorimeter Trigger (L1Calo), the Muon Trigger (L1Muon) and the Central Trigger Processor (CTP). By 2015, there will be a new electronics element in the chain: the Topological Processor System (L1Topo system).
The L1Topo system consist of a single AdvancedTCA shelf equipped with three L1Topo processor blades. It will make it possible to use detailed information from L1Calo and L1Muon processed in individual state-of-the-art FPGA processors. This allows the determination of angles between jets and/or leptons and calculates kinematic variables based on lists of selected/sorted objects. The system is designed to receive and process up to 6Tb/s of real time data. The paper reports the relevant upgrades of the Level-1 trigger with focus on the topological processor design and commissioning.

1. Introduction

ATLAS[1] is one of the multi-purpose experiments at the Large Hadron Collider (LHC) at the European Organization for Nuclear Research CERN in Switzerland. LHC collides bunches of protons at a frequency of 40 MHz. The ATLAS Trigger system filters out collision events without physics interest, lowering the average output rate to a level of few hundreds Hz. It is realized by means of multi level trigger. During Run I, the Level-1 Trigger uses muon and calorimeter signals to determine "Regions of Interest" (RoI) and, based on counting clusters of jets, τ, electron/γ and missing E_T at various energy thresholds, reduces the event rate to 75 kHz. The Level-2 Trigger uses Level-1 candidates and look at detailed physics properties to achieve a further reduction in rate to 2-3 kHz. Finally a third level (event filter) uses full event information, and decides upon storage of the event for offline analysis with a final rate of 300-400 Hz. This paper focuses on the Level-1 upgrade, further description of Level-2 and event filter can be found in [2]. The ATLAS Level-1 Trigger is a fixed latency, 40 MHz, pipe-lined, synchronous system, built

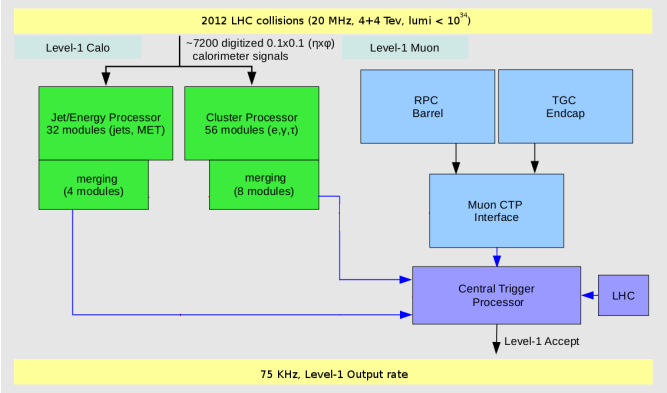

Figure 1. The Run 1 ATLAS Level-1 trigger system (2010-2103). Trigger information goes directly from the detector into the electronics cavern located in the ATLAS underground area. L1Calo: the signals go into pre-processors and the digitized information is then fed into the Jet/Energy and Cluster processors. L1Muon: signal from RPC and TGC detectors are processed into the MUCTPI processors to identify muon clusters. The results are then merged and sent to the Central Trigger Processor which sends the Level-1 Accept of the event.

to operate at the LHC design instantaneous luminosity of $\approx 10^{34} cm^{-2} s^{-1}$. The Level-1 trigger system consists of three sub-systems: The Level-1 Calo Trigger (L1Calo) [3], the Level-1 Muon Trigger (L1Muon) [4], and the Central Trigger Processor (CTP) [5]. The hardware of the Level-1 Trigger is primarily based on FPGAs and custom ASICs. Including cabling, the maximum latency budget of the Level-1 electronics chain is 2.5 μs. A simplified outline of the Level-1 trigger is show in Fig.1. In the CTP the trigger decision is made, based on thresholds received from L1Calo and L1Muon, and forwarded to the higher levels of the trigger. The L1Calo input data comes from 7200 analog "trigger towers". The trigger towers are built with a granularity of 0.1×0.1 in the $\eta - \phi$ range covered by the ATLAS electromagnetic and hadronic calorimeters (η is the pseudorapidity and ϕ the angle on the transverse plane to the proton beams). Digitization of the input signals and digital filtering is done on a mixed-signal Pre-Processor. Then the trigger tower signals are forwarded to two feature processors, namely the Cluster Processor (CP) and the Jet/Energy-sum Processor (JEP). The CP identifies electron, photon, tau and hadron candidates with a Transverse Energy E_T above a set of programmable thresholds [6]. The JEP identifies jet candidates and produces global sums of total, missing, and jet-sum E_T. Inside the CP and the JEP are the Common Merging Modules (CMMs) which counts the multiplicities of trigger objects and send the results to the CTP. Upon receiving the "Level-1 Accept" signal from the CTP, the coordinates in the $\eta - \phi$ plane for each trigger object (so called Regions of Interest , RoIs), which were identified by the feature processors at Level-1, are sent through Read-Out Drivers (RODs) on to the Level-2 Trigger. The L1Muon input data comes from 800k Resistive Plate Chamber (RPC) strips in the barrel region and Thin Gap Chambers (TGCs) in the endcap regions. Multiplicities for six momentum thresholds are measured by coincident hits in the RPC and TGC planes. The logic for multiplicity counting of the different thresholds is provided by the Muon Central Trigger Processor Interface (MUCTPI) [4].

2. Level-1 topological trigger

From 2015 (Run 2), the increased instantaneous luminosity and collision frequency implies background rates higher than the Level-1 trigger was designed for. To maintain the Level-1 trigger rates at the current level without unduly raising thresholds or prescaling trigger streams

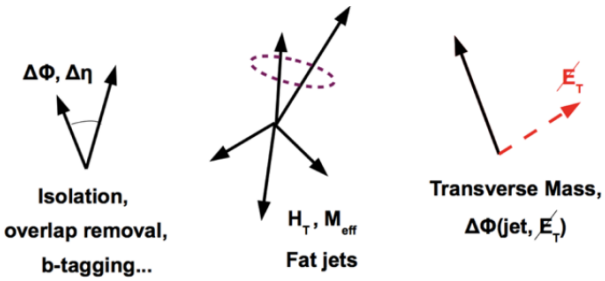

Figure 2. Examples of topologies used for topological trigger decisions. Angular distributions are illustrated (left), hardness of the interaction or sums of energy or momenta (center) and invariant mass can be used to do topological cuts.

of physics interest, the selections can't be based just on counting of physics objects. To achieve additional background rate reduction at Level-1, the topological information on jet or muon direction in space can be used. For doing so, the CMMs have been replaced by new "CMX" [7] modules capable of receiving and processing the high-speed backplane data and transmitting the real-time data to a completely new element in the Level-1 chain: the Topological Processor (L1Topo). An outline of the upgraded Level-1 Trigger is shown in Fig.3. The L1Topo allows a trigger decision to be made using more than just p_T or E_T whose thresholds would be impossible to maintain in 2015 after the LHC upgrade. This is essential because interesting physics events have specific topologies (see Fig.2). These decisions can be loosely assigned to three categories defined as: angular separation, invariant mass, and hardness of interaction (see Fig.2). L1Topo provides high optical input bandwidth and powerful state-of-the-art FPGAs, receiving and processing L1Calo and L1Muon information within 200 ns.

L1Topo processes real-time event information based on the geometric and kinematic relationships between Trigger OBjects (TOBs) (i.e. electrons/photons, muons, jets, and taus), as well as event-level quantities such as missing transverse energy, invariant mass etc. Algorithms are implemented in VHDL and operated in parallel in FPGAs. L1Topo input data formats, the number of TOBs and corresponding input fibers from L1Calo and L1Muon subsystem have been defined and so has the data transmission protocol. In parallel with the hardware development, simulation studies on possible successfull topology are going on. Currently the proposed L1Topo algorithms have been implemented in VHDL.

3. L1Topo system

In this section the requirements of the L1Topo system and a brief description of the L1Topo blade design are given.

3.1. L1Topo requirements

Each L1Topo blade has to meet the target data rates on the optical real-time I/O of 6.4 Gb/s. For future use the real time input is designed to sustain up to 12.8 Gb/s. Total link bandwidth and logic resource availability are fixed by the chosen components and cannot be changed. The availability of resources was checked against the needs of the physics algorithms. Given the scalability of the system, more requirements implies more blades. At present, a L1Topo system equipped with two blades satisfies the requirements during Run2. Another requirement is the total latency of L1Topo system. The ATLAS latency envelope for Run2 implies a total latency of about 10 LHC bunch crossing (BC). Data receiving and transmission on Multi Gigabit Tranceiver (MGT) requires 4 BC. De-serialization into the LHC bunch clock domain takes one

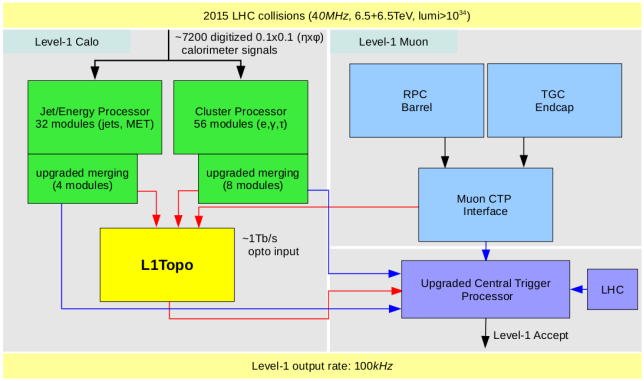

Figure 3. Simplified scheme of the upgraded Level-1 with the inclusion of the L1Topo subsystem.

BC. The algorithmic latency is up to 4 BC. CRC check sum decoding implies an extra 0.25 BC.

3.2. L1Topo implementation
The Topological Processor is a single processor shelf equipped with two processor blades. The processor blades are identical copies, with firmware adapted to the specific topologies to operate on.
Data are transmitted on optical fibers. After conversion to electrical representation, data are received and processed in FPGAs equipped with MGTs. In Run2 results are sent to the CTP electrically from the front panel to reduce latency. The L1Topo module is designed in AdvancedTCA form factor. A picture of a bare L1Topo blade before fiber assembly is shown in Fig.4.

3.2.1. Real-time data path ATCA Backplane zone 3 of L1Topo is used for real-time data transmission. The input data enter L1Topo optically through the backplane. The fibers are fed via four to five blind-mate backplane connectors that can carry up to 72 fibers each. In the baseline design 48-way connectors are used. The optical signals are converted to electrical signals in 12-fiber receivers. For reasons of design density miniPOD receivers are used. The electrical high-speed signals are routed into two FPGAs, where they are de-serialized in MGT receivers into the FPGA fabric. The two FPGAs operate on their input data independently and in parallel. High bandwidth, low latency parallel data paths allows real-time communication between the two processors. The final results are transmitted towards the CTP on both optical fibers and electrical cables. The electrical signals are routed via an extension mezzanine.

Data reception The optical data arrive on the main board on fourteen 12-fiber ribbons. Since the backplane connectors support multiples of 12 fibers, the optical signals are routed via pigtails, separating 48 fibers into groups of 12. Two 12-fiber ribbons to input the Level-1 Muon data are instead placed on the front panel. The opto-electrical conversion is performed in Avago miniPOD 12-channel devices. The opto receivers exhibit programmable pre-emphasis so as to allow for improvement on signal integrity for given track length. After just a few centimeters of electrical trace length, the multi-gigabit signals are de-serialized in the processor FPGAs. They allow for programmable signal equalization on their inputs. The exact transmission protocol is defined and include standard 8b/10b encoding (envisaged for purpose of run length limitation

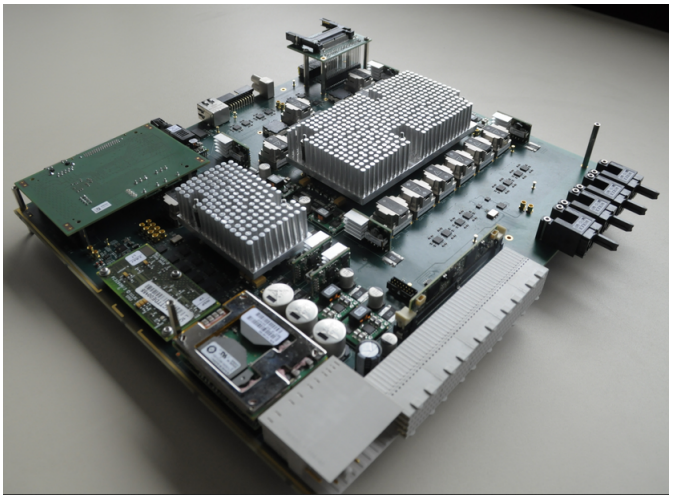

Figure 4. Bare L1Topo blade with no front panel and fiber assembly.

and DC balance) and a baseline speed of 6.4 Gb/s. The processors are supplied with required bias and termination voltages, as well as suitable reference clocks.

Data processing Topology data are processed in two XC7VX690T FPGAs. There is no data duplication implemented at PCB level. The two processors can communicate via their fabric interface to get access to data that cannot be received directly via the multi-gigabit links. Those inter-FPGA which link differential pairs are envisaged to be used at 1 Gb/s. This sets the parallel connectivity to 238 Gb/s of aggregate bandwidth, corresponding to 24×238 bits per BC (5712 bits). In this way more than 250 generic trigger objects (TOBs) can be shared (more than all input TOBs). Since this data path adds approximately one bunch tick of latency, in Run-II, data is fan out optically at the source so that both processors are supplied with the same data. Due to the large amount of logic resources in the chosen FPGAs, a signicant number of algorithms are expected to be run in parallel on real-time data. The expected output to the CTP consists of 32 bits per processor, indicating whether a specific topological algorithm passed. The resulting trigger data are expected to exhibit a rather small volume. As required by future upgrades post Run2, a single fiber-optical ribbon connection per processor FPGA, running through the front panel of the blade, is provided for optical transmission to the CTP.

3.2.2. Clock distribution The operation of the real-time data path requires low-jitter clocks throughout the system. For synchronous operation, data transmitters operates with clean multiples of the LHC bunch clock. The L1Topo blade is designed for 40.0789 MHz operation of the real-time data path only. The MGTs are clocked off multiples of the LHC clock. The jitter on the MGT bunch clock path is tightly controlled with help of a PLL device. The clock fan-out chips chosen are devices with multiple signal level input compatibility, and output levels suitable for their respective use, either LVDS or CML.

Pre-configuration access and blade control L1Topo is a purely FPGA-based ATCA blade. All communications channels are controlled by programmable logic devices and become functional only after successful device configuration. The ATLAS standard LAPP IPMC (mini-DIMM format) mezzanine is mounted on L1Topo which perform the initial step of blade initialization and communicates to the shelf via an I2C port (IPMB) available on all ATCA blades. Module

control is provide by IP connectivity via an Ethernet port in the front panel wired via an SGMII Phy device. Further Ethernet connectivity is provided on the backplane in zone 2 (redundant base interface).

FPGA configuration The baseline (legacy) FPGA configuration scheme on L1Topo is via a CompactFlash card and the Xilinx System ACE chip. The required board-level connectivity is implemented on L1Topo, to write the flash cards through a network connection to the FPGAs, once they are configured. A local SPI memory and SD card are also wired in the design to provide alternative configuration methods. Both devices are placed on a mezzanine to adapt for future changes.

Monitoring and control The default ATCA monitoring and control path is via I2C links in zone 1. The backplane I2C port (IPMB) is connected to the IPMC DIMM. On L1Topo, configured FPGAs can be monitored for die temperature and internal supply voltage.

4. L1Topo commissioning post-production

The L1Topo blades after assembly have been subjected to rigorous tests. After an initial power-up test a boundary scan is performed to control the electrical connections among FPGAs and the external interfaces. A jitter analysis is done on all PLL devices including the TTC decoded clock before and after a jitter cleaner. The TTC is also checked to ensure that the duty cycle is within specifications. Following those basic functional tests, the module performance was measured.

4.1. Power

Power ripple on low voltages supplies are measured to be within specification. The blade after configuration and firmware load, is checked for voltage drop and the maximum current absorbed is measured on individual suppy to verify is within the limit. Voltage and current are monitored by means of sensors. Power tests showed the module would sustain the operation at 12.8 Gb/s envisage by 2018.

4.2. IPbus module control

IPbus has been adopted for blade control. Read and write access at 400 MHz DDR into a block of RAM is used to estimate potential issues in the communication to the master (control FPGA) and the slaves (processors). The test is performed using a direct ethernet link into the module front panel to simulate the experimental condition and the error rate measured over several minutes.

4.3. High Speed Links

The L1Topo blades are equipped with two XC7VX690T-3 devices. This type of devices supports data rates (in terms of LHC clock multiples) up to 12.8 Gb/s (80 tranceivers per device). The performance has been tested at the baseline 6.4 Gb/s by means of eye diagrams and bathtub profiles. Error free data transmission was observed and the bathtub profile above 50%. An example of bathtub measured at 12.8 Gb/s is shown in Fig.5. An upper limit on aggregate data transmission was measured on a single blade and the bit error rate limit was set below $\times 10^{-18}$ with no errors observed. Systematic tests to optimize MGT and miniPOD parameters have been performed.

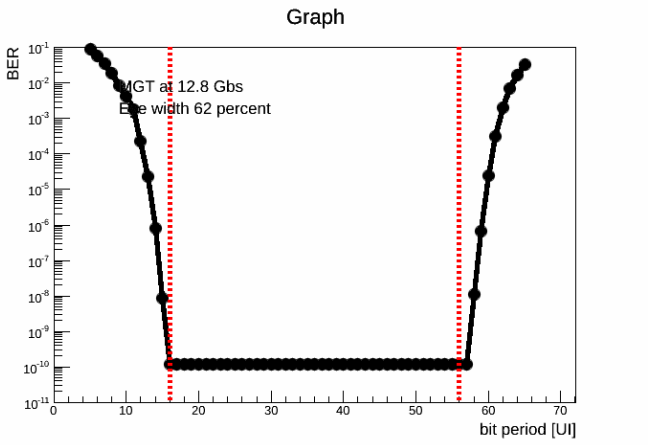

Figure 5. Bit error rate measured at 12.8 Gb/s over a bit period in steps of 1.3 ps. The picture is called "bathtube" and the plateau correspond to the error free region and qualify the quality of the link.

5. L1Topo commissioning in ATLAS

After qualifying the blade functionalities and basic performance, the blades were transported to CERN and integrated in the ATLAS trigger infrastructure. The commissioning in ATLAS aims at verifying the external interfaces and developing the software necessary to configure and run the L1Topo sub-system with the entire ATLAS detector.

5.1. Level-1 Calorimeter Input (L1Calo)

Data transmission and signal integrity have been tested by means of bathtub profiles at 6.4 Gb/s. Error free data transmission is observed and bathtub profiles shown an excellent average opening above 55%. The routing through the fiber plant and the data format have been tested.

5.2. Level-1 Muons Input (L1Muon)

The L1Muon provides in Run2 only high graularity data on just three fiber to individual L1Topo processors. The baseline speed is of 6.4 Gb/s. As for the L1Calo, data transmission and signal integrity have been tested by means of bathtub profiles at 6.4 Gb/s. Error free data transmission is observed and bathtub profiles shown an excellent average opening above 55%. The routing through the fiber plant and the data format have been tested.

5.3. L1Topo output

The real time output of a single L1Topo blade consists of 64 bits per BC to the Central Trigger Processor (CTP). For latency reason during Run-2 those bit run over a 68 pin high density SCSI cable. The L1Topo blade is designed to provide twelve high speed optical links to the CTP but this will be relevant in the future. Individual electrical link to the CTP is tested to guarantee timing calibration and error free signal transmission.

5.4. L1Topo Readout

L1Topo provide its own readout. Up to twelve S-Link are emulated into the control FPGA firmware and the links run through two miniPOD (one receiver and one transmitter) fanned into 12 duplex on the L1Topo front panel. Currently the readout firmware has been written and

the communication to the systems downstream (ROS and RoIB) established. The logic of the readout is under final firmware debug.

6. Conclusions

In this document, an overview of the L1Topo system is presented. The L1Topo is a completely new element of the ATLAS Level-1 Trigger. With L1Topo is possible for the first time to apply topological cuts at Level-1 using detailed information from calorimeters and muon sub-detectors. The L1Topo requires additional firmware and hardware upgrades to the existing L1Calo and L1Muon systems which have been here only marginally mentioned. L1Topo receives input from new CMX modules which are part of the L1Calo upgrade. It uses these inputs to make topological based decisions, thus allowing much important physics to be saved from the alternative of raising the p_T and E_T thresholds. Real-time L1Topo output is sent to the CTP, where the final Level-1 decision is taken. The crucial aspect here is the design of the topology algorithms, including optimization of bandwidth, FPGA resources and latency. The L1Topo system has been installed and integrated and currently is in its final commissioning phase.

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