ECE M16 Homework 2

Lawrence Liu

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Problem 1

(a)

It will toggle, if the latch is reset, ie Q=0 and $\bar{Q}=1$. Then the output will be Q=1 and $\bar{Q}=0$ following the clock pulse

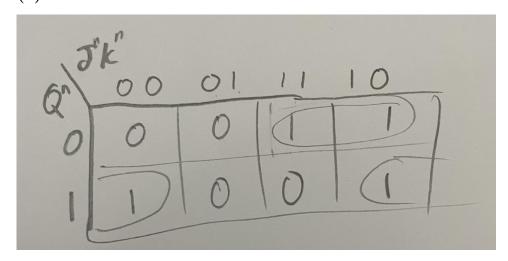
(b)

if C=0 it will latch, but with C=1 there will be following transition table

J	K	Q current	Q next
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Therefore this is like a SR latch however it will toggle at J=K=1, unlike the SR latch.

(c)



$$Q^{n+1} = J^n.\overline{Q^n} + \overline{K^n}.Q^n$$

(d)

The transition table of the D latch is:

$\mid C \mid$	$\mid D \mid$	Q next
0	X	Q
1	0	0
1	1	1

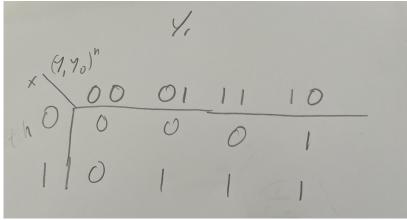
Which is the same as the transition table of the JK latch with $J=\bar{K}=D.$

С	J=D	$K = \bar{D}$	Q next
0	X	X	Q
1	0	1	0
1	1	0	1

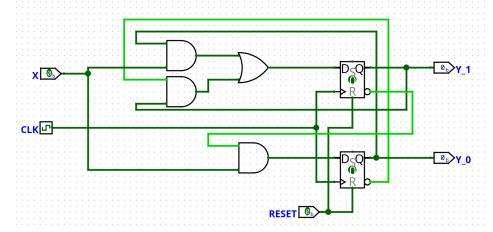
Problem 3

(a)

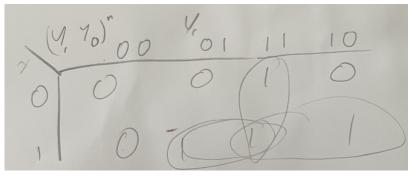
The kmaps for assignment 1 are:



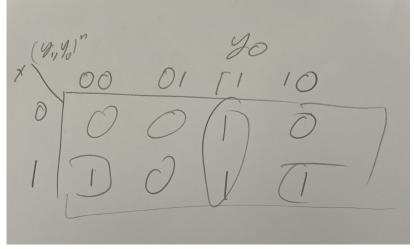
For y_1 and y_0 respectively, therefore the corresponding circuit is:



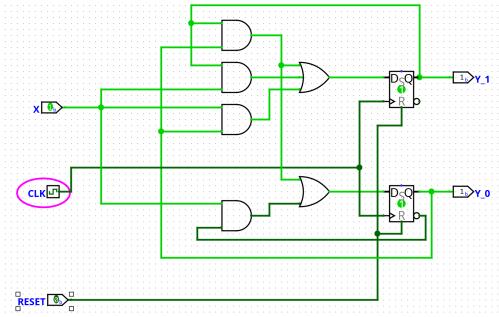
Likewise for assignment 2, the kmaps are:



and



For y_1 and y_0 respectively, therefore the corresponding circuit is:

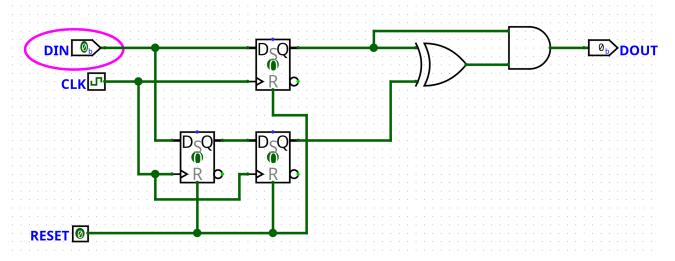


(b)

Therefore assignment 1 is more economical since it uses less gates.

Problem 4

Because we can use D flip flops to delay a signal, we have the following circuit

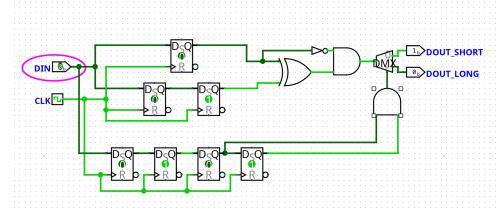


With the following timing diagram

Signal Name	Signal Value	1945.0 s	1950.0 s	1955.0 s 19	1965.0 s	1970.0 s	1975.0 s 1980.0 s 1:
CLK	-	$\int_{1}^{1} \int_{0}^{1} \int_{1}^{0} \int_{1}^{1} \int_{0}^{1} \int_{1}^{1} \int_{0}^{1} \int_{0$	0 1 0 1 0	$\int_1 \int_0 \int_1 \int_0 \int_0 \int_0 \int_0 \int_0 \int_0 \int_0 \int_0 \int_0 \int_0$	1 0 1 0 1 0 1	0 1 0 1 0 1 0	
→ DIN	1	1	0	1	0	1 0	1 0
D DOUT	0	1	0	1 ()	1 0	1 0

Problem 5

Once again we can use D flip flops to delay the signal, therefore using a mux we have the following circuit



With the following timing diagram

Signal Name	Signal Value	805.0 s	810.0 s	815.0 s	820.0 s	825.0 s	830.0 s	835.0 s	840.0 s	845.0 s	850.0 s	855.0 s	860.0 s	865.0 s	870.0 s
CLK	0	0 1 0 1 0	1 0 1 0 1	0 1 0 1	0 1 0 1 0	1 0 1 0 1	0 1 0 1 0 1	0 1 0 1 0	1 0 1 0 1	0 1 0 1 0	1 0 1 0 1	0 1 0 1	0 1 0 1 0	1 0 1 0 1 0	0 1 0 1 0
D- DIN	0	1 0	1 0	1	0 1		0		1		0 /1	0			
DOUT_SHORT	0		1	0	1	0						1	0		
DOUT_LONG	0						1 0				1 0				

Problem 6

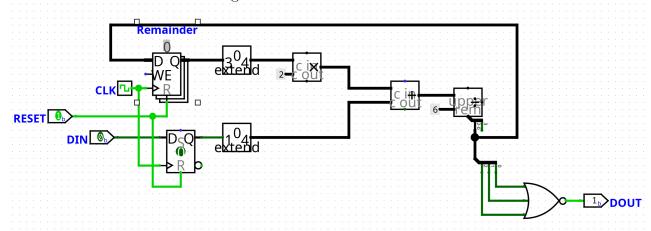
Let the remainder at step n be r_n , if the input bit is 0 we get that the remainder at step n+1 is

$$r_{n+1} = (2r_n)\%6$$

and if the input bit is 1 we get that the remainder at step n+1 is

$$r_{n+1} = (2r_n + 1)\%6$$

. Therefore we have the following circuit



With the following timing diagram

***************************************	9 414-01411						
Signal Name	Signal Value	7 μs	540.0 μs	560.0 μs	580.0 μs	600.0 μs	620.0 µs
□ CLK	1	1	0 1 0 1 0	1 0 1 0	$\int_{1}^{1} \int_{0}^{1} \int_{0}^{0}$	1 0 1 0	$\int 1 \int 0 \int 1 \int 0$
D DIN	1		1 0	1 0	1	0	1
D DOUT	0		0	1 0		1	0