ECE M16 Homework 4

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Problem 1

(a)

$$\boxed{220pS}$$

(b)

$$\boxed{420pS}$$

(c)

since the propagation delay is $420pS$, the clock cycle to satisfy the setup time constraint is

$$t_{cy} \geq t_{dCQ} + t_{dMax} + t_s$$

$$t_{cy} \geq 10pS + 420pS + 10pS$$

$$t_{cy} \geq \boxed{440pS}$$

(d)

The hold time constraint with skew is

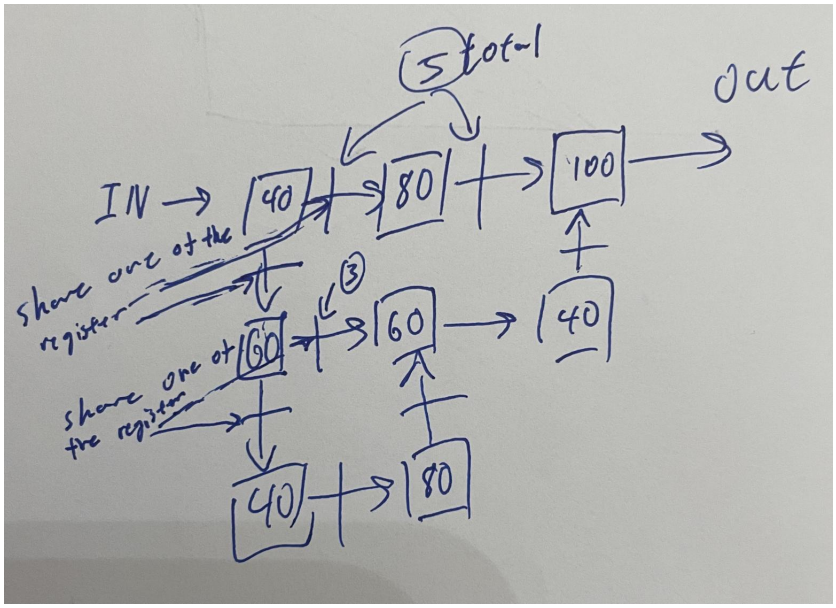
$$t_h \leq t_{cCQ} + t_{cMin} - t_k$$

$$10pS \leq 10pS + 220pS - t_k$$

$$t_k \leq 220pS$$

However t_k can be negative and the hold time constraint will still be satisfied, so the clock skew constraint is that clkd must be no later than 220pS after clk.

(e)



placing registers as the vertical marks and placing multiple of them at the circled places to avoid timing problems, we can get it down to the bottleneck of the slowest moduel so therefore the fastest clock cycle is

$$t_{cy} \geq t_{dCQ} + t_{dMax} + t_s$$

$$t_{cy} \geq 10pS + 100pS + 10pS = \boxed{120pS}$$

This can be accomplished with 11 registers. I did not add a register after the 100pS block because it was connected straight to a register

(f)

The signal would have to pass through 5 registers and given that the register overhead is

$$t_r = t_{dCQ} + t_s = 20pS$$

The latency is

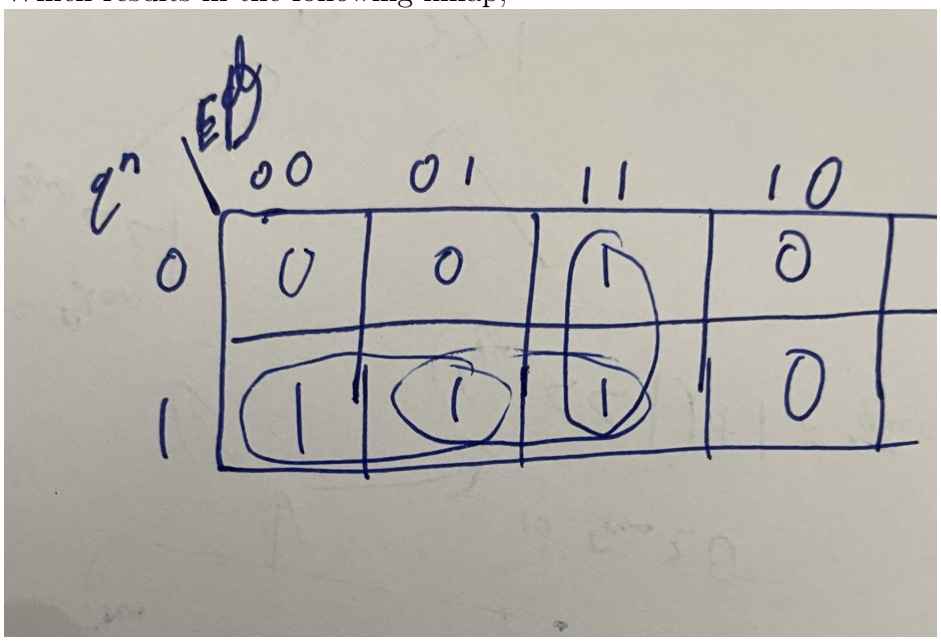
$$T = 5(100pS + 20pS) = \boxed{600pS}$$

Problem 2

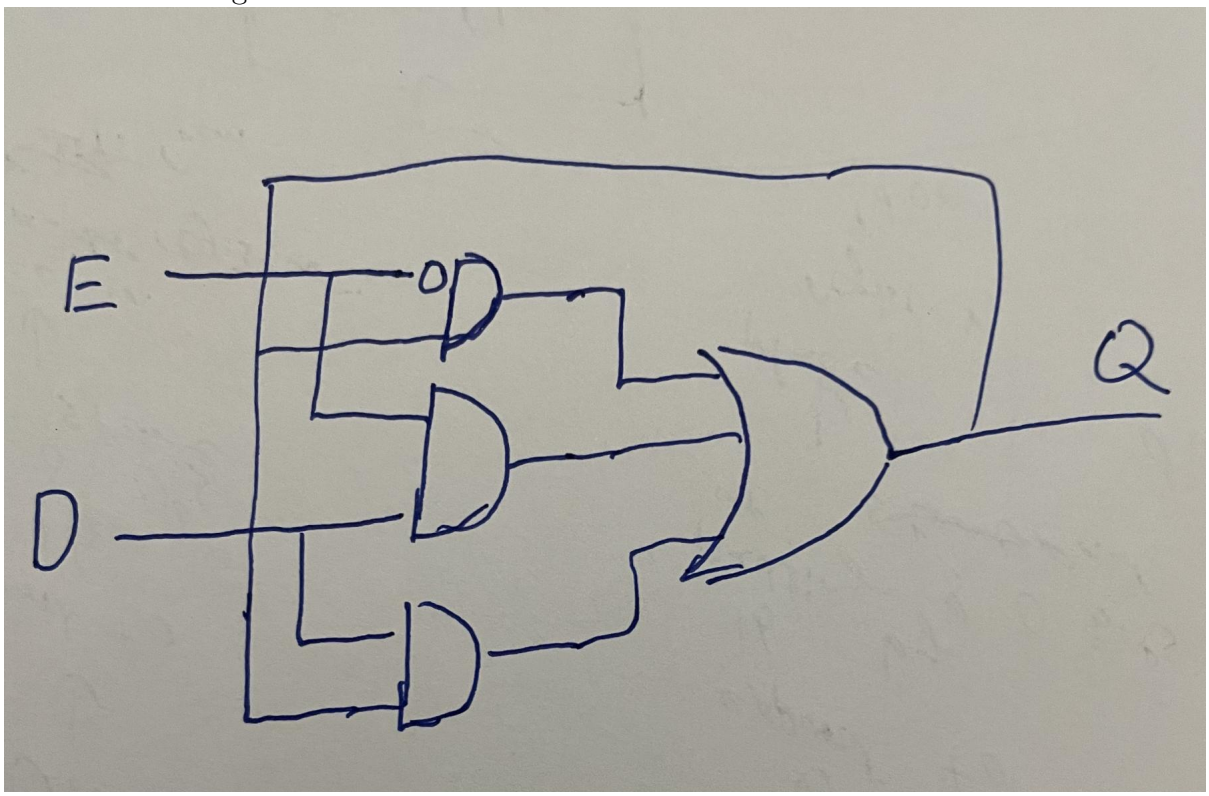
The flow table is

E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

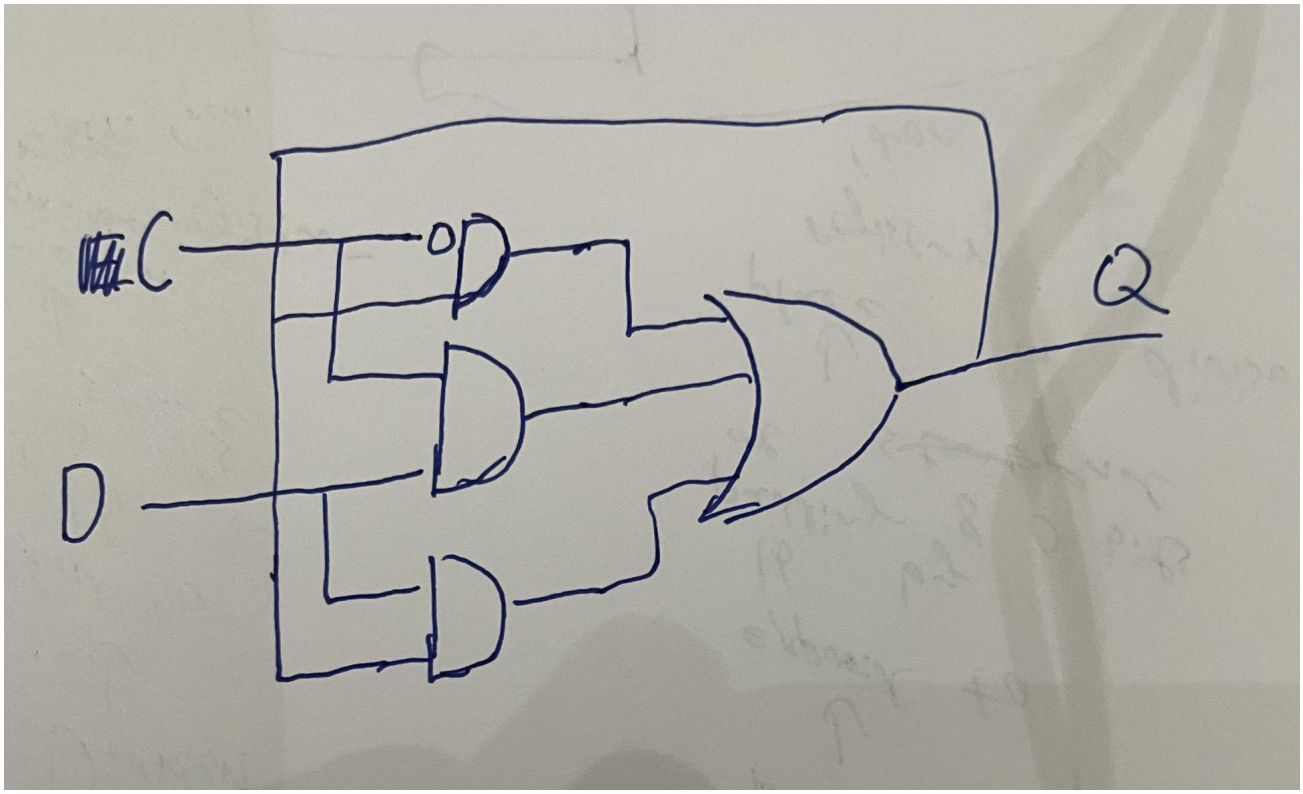
Which results in the following kmap,



And the following circuit



Converting it to a flip flop involves just simply switching E to the clock input C which results in the following circuit



Two of these are the same circuit as the one discussed in lecture.

Problem 3

(a)

$$Y_1 = \overline{(\overline{y_1.c}).(\overline{y_3.d})}$$
$$Y_2 = \overline{(\overline{y_1.c}).(\overline{y_3.y_2})}$$
$$Y_3 = \overline{c.(\overline{y_1.c}).(\overline{y_3.d})}$$

(b)

The state table is

Y1Y2Y3	cd			
	00	01	11	10
000	001	001	000	000
001	001	101	101	000
010	001	001	000	000
011	011	111	111	010
100	001	001	111	111
101	001	101	111	111
110	001	001	111	111
111	011	111	111	111

or in terms of states

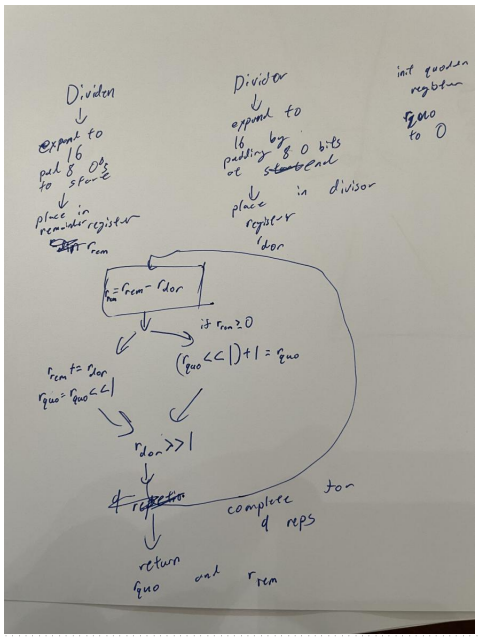
Y1Y2Y3	cd			
	00	01	11	10
S0	S1	S1	S0	S0
S1	S1	S5	S5	S0
S2	S1	S1	S0	S0
S3	S3	S7	S7	S2
S4	S1	S1	S7	S7
S5	S1	S5	S7	S7
S6	S1	S1	S7	S7
S7	S3	S7	S7	S7

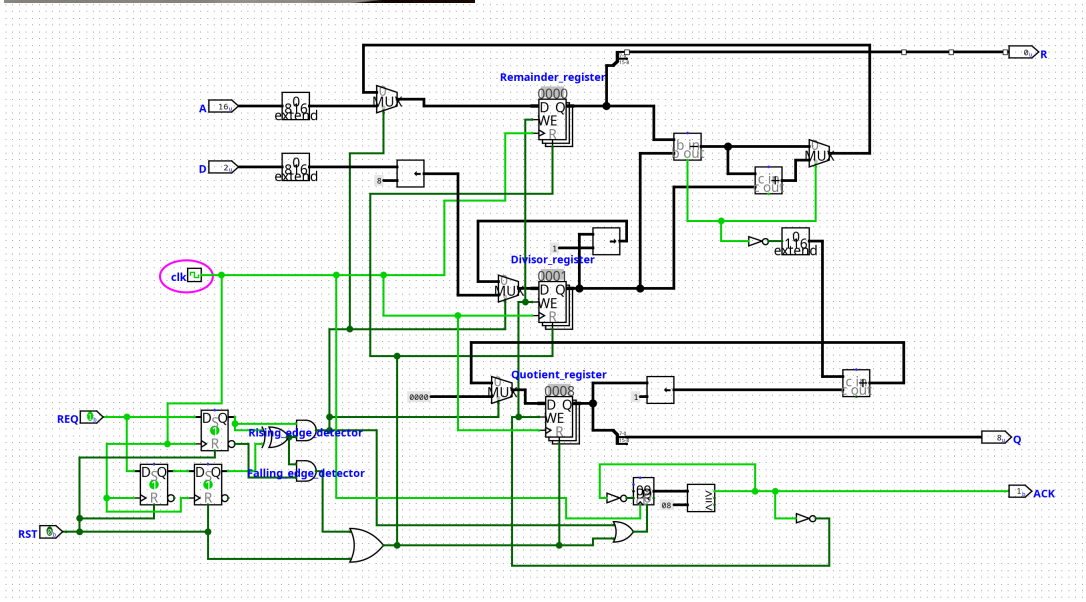
Keeping only the stable total states we get the following flow table

Y1Y2Y3	cd			
	00	01	11	10
S0	x	x	S0	S0
S1	S1	x	x	x
S3	S3	x	x	x
S5	x	S5	x	x
S7	x	S7	S7	S7

This is the correct flow table for a d flip flop.

Problem 5


Dividend
Divisor
init quotient register to 0
expand to 16 bits put 8 0's to start
append to 16 by padding 8 0 bits at end
place in remainder register
place in divisor register
r_rem
r_dor
r_rem = r_rem - r_dor
if r_rem ≥ 0
(r_quo << 1) + 1 = r_quo
r_rem += r_dor
r_quo = r_quo << 1
r_dor >> 1
complete for 8 reps
return r_quo and r_rem


Remainder_register
Divisor_register
Quotient_register
A
D
clk
REQ
RST
R
Q
ACK
Rising edge detector
Falling edge detector
extend
MUX
ADD