ECE M16 Homework 2

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Problem 1

(a)

It will toggle, if the latch is reset, ie $Q = 0$ and $\bar{Q} = 1$. Then the output will be $Q = 1$ and $\bar{Q} = 0$ following the clock pulse

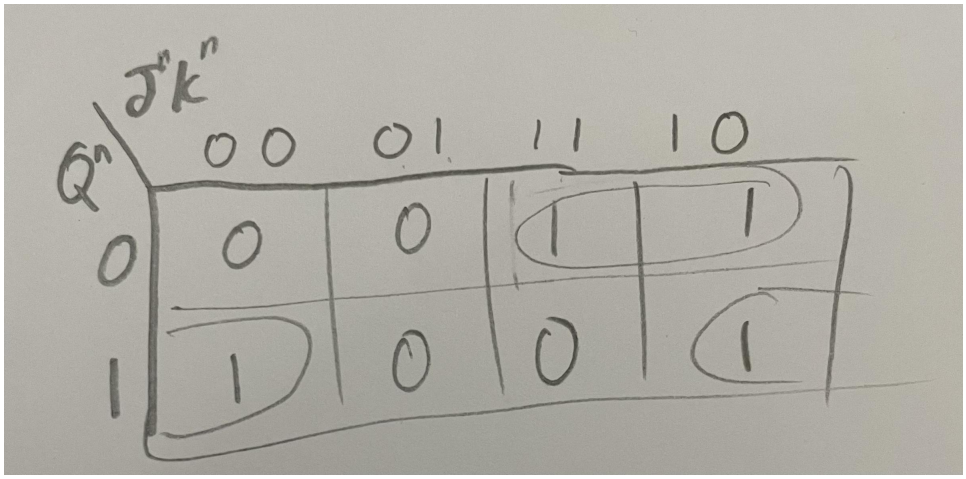
(b)

if $C = 0$ it will latch, but with $C = 1$ there will be following transition table

J	K	Q current	Q next
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Therefore this is like a SR latch however it will toggle at $J = K = 1$, unlike the SR latch.

(c)



$$Q^{n+1} = J^n.\overline{Q^n} + \overline{K^n}.Q^n$$

(d)

The transition table of the D latch is:

C	D	Q next
0	x	Q
1	0	0
1	1	1

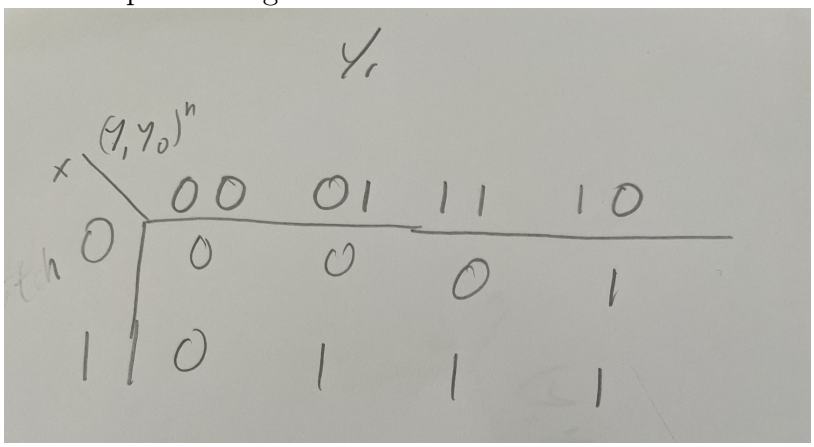
Which is the same as the transition table of the JK latch with $J = \bar{K} = D$.

C	J=D	$K = \bar{D}$	Q next
0	x	x	Q
1	0	1	0
1	1	0	1

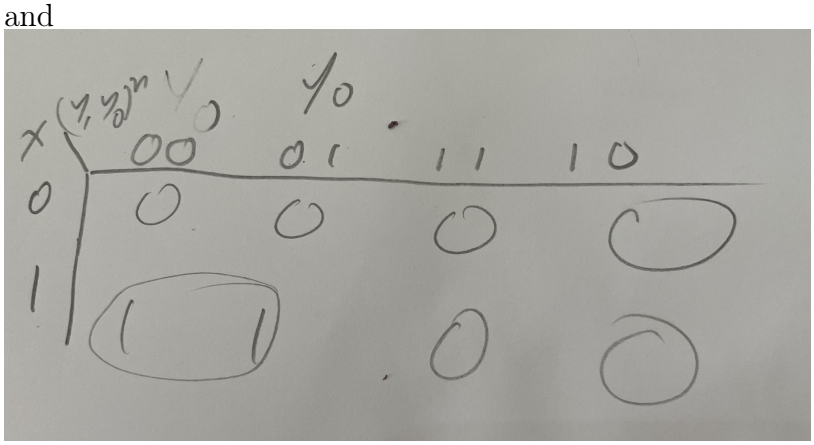
Problem 3

(a)

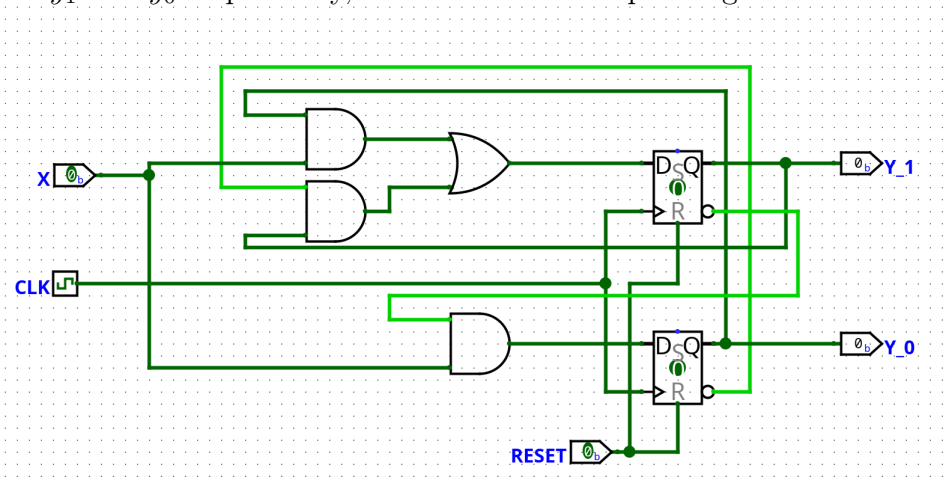
The kmaps for assignment 1 are:



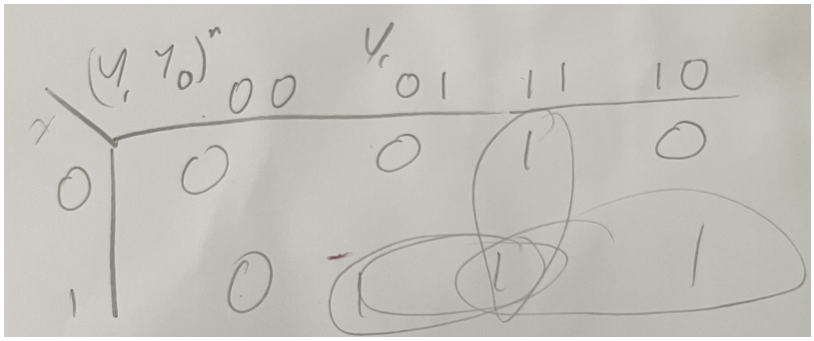
and



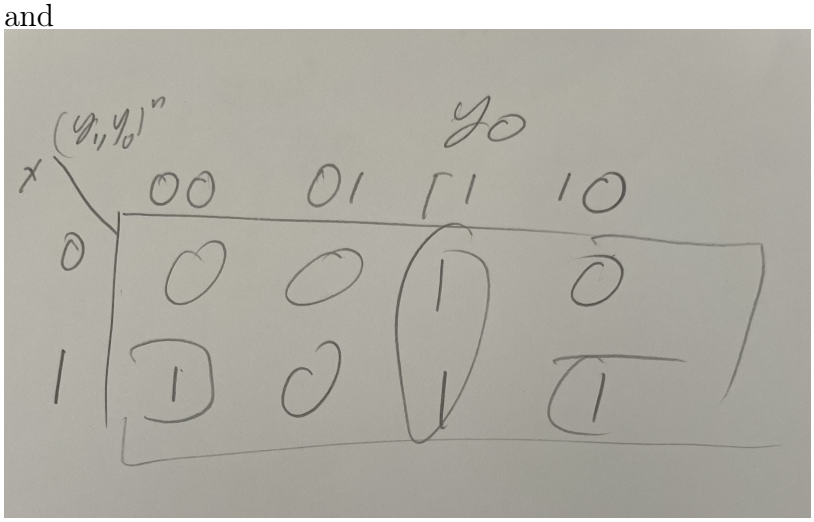
For y_1 and y_0 respectively, therefore the corresponding circuit is:



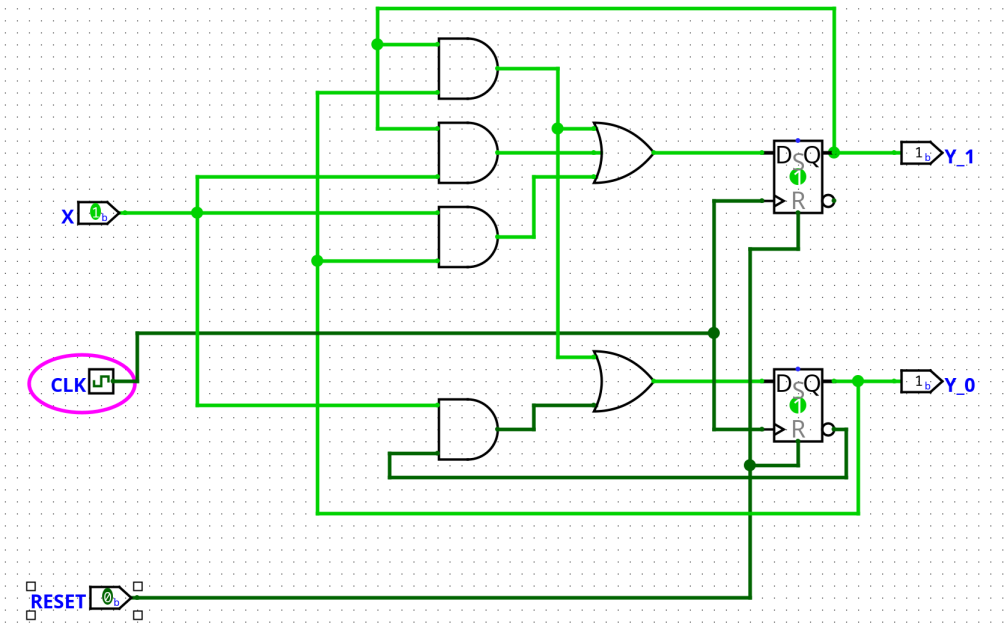
Likewise for assignment 2, the kmaps are:



and



For y_1 and y_0 respectively, therefore the corresponding circuit is:

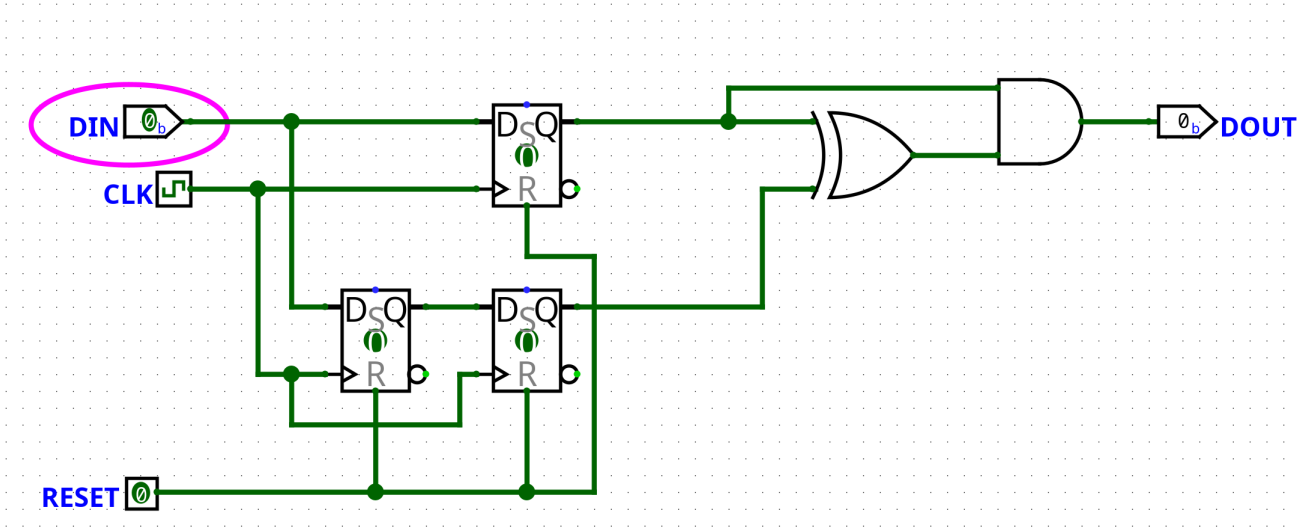


(b)

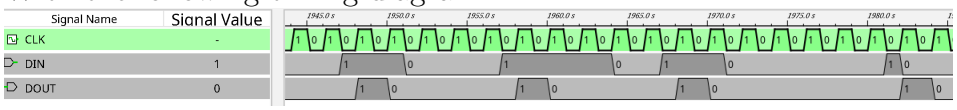
Therefore assignment 1 is more economical since it uses less gates.

Problem 4

Because we can use D flip flops to delay a signal, we have the following circuit

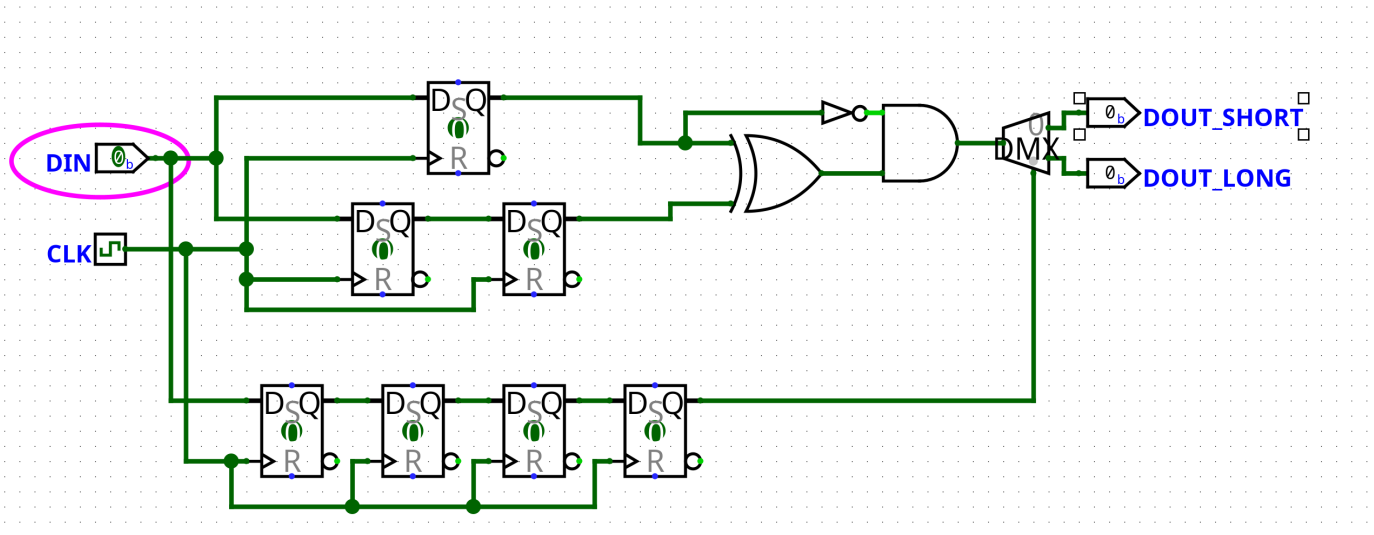


With the following timing diagram

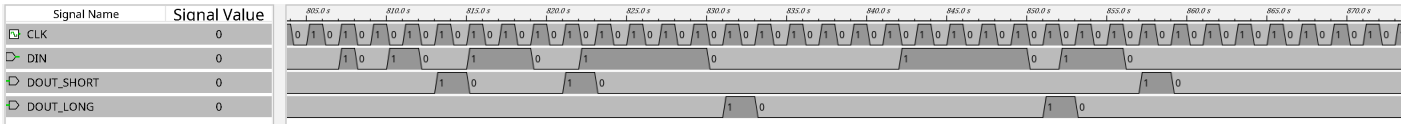


Problem 5

Once again we can use D flip flops to delay the signal, therefore using a mux we have the following circuit



With the following timing diagram



Problem 6

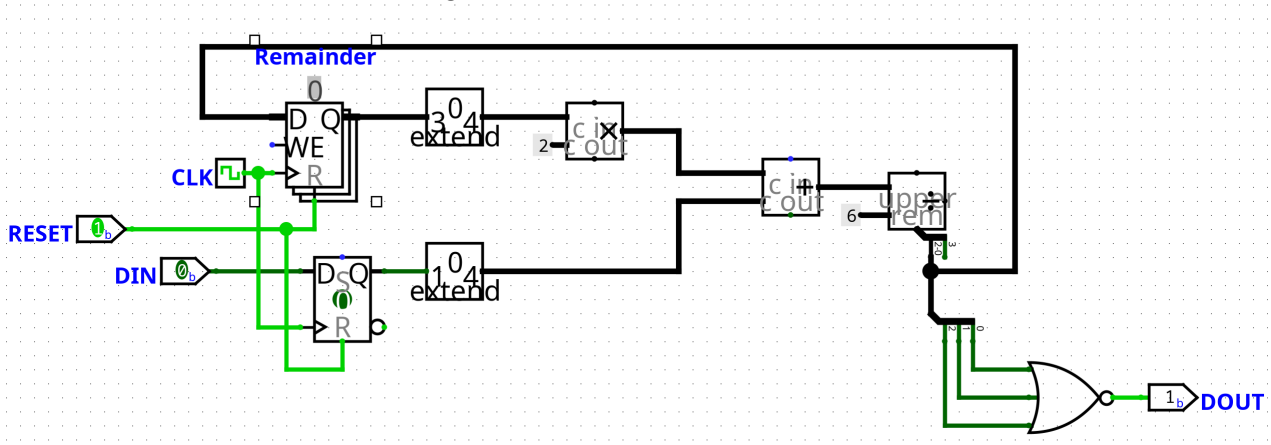
Let the remainder at step n be r_n, if the input bit is 0 we get that the remainder at step $n+1$ is

$$r_{n+1} = (2r_n)\%6$$

and if the input bit is 1 we get that the remainder at step $n+1$ is

$$r_{n+1} = (2r_n + 1)\%6$$

. Therefore we have the following circuit



With the following timing diagram