ECE M16 Homework 2

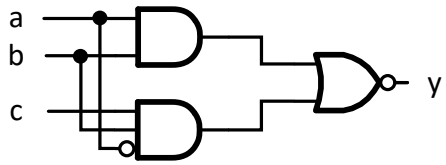
Instructor: Hooman Darabi

Sections covered: Logic gates and K-maps, combinational logic design and verification

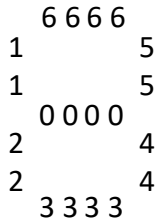
Total of 6 questions, 17 points each. Due: 11:59PM Friday of week 4.

For all Logisim question, you must use version logisim-evolution-2.14.8.4-cornell.jar which you can download from:
http://www.cs.cornell.edu/courses/cs3410/2019sp/logisim/logisim-evolution.jar.
Submit a copy of your Logisim schematic, your design process, and any results.

1. Identify and fix the hazard that may occur in the circuit below:



2. A decimal seven segment decoder is a combinational circuit with a four-bit input a representing number 0 to 9, and a seven-bit output q. Each bit of q corresponds to one of the seven segments of a display according to the following pattern. That is, bit 0 (the LSB) of q controls the middle segment, bit 1 the upper left segment, and so on, with bit 6 (the MSB) controlling the top segment. Design a sum-of-products circuit for segments 2 and 5 of a full seven-segment decoder.



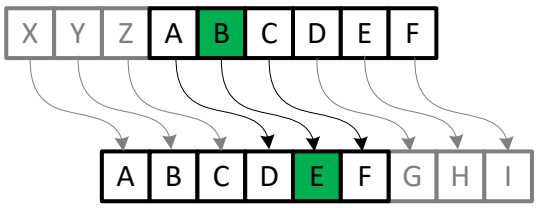
3. Design assignment: Using Logisim, design a $6 \rightarrow 64$ decoder with input $A[5:0]$ and outputs $X0[15:0]$, $X1[15:0]$, $X2[15:0]$, and $X3[15:0]$ which works as follows: If $A[5:4] = i$ (where $i = 0,1,2,3$) then the one-hot coded version of $A[3:0]$ is output on $Xi[15:0]$, and all the other outputs are 0. For example, say $A[5:0] = 100001$, then since $A[5:4] = 10_2 = 2_{10}$, all the bits of $X0$, $X1$, $X3$ will be 0, while $X2 = 0000000000000010$.

   Allowed Logisim Modules: Any from Wiring, Gates, Plexers, Arithmetic, Memory, and Input/Output except for RAM and ROM.

4. Design assignment: Using Logisim, design a circuit that takes three 4-bit unsigned binary numbers $A[3:0]$, $B[3:0]$, $C[3:0]$ and outputs the median of the three values on $M[3:0]$. Make sure that your design works correctly for all possible orderings of A, B, and C, and for cases when two or more of the numbers are identical.

   Allowed Logisim Modules: Any from Wiring, Gates, Plexers, Arithmetic, Memory, and Input/Output except RAM and ROM.

5. Design assignment: Design a combinational circuit implementing a simple encryption approach called Caesar Cipher (https://en.wikipedia.org/wiki/Caesar_cipher). This Caesar Encryptor takes two 5-bit inputs P and K, and produces one 5-bit output C, as in the figure below. $P[4:0]$ represents letters {'A', 'B', 'C', ...'Z'} where 'A' is 0, 'B' is 1, and so on. So, for example, the letter Z will be represented by 25, which is $P = 11001$. $K[4:0]$ is the key of the code, and is a 5-bit number in the range 0 to 25. The output $C[4:0]$ also represents letters {'A', 'B', 'C', ...'Z'}, except this letter is the one that is obtained by mapping the letter at the input to the letter that is obtained by moving K steps down the alphabet. For purposes of moving down the alphabet, we roll back to 'A' after 'Z'. So, for example, if $K = 3$ and P represents the letter 'Y' then C will output the letter 'B'. The following figure shows how letters would be coded if K was 3.



   Allowed Logisim Modules: Any from Wiring, Gates, Plexers, Arithmetic, Memory, and Input/Output, except that you may not use Multiplier, Divider, RAM and ROM.

6. Design assignment: Design a circuit to convert unsigned 2-digit Binary Code Decimal integers to unsigned binary integers. In Binary Code Decimal each decimal digit is represented separately as a 4-bit binary number. Your circuit would take the 2-digit Binary Code Decimal number on inputs $D1[3:0]$ and $D0[3:0]$ that represent the tens and units digits respectively, and creates the output $Z[6:0]$ an unsigned binary integer with the same numeric value as the decimal number formed by $D1$ and $D0$. For example, the number 45 will have $D1[3:0] = 0100$ and $D0[3:0] = 0101$, with the output being $Z[6:0] = 0101101$.

   Allowed Logisim Modules: Any from Wiring, Gates, Plexers, Arithmetic, Memory, and Input/Output, except that you may not use Multiplier, Divider, RAM and ROM.