CAP 208 Assignment

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Q 1) a) A stack is a storage device that stores information in such a manner that the item stored last is the first item retrieved or last-in, first-o (LIFO) list.

Basic stack operations are:

- Push
- Pop

Push → Operation to insert an item into the top of the stack.

Pop :→ Operation to remove an item from the top of the stack.

Push

SP ← SP + 1
M[SP] ← DR
IF (SP = 0) then (FULL ← 1)
Empty ← 0

Pop

DR ← M[SP]
SP ← SP - 1
If (SP = 0) then (EMPTY ← 1)
FULL ← 0

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(6) General Register Organization is a common unit that can perform all the arithmetic, logic and shift microoperations in the processor.

The major components of General Register organization are:

→ Registers from R1-R7

→ Two Multiplexers (MUX)

→ Arithmetic Logic Unit (ALU)

→ Decoder

→ Buses

The output of each register is connected to multiplexers (MUX) to form the two Buses A and B. The selection in each multiplexer select one register or the input data for particular bus.

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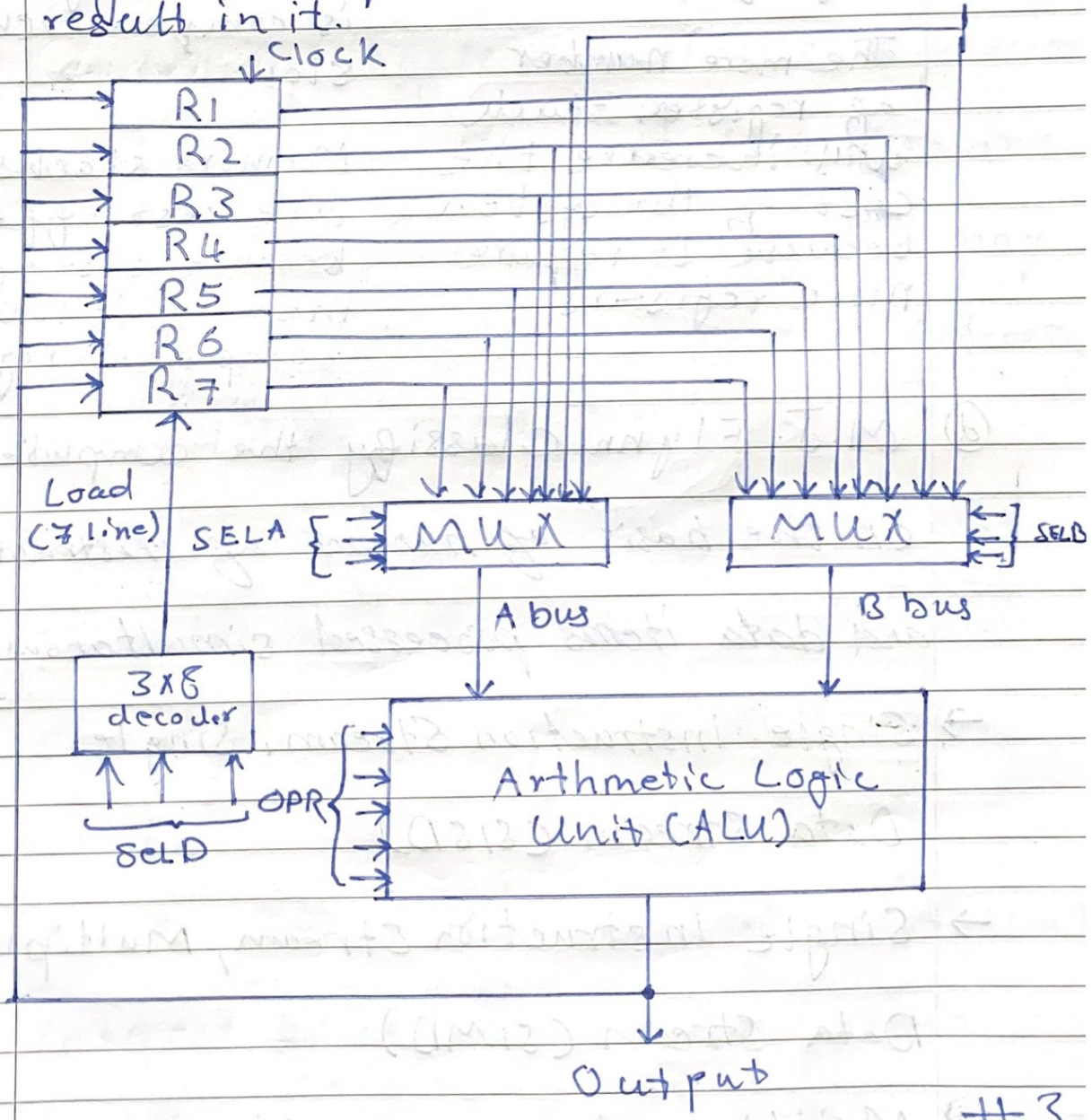
The A and B buses form the two inputs of an ALU. The operation select lines decide the microoperation to be performed by ALU. The result of microoperation is available at the output bus. The output bus connected to the inputs of all registers, by selecting a distination register it is possible to store the result in it.



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(c)

Register Stack	Memory Stack
It is implemented using CPU registers.	It is implemented using computer memory (RAM)
The operation of this stack is done at very fast rate	The operation of Memory stack is comperatively slow.
The more number of register stack will increase the cost of the system because it require more registers	Memory stacks are cost effective because cost of memory is lower compare to registers

(d) M.J. Flynn classify the computer on the basis of number of instruction and data items processed simultanously.

→ Single Instruction Stream, Single Data Stream (SISD)

→ Single Instruction Stream, Multiple Data Stream (SIMD)

#4 → Multiple Instruction Stream,

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Single Data Stream (MISD)

→ Multiple Instruction stream, Multiple Data stream (MIMD)

SISD: represents the organization containing single control unit, a processor unit and a memory unit. Instruction are executed sequentially and system may or may not have internal parallel processing capabilities.

SIMD: represents an organization that includes many processing units under the supervision ~~of~~ a common control unit.

MISD: structure is ~~of~~ only theoretical interest since no practical system has been constructed using this.

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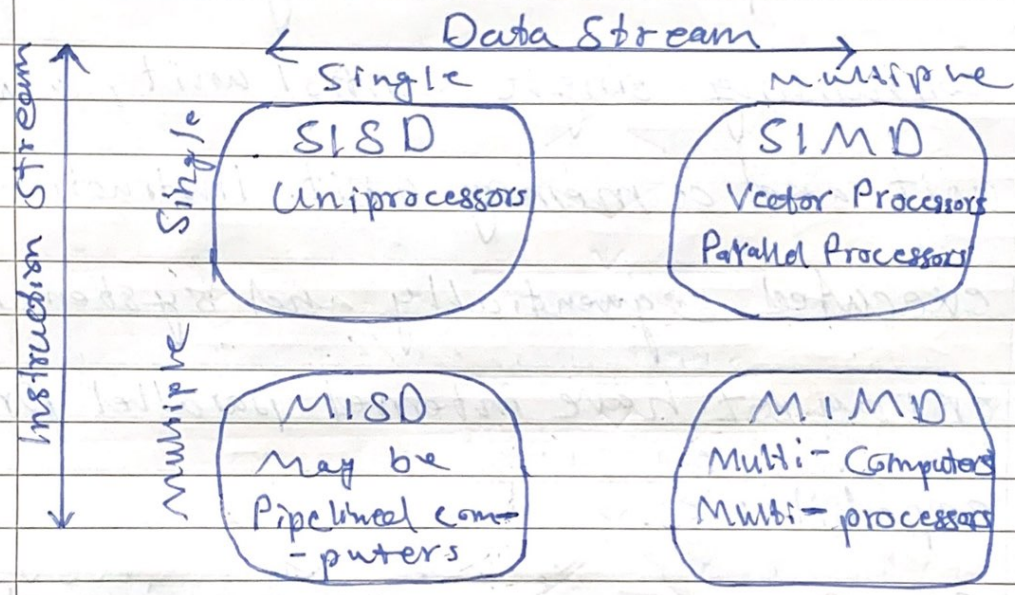
MIMD : organization refers to a computer system capable of processing several programs at the same time.



(e) Pipeline arithmetic units are usually found in very high speed computers. They are used to implements floating point operations, multiplication of fixed-point numbers & similar computation in scientific problems.

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The steps of the working of Arithmetic (floating point pipeline)

1. Compare the exponents
2. Align the mantissas
3. Add or subtract the mantisses
4. Normalize the result

(F) An instruction pipeline reads consecutive instruction from memory while previous instruction are being executed in other segments.

This caused the instruction fetch and execute segments to overlap and perform simultanous operation.

Pipeline Hazards:

→ Structure Hazard
→ Data Hazard
→ Control Hazard

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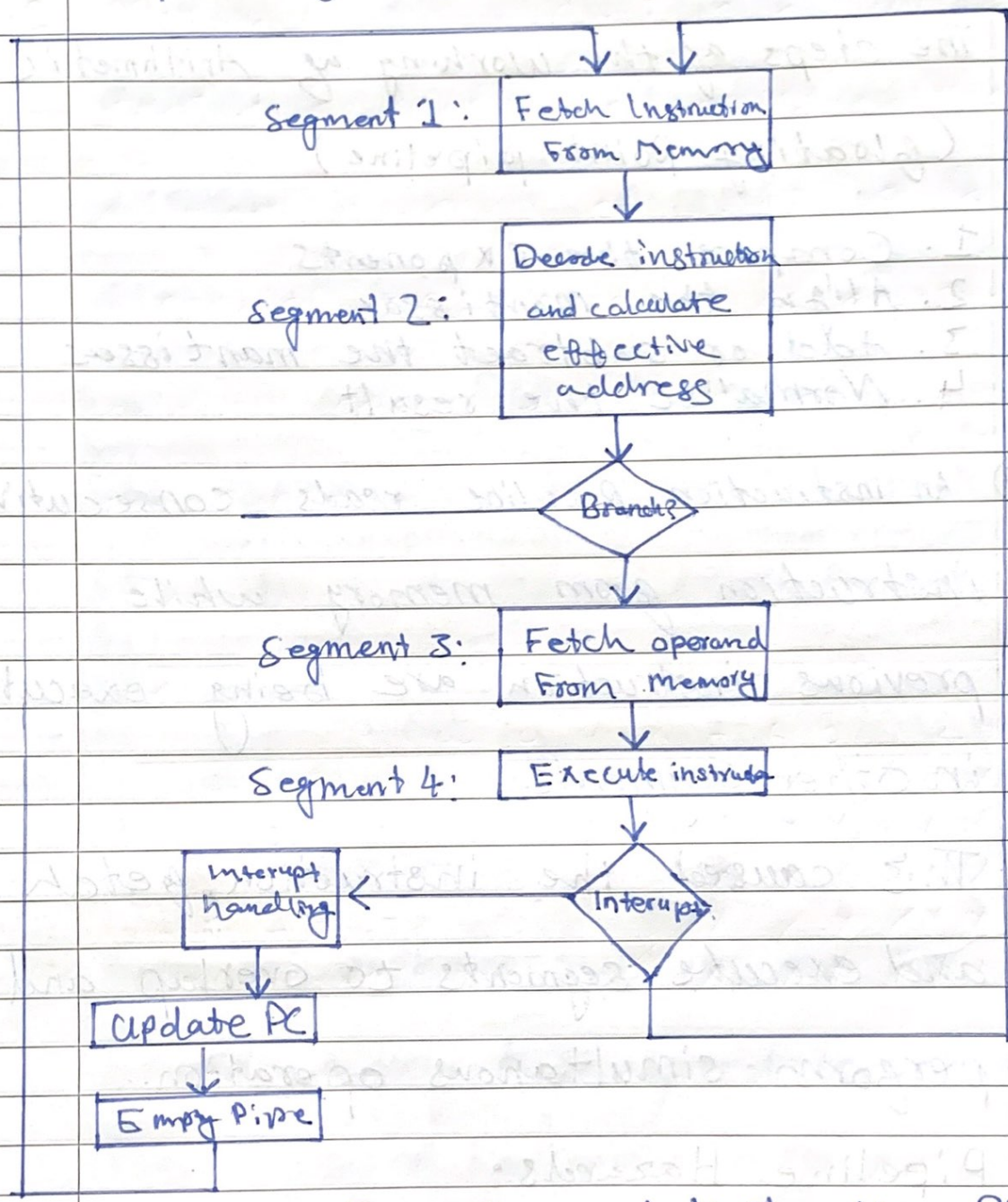
Example of Instruction Pipeline



Four-Segement Instruction Pipelin

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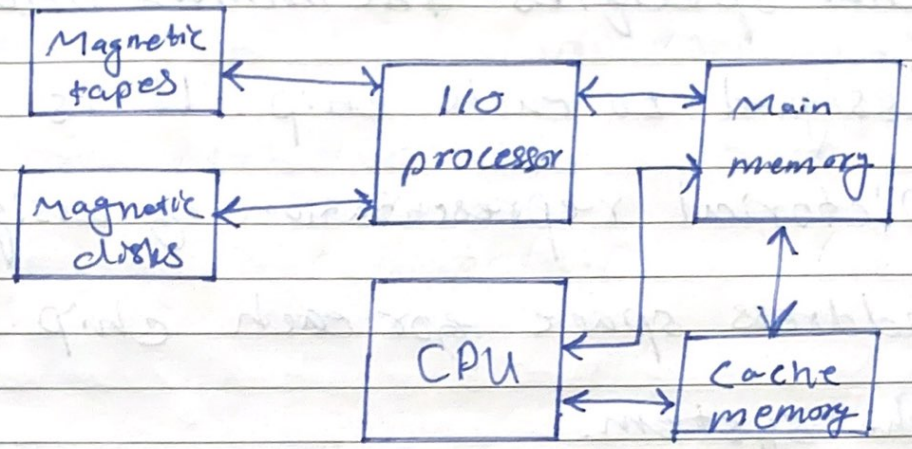
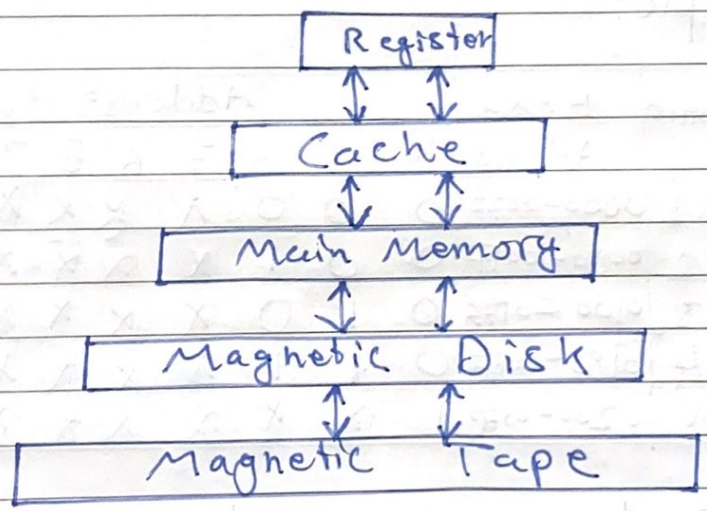
(a) Memory hierarchy Diagram





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(h) Memory Address Map : is a table that specifies the memory address assigned to each chip. It is a pictorial representation of assigned address space for each chip in the system.

Example:

Component	Hexa Address	Address Bus								
		10	9	8	7	6	5	3	2	1
RAM1	0000-007F	0	0	0	x	x	x	x	x	x
RAM2	0080-00FF	0	0	1	x	x	x	x	x	x
RAM3	0100-017F	0	1	0	x	x	x	x	x	x
RAM4	0180-01FF	0	1	1	x	x	x	x	x	x
ROM	0200-03FF	1	x	x	x	x	x	x	x	x

512 bytes RAM and 512 bytes of ROM

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(i) CPU-IOP Communication: An Input-output processor (IOP) is a processor with direct memory access capability. In this the computer system is divided into a memory unit and number of processors. Each IOP controls and manage the Input-output tasks. The IOP is similar to CPU except that it handles only the details of I/O processing.

The communication between CPU and IOP may take different forms, depending on the particular computer.

The CPU can act as master and the IOP act as slave processor. The CPU assigns task of initiating operation but it is the IOP, who executes

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the instructions, and not the CPU. CPU instructions provide operations to start an I/O transfer. The IOP asks for CPU through interrupt. Instructions that are read from memory by an IOP are also called commands, to distiguish them from instruction that read by CPU.

(j) Direct Memory Access (DMA)

DMA is a technique that allows peripheral (Input/Output) device to send or receive data directly to or from main memory, by passing the CPU to speed up transfer operations. This process is managed by a chip called as

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DMA controller (DMAC).

DMA controller - Interface which allows I/O transfer directly between Memory & ~~Device~~ Device, freeing CPU for other tasks.

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Part-B

Q2 (b) (i) Pipelining :-

Pipelining is a technique of decomposing a sequential process into suboperations, with each subprocess being executed in a special dedicated segment that operates concurrently with all other segments.

Each segment perform partial processing dictated by the way task is partitioned. The result from each segment is transferred to next segment. The final result is obtained when data have passed through all segments.

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Example: Let us see a real life example that works on the concept of pipelined operation. Consider a water bottle packaging plant. Let there be 3 stages that a bottle should pass through, Inserting the bottle (I), Filling water in bottle (F), and sealing the bottle (S). Let us consider stage 1, 2, 3 respectively. Let each stage take 1 minute to complete its operation.

Now in non pipelined operation, a bottle is first inserted in the plant, after 1 minute it is move to stage 2 where water is filled. Now, in stage nothing is happening. Similarly, when the bottle moves to stage 3 both stage 1 and 2 are idle.

But in pipelined operation, when the bottle is in stage 2, another bottle can be loaded at stage 1. In the same way when bottle is in stage 3 there can be one bottle each in stage 1 and stage 2.

Types of Pipeline:

1) Arithmetic
2) Instruction

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Arthmetic Pipelining (Steps)

1. Compare the exponents
2. Align the mantissas
3. Add or subtract mantissas
4. Normalize the result

Instruction Pipelining (Steps)

1. Fetch the instruction from memory
2. Decode the instruction
3. Caculate the effective address
4. Fetch the operands from memory
5. Execute the instruction
6. store the result in the proper place

Advantages of Pipelining

1. The cycle of the processor is reduced.
2. It increases the throughput of the system.
3. It makes the system reliable

Disadvantage of Pipelining

1. The design of pipelined processor is complex and costly to manufacture
2. The instruction latency is more.

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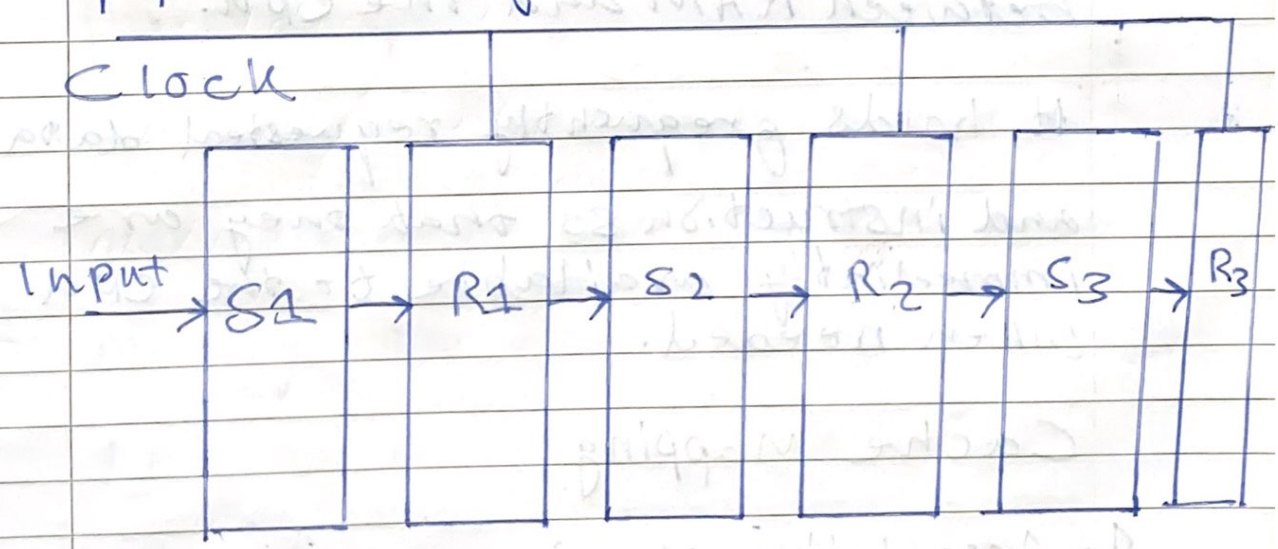
Pipeline Registers:

Pipeline registers are used to carry data across the datapath from one pipe stage to the next between clockpulses.

All registers needed to hold values temporarily clock cycles within one instruction are subsumed into these pipeline registers. The pipeline registers both data and control from one pipeline stage to the next.



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(b) (ii) Cache Memory is a special very high-speed memory. It is used to speedup and synchronizing with high-speed CPU. Cache memory is costlier than main memory or disk memory but economical than CPU registers.

Cache memory is an extremely fast memory type that acts as a buffer between RAM and the CPU.

It holds frequently requested data and instruction so that they are immediatly available to the CPU when needed.

Cache Mapping

1. Associative Mapping
2. Direct Mapping
3. Set-associative Mapping

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Associative Mapping:

The fastest and most flexible cache organization uses an associative memory. In this type of, the associative memory is used to store the content and addresses of the memory word. Any block can go into any line of the cache. It is considered to be the fastest and the most flexible mapping form.

Direct Mapping:

The simplest technique, known as direct mapping, maps each block of main memory into only one possible cache-line. In Direct mapping, assign each memory block to a specific line in the cache. If a line is previously

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taken up by a memory block when a new block needs to be loaded, the old is trashed.

Set-Associative Mapping:

This form of mapping is an enhanced form of direct mapping where the drawbacks of direct mapping are removed. Set associative addresses the problem of possible thrashing in the direct mapping method. It does this by saying that instead of having exactly one line that a block can map to in the ~~cache~~ cache

Page Replacement:

Page replacement is a process of swapping out an existing page from the frame of a main

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memory and replacing it with the required page.

Page replacement is required when-

- All the frames of main memory are already occupied
- Thus, a page has to replaced to create a room for the required page.

Page Replacement techniques:

Page replacement algorithms help to decide which page must be swapped out from the main memory to create a room for the incoming page.

FIFO (First-in, First-out) Algorithm
LIFO (Last-in, First-out) Algorithm
LRU (Least Recently Used) Algorithm
Optimal Page Replacement Algorithm
Random Page Replacement Algorithm

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