Lovely Professional University, Punjab

Course Code	Course Title	Course Planner	Lectures	Tutorials	Practicals	Credits
CAP208	COMPUTER ORGANIZATION AND DESIGN	12348::Monika Kalani	4	0	0	4
Course Weightage	ATT: 5 CA: 25 MTT: 20 ETT: 50	**Exam Category: 13: Mid Term Exam: All MCQ – End Term Exam: MCQ + Subjective**				
Course Orientation	KNOWLEDGE ENHANCEMENT					

	TextBooks (T)		
Sr No	**Title**	**Author**	**Publisher Name**
T-1	COMPUTER SYSTEM ARCHITECTURE	MORRIS MANO	PEARSON

	Reference Books (R)		
Sr No	**Title**	**Author**	**Publisher Name**
R-1	COMPUTER ORGANIZATION AND ARCHITECTURE	V RAJARAMAN	PRENTICE HALL
R-2	COMPUTER ARCHITECTURE A QUANTITATIVE APPROACH	DAVID A PATTERSON	PRENTICE HALL
R-3	COMPUTER ORGANIZATION AND ARCHITECTURE: DESIGNING AND PERFORMANCE	WILLIAM STALLINGS	PEARSON
R-4	COMPUTER ORGANIZATION	V. CARL HAMACHER, SAFWAT G. ZAKY AND ZVONKO G. VRANESIC	MCGRAW HILL EDUCATION

Other Reading (OR)	
Sr No	**Journals articles as Compulsary reading (specific articles, complete reference)**
OR-1	http://jes.eurasipjournals.com/content/2009/1/758480 ,

Relevant Websites (RW)		
Sr No	**(Web address) (only if relevant to the course)**	**Salient Features**
RW-1	http://www.cs.iastate.edu/~prabhu/Tutorial/title.html	Brief introduction about addressing Modes and Instruction formats
RW-2	http://www.tutorialspoint.com/computer_logical_organization/	Practical examples on Number System and gates
RW-3	http://www.labri.fr/perso/strandh/Teaching/AMP/Common/Strandh-Tutorial/Dir.html	Explanation of Registers and Multiplexers
RW-4	http://bottomupcs.sourceforge.net/csbu/c1453.htm	Components of CPU explained
RW-5	http://www.personal.kent.edu/~rmuhamma/ComArchitec/comArchitec.html	Explanation of Pipeline Processing

Audio Visual Aids (AV)		
Sr No	**(AV aids) (only if relevant to the course)**	**Salient Features**
AV-1	http://nptel.ac.in/video.php?subjectId=106102062	Explanation of Instruction sets, Memory Hierarchy and Input output subsystems
AV-2	http://freevideolectures.com/Course/2274/Computer-Architecture#	Introduction to computer architecture
AV-3	https://www.youtube.com/watch?v=BJ87rZCGWU0	Basics of computer architecture

LTP week distribution: (LTP Weeks)	
Weeks before MTE	7
Weeks After MTE	7
Spill Over (Lecture)	8

Detailed Plan For Lectures

Week Number	Lecture Number	Broad Topic(Sub Topic)	Chapters/Sections of Text/reference books	Other Readings, Relevant Websites, Audio Visual Aids, software and Virtual Labs	Lecture Description	Learning Outcomes	Pedagogical Tool Demonstration/ Case Study / Images / animation / ppt etc. Planned	Live Examples
Week 1	Lecture 1	Register Transfer and Microoperations(Number System)	T-1 R-1		L1:Introductory lecture L0: Lecture 0	L1:As a result of this lecture student will understand the importance of computer architecture its design and organization	Blend of powerpoint presentation with AV	
	Lecture 2	Register Transfer and Microoperations (Compliments)	T-1		L2: Detailed explanation of Number System including Binary,Decimal, Octal and Hexadecimal L3: Complements of number like 1's complement,2's complement,9's complement,10's complement etc.	L2: As a result of this lecture student will understand that how users in different langauge can interact with computers in binary form. L3:Students will learn to do the complements of the any given number	Demonstration using board or presentation	1's complement of 1100 is 0011 2's complement of 1100 is 0011+1=0100

Week 1	Lecture 3	Register Transfer and Microoperations (Compliments)	T-1		L2: Detailed explanation of Number System including Binary,Decimal, Octal and Hexadecimal L3: Complements of number like 1's complement,2's complement,9's complement,10's complement etc.	L2: As a result of this lecture student will understand that how users in different langauge can interact with computers in binary form. L3:Students will learn to do the complements of the any given number	Demonstration using board or presentation	1's complement of 1100 is 0011 2's complement of 1100 is 0011+1=0100
	Lecture 4	Register Transfer and Microoperations(Fixed point and floating point representation)	T-1 R-2		L4: Floating point numbers and its explanation L5: Fixed Point representation that includes arithmetic addition and subtraction	L4: Student will learn the conversion of floating point numbers into other number systems L5: Student will learn the difference between fixed point representation and its error detection	Demonstration on white board	10.0111 to decimal:
Week 2	Lecture 5	Register Transfer and Microoperations(Fixed point and floating point representation)	T-1 R-2		L4: Floating point numbers and its explanation L5: Fixed Point representation that includes arithmetic addition and subtraction	L4: Student will learn the conversion of floating point numbers into other number systems L5: Student will learn the difference between fixed point representation and its error detection	Demonstration on white board	10.0111 to decimal:
	Lecture 6	Register Transfer and Microoperations(Register Transfer)		RW-1 RW-2	Introduction to registers and its types	As a result of this lecture students will come to know the implementation of logic gates in designing the circuits	Demonstration using presentation	Addition of 2 bits or 3 bits using with or without carry
	Lecture 7	Register Transfer and Microoperations(Register Transfer Language)	T-1 R-3	RW-2 RW-3	Basic of Register Transfer Language	Student will learn about the communication of registers and their communication language	Blend of powerpoint presentation with AV	R3<- R1+R2 i.e. adding the contents of register 2 and register 3 and then transfer the result into register 1

Week 2	Lecture 8	Register Transfer and Microoperations(Bus and Memory Transfer)	T-1		Implementation of 3 state bus buffers and memory transfer	Student will learn the transferring of information from one register to another using bus system of 4 registers	Demonstration on white board	Connectivity of 4 bit register that includes mesh connectivity by connecting each bit of register with each bit of multiplexer
Week 3	Lecture 9	Register Transfer and Microoperations(Arithmetic Microoperations)	T-1		L9: Arithmetic micro operations in detail L10: Implementation of arithmetic operations using circuit diagram	L9: Students will understand different micro operation along with symbolic structure L10: As a result of this lecture students will be able to understand the implementation of all the arithmetic micro operations using single circuit	Demonstration on white board	Increment,Decrement, Binary Addition, Binary Subtract, 1s complement,2s complement.
	Lecture 10	Register Transfer and Microoperations(Arithmetic Microoperations)	T-1		L9: Arithmetic micro operations in detail L10: Implementation of arithmetic operations using circuit diagram	L9: Students will understand different micro operation along with symbolic structure L10: As a result of this lecture students will be able to understand the implementation of all the arithmetic micro operations using single circuit	Demonstration on white board	Increment,Decrement, Binary Addition, Binary Subtract, 1s complement,2s complement.
	Lecture 11	Register Transfer and Microoperations(Logic microoperations)	T-1	RW-3	Logic Micro operations and its applications	As a result of this lecture student will come to know how to apply different logic micro operations	Powerpoint presentation	1100 AND 0101 will give 0100
	Lecture 12	Register Transfer and Microoperations(Shift Microoperations)		RW-2	Detailed Implementation of half adder ,full adder and shift micro operations	Students will be able to understand the difference between logical shift left and right or circular shift left and right,half adder full adder	Powerpoint presentation	Logical shift left on 1100 will give 1000

Week 3	Lecture 12	Register Transfer and Microoperations(Half Adder and Full Adder)		RW-2	Detailed Implementation of half adder ,full adder and shift micro operations	Students will be able to understand the difference between logical shift left and right or circular shift left and right,half adder full adder	Powerpoint presentation	Logical shift left on 1100 will give 1000
Week 4	Lecture 13	Instruction Codes and Instruction Cycle(Instruction codes)	T-1	AV-1	Explanation of Instruction codes, illustration of stored program organization and difference of direct and indirect addressing	As a result of this lecture students will come to know the size of basic computer's memory, its addressing and difference between direct and indirect addressing	Demonstration using white board	Size of memory in basic computer is 4096 * 16 which states that memory consists of 4096 words and each word is 16 bits in length
	Lecture 14	Instruction Codes and Instruction Cycle(Common Bus System)	T-1	AV-1	L14: Brief introduction of all the registers being used in basic computer L15: Implementation of common bus system to ensure the efficient communication between registers	L14: Students will come to know the size and functionality of each register used L15: Students will understand how different registers used to communicate by having less circuitry involved	Blend of powerpoint presentation with AV	L14: PC is used to store the address of next instruction like we used to implement one counter outside the classroom which denotes that the next students who entered the class will sit on which particular seat
	Lecture 15	Instruction Codes and Instruction Cycle(Common Bus System)	T-1	AV-1	L14: Brief introduction of all the registers being used in basic computer L15: Implementation of common bus system to ensure the efficient communication between registers	L14: Students will come to know the size and functionality of each register used L15: Students will understand how different registers used to communicate by having less circuitry involved	Blend of powerpoint presentation with AV	L14: PC is used to store the address of next instruction like we used to implement one counter outside the classroom which denotes that the next students who entered the class will sit on which particular seat

Week 4	Lecture 16	Instruction Codes and Instruction Cycle(Types of instructions)	T-1		Detailed explanation of different types of instruction using their formats	As a result of this lecture students will understand the representation of 3 different types of instructions in memory	Demonstration using white board	
Week 5	Lecture 17	Instruction Codes and Instruction Cycle(Timing and control)	T-1	AV-3	L17: Timing and control structure representation L18: Timing and control plus Allocation of test	Students will learn the timing sequence of instructions in which they execute	Demonstration using white board	Instruction1 will be completed in 3 sec and Instruction 2 will be completed in 4 secs, then calculate the total time taken to execute the instruction
	Lecture 18	Instruction Codes and Instruction Cycle(Timing and control)	T-1	AV-3	L17: Timing and control structure representation L18: Timing and control plus Allocation of test	Students will learn the timing sequence of instructions in which they execute	Demonstration using white board	Instruction1 will be completed in 3 sec and Instruction 2 will be completed in 4 secs, then calculate the total time taken to execute the instruction
	Lecture 19	Instruction Codes and Instruction Cycle(Instruction Cycle)	T-1 R-4	RW-3 AV-1	L19: Four steps of instruction cycle along with Flowchart L20: Detailed explanation of each memory reference and register reference instruction	L19: As a result of this lecture student learn how an instruction executes L20: Students will learn the functionality of each instruction	Demonstration using white board	L19: Fetch, decode, read an effective address and execute the instruction L20: Add,sub,mul,div ,mov instructions
	Lecture 20	Instruction Codes and Instruction Cycle(Instruction Cycle)	T-1 R-4	RW-3 AV-1	L19: Four steps of instruction cycle along with Flowchart L20: Detailed explanation of each memory reference and register reference instruction	L19: As a result of this lecture student learn how an instruction executes L20: Students will learn the functionality of each instruction	Demonstration using white board	L19: Fetch, decode, read an effective address and execute the instruction L20: Add,sub,mul,div ,mov instructions

Week 6	Lecture 21	Machine Language and Programming(Introduction of Machine Language)	T-1	OR-1	Machine language and assembly language difference along with elements of assembly language	As a result of this lecture students will understand the programmatic structure of assembly language.	Blend of powerpoint presentation with AV	ORG, END, MACRO, MEND are pseudo instructions and cannot be converted to machine
		Machine Language and Programming(Assembly Language Basics)	T-1	OR-1	Machine language and assembly language difference along with elements of assembly language	As a result of this lecture students will understand the programmatic structure of assembly language.	Blend of powerpoint presentation with AV	ORG, END, MACRO, MEND are pseudo instructions and cannot be converted to machine
	Lecture 22	Machine Language and Programming(Assembler Basics)	T-1	RW-1 AV-2	Assembler first pass and second pass	Students will understand how assembler converts assembly language program to machine code	Powerpoint presentation	Source code (assembly language) -> Assembler -> Machine Code
	Lecture 23	Machine Language and Programming(Arithmetic and Logic Operation programming)	T-1	RW-1	Circuit explaining arithmetic and logic micro programming	As a result of this lecture students will understand the implementation of ALU tasks	Demonstration using white board	P: R1<- R2, (3 + 5) \times 2
	Lecture 24				Test 1			
Week 7	Lecture 25	Machine Language and Programming(program loops)	T-1		Implementation of subroutines and program loops	Students will learn the difference between functions and subroutines and the use of program loops	Powerpoint presentation	Language support, Selfmodifying code, Subroutine libraries, Return by indirect jump
		Machine Language and Programming(Subroutines)	T-1		Implementation of subroutines and program loops	Students will learn the difference between functions and subroutines and the use of program loops	Powerpoint presentation	Language support, Selfmodifying code, Subroutine libraries, Return by indirect jump
		Machine Language and Programming(Programming loops)	T-1		Implementation of subroutines and program loops	Students will learn the difference between functions and subroutines and the use of program loops	Powerpoint presentation	Language support, Selfmodifying code, Subroutine libraries, Return by indirect jump

Week 7	Lecture 26	Machine Language and Programming(Input-Output programming)	T-1	AV-1 AV-2 AV-3	Input output interfacing	Students should learn in the lecture about the programming examples	Discussion and Demonstration using white board	Channel I/O and Port-mapped I/O
		SPILL OVER						
Week 7	Lecture 27				Spill Over			
	Lecture 28				Spill Over			
		MID-TERM						
Week 8	Lecture 29	Central Processing Unit (General Register Organization)	T-1	RW-4	L29: Components of CPU, Control word L30: CPU organizations and micro operations	L29: Students will come to know the basic parts of CPU L30: Students will come to know the different ways of organization of a computer	Discussion and demonstration using white board	LC4/MIPS/x86 Registers
	Lecture 30	Central Processing Unit (General Register Organization)	T-1	RW-4	L29: Components of CPU, Control word L30: CPU organizations and micro operations	L29: Students will come to know the basic parts of CPU L30: Students will come to know the different ways of organization of a computer	Discussion and demonstration using white board	LC4/MIPS/x86 Registers
	Lecture 31	Central Processing Unit (Organization of stacks)	T-1	RW-4	L31: Basics of control word, stacks and operations on stacks L32: Register stack organization along with PUSH, POP L33: Memory stack organization along with PUSH,POP	L31: Students will learn the basic data structure stack before staring its implementation L32: Students will understand the representation of stacks in registers L33: Students will come to know the memory representation of stacks	Discussion and demonstration using powerpoint presentation	STACK-> LIFO PUSH-> Insert new element POP-> Remove from TOS

Week 8	Lecture 32	Central Processing Unit (Organization of stacks)	T-1	RW-4	L31: Basics of control word, stacks and operations on stacks L32: Register stack organization along with PUSH, POP L33: Memory stack organization along with PUSH,POP	L31: Students will learn the basic data structure stack before staring its implementation L32: Students will understand the representation of stacks in registers L33: Students will come to know the memory representation of stacks	Discussion and demonstration using powerpoint presentation	STACK-> LIFO PUSH-> Insert new element POP-> Remove from TOS
Week 9	Lecture 33	Central Processing Unit (Organization of stacks)	T-1	RW-4	L31: Basics of control word, stacks and operations on stacks L32: Register stack organization along with PUSH, POP L33: Memory stack organization along with PUSH,POP	L31: Students will learn the basic data structure stack before staring its implementation L32: Students will understand the representation of stacks in registers L33: Students will come to know the memory representation of stacks	Discussion and demonstration using powerpoint presentation	STACK-> LIFO PUSH-> Insert new element POP-> Remove from TOS
	Lecture 34	Central Processing Unit (Reverse Polish Notation)	T-1	RW-1 RW-4 AV-3	Infix, prefix and post fix notations	Learn about different types of notations	Discussion and Demonstration of Animation	5 1 2 + 4 Ã— + 3 -.The expression is evaluated left toright
	Lecture 35	Central Processing Unit(One Address Instructions)	T-1	RW-1 RW-4	Implementation of zero address and one address instructions	Learn about three address instruction with the help of example	Demonstration using white board	Addition of R2 AND R3 and transfer the same to R1
		Central Processing Unit (Zero Address Instructions)	T-1	RW-1 RW-4	Implementation of zero address and one address instructions	Learn about three address instruction with the help of example	Demonstration using white board	Addition of R2 AND R3 and transfer the same to R1
	Lecture 36	Central Processing Unit (Three address Instructions)	T-1	RW-1	Implementation of three AND two address instruction	Student will learn its implementation	Demonstration on white board	Add R1,R2,R3
		Central Processing Unit (Two Address Instructions)	T-1	RW-1	Implementation of three AND two address instruction	Student will learn its implementation	Demonstration on white board	Add R1,R2,R3

Week 10	Lecture 37	Central Processing Unit (Addressing Modes)		RW-1	L37:Discussion of addressing modes and implementation of modes using numericals	L37: Students will learn the types of addressing in memory	Demonstration using white board	
	Lecture 38				Test 2			
	Lecture 39	Central Processing Unit (RISC Instructions)	T-1	RW-4	RISC and CISC characteristics	Students will learn the difference between RISC and CISC processors	Demonstration using powerpoint presentation	Computers using RISC and computers using CISC
	Lecture 40	Pipeline processing(Parallel processing)	T-1	RW-5	L40: Parallel processing L41: Pipeline Processing	L40: Students will come to know about parallel processing and ways to improve the efficiency of system L41: Learn that how pipeline helps to improve the efficiency of system	Blend of powerpoint presentation with AV	Execute 5 instructions simultaneously and calculate the efficiency
Week 11	Lecture 41	Pipeline processing(Parallel processing)	T-1	RW-5	L40: Parallel processing L41: Pipeline Processing	L40: Students will come to know about parallel processing and ways to improve the efficiency of system L41: Learn that how pipeline helps to improve the efficiency of system	Blend of powerpoint presentation with AV	Execute 5 instructions simultaneously and calculate the efficiency
	Lecture 42	Pipeline processing (Instruction and arithmetic pipeline)	T-1	RW-5	L42: implementation of arithmetic pipeline L43: Implementation of instruction pipeline	L42: Learn about the addition or subtraction of two floating point numbers L43: Learn about how interrupt hinders the normal flow of execution	Discussion and demonstration using white board	Addition of 0.9504 and 0.8200
	Lecture 43	Pipeline processing (Instruction and arithmetic pipeline)	T-1	RW-5	L42: implementation of arithmetic pipeline L43: Implementation of instruction pipeline	L42: Learn about the addition or subtraction of two floating point numbers L43: Learn about how interrupt hinders the normal flow of execution	Discussion and demonstration using white board	Addition of 0.9504 and 0.8200

Week 11	Lecture 44	Pipeline processing(Pipeline hazards and their resolution)	T-1	RW-5	Pipeline hazards that includes resource conflicts, data conflicts and control conflicts	Students will learn that by the use of pipeline there are certain parameters that hinders its execution	Powerpoint presentation	Data dependency conflict: ADD: R1,R2,R3 SUB: R4,R1,R5 SUB instruction is dependent on the execution of ADD instruction
Week 12	Lecture 45	I/O subsystems(Input-output devices)	T-1		Peripheral Devices and its implementation	Learn about the use of various I/O devices	Powerpoint presentation	Magnetic tape , magnetic disk etc
	Lecture 46	I/O subsystems(Interfacing with IO devices)	T-1		Interfacing of I/O bus and Interface modules	Learn about the interface of I/O systems	Demonstration on white board	Connection of one bus using various devices
	Lecture 47	I/O subsystems (Asynchronous data transfer)	T-1	AV-1 AV-2	Asynchronous data transfer mechanism	Learn about various transfer mechanisms	Powerpoint presentation	
	Lecture 48				Test 3			
Week 13	Lecture 49	I/O subsystems(Concept of handshaking)	T-1		Implementation details of direct memory access, Handshaking	Learn about the use of DMA ,its functions and handshaking	Powerpoint presentation	CPU-IOP communication
		I/O subsystems(DMA data transfer)	T-1		Implementation details of direct memory access, Handshaking	Learn about the use of DMA ,its functions and handshaking	Powerpoint presentation	CPU-IOP communication
	Lecture 50	Memory technology (Memory hierarchy)	T-1		Hierarchy of memories available	Learn about the different types of memory present	Powerpoint presentation	Main memory, Auxiliary memory, static and dynamic
	Lecture 51	Memory technology(Cache memory and memory hierarchy)	T-1		RAM and Cache difference	Learn about the difference between RAM and cache and its use	Powerpoint presentation	Selection of books from Library is MAIN memory and placing the selected books on your book shelf at your home is Cache memory

Week 13	Lecture 51	Memory technology(Cache memory)	T-1		RAM and Cache difference	Learn about the difference between RAM and cache and its use	Powerpoint presentation	Selection of books from Library is MAIN memory and placing the selected books on your book shelf at your home is Cache memory
	Lecture 52	Memory technology (Associative memory)	T-1		Implementation and components of auxiliary memory and associative memory	Learn about the use of associative and auxiliary memory	Powerpoint presentation	
Week 14	Lecture 53	Memory technology(Virtual memory and memory management unit)	T-1		Logical and physical address space	Learn about the hardware used for virtual memory management	Discussion and demonstration using animation	Paging and segmentation hardware can be discussed
	Lecture 54	Memory technology(Virtual memory and memory management unit)	T-1		Logical and physical address space	Learn about the hardware used for virtual memory management	Discussion and demonstration using animation	Paging and segmentation hardware can be discussed
		SPILL OVER						
Week 14	Lecture 55				Spill Over			
	Lecture 56				Spill Over			
Week 15	Lecture 57				Spill Over			
	Lecture 58				Spill Over			
	Lecture 59				Spill Over			
	Lecture 60				Spill Over			

Scheme for CA:

CA Category of this Course Code is:A0203 (2 best out of 3)

Component	Weightage (%)
Test	50
Test	50
Test	50

Details of Academic Task(s)

Academic Task	Objective	Detail of Academic Task	Nature of Academic Task (group/individuals)	Academic Task Mode	Marks	Allottment / submission Week
Test 1	To evaluate the student performance on the basis of contents taught in class	Basic organization of computers : Block level description of the functional units,Fetch cycle, Decode and execute cycle,Machine instructions : Instruction set architectures, Assembly language programming, Addressing modes, Instruction cycles, Registers and storage, RISC versus CISC architectures, Inside a CPU ,Information representation : Floating point representation,Computer arithmetic and their implementation, Fixed-point arithmetic, Arithematic addition and subtraction, Multiplication and division, Arithmetic logic units control	Individual	Offline	30	3 / 5
Test 2	To evaluate students on the basis of their understanding in class	General Register Organization, Addressing Modes, Reverse Polish Notation, Three address Instructions, One Address Instructions, RISC Instructions, Zero Address Instructions, Two Address Instructions, Organization of stacks	Individual	Offline	30	10 / 11
Test 3	To evaluate the student performance on the basis of contents taught in class	Pipeline processing : Instruction and arithmetic pipeline, Pipeline hazards and their resolution, Parallel processing. Memory technology : Cache memory and memory hierarchy, Virtual memory and memory management unit, Memory hierarchy, Associative memory, Cache memory I/O subsystems : Input-output devices, Interfacing with IO devices, Concept of handshaking.	Individual	Offline	30	11 / 12