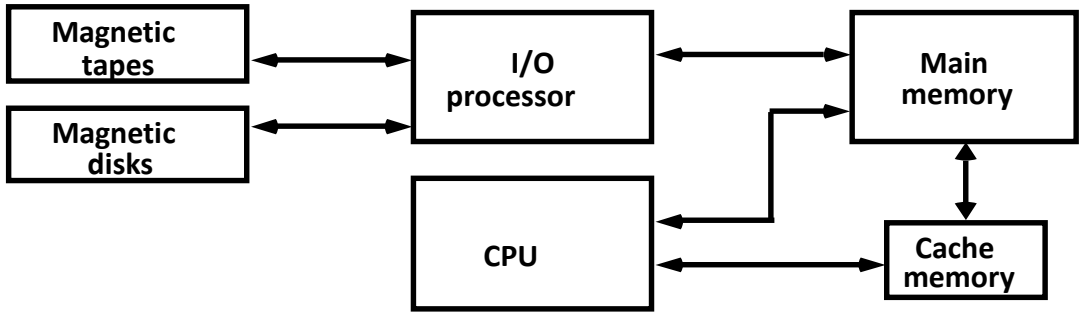
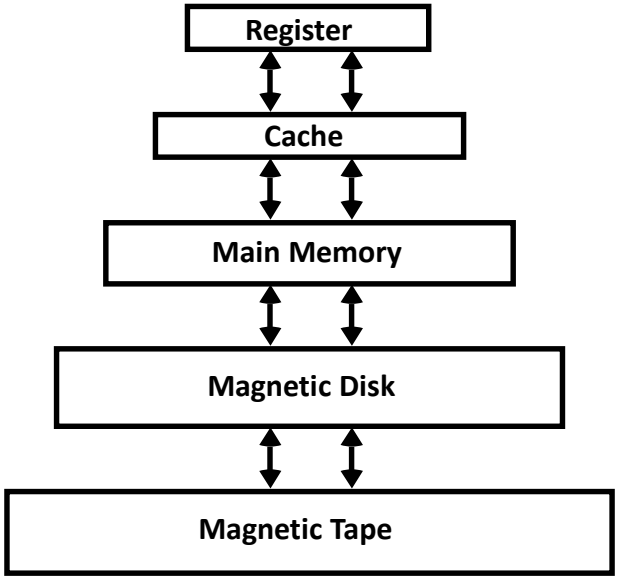
Overview

- Memory Hierarchy
- Main Memory
- Auxiliary Memory
- Associative Memory
- Cache Memory
- Virtual Memory

Memory Hierarchy

Memory Hierarchy is to obtain the highest possible access speed while minimizing the total cost of the memory system

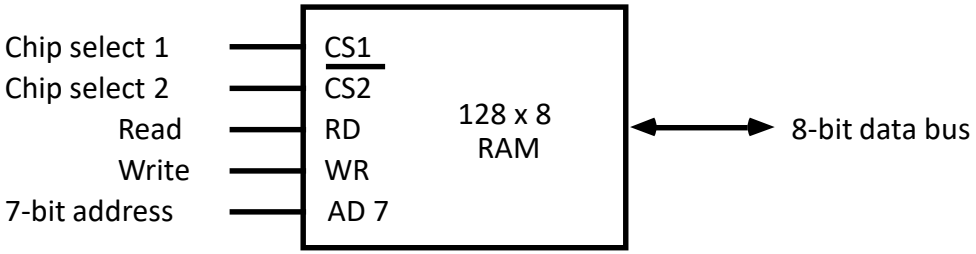




Main Memory

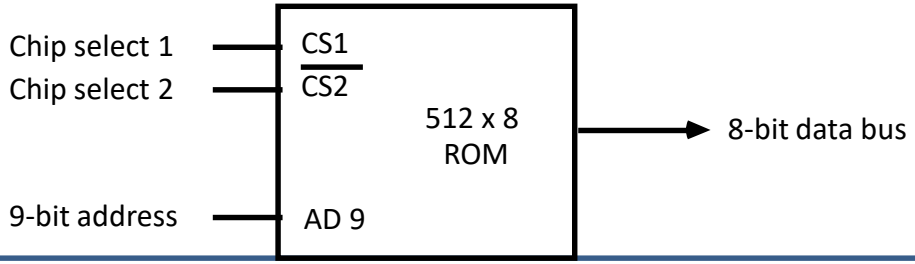
RAM and ROM Chips

Typical RAM chip



CS1	$\overline{CS2}$	RD	WR	Memory function	State of data bus
0	0	x	x	Inhibit	High-impedence
0	1	x	x	Inhibit	High-impedence
1	0	0	0	Inhibit	High-impedence
1	0	0	1	Write	Input data to RAM
1	0	1	x	Read	Output data from RAM
1	1	x	x	Inhibit	High-impedence

Typical ROM chip



Connection of Memory to CPU

RAM chip is better suited for communication with CPU
Control inputs selects the chip only when needed
A bidirectional data bus allows the transfer of data either from memory to CPU during read /write operation

A bidirectional bus is made of Tri state buffer

The capacity of memory is 128 words of 8 bits

It requires 7 Bit address and 8 bit bidirectional data bus

The unit is operational only when CS1=0 and bar CS2=0

The small x's under the address bus lines designate those line that must be connected to the address inputs in each chip

Memory Address Map

Address space assignment to each memory chip

Example: 512 bytes RAM and 512 bytes ROM

Component	Hexa address	Address bus 10 9 8 7 6 5 4 3 2 1
RAM 1	0000 - 007F	0 0 0 x x x x x x x
RAM 2	0080 - 00FF	0 0 1 x x x x x x x
RAM 3	0100 - 017F	0 1 0 x x x x x x x
RAM 4	0180 - 01FF	0 1 1 x x x x x x x
ROM	0200 - 03FF	1 x x x x x x x x x

Memory Connection to CPU

-**RAM and ROM chips are connected to a CPU through the data and address buses**

-- **The low-order lines in the address bus select the byte within the chips and other lines in the address bus select a particular chip through its chip select inputs**

Connection of Memory to CPU