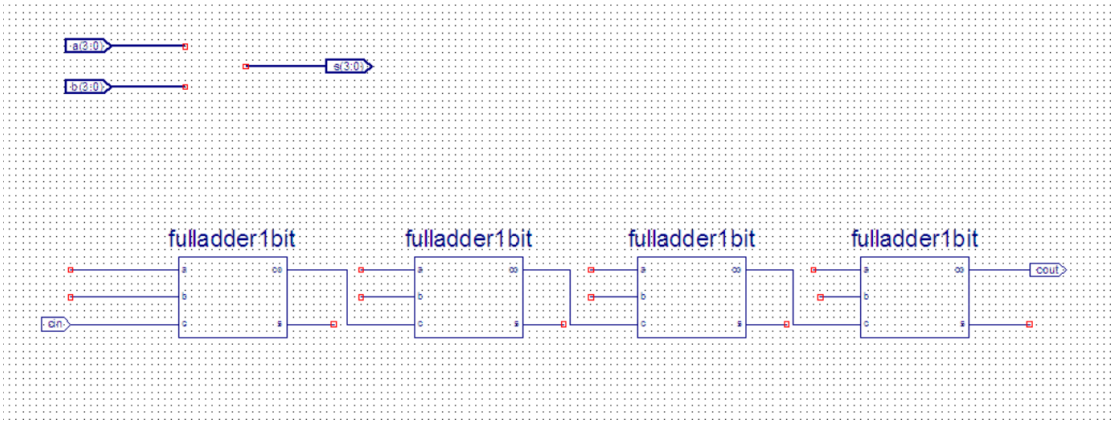
EE533 - Laboratory 2

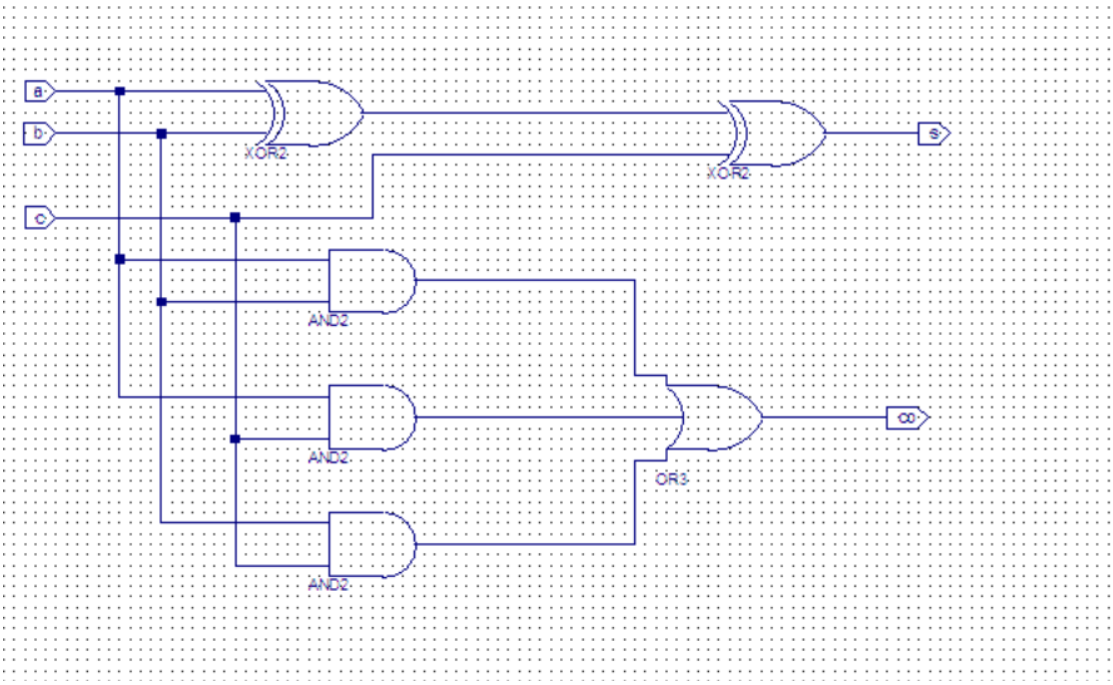
1. Xilinx ISE 10.1 In-depth Tutorial

1.1. Screen capture of schematics

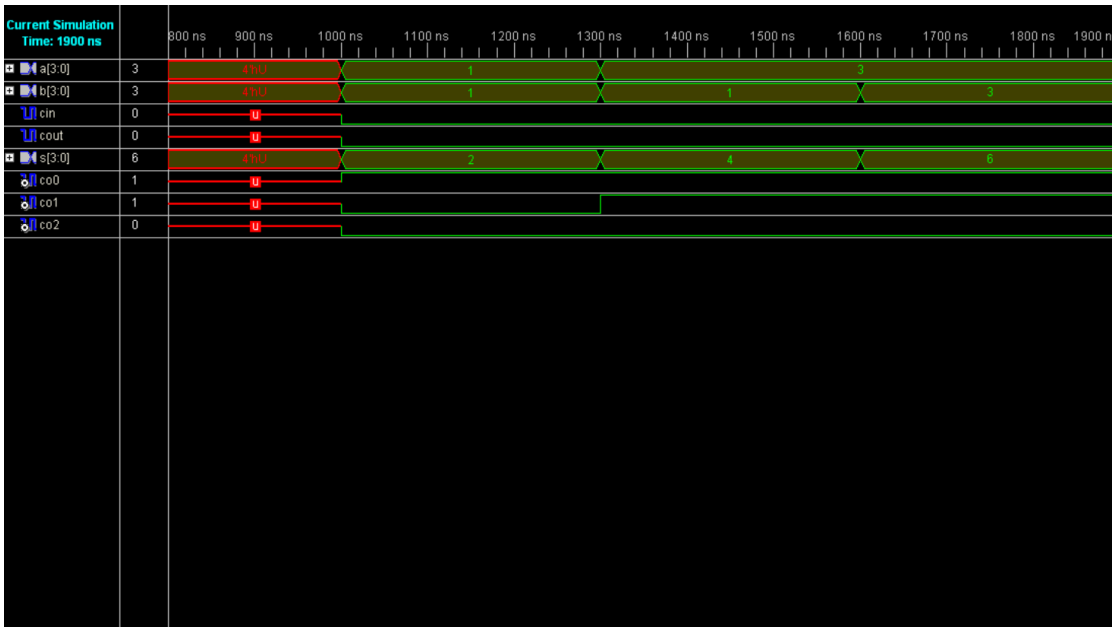
Since the original tutorial's "stopwatch.sch" was no longer compilable, I use the ise_tutorial.mkv video for the tutorial section. The following is a 4-bit adder, which uses 4 1-bit full adders as components.



Inside the 1-bit full adder:



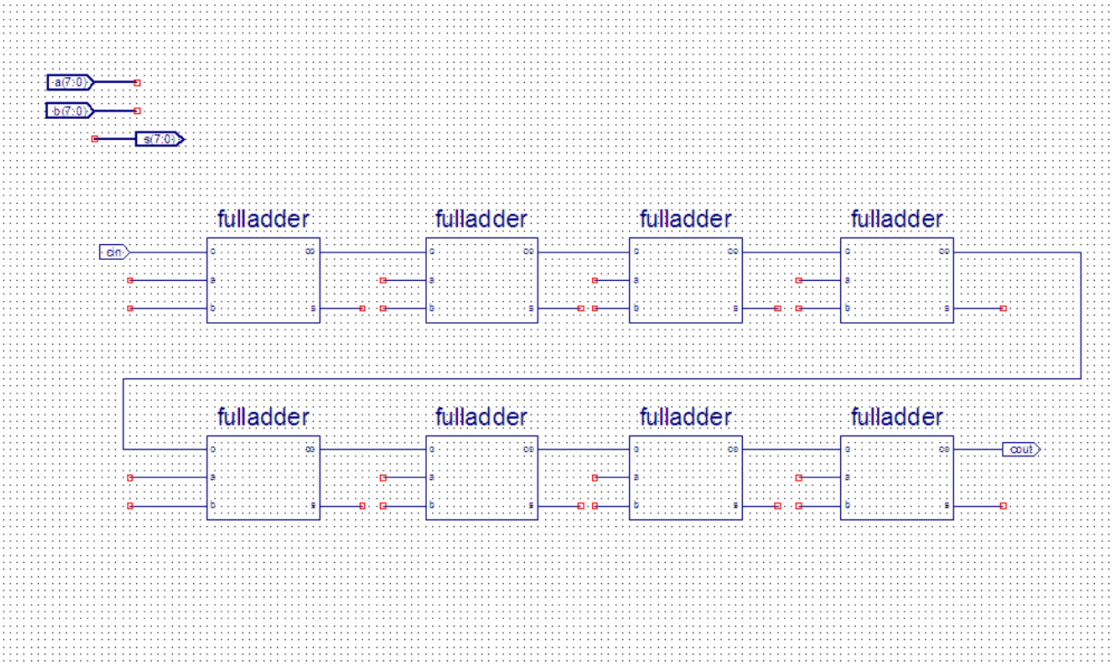
1.2. Waveform

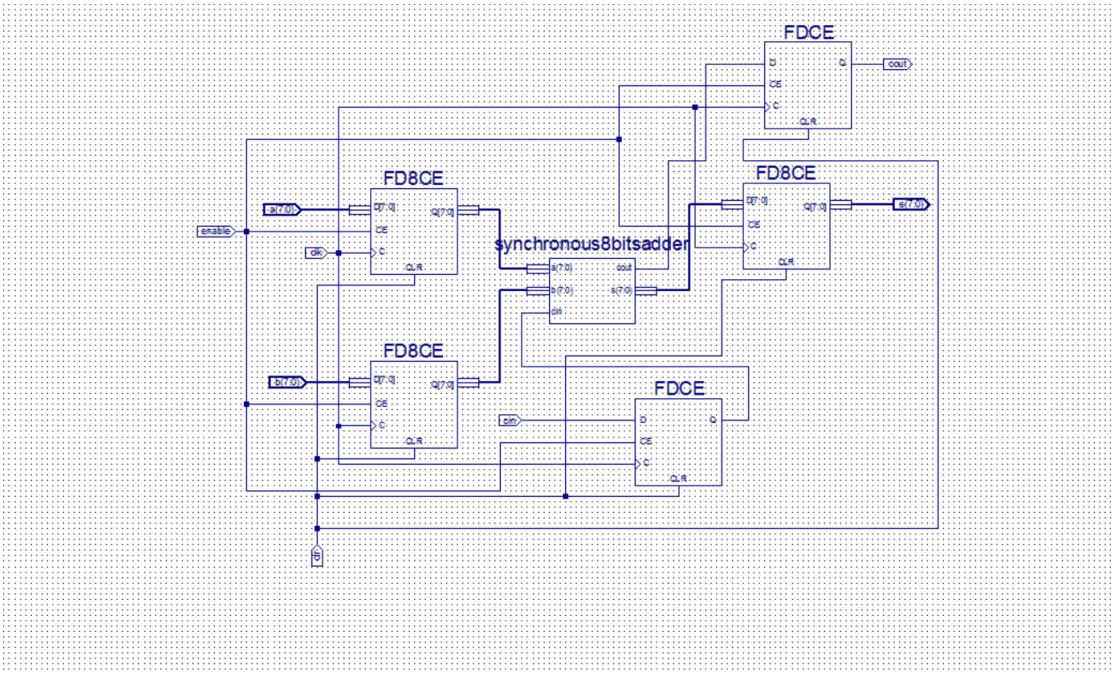

Current Simulation Time: 1900 ns
800 ns
900 ns
1000 ns
1100 ns
1200 ns
1300 ns
1400 ns
1500 ns
1600 ns
1700 ns
1800 ns
1900 n
a[3:0]
3
4'hU
1
3
b[3:0]
3
4'hU
1
1
3
cin
0
U
cout
0
U
s[3:0]
6
4'hU
2
4
6
co0
1
U
co1
1
U
co2
0
U

2. Designing and Simulating a Synchronous 8-bit Adder

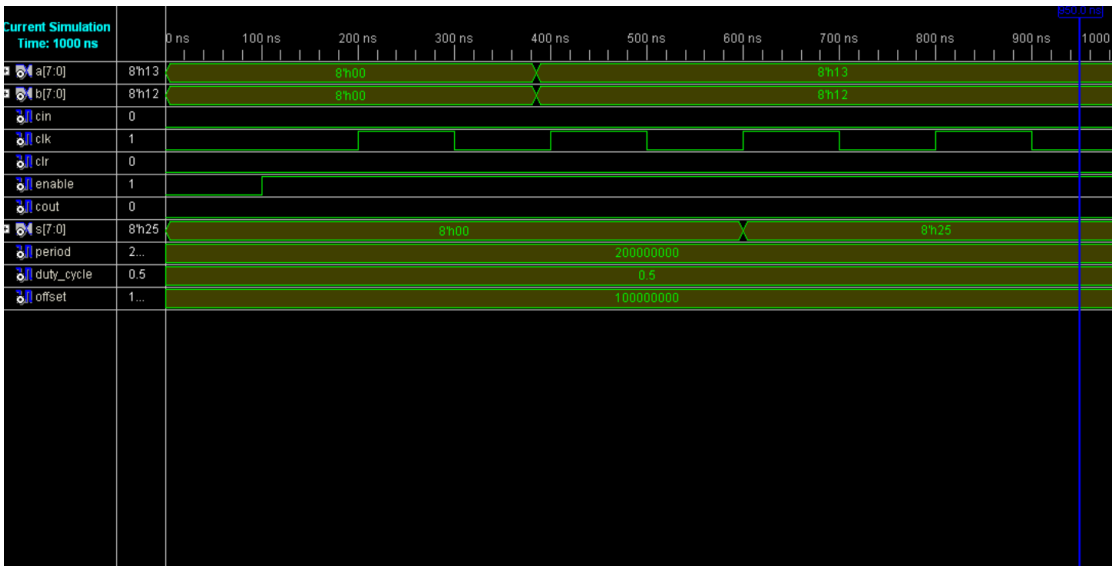
2.1. Designing and Simulating a Synchronous 8-bit Adder

A synchronous 8-bit Adder uses 8 1-bit full adders in a sequential manner. To have the synchronous functionality, I use DFFs in front of inputs and after the outputs. So that when the positive edge of the clock comes, the input of the adder changes.





2.2. Waveforms

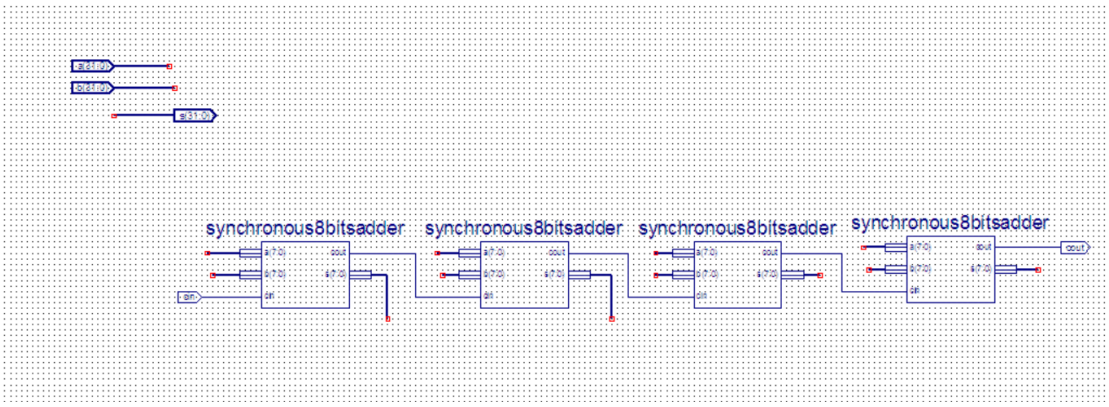


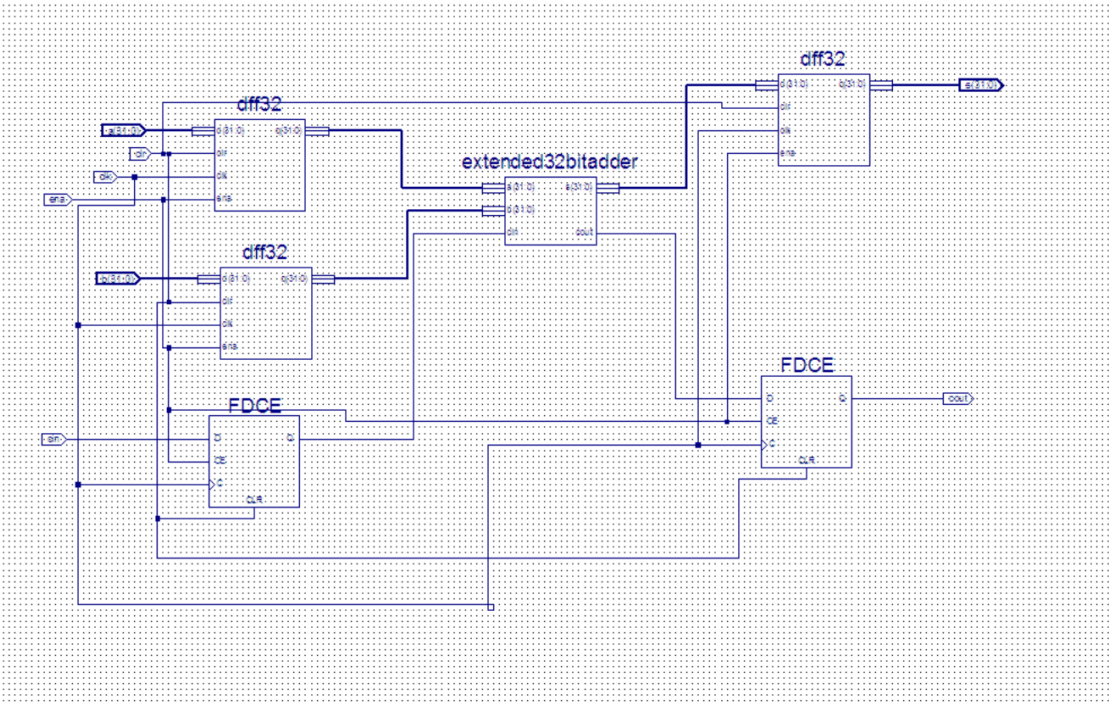
3. Extending Adder into 32-bit ALU

3.1. 32-bit Adder

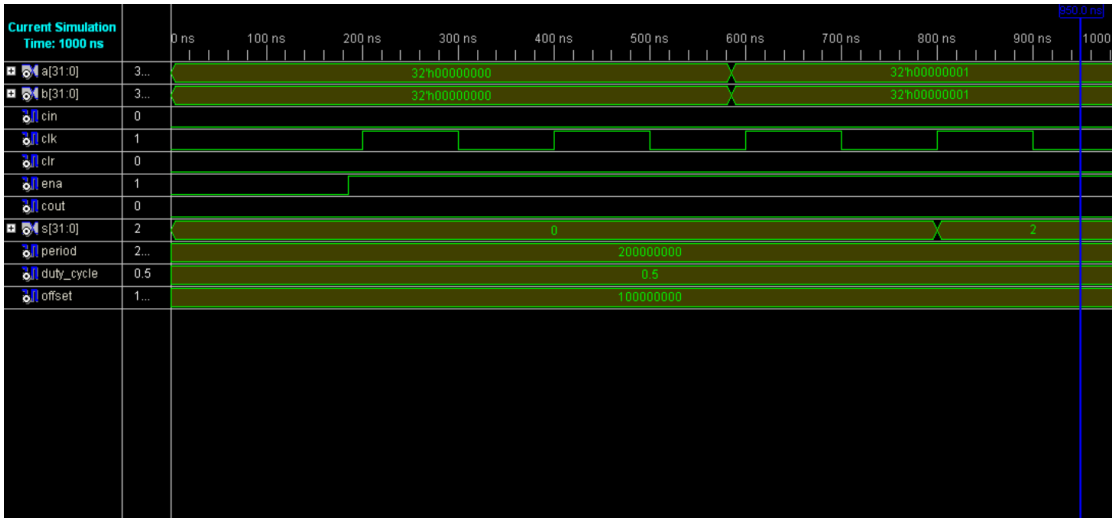
3.1.1. Screen capture of schematics

Same as the 32-bit adder, but without 32-bit DFFs, I use 2 16-bit DFFs combined to a 32-bit DFF.



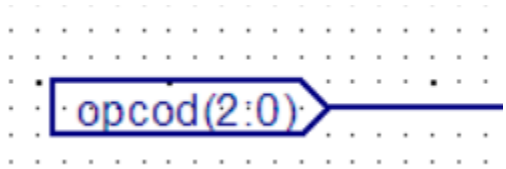


3.1.2. Waveforms



3.2. ALU

3.2.1. Brief description of the functions



In this section,

When the opcode is 000, the ALU does add calculation.

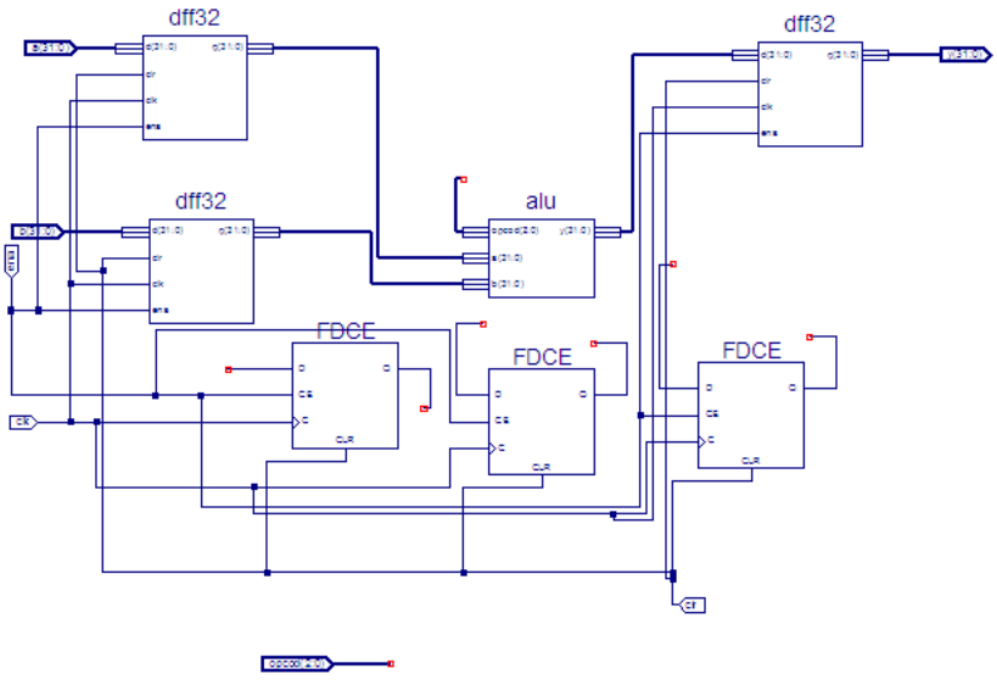
When the opcode is 001, the ALU does sub calculation.

When the opcode is 010, the ALU does and calculation.

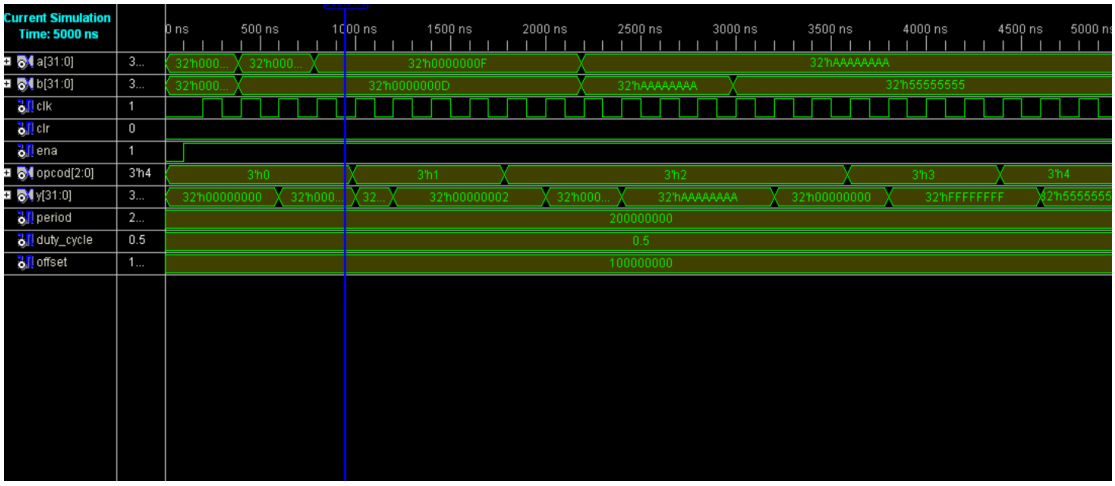
When the opcode is 011, the ALU does or calculation.

When the opcode is 100, the ALU does SHL calculation.

3.2.2. Screen capture of schematics



3.2.3. Waveforms



3.2.4. Log file of the mapper

Release 10.1 Map K.31 (nt)

Xilinx Mapping Report File for Design 'tb_syn_alu'

Design Information

Command Line : map -ise "C:/Documents and

Settings/student/Desktop/ee533/ee533_lab2/ee533_lab2.ise" -intstyle ise -p

xc2v1000-bg575-6 -cm area -pr off -k 4 -c 100 -tx off -o tb_syn_alu_map.ncd

tb_syn_alu.ngd tb_syn_alu.pcf

Target Device : xc2v1000

Target Package : bg575

Target Speed : -6

Mapper Version : virtex2 -- $Revision: 1.46 $

Mapped Date : Fri Jan 23 20:13:09 2026

Design Summary

Number of errors: 0

Number of warnings: 0

Logic Utilization:

Number of Slice Flip Flops: 99 out of 10,240 1%

Number of 4 input LUTs: 160 out of 10,240 1%

Logic Distribution:

Number of occupied Slices: 114 out of 5,120 2%

Number of Slices containing only related logic: 114 out of 114 100%

Number of Slices containing unrelated logic: 0 out of 114 0%

*See NOTES below for an explanation of the effects of unrelated logic.

Total Number of 4 input LUTs: 160 out of 10,240 1%

Number of bonded IOBs: 102 out of 328 31%

Number of BUFGMUXs: 1 out of 16 6%

Peak Memory Usage: 146 MB

Total REAL time to MAP completion: 0 secs

Total CPU time to MAP completion: 0 secs

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs. When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Table of Contents

Section 1 - Errors

Section 2 - Warnings

Section 3 - Informational

INFO:MapLib:562 - No environment variables are currently set.

INFO:LIT:244 - All of the single ended outputs in this design are using slew
rate limited output drivers. The delay on speed critical single ended outputs
can be dramatically reduced by designating them as fast outputs.

Section 4 - Removed Logic Summary

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4 block(s) removed

3 block(s) optimized away

3 signal(s) removed

Section 5 - Removed Logic

The trimmed logic report below shows the logic removed from your design due to
sourceless or loadless signals, and VCC or ground connections. If the removal
of a signal or symbol results in the subsequent removal of an additional signal
or symbol, the message explaining that second removal will be indented. This
indentation will be repeated as a chain of related logic is removed.

To quickly locate the original cause for the removal of a chain of logic, look
above the place where that logic is listed in the trimming report, then locate
the lines that are least indented (begin at the leftmost edge).

Loadless block "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXI_6" (OR) removed.
The signal "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXN_15" is loadless and has been
removed.
Loadless block "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXI_5" (AND) removed.
The signal "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXN_14" is loadless and has been
removed.
Loadless block "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXI_4" (AND) removed.
The signal "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXN_13" is loadless and has been
removed.
Loadless block "XLXI_1/XLXI_1/XLXI_1/XLXI_4/XLXI_9/XLXI_3" (AND) removed.

Optimized Block(s):

TYPE	BLOCK
AND2	XLXI_1/XLXI_10/XLXI_2/XLXI_1/XLXI_1/XLXI_1/I_36_9
BUF	XLXI_1/XLXI_5/XLXI_34

GND XST_GND

To enable printing of redundant blocks removed and signals merged, set the

detailed map report option and rerun map.

Section 6 - IOB Properties

IOB Name	Type	Direction	IO Standard	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
a<0>	IOB	INPUT	LVTTL					
a<1>	IOB	INPUT	LVTTL					
a<2>	IOB	INPUT	LVTTL					
a<3>	IOB	INPUT	LVTTL					
a<4>	IOB	INPUT	LVTTL					
a<5>	IOB	INPUT	LVTTL					
a<6>	IOB	INPUT	LVTTL					
a<7>	IOB	INPUT	LVTTL					
a<8>	IOB	INPUT	LVTTL					
a<9>	IOB	INPUT	LVTTL					
a<10>	IOB	INPUT	LVTTL					
a<11>	IOB	INPUT	LVTTL					
a<12>	IOB	INPUT	LVTTL					
a<13>	IOB	INPUT	LVTTL					
a<14>	IOB	INPUT	LVTTL					
a<15>	IOB	INPUT	LVTTL					
a<16>	IOB	INPUT	LVTTL					
a<17>	IOB	INPUT	LVTTL					
a<18>	IOB	INPUT	LVTTL					
a<19>	IOB	INPUT	LVTTL					
a<20>	IOB	INPUT	LVTTL					
a<21>	IOB	INPUT	LVTTL					
a<22>	IOB	INPUT	LVTTL					
a<23>	IOB	INPUT	LVTTL					
a<24>	IOB	INPUT	LVTTL					
a<25>	IOB	INPUT	LVTTL					
a<26>	IOB	INPUT	LVTTL					
a<27>	IOB	INPUT	LVTTL					
a<28>	IOB	INPUT	LVTTL					
a<29>	IOB	INPUT	LVTTL					
a<30>	IOB	INPUT	LVTTL					
a<31>	IOB	INPUT	LVTTL					

b<0>	IOB	INPUT	LVTTL					
b<1>	IOB	INPUT	LVTTL					
b<2>	IOB	INPUT	LVTTL					
b<3>	IOB	INPUT	LVTTL					
b<4>	IOB	INPUT	LVTTL					
b<5>	IOB	INPUT	LVTTL					
b<6>	IOB	INPUT	LVTTL					
b<7>	IOB	INPUT	LVTTL					
b<8>	IOB	INPUT	LVTTL					
b<9>	IOB	INPUT	LVTTL					
b<10>	IOB	INPUT	LVTTL					
b<11>	IOB	INPUT	LVTTL					
b<12>	IOB	INPUT	LVTTL					
b<13>	IOB	INPUT	LVTTL					
b<14>	IOB	INPUT	LVTTL					
b<15>	IOB	INPUT	LVTTL					
b<16>	IOB	INPUT	LVTTL					
b<17>	IOB	INPUT	LVTTL					
b<18>	IOB	INPUT	LVTTL					
b<19>	IOB	INPUT	LVTTL					
b<20>	IOB	INPUT	LVTTL					
b<21>	IOB	INPUT	LVTTL					
b<22>	IOB	INPUT	LVTTL					
b<23>	IOB	INPUT	LVTTL					
b<24>	IOB	INPUT	LVTTL					
b<25>	IOB	INPUT	LVTTL					
b<26>	IOB	INPUT	LVTTL					
b<27>	IOB	INPUT	LVTTL					
b<28>	IOB	INPUT	LVTTL					
b<29>	IOB	INPUT	LVTTL					
b<30>	IOB	INPUT	LVTTL					
b<31>	IOB	INPUT	LVTTL					
clk	IOB	INPUT	LVTTL					
clr	IOB	INPUT	LVTTL					
ena	IOB	INPUT	LVTTL					
opcod<0>	IOB	INPUT	LVTTL					
opcod<1>	IOB	INPUT	LVTTL					
opcod<2>	IOB	INPUT	LVTTL					
y<0>	IOB	OUTPUT	LVTTL	12	SLOW			
y<1>	IOB	OUTPUT	LVTTL	12	SLOW			
y<2>	IOB	OUTPUT	LVTTL	12	SLOW			
y<3>	IOB	OUTPUT	LVTTL	12	SLOW			
y<4>	IOB	OUTPUT	LVTTL	12	SLOW			
y<5>	IOB	OUTPUT	LVTTL	12	SLOW			

y<6>	IOB	OUTPUT	LVTTL	12	SLOW			
y<7>	IOB	OUTPUT	LVTTL	12	SLOW			
y<8>	IOB	OUTPUT	LVTTL	12	SLOW			
y<9>	IOB	OUTPUT	LVTTL	12	SLOW			
y<10>	IOB	OUTPUT	LVTTL	12	SLOW			
y<11>	IOB	OUTPUT	LVTTL	12	SLOW			
y<12>	IOB	OUTPUT	LVTTL	12	SLOW			
y<13>	IOB	OUTPUT	LVTTL	12	SLOW			
y<14>	IOB	OUTPUT	LVTTL	12	SLOW			
y<15>	IOB	OUTPUT	LVTTL	12	SLOW			
y<16>	IOB	OUTPUT	LVTTL	12	SLOW			
y<17>	IOB	OUTPUT	LVTTL	12	SLOW			
y<18>	IOB	OUTPUT	LVTTL	12	SLOW			
y<19>	IOB	OUTPUT	LVTTL	12	SLOW			
y<20>	IOB	OUTPUT	LVTTL	12	SLOW			
y<21>	IOB	OUTPUT	LVTTL	12	SLOW			
y<22>	IOB	OUTPUT	LVTTL	12	SLOW			
y<23>	IOB	OUTPUT	LVTTL	12	SLOW			
y<24>	IOB	OUTPUT	LVTTL	12	SLOW			
y<25>	IOB	OUTPUT	LVTTL	12	SLOW			
y<26>	IOB	OUTPUT	LVTTL	12	SLOW			
y<27>	IOB	OUTPUT	LVTTL	12	SLOW			
y<28>	IOB	OUTPUT	LVTTL	12	SLOW			
y<29>	IOB	OUTPUT	LVTTL	12	SLOW			
y<30>	IOB	OUTPUT	LVTTL	12	SLOW			
y<31>	IOB	OUTPUT	LVTTL	12	SLOW			

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Modular Design Summary

Modular Design not used for this design.

Section 11 - Timing Report

This design was not run using timing mode.

Section 12 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 13 - Control Set Information

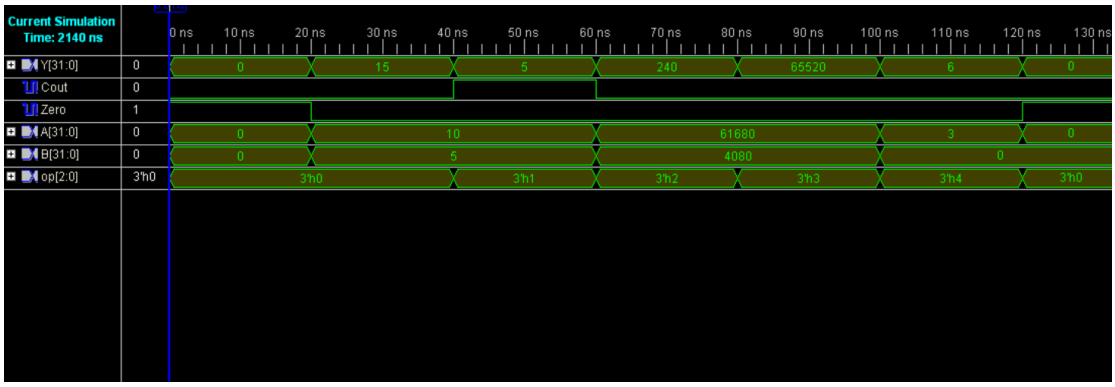
No control set information for this architecture.

Section 14 - Utilization by Hierarchy

This feature is not supported for this architecture.

3.3. 32-bit ALU Verilog Version

3.3.1. Waveforms



3.3.2. Log file of the mapper

Release 10.1 Map K.31 (nt)

Xilinx Mapping Report File for Design 'alu32'

Design Information

Command Line : map -ise "C:/Documents and

Settings/student/Desktop/ee533/alu_new/alu_new.ise" -intstyle ise -p

xc2v1000-bg575-6 -cm area -pr off -k 4 -c 100 -tx off -o alu32_map.ncd alu32.ngd

alu32.pcf

Target Device : xc2v1000

Target Package : bg575

Target Speed : -6

Mapper Version : virtex2 -- $Revision: 1.46 $

Mapped Date : Fri Jan 23 20:05:53 2026

Design Summary

Number of errors: 0

Number of warnings: 0

Logic Utilization:

Number of 4 input LUTs: 106 out of 10,240 1%

Logic Distribution:

Number of occupied Slices: 53 out of 5,120 1%

Number of Slices containing only related logic: 53 out of 53 100%

Number of Slices containing unrelated logic: 0 out of 53 0%

*See NOTES below for an explanation of the effects of unrelated logic.

Total Number of 4 input LUTs: 106 out of 10,240 1%

Number of bonded IOBs: 101 out of 328 30%

Peak Memory Usage: 145 MB

Total REAL time to MAP completion: 0 secs

Total CPU time to MAP completion: 0 secs

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs. When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

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INFO:LIT:244 - All of the single ended outputs in this design are using slew

rate limited output drivers. The delay on speed critical single ended outputs

can be dramatically reduced by designating them as fast outputs.

Section 4 - Removed Logic Summary

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2 block(s) optimized away

Section 5 - Removed Logic

Optimized Block(s):

TYPE BLOCK

GND XST_GND

VCC XST_VCC

Section 6 - IOB Properties

IOB Name	Type	Direction	IO Standard	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
A<0>	IOB	INPUT	LVTTL					
A<1>	IOB	INPUT	LVTTL					
A<2>	IOB	INPUT	LVTTL					
A<3>	IOB	INPUT	LVTTL					
A<4>	IOB	INPUT	LVTTL					
A<5>	IOB	INPUT	LVTTL					
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A<8>	IOB	INPUT	LVTTL					
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A<10>	IOB	INPUT	LVTTL					
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A<13>	IOB	INPUT	LVTTL					
A<14>	IOB	INPUT	LVTTL					
A<15>	IOB	INPUT	LVTTL					

A<16>	IOB	INPUT	LVTTL						
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A<30>	IOB	INPUT	LVTTL						
A<31>	IOB	INPUT	LVTTL						
B<0>	IOB	INPUT	LVTTL						
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B<25>	IOB	INPUT	LVTTL						
B<26>	IOB	INPUT	LVTTL						
B<27>	IOB	INPUT	LVTTL						

B<28>	IOB	INPUT	LVTTL					
B<29>	IOB	INPUT	LVTTL					
B<30>	IOB	INPUT	LVTTL					
B<31>	IOB	INPUT	LVTTL					
Cout	IOB	OUTPUT	LVTTL	12	SLOW			
Y<0>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<1>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<2>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<3>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<4>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<5>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<6>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<7>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<8>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<9>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<10>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<11>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<12>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<13>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<14>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<15>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<16>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<17>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<18>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<19>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<20>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<21>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<22>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<23>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<24>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<25>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<26>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<27>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<28>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<29>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<30>	IOB	OUTPUT	LVTTL	12	SLOW			
Y<31>	IOB	OUTPUT	LVTTL	12	SLOW			
Zero	IOB	OUTPUT	LVTTL	12	SLOW			
op<0>	IOB	INPUT	LVTTL					
op<1>	IOB	INPUT	LVTTL					
op<2>	IOB	INPUT	LVTTL					

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Modular Design Summary

Modular Design not used for this design.

Section 11 - Timing Report

This design was not run using timing mode.

Section 12 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 13 - Control Set Information

No control set information for this architecture.

Section 14 - Utilization by Hierarchy

This feature is not supported for this architecture.

3.3.3. Brief comment on the number of gates as compared to the schematic version

The schematic implementation utilized 160 LUTs and 114 slices, while the Verilog implementation required only 106 LUTs and 53 slices. This demonstrates that the Verilog version achieves significantly better logic efficiency. The number of bonded I/O blocks (IOBs) was similar in both designs (102 for schematic and 101 for Verilog), indicating that the interface complexity is nearly identical and that the primary differences arise from internal logic optimization.