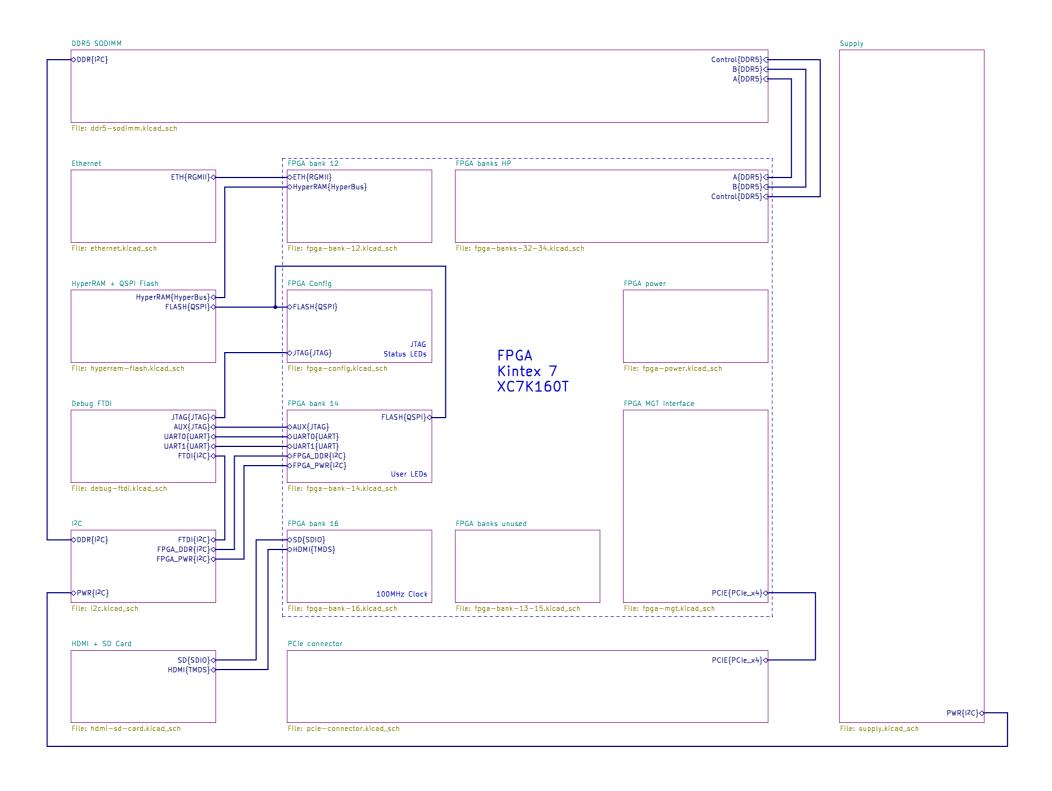
SO-DIMM DDR5 Tester











960-27-12-D-AB-0 H2 Lightpipe_Mentor_1296.2013 Antmicro Ltd
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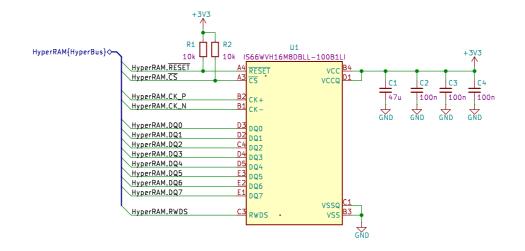
Sheet: /
File: sodimm-ddr5-tester.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18 Rev: 1.1.1

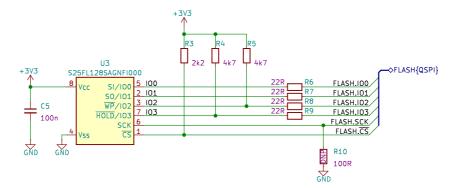
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1 Id: 1/17

HyperRAM



(Q)SPI flash

Master SPI Quad (x4) configuration scheme Follows Figure 2—14 7 Series FPGAs Configuration User Guide UG470 (v1.13.1)







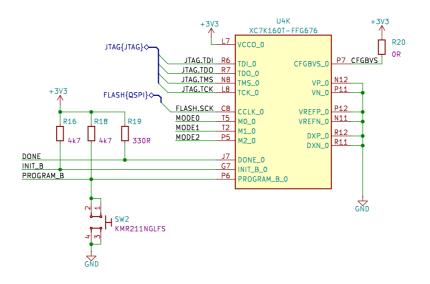
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Sheet: /HyperRAM + QSPI Flash/ File: hyperram-flash.kicad_sch

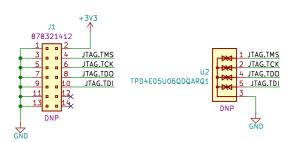
Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1

FPGA BANK 0



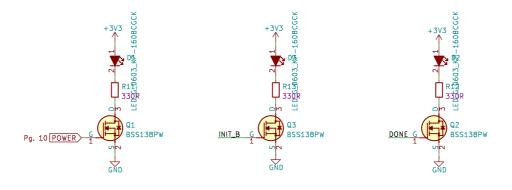
JTAG Connector
Compatible with Xilinx Platform Cable



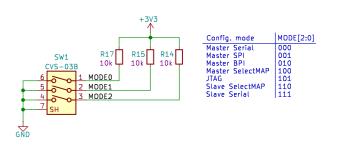




STATUS LEDs



Configuration ModesFor details, see UG470 p. 21

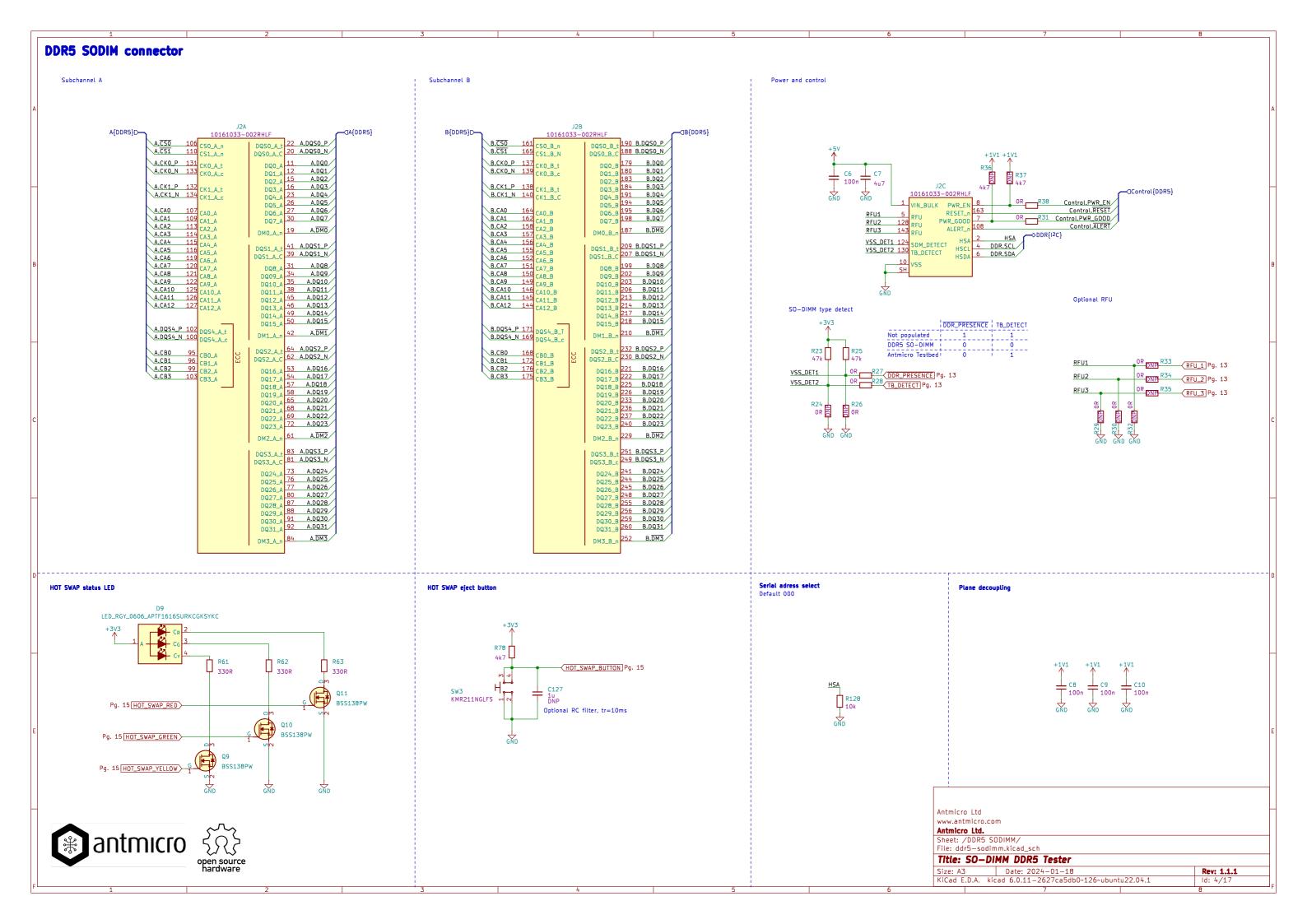


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Sheet: /FPGA Config/ File: fpga—config.kicad_sch

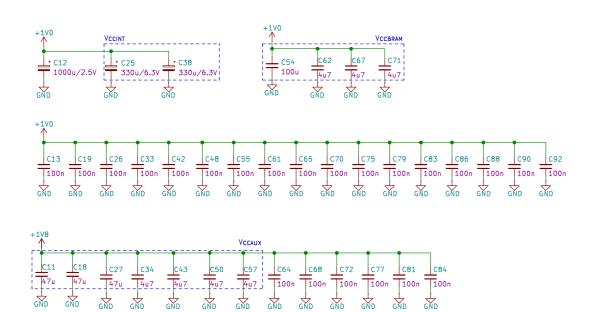
Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1

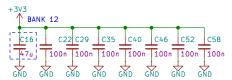


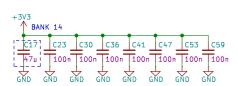
FPGA Power rails

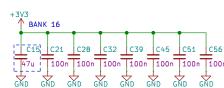
Bank marked by dahed line referenced from 7 Series FPGAs PCB Design Guide UG483 (FFG+FBG Package worst case) MGT decoupling marked by dahed line referenced from 7 Series FPGAs PCB Design Guide UG482 (FFG+FBG Package worst case)

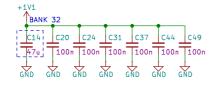


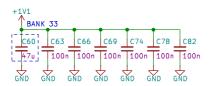


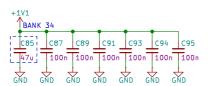


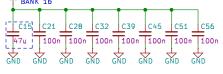




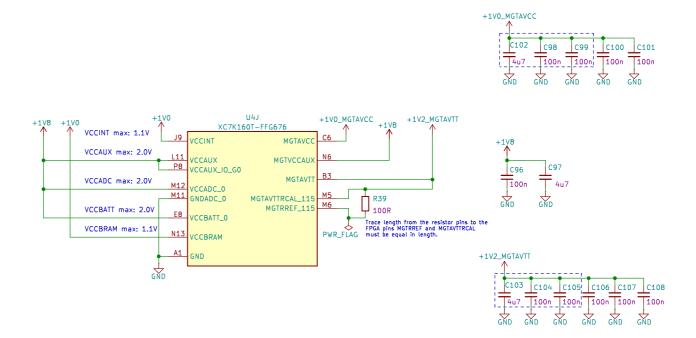






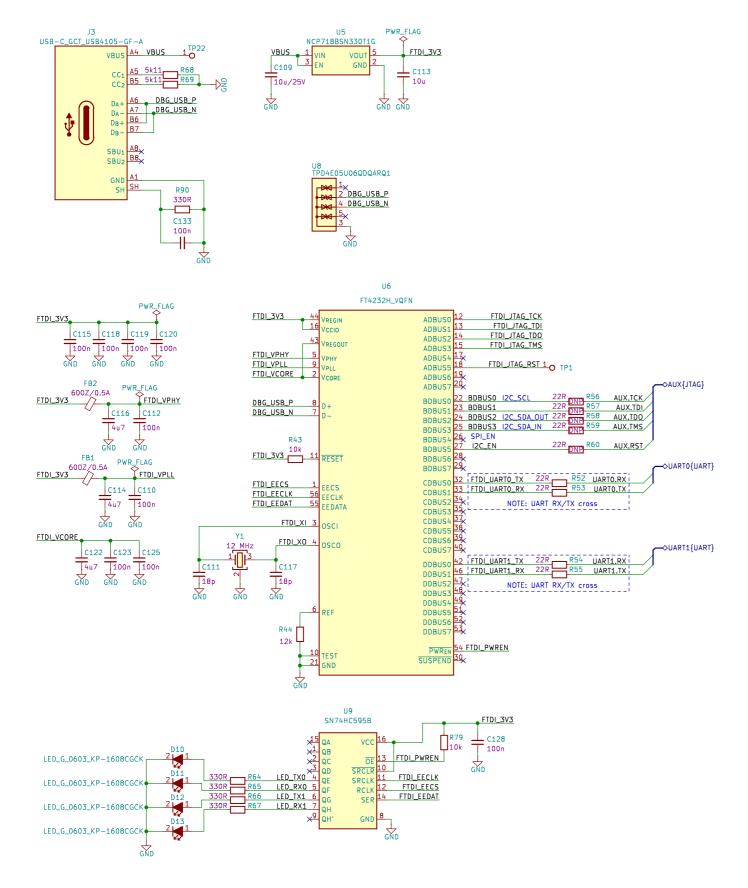


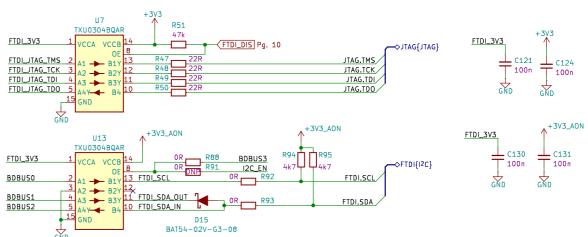




Antmicro Ltd www.antmicro.com Antmicro Ltd. Sheet: /FPGA power/ File: fpga-power.kicad_sch Title: SO-DIMM DDR5 Tester Size: A3 Date: 2024-01-18
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1

Debug FTDI





Antmicro Ltd www.antmicro.com Antmicro Ltd. Sheet: /Debug FTDI/ File: debug-ftdi.kicad_sch

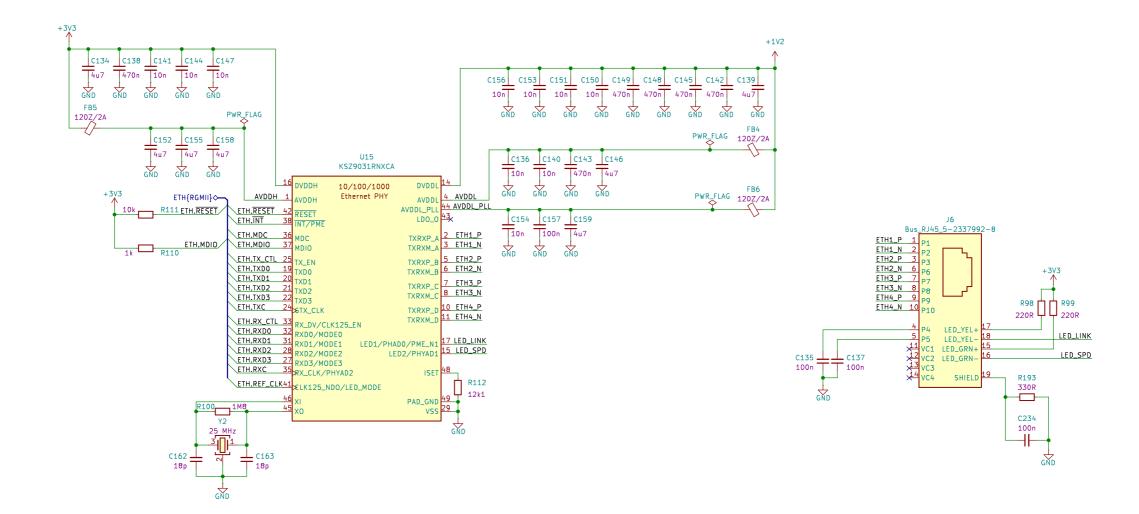
Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1

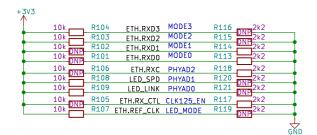




Gigabit Ethernet



Bootstrap configuration



MODE[3:0]: 1100 (RGMII mode - Advertise 1000BASE-T full-duplex only) PHYAD[4:0]: 00011 CLK125_EN: 0, disabled LED_MODE: 1, Single-LED mode





Reference plane decoupl

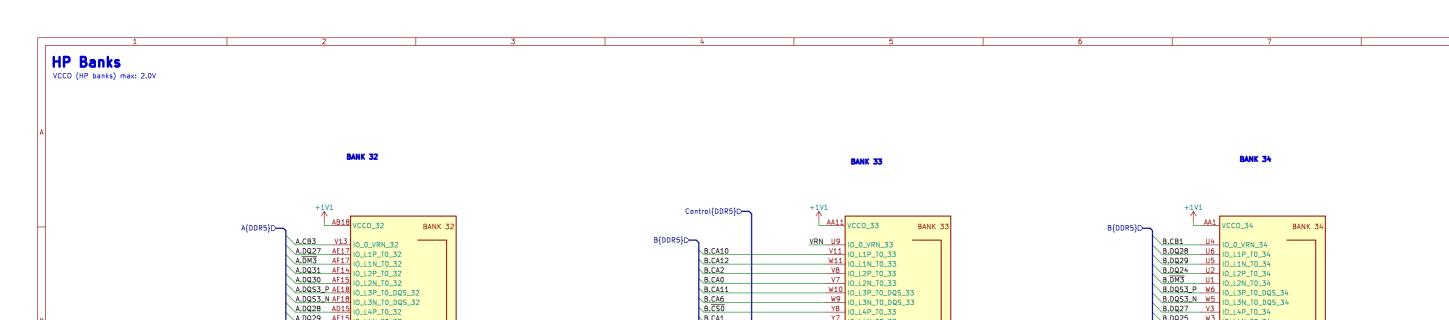


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Sheet: /Ethernet/
File, othernet kiese seh

File: ethernet.kicad_sch

Title: SO-DIMM DDR5 Tester

ze: A3	Date: 2024-01-18	Rev: 1.1.1
Cad F D A	kicad 6 0 11 - 2627ca5db0~126~ubuntu22 04 1	Id: 8/17



B.CA1

B.CA5

B.CA4

B.DQS4_P

B.DQS4_N

B.CKO_P B.CKO_N

B.CA7

B.CA8

B.CA9

B.CK1_P

B.CK1_N

Control.PWR_EN

Control.ALERT

B.CA3

A(DDR5)D-

A.CA12

A.CA8

A.CA11

A.CA10

A.CA5

A.CA6

A.CA4

A.CA7

A CKO P

A.CKO_N

A.CS1

A.CA1

A.CSO

A.CA3

A.CAO

A.CA2

A.CK1_P

A.CK1_N

A.DQS4_P

A.DQS4_N

Y7 | 10_L4N_T0_33 | 10_L5P_T0_33

Y10 IO_L5N_T0_33

VEEF W8 10_L6P_T0_33

AE7 10_L7P_T1_33

AF7 10_L7P_T1_33

AA8 10_L8P_T1_33

AA7 10_L8N_T1_33

ACB IO_L9P_T1_DQS_33

AC7 | IO_L10N_T1_33 | AA9 | IO_L11P_T1_SRCC_33 | IO_L11P_T1_SRCC_33

AB9 IO_L11N_T1_SRCC_33
AC9 IO_L12P_T1_MRCC_33

AB10 10_L14N_T2_SRCC_33

AB12 | IO_L15P_T2_DQS_33 | AC12 | IO_L15P_T2_DQS_33 | AA13 | IO_L16P_T2_33 | AI3 | IO_L16P_T2_33 | AI3 | AI3 | IO_L16P_T2_33 | AI3 | IO_L16P_T2_5 | AI3 | AI3 | IO_L16P_T2_5 | AI3 | AI3 | IO_L16P_T2_5 | AI3 | AI3

IO_L18P_T2_33

AA12 10_L16N_T2_33

AC13 IO_L17P_T2_33

AD13 IO_L17N_T2_33

Y12 | IO_L18F_12_33 AD11 | IO_L19P_T3_33 VREFAE11 | IO_L19P_T3_33 VREFAE10 | IO_L20P_T3_33

AE13 IO_L23P_T3_33

AF13 IO_L23N_T3_33

AF10 IO_L24P_T3_33

AF9 10_L24N_T3_33

VRP V12 10_25_VRP_33

AE12 10_L21P_T3_DQS_33

O_L21N_T3_DQS_33 AE8 10_L22P_T3_33 AF8 10_L22N_T3_33

Y13

Control.PWR_GOOD AE10 10_L20N_T3_33

AF12

XC7K160T-FFG676

AD8 | IO_L9N_T1_DQS_33

AB7 IO_L10P_T1_33

O_L3N_T0_DQS_34

0_L6N_T0_VREF_34

0 L9N T1 DQS 34

D_L11P_T1_SRCC_3

O_L11N_T1_SRCC_34

0 L12P T1 MRCC 34

0 L13P T2 MRCC 34

0 114P T2 SRCC 34

O_L14N_T2_SRCC_34

0 115P T2 DQS 34

0_L15N_T2_DQS_34

O_L16P_T2_34

0 I 16N T2 34

0 117N T2 34

D_L18P_T2_34

0 L18N T2 34

0_L19P_T3_34

0_L20P_T3_34

0_L20N_T3_34

0 L22P T3 34

0_L22N_T3_34

0_L23P_T3_34

0 L23N T3 34

D_L24P_T3_34

0 L24N T3 34

O L21P T3 DQS 34

O_L19N_T3_VREF_34

XC7K160T-FFG676

0_L4P_T0_34

O_L4N_T0_34

0_L5P_T0_34

0 L6P T0 34

0 L7P T1 34

0_L8P_T1_34

0_L8N_T1_34

O 110N T1 34

B.DQ27 V3

B.DQ25 W3

B.DQ31 U7 B.DQ30 V6

B.DQ26 V4

B.DQ18 Y3

\B.DQ21 Y2

B.DQ23 V2

B.DQ22 V1 B.DQS2_P AB1

B.DQS2_N AC1

B.DQ20 W1 B.DM2 Y1

B.DQ16 AB2

B.DQ19 AC2

B.CB2 AA3 B.DQ17 AA2

B.DQ15 AA4

B.DQ14 AB4

B.DQ13 AC4

B.DQ12 AC3

B.DQS1_P AA5

B.DQS1_N AB5

B.DQ11 AC6

B.DQ9 Y6

B.DQ10 Y5 B.CB0 AD6

B.DM1 AD5

B.DQ1 AD4 VREF AD3 B.DQ7 AD1

B.DQ6 AE1

B.DQSO_P AF5
B.DQSO_N AF4
B.DMO AE3

∖B.DQ5 AE2

N.DQO

B.DQ4

B.CB3

B.DQ3 AE6

B.DQ2 AF3

AE5

AF2 T7

B.DQ8 AB6

VREF W4

0_L3N_T0_DQS_32 0_L4P_T0_32

D_L6N_T0_VREF_32

_L9P_T1_DQS_32

O_L9N_T1_DQS_32 O_L10P_T1_32

)_L11P_T1_SRCC_32

IO_L11N_T1_SRCC_32 IO_L12P_T1_MRCC_32

0 L13P T2 MRCC 32

D_L13N_T2_MRCC_32

D_L14N_T2_SRCC_32

O_L15P_T2_DQS_32 O_L15N_T2_DQS_32

D_L16P_T2_32

) I 16N T2 32

D_L17N_T2_32

)_L18P_T2_32

O_L18N_T2_32 O_L19P_T3_32

D_L19N_T3_VREF_32

D_L21N_T3_DQS_32

0 114P T2 SRCC 32

XC7K160T-FFG676

D_L4N_T0_32

0_L5P_T0_32

0 L6P T0 32

0_L7P_T1_32 10_L7N_T1_32

_L8P_T1_32

0_L8N_T1_32

A.DQ28 AD15

A.DQ29 AE15

A.DQ26 AF19

A.DQ24 AF20

A.DQ25 AD16

A.CBO AA14 A.DM2 AA15

A.DQ21 AC14

A.DQ20 AD14 A.DQS2_P Y15

A.DQS2_N Y16

A.DQ22 AB14

A.DQ17 AA17

A.DQ18 AB16

A.DQ12 AC18

A.DQ15 AD18

A.DQ9 AB17

A.DQ14 AC17

A.DQS1_P AD20

A.DQS1_N AE20 A.DQ8 AA19

A.DQ11 AA20 A.DM1 AC19

A.DQ13 AD19

A.DQ10 AB19

A.CB1 AB20

A.DQSO_N W19

VREF Y18

A.DQ1 V16 | 10_L20P_T3_32 | 10_L20N_T3_32 | 10_L20N_T3_32

A.DQ4 W15 10_L22P_T3_32

A.DQ5 W16 IO_L22P_T3_32 A.DQ3 V18 IO_L22P_T3_32 A.DM0 V19 IO_L23P_T3_32 A.DQ0 V14 IO_L23P_T3_32 A.DQ7 W14 IO_L24P_T3_32 A.DQ7 W14 IO_L24P_T3_32

A.CB2 W13 10_25_VRP_32

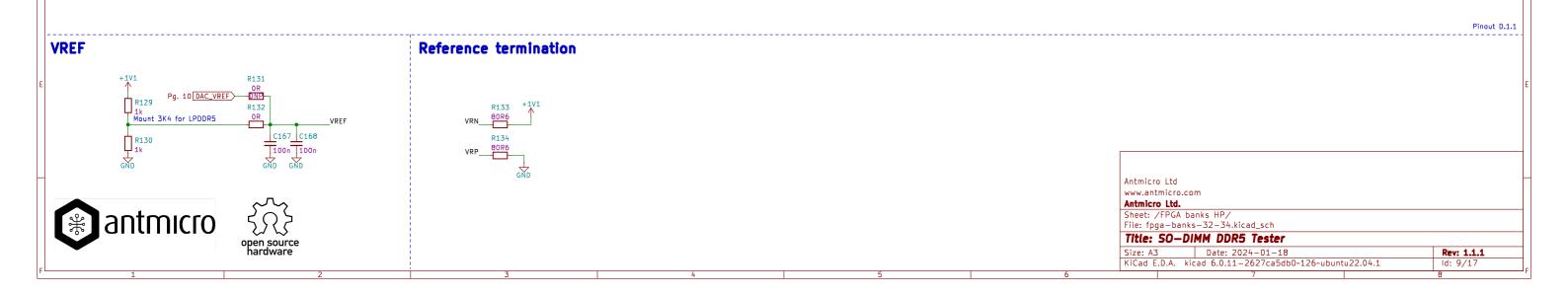
A.DQSO_P W18 | 10_L21P_T3_DQS_32

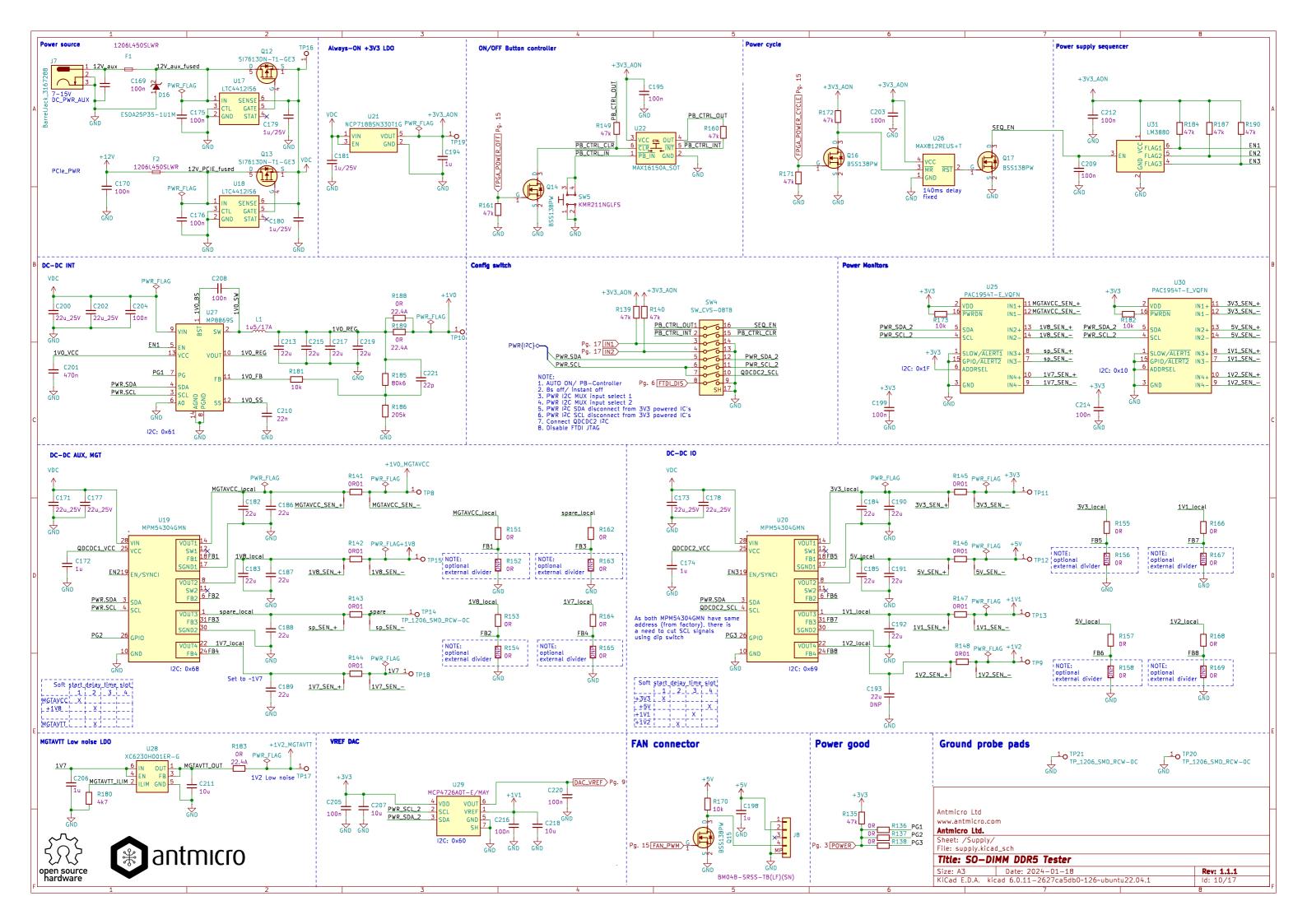
A.DQ6 Y17

A.DQ19 AC16

A.DQ23 AB15 10_L10N_T1_32

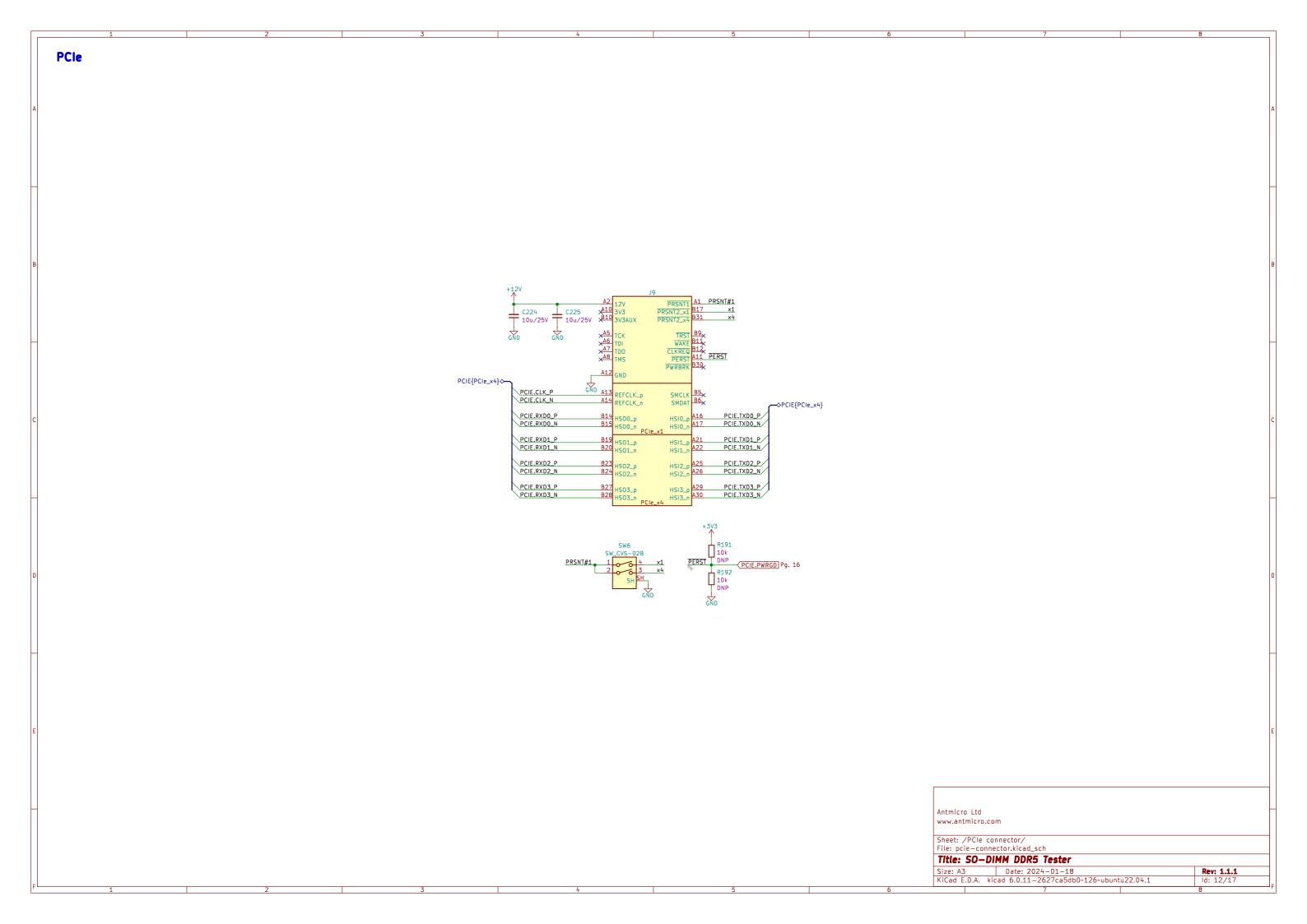
VREF AE16





MGT Interface Place capacitors close to connector BANK 115 U4| BANK 116

XC7K160T-FFG676 →PCIE{PCIe_x4} PCIE.TXD3_P GTX_TX0_P X-P2 X-P1 MGTXTXP0_115 X-M2 X-M1 MGTXTXP1_115 X-M2 MGTXTXP1_115 X-M2 MGTXTXP2_115 X-M3 MGTXTXP2_115 X-M3 MGTXTXP3_115 X-M3 MGTXTXP3_115 MGTXTXN3_115 GTX_TX0_P GTX_TX0_N GTX_TX1_P GTX_TX0_N MGTXTXP0_116 MGTXTXN0_116 100n C227 PCIE.TXD2_P MGTXTXP1_116 MGTXTXN1_116 D1
MGTXTXP2_116 B2
MGTXTXN2_116 B1
MGTXTXP3_116 A4 GTX_TX1_N GTX_TX2_P GTX_TX2_N GTX_TX3_P GTX_TX3_N GTX_TX1_P GTX_TX1_N 100n C231 PCIE.TXD1_P/
100n C233 PCIE.TXD1_N/ 100n C228 GTX_TX2_P GTX_TX2_N MGTXTXN3_116 A3 XR4 XR3 MGTXRXNO_115 XN4 MGTXRXP1_115 XN3 MGTXRXP1_115 XL4 MGTXRXP2_115 MGTXRXN2_115 XJ4 MGTXRXNS_115 MGTXRXNS_115 GTX_RX0_P MGTXRXP0_116 MGTXRXPO.116 G3
MGTXRXNO.116 E4
MGTXRXNI.116 E3
MGTXRXXI.116 C4
MGTXRXXI.116 C3
MGTXRXP3.116 B6
MGTXRXN3.116 B5 GTX_RX0_P GTX_RX1_P GTX_RX1_N GTX_RX2_P 100n C229 GTX_TX3_P GTX_TX3_N PCIE.TXDO_N/ GTX_RX0_P PCIE.RXD3_P GTX_RX2_P GTX_RX3_P GTX_RX3_N GTX_RX0_N PCIE.RXD3_N GTX_RX1_P PCIE.RXD2_P GTX_RX1_N PCIE.RXD2_N MGTREFCLKOP_116
MGTREFCLKON_116
MGTREFCLK1P_116
MGTREFCLK1N_116
MGTREFCLK1N_116
MGTREFCLK1N_116
MGTREFCLK1N_116
MGTREFCLK1N_116
MGTREFCLK1N_116
MGTREFCLK0P_116
MGTREFCLK0P_11 ×H6 ×H5 ×K5 MGTREFCLKOP_115 ×K6 MGTREFCLK1P_115 MGTREFCLK1P_115 PCIE.RXD1_P PCIE.RXD1_N GTX_RX2_P GTX_RX2_N GTX_RX3_P PCIE.RXD0_P GTX_RX3_N PCIE.RXDO_N PCIE.CLK_P GTR_REFCLKO_P GTR_REFCLKO_N PCIE.CLK_N 100n C223 Antmicro Ltd www.antmicro.com Sheet: /FPGA MGT Interface/ File: fpga-mgt.kicad_sch Title: SO-DIMM DDR5 Tester Size: A3 Date: 2024-01-18
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1



BANK 12

VCC (18 berk) mer 3.67

VCC (18 berk) mer 3.6

U21	O_O_12
U22	O_L1P_TO_12
U25	O_L1P_TO_12
U25	O_L2P_TO_12
U25	O_L2P_TO_12
U25	O_L3P_TO_DQS_12
U26	O_L3P_TO_DQS_12
U26	O_L4P_TO_12
U26	O_L5P_TO_12
U26	O_L5P_TO_12
U26	O_L5P_TO_12
U27	O_L6P_TO_12
U28	O_L7P_T1_12
U29	O_L7P_T1_12
U29	O_L7P_T1_12
U29	O_L4P_T1_DQS_12
U29	O_L4P_T1_DQS_12
U29	O_L10P_T1_DQS_12
U29	O_L10P_T1_DQS_12
U20	O_L11P_T1_SRCC_12
U20	O_L13P_T2_MRCC_12
U20	O_L13P_T2_MRCC_12
U20	O_L15P_T2_DQS_12
U21	O_L15P_T2_DQS_12
U21	O_L15P_T2_DQS_12
U21	O_L15P_T2_12
U22	O_L17P_T2_12
U20	O_L17P_T2_12
U20	O_L10P_T3_12
U20	U20P_T3_12
U20P_T3_12 ETH{RGMII}♦ ETH_SEL XU24 ETH.RXD3 ETH.TX_CTL ETH.RXD2 ETH.RXD1 ETH.RXD0 ETH.MDC ETH.TXDO ETH.MDIO HyperRAM{HyperBus}↔ HyperRAM.CS ETH.RX_CTL ETH.TXD1 ETH.REF_CLK ETH.RXC ETH.TXC ETH.TXD2 ETH.RESET U4A XC7K160T-FFG676 HyperRAM.RESET ETH.TXD3 HyperRAM.RWDS HyperRAM.DQ7 AD23 (
AD24 (
AD24 (
AB22 (
AC22 (
AC21 (
AC HyperRAM.DQ2 HyperRAM.DQ5 HyperRAM.CK_P HyperRAM.CK_N HyperRAM.DQ0 AF23 (CAPTION AF23 | CAPTION AF23 | CAPTION AF24 | AF25 | CAPTION AF24 | AF24 | CAPTION AF44 | C HyperRAM.DQ4 HyperRAM.DQ1 HyperRAM.DQ6 HyperRAM.DQ3 0_25_12

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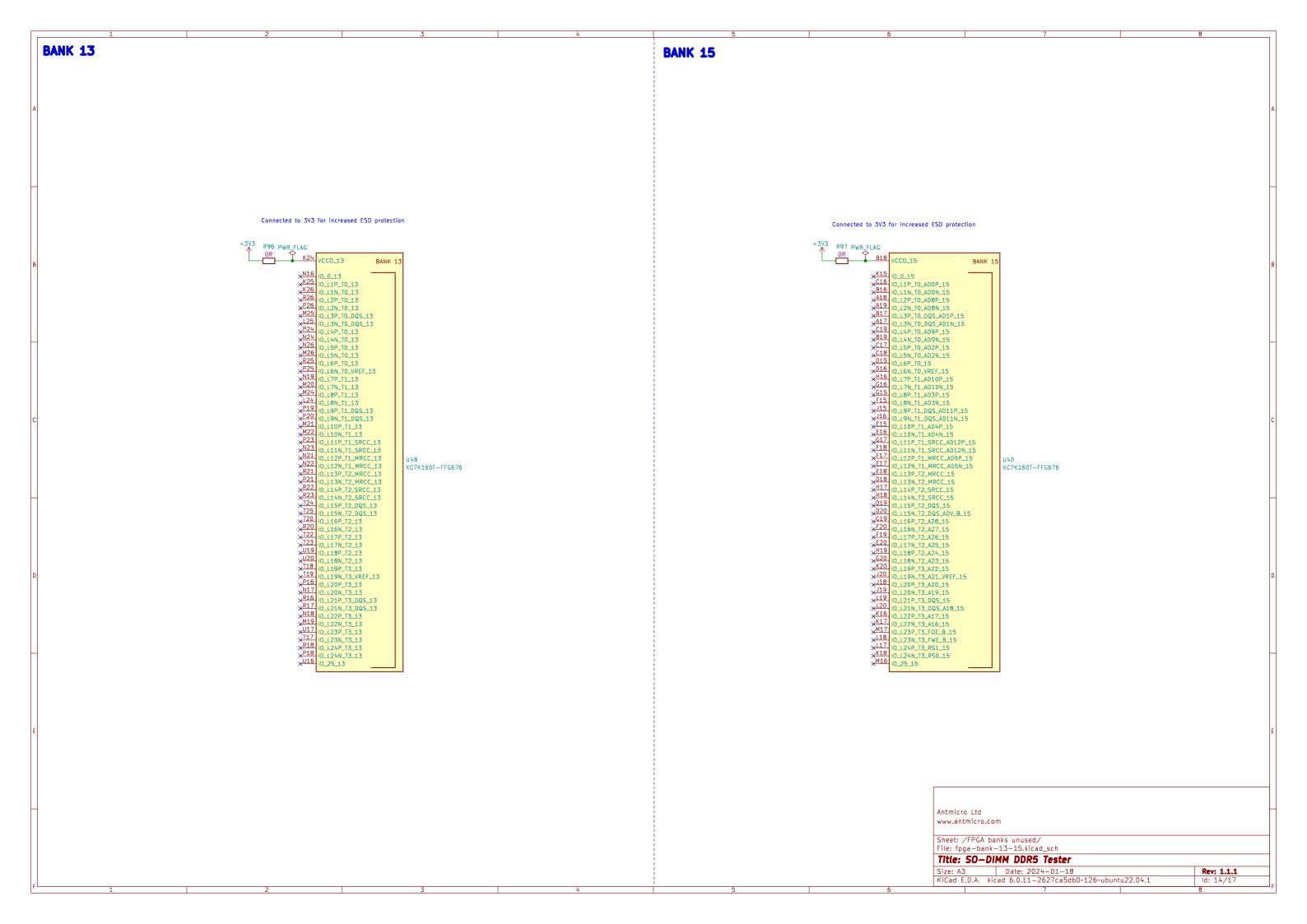
Sheet: /FPGA bank 12/ File: fpga-bank-12.kicad_sch

Title: SO-DIMM DDR5 Tester

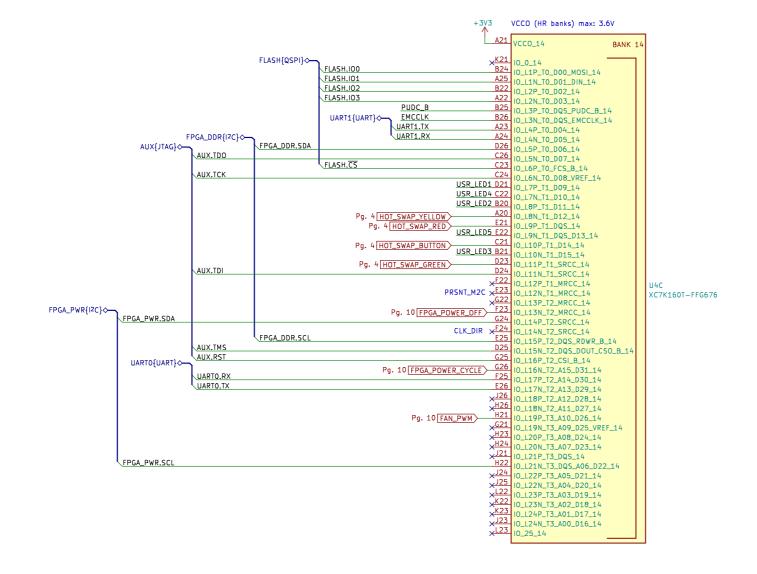
Size: A3 Date: 2024-01-18
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1

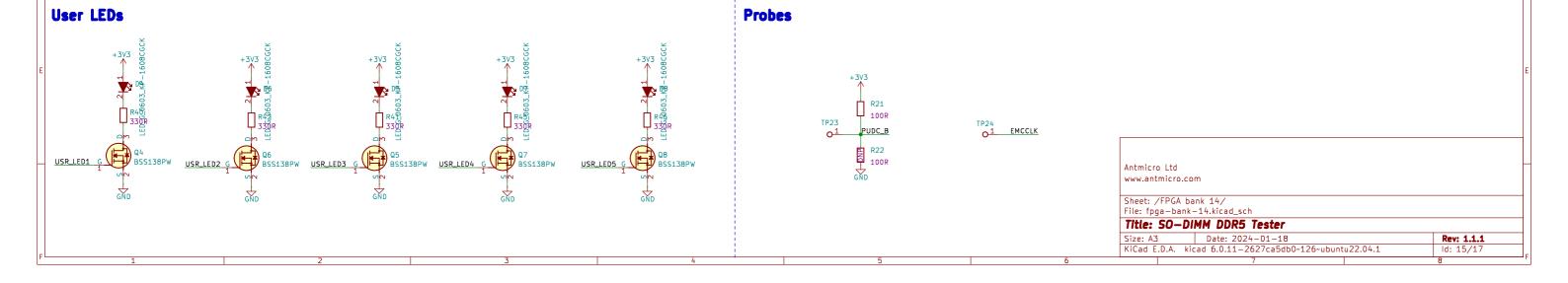
KiCad E.D.A. kicad 6.

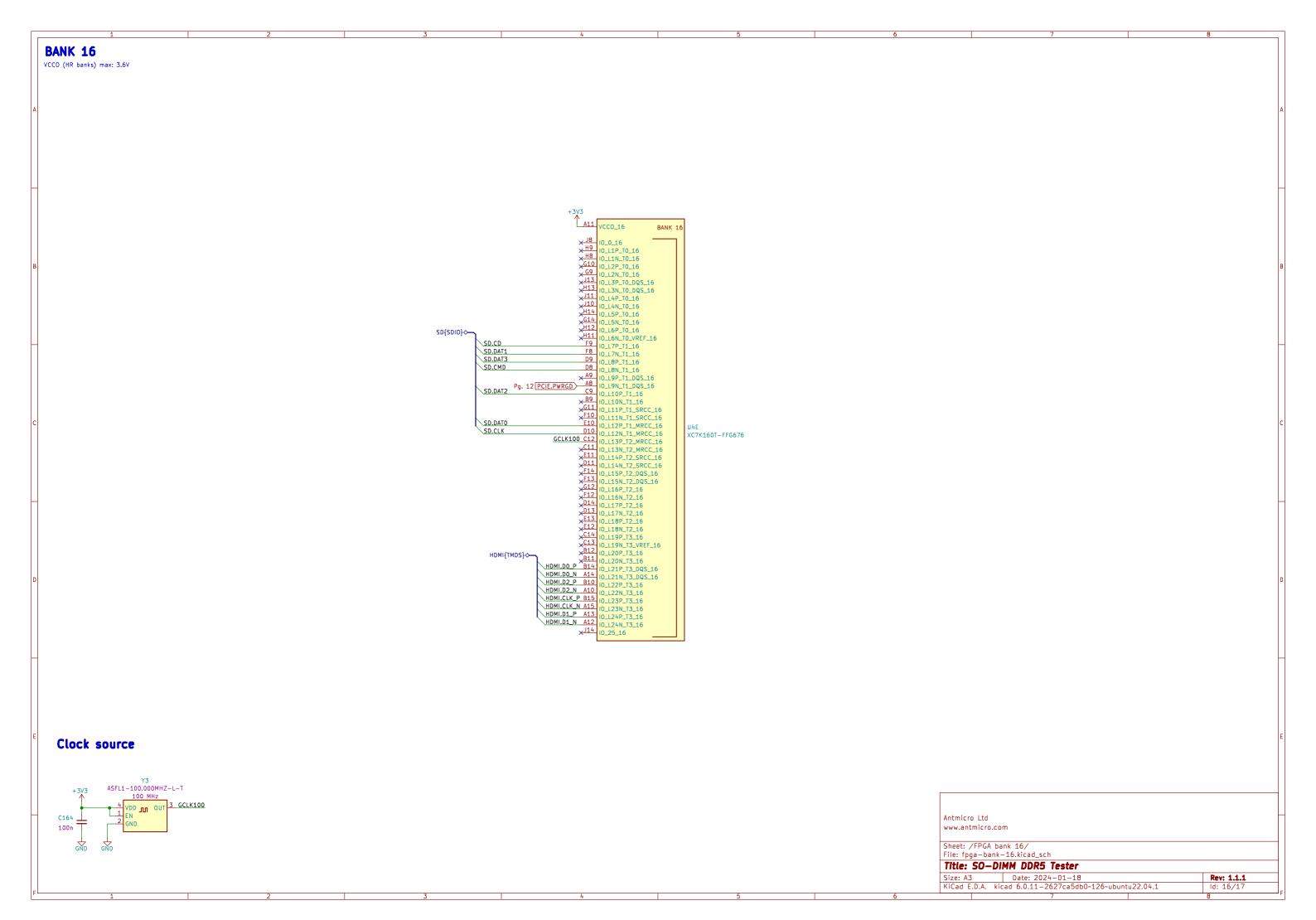
ld: 13/17



BANK 14







12C logic translator

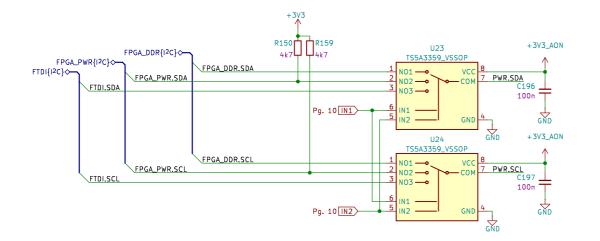
A

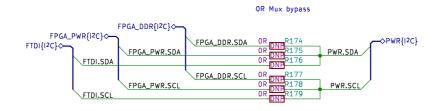
13C logic translator

13C logic translator

13C logic translator

PWR I2C MUX





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Sheet: /|2C/
File: 12c.kicad_sch

Title: SO-DIMM DDR5 Tester

 Size: A3
 Date: 2024-01-18
 Rev: 1.1.1

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 Id: 17/17

