Project:

Objective:

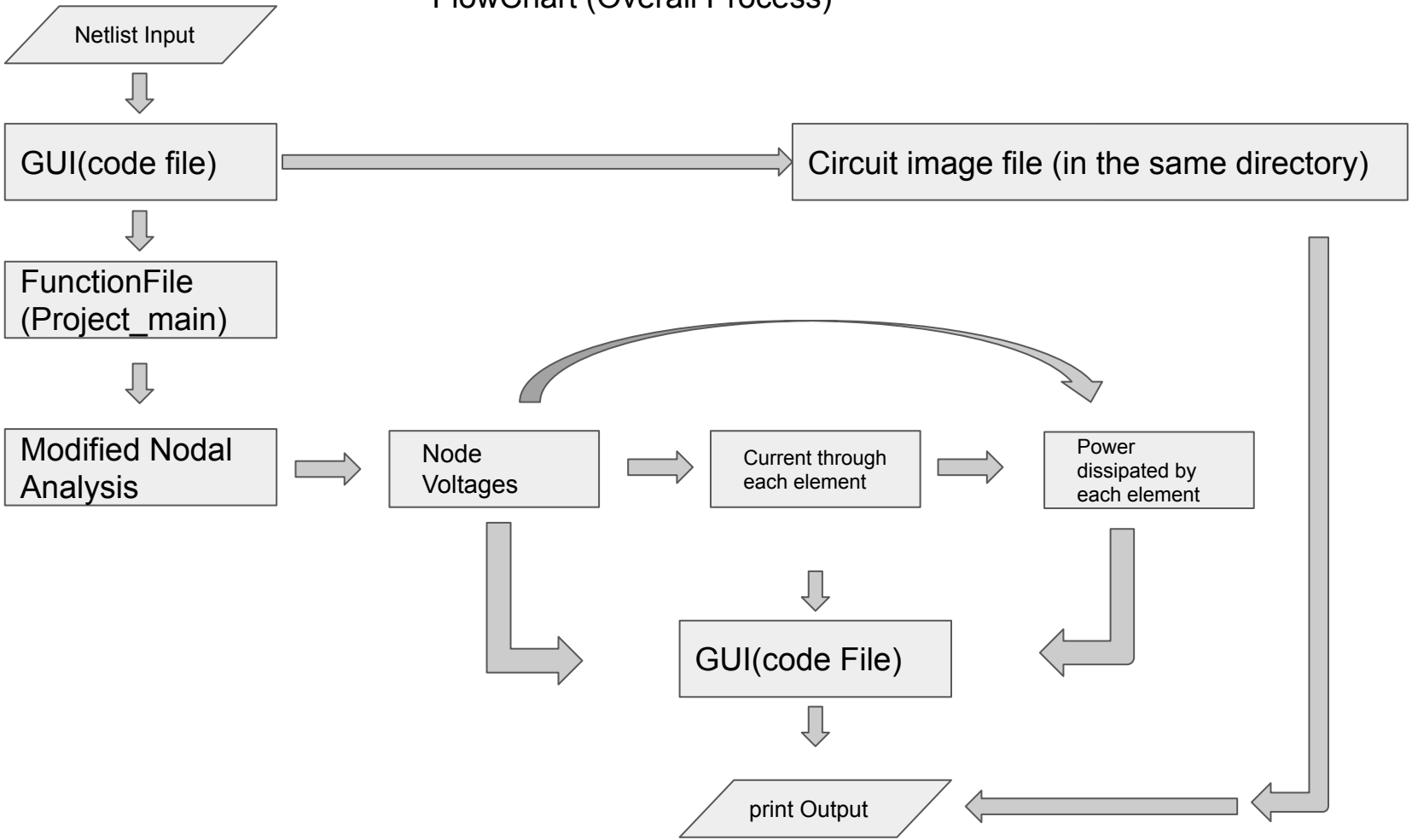
Solving an AC or DC circuit

- Input is the value of each element (R, L, C voltage source etc.)
- Circuit may contain both the independent and dependent current or voltage source.
- Show the schematic of the given circuit
- Also show the current, voltage in each node and branch respectively, power dissipation or supply for each element
- Make a suitable GUI for this project.
- Show result and analysis for at least 10 test cases

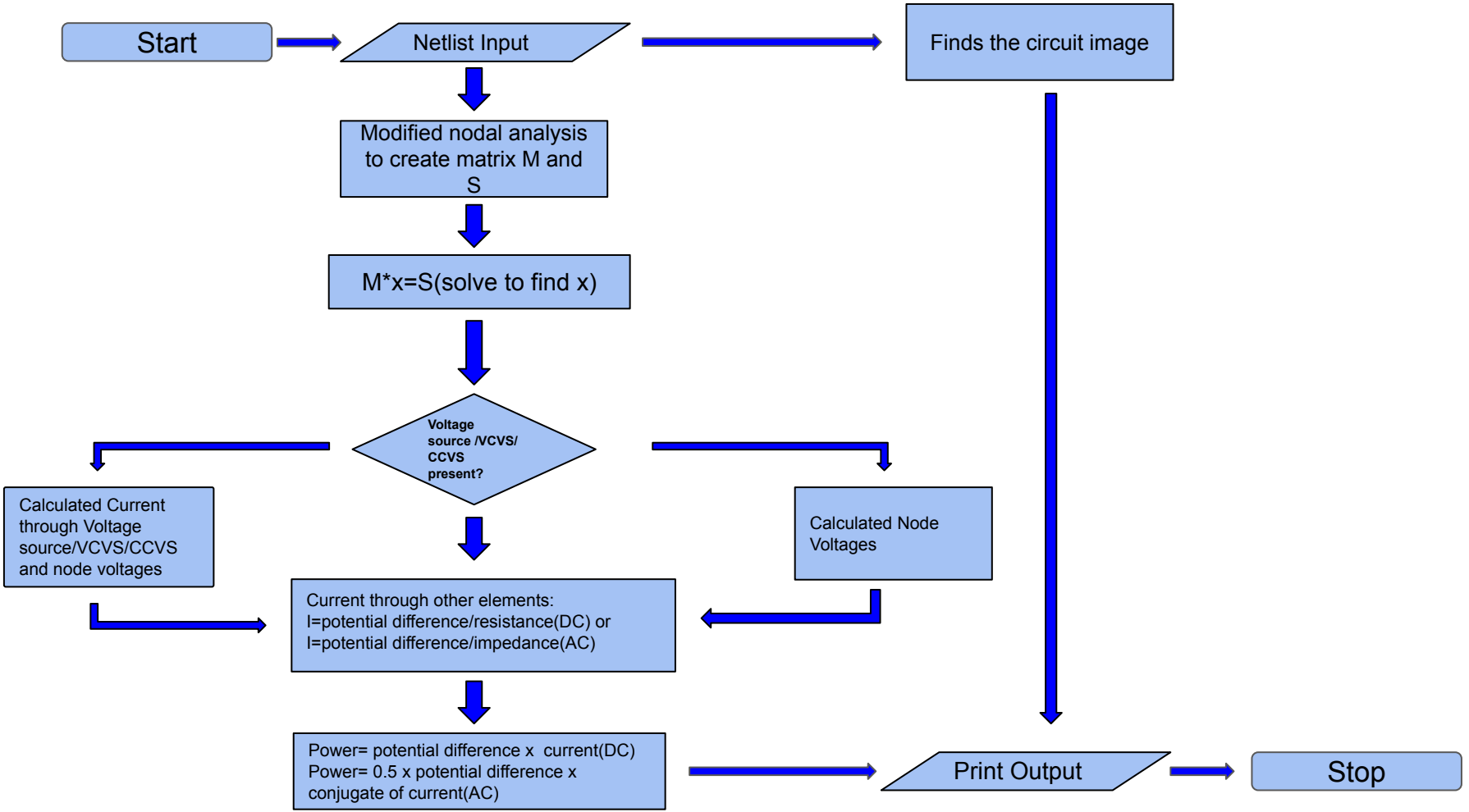
GUI Code:

```
function varargout = proj_gui(varargin)
% PROJ_GUI MATLAB code for proj_gui.fig
%      PROJ_GUI, by itself, creates a new PROJ_GUI or raises the existing
%      singleton*.
%
%      H = PROJ_GUI returns the handle to a new PROJ_GUI or the handle to
%      the existing singleton*.
%
%      PROJ_GUI('CALLBACK',hObject,eventData,handles,...) calls the local
%      function named CALLBACK in PROJ_GUI.M with the given input arguments.
%
%      PROJ_GUI('Property','Value',...) creates a new PROJ_GUI or raises the
%      existing singleton*.  Starting from the left, property value pairs are
%      applied to the GUI before proj_gui_OpeningFcn gets called.  An
%      unrecognized property name or invalid value makes property application
%      stop.  All inputs are passed to proj_gui_OpeningFcn via varargin.
%
%      *See GUI Options on GUIDE's Tools menu.  Choose "GUI allows only one
%      instance to run (singleton)".
%
% See also: GUIDE, GUIDATA, GUIHANDLES

% Edit the above text to modify the response to help proj_gui

% Last Modified by GUIDE v2.5 21-Jul-2021 11:38:33
```

FlowChart (Overall Process)



FlowChart (Algorithm)



Test Case 1: Voltage Sources and resistors

proj_gui

Netlist Input

```
circuit_2.jpg
V1 1 0 DC 15
V2 4 0 DC 10
R1 1 2 5
R2 2 4 10
R3 2 3 6
R4 3 0 4
END
```

SIMULATE

Node Voltages

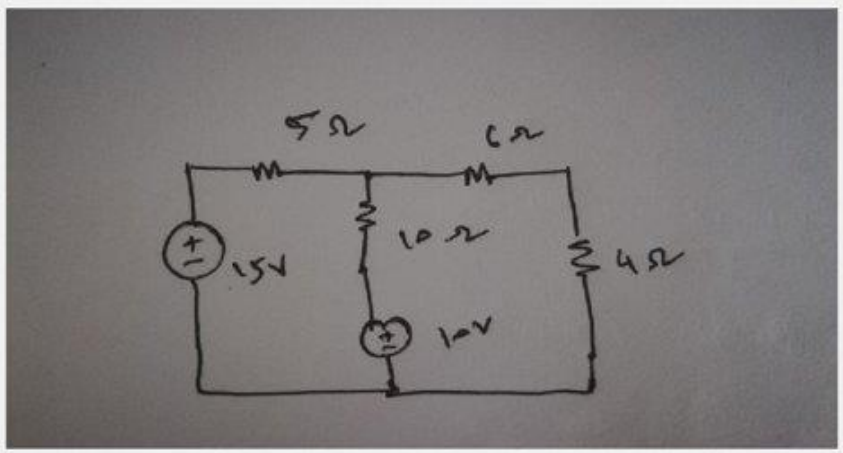
V0= 0V
V1= 15
V2= 10
V3= 4
V4= 10

Branch Currents

Current through,
V1: -1 A
V2: 0 A
R1: 1 A
R2: 0 A
R3: 1 A
R4: 1 A

Power Dissipated

Power Dissipated by,
V1: -1 VA
V2: 0 VA
R1: 5 VA
R2: 0 VA
R3: 6 VA
R4: 4 VA



Test Case 2:(Voltage Source, Current Source and resistor)

proj_gui

Netlist Input

```
circuit_3.jpg
V1 1 0 DC 10
R1 1 2 4
R2 2 0 6
R3 2 3 3
I1 0 3 DC 5
END
```

SIMULATE

Node Voltages

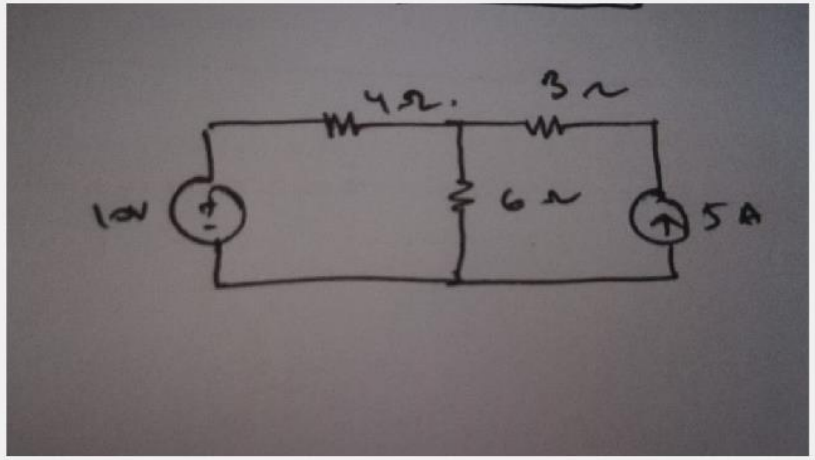
V0= 0V
V1= 10
V2= 18
V3= 33

Branch Currents

Current through,
V1: 2 A
I1: 5 A
R1: -2 A
R2: 3 A
R3: -5 A

Power Dissipated

Power Dissipated by,
V1: 2 VA
I1: -165 VA
R1: 16 VA
R2: 54 VA
R3: 75 VA



Test Case 3: CCCS with sources and resistor(DC)

proj_gui

Netlist Input

```
circuit_4.png
R1 1 0 6
R2 1 2 2
I1 1 2 DC 5
V1 4 0 DC 10
R3 2 3 4
R4 3 0 8
R5 3 4 2
F1 2 0 V1 -3
END
```

SIMULATE

Node Voltages

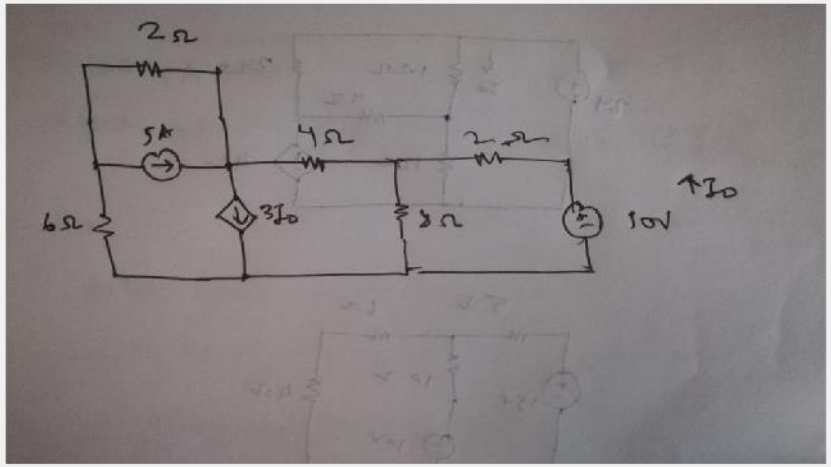
V0= 0V
V1= 15
V2= 30
V3= 14.2857
V4= 10

Branch Currents

Current through,
V1: 2.1429 A
I1: 5 A
F1: -6.4286 A
R1: 2.5 A
R2: -7.5 A
R3: 3.9286 A
R4: 1.7857 A
R5: 2.1429 A

Power Dissipated

Power Dissipated by,
V1: 2.1429 VA
I1: -75 VA
F1: -192.8571 VA
R1: 37.5 VA
R2: 112.5 VA
R3: 61.7347 VA
R4: 25.5102 VA
R5: 9.1837 VA



Test Case 4: Capacitor (DC circuit)

proj_gui

Netlist Input

```
circuit_10.jpg
V1 1 0 DC 15
R1 1 2 2
C1 2 0 0.333
R2 2 3 6
V2 0 3 DC 7.5
END
```

SIMULATE

Node Voltages

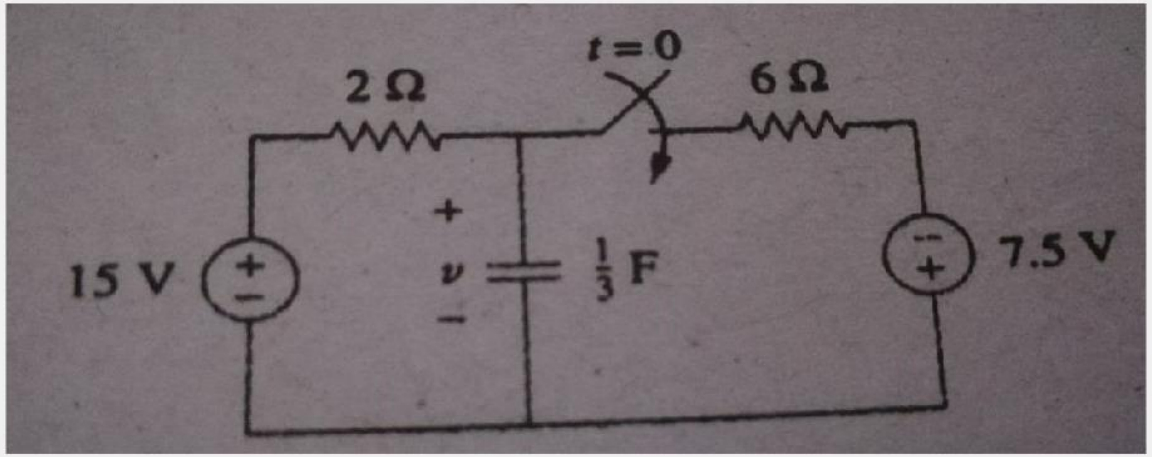
V0= 0V
V1= 15
V2= 9.375
V3= -7.5

Branch Currents

Current through,
V1: -2.8125 A
V2: -2.8125 A
R1: 2.8125 A
R2: 2.8125 A
C1: 0 A

Power Dissipated

Power Dissipated by,
V1: -2.8125 VA
V2: -2.8125 VA
R1: 15.8203 VA
R2: 47.4609 VA
C1: 0 VA



Test Case 5: CCVS(DC)

proj_gui

Netlist Input

```
circuit_1.jpg
V1 1 0 DC 24
V2 1 2 DC 0
R1 3 0 12
R2 2 3 10
R3 3 4 4
R4 1 4 24
H1 4 0 V2 4
END
```

SIMULATE

Node Voltages

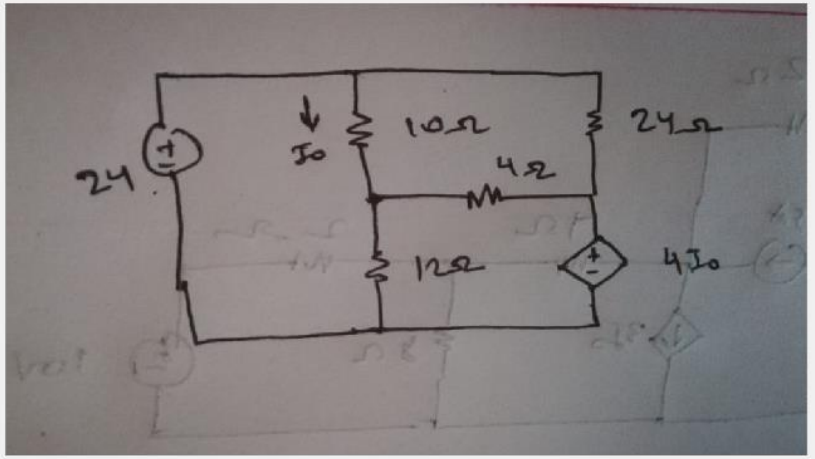
V0= 0V
V1= 24
V2= 24
V3= 9
V4= 6

Branch Currents

Current through,
V1: -2.25 A
V2: 1.5 A
H1: 1.5 A
R1: 0.75 A
R2: 1.5 A
R3: 0.75 A
R4: 0.75 A

Power Dissipated

Power Dissipated by,
V1: -2.25 VA
V2: 1.5 VA
H1: 9 VA
R1: 6.75 VA
R2: 22.5 VA
R3: 2.25 VA
R4: 13.5 VA



Test Case 6: CCCS (AC circuit)

proj_gui

Netlist Input

```
circuit_5.jpg
V1 1 0 AC 8 -0.698 159.2
R1 1 2 4000
V2 2 3 AC 0 0 159.2
C1 3 0 0.000002
L1 2 4 0.05
R2 4 0 2000
F1 0 4 V2 0.5
END
```

SIMULATE

Node Voltages

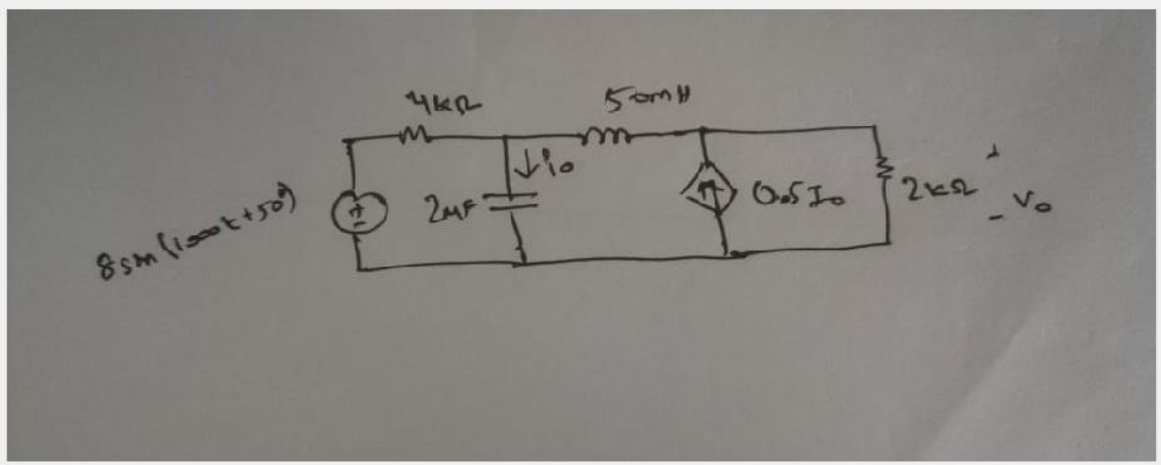
V0= 0V
V1= 6.129-5.1415i
V2= -0.10656-1.6284i
V3= -0.10656-1.6284i
V4= -0.13983-1.5434i

Branch Currents

Current through,
V1: -0.0015589+0.00087829i A
V2: 0.0032576-0.00021318i A
F1: 0.0016288-0.00010659i A
R1: 0.0015589-0.00087829i A
R2: -6.9913e-05-0.00077169i A
C1: 0.0032576-0.00021318i A
L1: -0.0016987-0.0006651i A

Power Dissipated

Power Dissipated by,
V1: -0.0015589+0.00087829i VA
V2: 0.0032576-0.00021318i VA
F1: 3.1619e-05+0.0012644i VA
R1: 0.0064031 VA
R2: 0.0006004-6.7763e-21i VA
C1: 0-0.0026636i VA
L1: 0+8.3224e-05i VA



Test Case 7: VCVS(AC)

proj_gui

Netlist Input

```
circuit_6.jpg
V1 1 0 AC 20 0 477.5
R1 1 2 2000
C1 2 0 0.000001
L1 2 3 2
R2 3 0 1000
R3 2 4 3000
E1 4 0 3 0 2
END
```

SIMULATE

Node Voltages

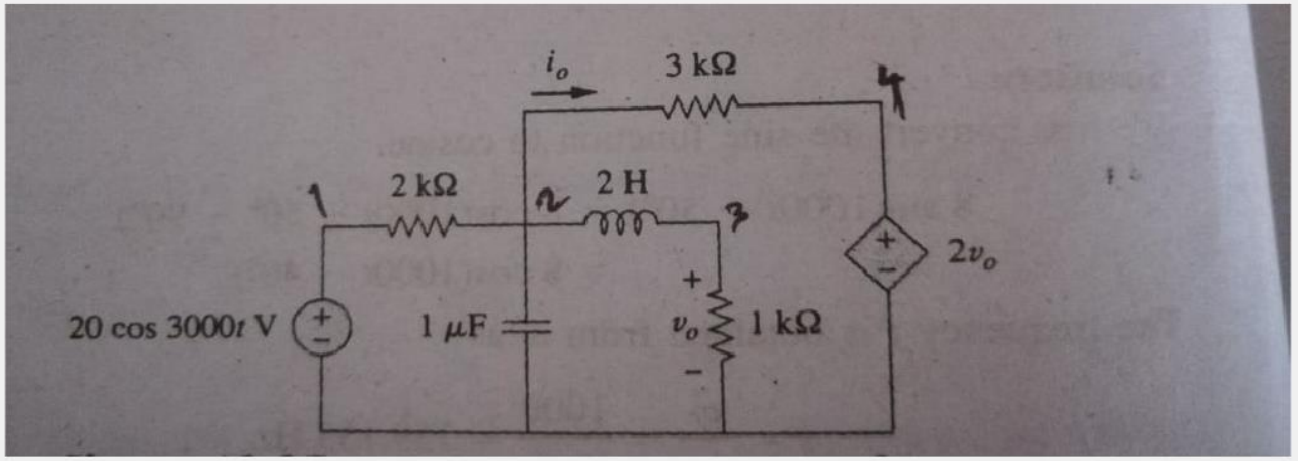
V0= 0V
V1= 20
V2= 0.89711-3.1377i
V3= -0.48454-0.23026i
V4= -0.96909-0.46052i

Branch Currents

Current through,
V1: -0.0095514-0.0015689i A
E1: 0.00062207-0.00089241i A
R1: 0.0095514+0.0015689i A
R2: -0.00048454-0.00023026i A
R3: 0.00062207-0.00089241i A
C1: 0.0094139+0.0026915i A
L1: -0.00048454-0.00023026i A

Power Dissipated

Power Dissipated by,
V1: -0.0095514-0.0015689i VA
E1: -9.5934e-05-0.00057565i VA
R1: 0.093691+1.7347e-18i VA
R2: 0.0001439-6.7763e-21i VA
R3: 0.001775 VA
C1: 0-0.015977i VA
L1: 0+0.00086347i VA



Test Case 8: VCCS(AC circuit)

proj_gui

Netlist Input

```
circuit_7.jpg
I1 0 1 AC 6 0.262 31.8
R1 1 0 20
C1 1 0 0.00005
R2 1 2 40
L1 2 0 0.1
G1 2 1 1 0 0.1
END
```

SIMULATE

Node Voltages

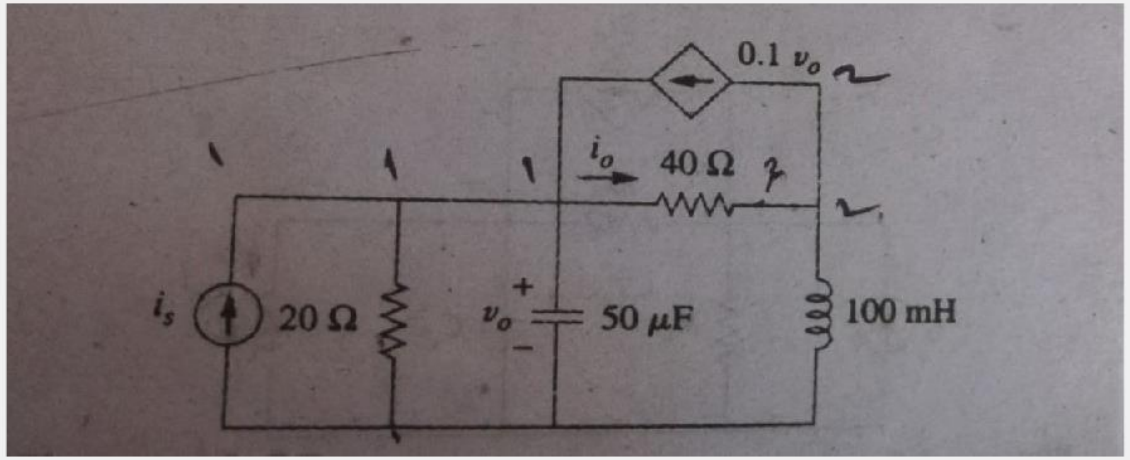
V0= 0V
V1= 2.374669-145.5754i
V2= -176.0109+84.36126i

Branch Currents

Current through,
I1: 5.7952+1.5541i A
G1: 0.622163-38.1408i A
R1: 0.11873-7.2788i A
R2: 4.4596-5.7484i A
C1: 1.4543+0.023724i A
L1: 4.2222+8.8091i A

Power Dissipated

Power Dissipated by,
I1: 106.2368+423.6676i VA
G1: -4440.4707-3330.3515i VA
R1: 529.9458 VA
R2: 1058.6535 VA
C1: 0-105.886i VA
L1: 5.684342e-14+953.3449i VA



Test Case 9: Simple AC circuit without any dependent sources

proj_gui

Netlist Input

```
circuit_8.jpg
V1 1 0 AC 50 0.5235 1.59
C1 1 2 0.5
R1 1 2 10
C2 2 0 0.05
END
```

SIMULATE

Node Voltages

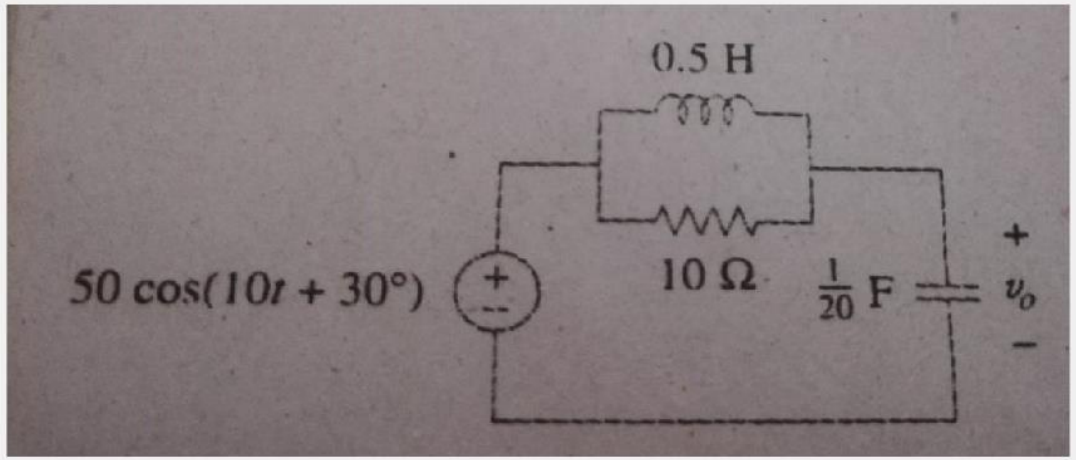
V0= 0V
V1= 43.3037+24.9957i
V2= 39.4097+22.6525i

Branch Currents

Current through,
V1: 11.3152-19.6857i A
R1: 0.38941+0.23432i A
C1: -11.7046+19.4513i A
C2: -11.3152+19.6857i A

Power Dissipated

Power Dissipated by,
V1: 11.3152-19.6857i VA
R1: 1.0327+5.5511e-17i VA
C1: 0-51.5855i VA
C2: 0-516.0619i VA



Test Case 10:Mixed Dependent sources (DC)

proj_gui

Netlist Input

```
circuit_11.jpg
V1 1 0 DC 80
R1 1 2 10
R2 2 3 20
E1 3 0 4 0 4
V2 2 6 DC 0
R3 5 6 40
V3 4 5 DC 96
R4 4 0 80
F1 0 4 V2 2
END
```

SIMULATE

Node Voltages

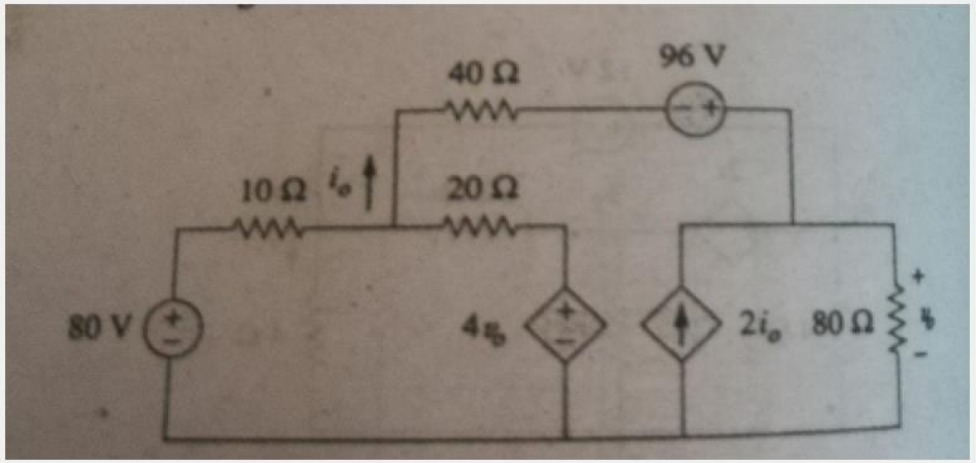
V0= 0V
V1= 80
V2= -1350.4
V3= -4300.8
V4= -1075.2
V5= -1171.2
V6= -1350.4

Branch Currents

Current through,
V1: -143.04 A
V2: -4.48 A
V3: 4.48 A
F1: -8.96 A
E1: 147.52 A
R1: 143.04 A
R2: 147.52 A
R3: 4.48 A
R4: -13.44 A

Power Dissipated

Power Dissipated by,
V1: -143.04 VA
V2: -4.48 VA
V3: 4.48 VA
F1: -9633.792 VA
E1: -634454.016 VA
R1: 204604.416 VA
R2: 435243.008 VA
R3: 802.816 VA
R4: 14450.688 VA



Netlist Syntax used for this program:

- First Line is for the name of the image to be uploaded. Example-”circuit_1.jpg” and the name must be in small letters.(optional)
- Rest of the letters in netlist must be in caps lock.
- “END” will be the end of the netlist input and also has to be in caps lock.
- Numbers must be used to name nodes. Numbers should increase from 1,2,3….n by a difference from 1. No numbers can be skipped.
- Syntax is very similar to the one used for PSPICE.

Discussion:

Here the steady state results were found by simulating the netlist. In DC state the value of inductance was taken as zero (acting as a short circuit) and capacitor as infinity(open circuit). Power dissipation, current through each element and node voltages were calculated and printed in the output. The left hand side of the GUI is for input of the netlist while the right hand side is for output.

Future Prospects/Improvements:

Only steady state results were found. For DC circuit analysis transient expressions can also be found. Plots can also be made for the transient analysis and AC analysis by using matlab canvas.

The connection of nodes can be visualized using breadth first search algorithm and then the graph plotted. Schematic can be generated using code from the netlist input and then printed in the canvas.