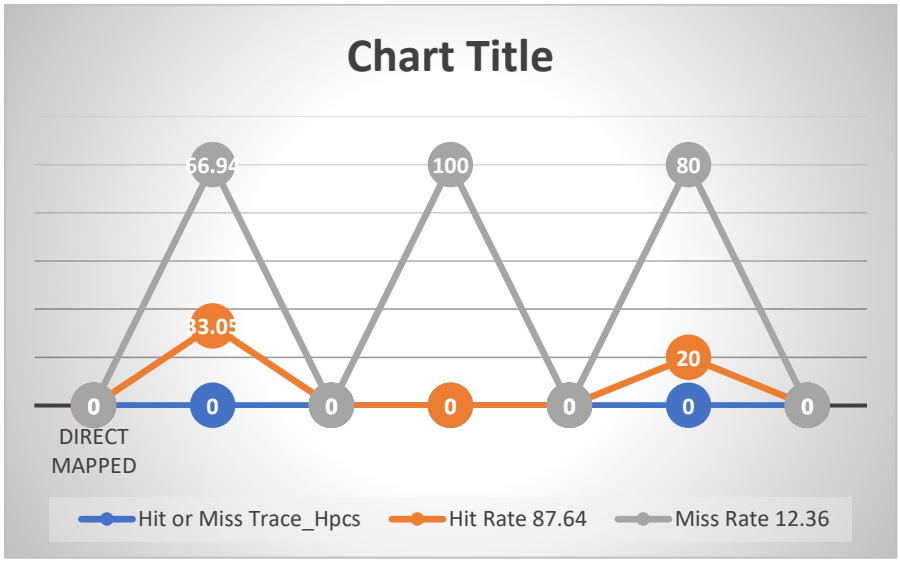
CS5375 Programming Project-1
Computer Systems Organization and Architecture

In this programming project, we were asked to develop a cache simulator and perform tests to observe how cache behaves. As said, a 32-bit machine was assumed, and memory address fed from trace files were 32-bit byte addresses.
I installed Global Protect vpn to connect to the Texas Tech vpn and connected to it with the help of TTU credentials. I used MobaXterm platform for code execution.

Part 1. Direct-mapped cache

A sample code was provided and in part 1 of this programming project, we were asked to compile the *cachesim.c* to generate the single-level direct-mapped cache simulator. After logging in with the credentials, I cloned to GitHub to use the CS5375 repository. Then changed the directory to CS5375 and then created the *cachesim.c* and *cachesim.h* files. Later with the help of source code I compiled it and executed it. The graphical representation is as follows:

Direct Mapped				
Hit or Miss	Trace_Hpcs	Trace_Stream	Trace_Stream_10	Trace_Stream_20
Hit Rate	87.64	33.05	0	20
Miss Rate	12.36	66.94	100	80

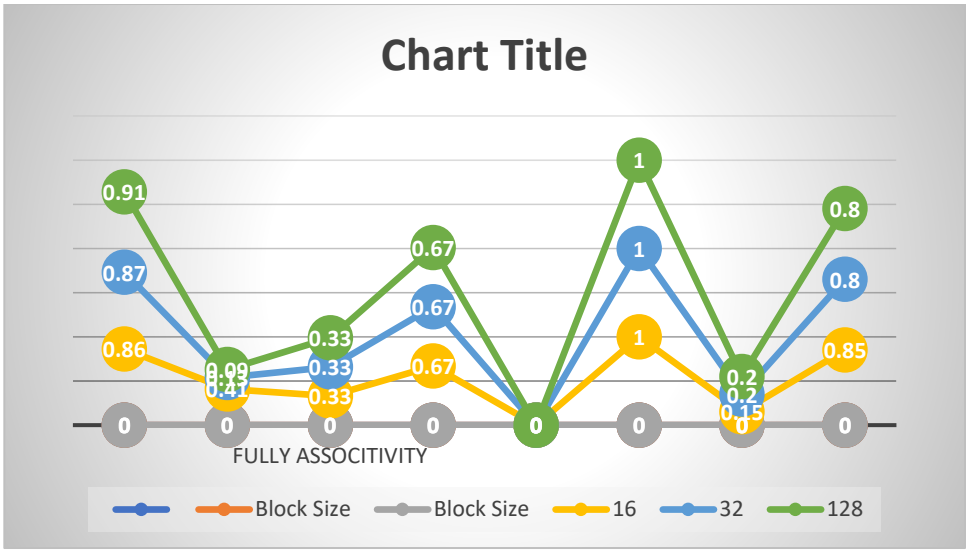


Part –2 Fully associative and n-way set associative cache

In this part, we were asked to further develop the simulator to simulate fully associative cache and n-way set associative cache. Further simulation was asked to configure with different settings like different cache capacity and different cache line size. The configuration was done for 32 bytes and 64 bytes.
The source code in *cachesim.c* was modified in order to execute it for fully associative cache and n-way associative set cache. Also the difference between direct mapped and associativity by developing the simulator for the fully associative and other n-way associative was shown. Here we developed 2-way, 4-way and 8-way associativity and shown the difference. The execution results for 128 block size are as follows:

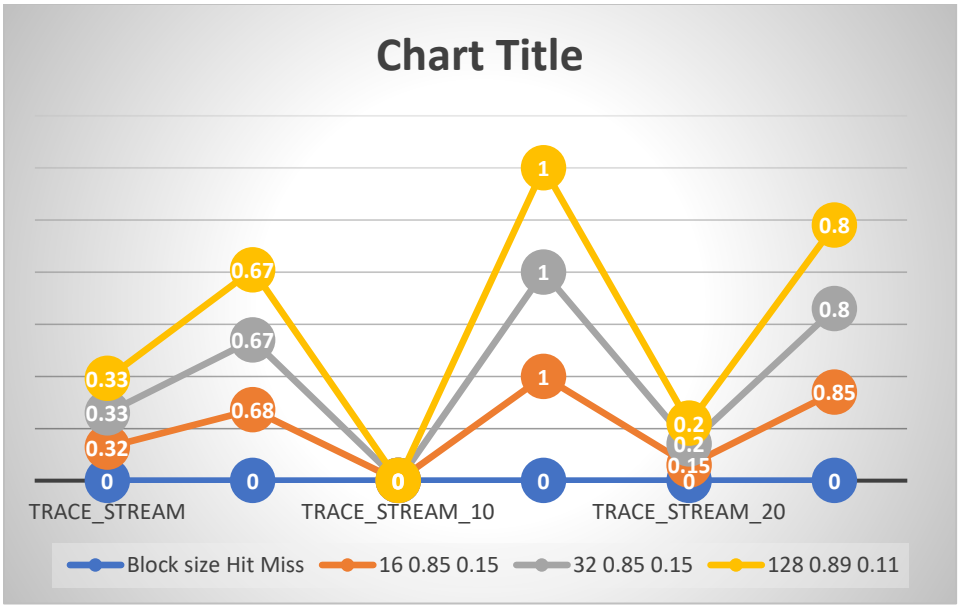
Fully Associtivity Cache:

					Fully Associtivity				
Block Size		Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
		Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16		0.86	0.41	0.33	0.67	0	1	0.15	0.85
32		0.87	0.13	0.33	0.67	0	1	0.2	0.8
128		0.91	0.09	0.33	0.67	0	1	0.2	0.8



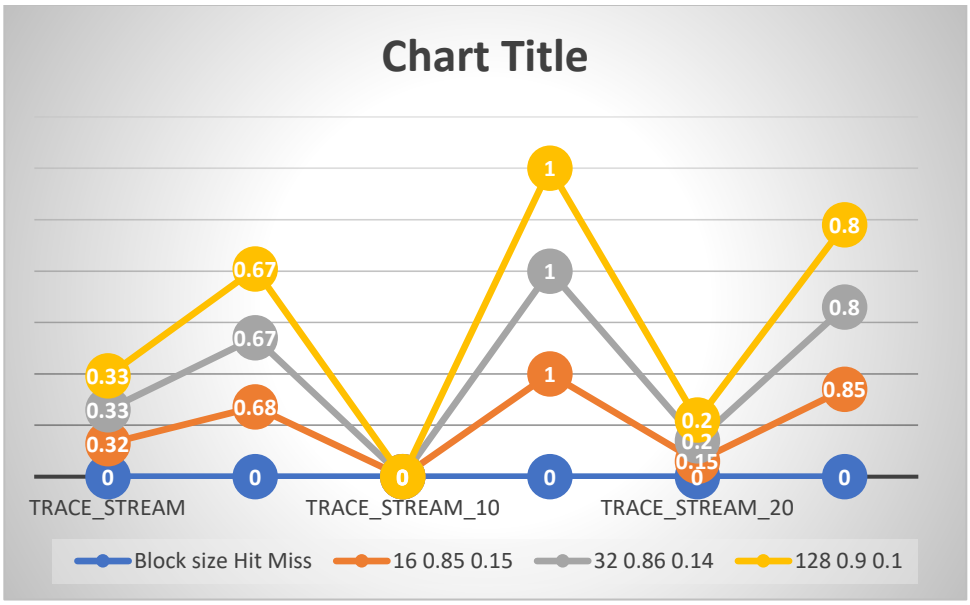
2 Way Associtivity Set Cache:

2 way set Associtivity								
Block size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16	0.85	0.15	0.32	0.68	0	1	0.15	0.85
32	0.85	0.15	0.33	0.67	0	1	0.2	0.8
128	0.89	0.11	0.33	0.67	0	1	0.2	0.8



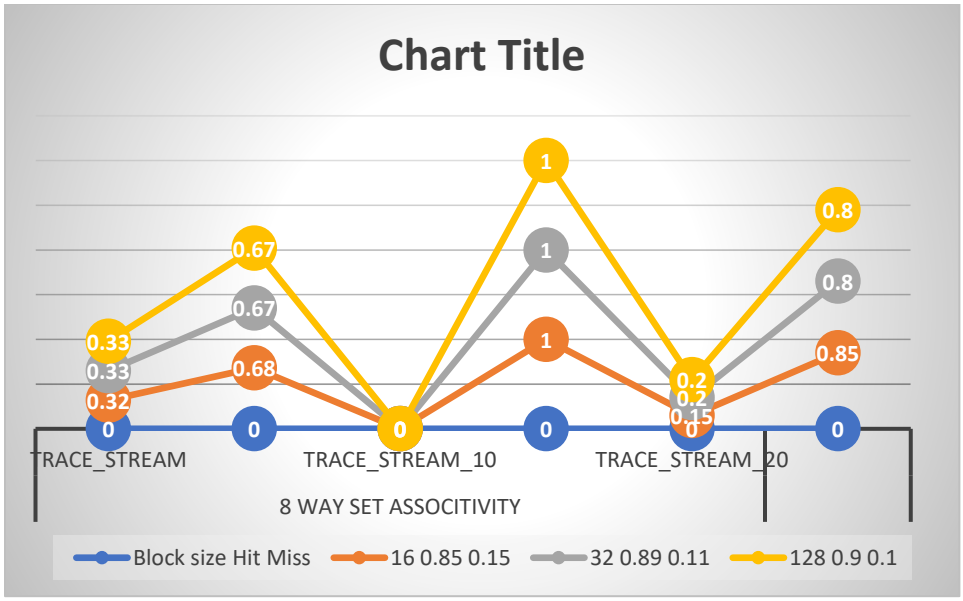
4 Way Associtivity Set Cache:

4 Way Set Associtivity								
Block size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16	0.85	0.15	0.32	0.68	0	1	0.15	0.85
32	0.86	0.14	0.33	0.67	0	1	0.2	0.8
128	0.9	0.1	0.33	0.67	0	1	0.2	0.8



8 Way Associtivity Set Cache:

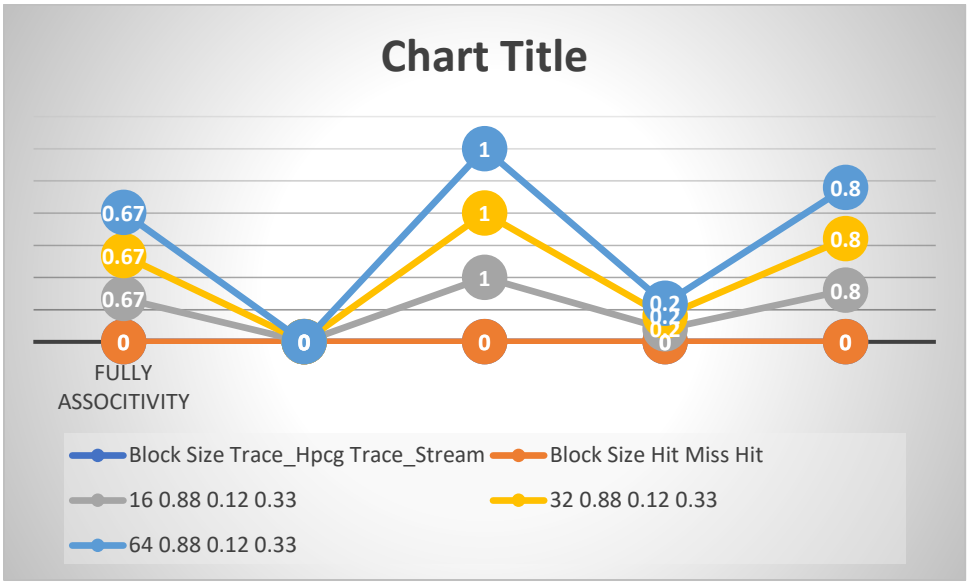
				8 Way Set Associtivity					
	Block size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
		Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
	16	0.85	0.15	0.32	0.68	0	1	0.15	0.85
	32	0.89	0.11	0.33	0.67	0	1	0.2	0.8
	128	0.9	0.1	0.33	0.67	0	1	0.2	0.8



The execution results for 64 KB block size are as follows:

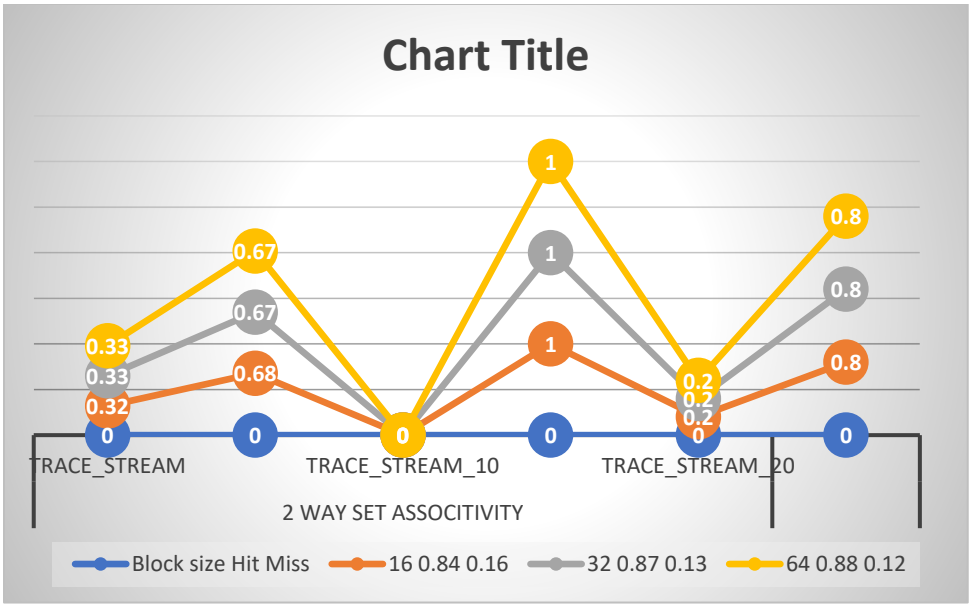
Fully Associtivity Cache:

Fully Associtivity								
Block Size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16	0.88	0.12	0.33	0.67	0	1	0.2	0.8
32	0.88	0.12	0.33	0.67	0	1	0.2	0.8
64	0.88	0.12	0.33	0.67	0	1	0.2	0.8



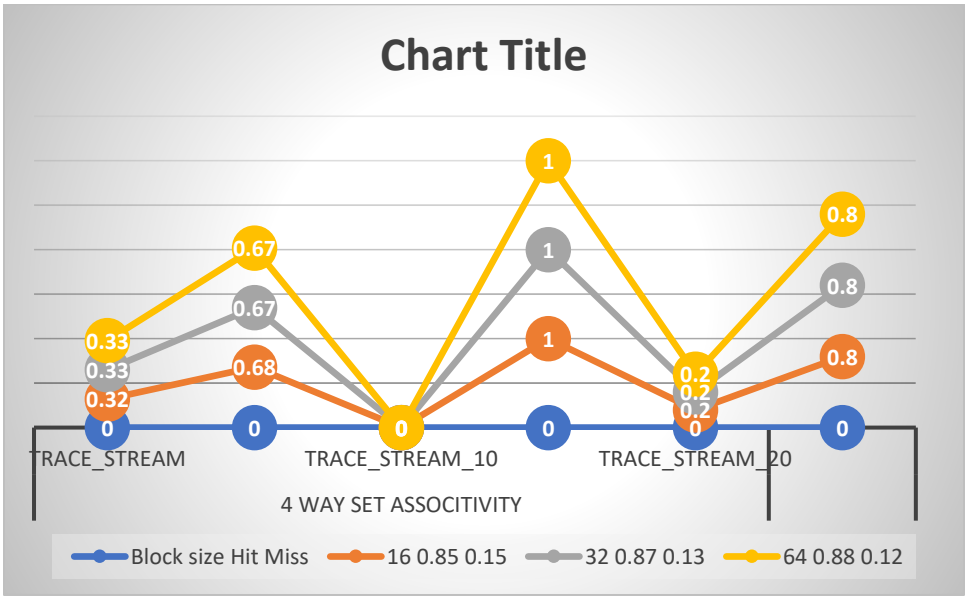
2 Way Associtivity Set Cache:

2 way set Associtivity								
Block size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16	0.84	0.16	0.32	0.68	0	1	0.2	0.8
32	0.87	0.13	0.33	0.67	0	1	0.2	0.8
64	0.88	0.12	0.33	0.67	0	1	0.2	0.8



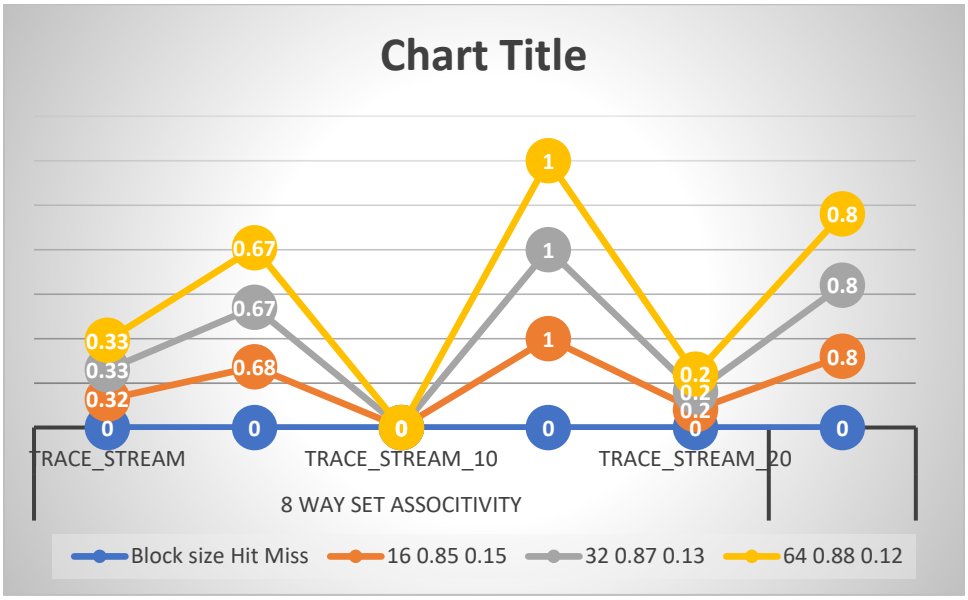
4 Way Associtivity Set Cache:

				4 Way Set Associtivity				
Block size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16	0.85	0.15	0.32	0.68	0	1	0.2	0.8
32	0.87	0.13	0.33	0.67	0	1	0.2	0.8
64	0.88	0.12	0.33	0.67	0	1	0.2	0.8



8 Way Associtivity Set Cache:

	8 Way Set Associtivity							
Block size	Trace_Hpcg		Trace_Stream		Trace_Stream_10		Trace_Stream_20	
	Hit	Miss	Hit	Miss	Hit	Miss	Hit	Miss
16	0.85	0.15	0.32	0.68	0	1	0.2	0.8
32	0.87	0.13	0.33	0.67	0	1	0.2	0.8
64	0.88	0.12	0.33	0.67	0	1	0.2	0.8



Part 3. Two-level cache simulation:

Here in this part, 2 level cache was developed and executed and results are shown below. Here levels are represented in L1 and L2 form. Here L1 is a 2-way 64KB cache with 64B block size and L2 is an 8- way where 1MB cache is taken with 64B block size as mentioned in the requirements.

	Two level cache simulation				
	Hit or miss	Trace_hpcg	Trace_Stream	Trace_Stream_10	Trace_Stream_20
L1	Hit rate	0.64	0.0011	0	0.05
	Miss rate	0.35	0.99	1	0.95
L2	Hit rate	0.65	0.33	0	0.16
	Miss rate	0.34	0.66	1	0.84

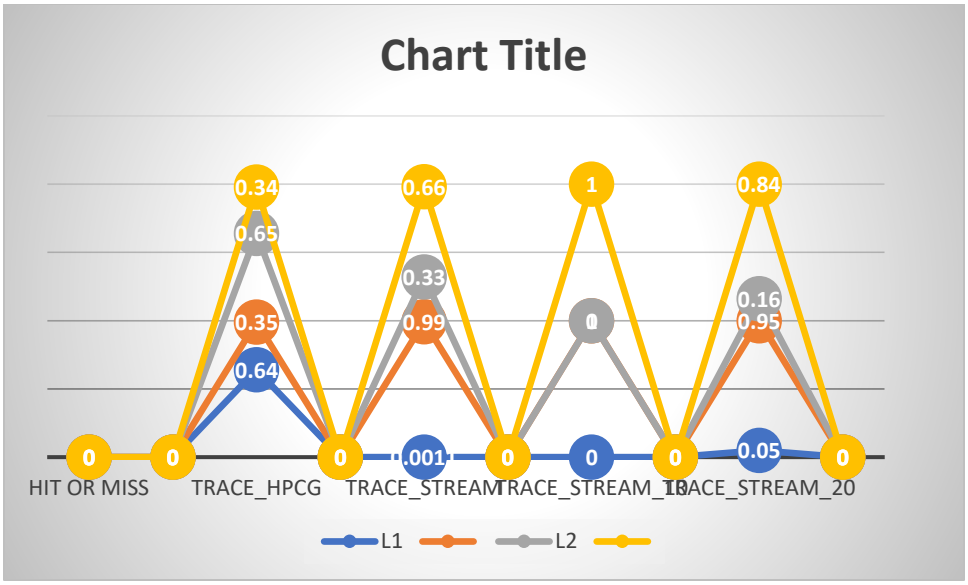


Chart Title
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HIT OR MISS
TRACE_HPCG
TRACE_STREAM
TRACE_STREAM_10
TRACE_STREAM_20
L1
L2