Himani Chaudhary

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EDUCATION

Indian Institute of Information Technology Guwahati Expected Graduation, 2026
B. TECH in Electronics and Communication Engineering
12th Boards (D.A.V. Public School Gandhinagar, Ranchi) Percentage: 91.8%
10th Boards (D.A.V. Public School Gandhinagar, Ranchi) Percentage: 93.6%

SKILLS

Chip Design / VLSI: Verilog HDL, System Verilog, Digital Electronics**,** RTL Design, Testbench Development, Timing Concepts**,** FPGA Basics, Synthesis Flow, Waveform Analysis (GTKWAVE)
Embedded & Hardware: ARM Cortex-M, PSoC Creator, Keil µVision, Timers, GPIO, UART, DMA, VDAC
Software: C, DSA, MATLAB, Python, Java**,** HTML, CSS, DBMS, OS, OOPS
Tools: MATLAB, Visual Studio, IntelliJ, Eclipse, Git, GitHub, Bootstrap, Simulink

PROFILE SUMMARY

Aspiring RTL/Verification Engineer with strong foundations in Digital Electronics, HDL design, and embedded systems. Skilled in digital module design, timing/sequence behavior, FSMs, pipelining, and CORDIC-based DSP, with experience in interrupts, register-level programming, and strong ECE problem-solving fundamentals.

PROJECTS

16-bit Round Multiplier – RTL Digital Design **March2025-May2025**
Tools: Verilog HDL, Vivado, ModelSim/iverilog, Basys-3 (Artix-7 FPGA), GTKWave

- Designed a **16-bit Braun multiplier** using hierarchical 2/4/8-bit array multipliers for structured partial products and carry-save addition.
- Synthesized and validated on **Artix-7 FPGA**, analysing timing (18.524 ns), power (450 mW), and LUT/FF usage.
- Built a **comprehensive Verilog testbench** and verified accurate 32-bit outputs simulation and waveform analysis.

Multi-Waveform Signal Generator using PSoC with CORDIC Algorithm **March2025-April2025**
Tools: PSoC Creator, Embedded C, CORDIC Algorithm, VDAC, DMA Controller, Fixed-Point Arithmetic

- Implemented CORDIC-based sine generation in Q1.15 fixed-point format for efficient hardware-friendly DSP.
- Designed LUT-based square, triangle, and DC waveforms with optimized digital logic.
- Configured DMA-to-VDAC streaming for continuous waveform output with minimal CPU usage.

Real-Time Digital Clock System using ARM Cortex-M **Jan2025 - Feb 2025**
Tools: Keil µVision, Embedded C, ARM Cortex-M, Timer/Counter Peripherals, GPIO, Seven-Segment Display

- Built a **timer-interrupt-driven digital clock** with millisecond-level accuracy.
- Interfaced **7-segment/LCD displays** using multiplexing and efficient GPIO control.
- Implemented **debounced user input** and time-setting logic using clean sequential design principles.

All-Optical 2×1 Multiplexer using Photonic Crystal (FDTD-Based Simulation) **Oct2025-Nov2025**
Tools: Lumerical FDTD, BandSOLVE (PWE), MATLAB (analysis)

- Designed a 2×1 photonic-crystal multiplexer (12×12 lattice) using line/point defects for optical switching at 1550 nm. Performed TM-mode bandgap analysis (1462–2514 nm) and validated all 8 input–select cases via field profiles and output power.
- Achieved 47.88 µm² area and 4.83 dB contrast ratio, confirming efficient optical routing and confinement.

CERTIFICATIONS

VLSI Test Workshop, IIIT Guwahati & IEEE Computer Society TTTC India
ICPC Algo Queen - The Girls Programming Cup 2025
Web development internship certificate, Dev Club, IIT Delhi, Unstop