

README FILE (Phase 2)

Group-6

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Git-Hub link to the project: <https://github.com/Silent-faith/RISC-V-Simulator>

Welcome to the phase 2 of the RISC-V simulator. In this phase, we have tried to incorporate pipelined execution (with or without data forwarding). We have built on our initial Phase 1 code.

You can either use the Non-GUI version of the code (`phase2_final_non_gui.py`) or use the GUI version (`phase2gui.py`)

INPUT TO CODE: A file with the machine code (here it is `code.mc`). This file has the machine code divided into two segments: data segment and text segment.

0x0	0x10000197	Text segment (instructions)
0x4	0x0001A183	
0x8	0x10000217	
0xc	0xFFC22203	
0x10000008	0x17020010	Data segment
0x10000004	0x83A10100	
0x10000000	0x97010010	

OUTPUT OF CODE:

In console: Displays the **5 step execution** of each instruction, by displaying the **fields** (*opcode, rs, rd, func3, func7, imm*) of each instruction when applicable. Also, displays the **register values** and **memory state** before and after execution. In order to check successful completion of the code, the user has to check necessary memory and register states at the end of execution.

In GUI simulator window: The register states can also be checked using the display GUI window. (To directly go to the process to use this simulator, jump to **HOW TO USE** part of this document)

After execution, all the data memory is written in the `memory.mc` file before the program terminates. (additional files `console.txt` and `register.mc` are used to facilitate the GUI operation)

INSTRUCTIONS SUPPORTED BY OUR CODE:

- R format - add, and, or, sll, slt, sra, srl, sub, xor, mul, div, rem
- I format - addi, andi, ori, lb, lh, lw, jalr
- S format - sb, sw, sh
- SB format - beq, bne, bge, blt
- U format - auipc, lui
- UJ format – jal
- This code ***DOES NOT*** support any pseudo instruction.

HOW TO RUN NON-GUI VERSION?

Step 1) Run `phase2_final_non_gui.py` on console.

Step 2) The user is given a choice to determine the method of the execution of machine code:
1 for non pipelined execution
2 for pipelined execution without data forwarding
3 for pipelined execution with data forwarding

Step 3) After user enters 1, 2 or 3, the execution begins and output is shown on console.

HOW TO USE THE SIMULATOR?

The Simulator has an in-built GUI feature to make the code more user-friendly. (Please install `bitstring` module and `PyQt5` module in Python before running this code) The following steps will show how to use the simulator.

Step 1) Run `phase2gui.py` on the console. A GUI window will pop-up automatically.

Step 2) Paste the machine code from `code.mc` into the 'Machine Code' text field.

Step 3) Select appropriate checkbox for **Pipelined, Non-pipelined, Pipelined with Data Forwarding**.

Click on these Checkboxes

The screenshot shows the RISC-V Simulator interface. At the top, there are three checkboxes: ☐ Pipelined, ☐ Non-pipelined, and ☒ Pipelined with Data Forwarding. Below these are buttons for Run, Reset, and Exit. The Machine Code input field is highlighted with a dashed blue border and contains the text: "Paste the Machine Code here (in proper format)". The Console output shows the execution of the program, including cycle numbers, instructions, and register values. The Register and Memory tables are also visible on the right side.

Register	Memory
	HexaDecimal Decimal
x0	0x00000000 0
x1	0x00000000 0
x2	0x00000003 3
x3	0x00000005 5
x4	0x00000005 5
x5	0x00000000 0
x6	0x00000000 0
x7	0x00000000 0
x8	0x00000000 0
x9	0x00000000 0
x10	0x00000000 0
x11	0x00000000 0
x12	0x00000000 0
x13	0x00000000 0
x14	0x00000000 0
x15	0x00000000 0
x16	0x00000000 0
x17	0x00000000 0

Step 4) **Double click** on RUN button to start execution.

Step 5) The Console text field will show the console output. The tables of Register and Memory will also show required values.

Register values

The screenshot shows the RISC-V Simulator interface after execution. The Console output shows the execution of the program, including cycle numbers, instructions, and register values. The Register and Memory tables are also visible on the right side. A red dashed box highlights the Register values in the table.

Register	Memory
	HexaDecimal Decimal
x0	0x00000000 0
x1	0x00000000 0
x2	0x00000003 3
x3	0x00000005 5
x4	0x00000005 5
x5	0x00000000 0
x6	0x00000000 0
x7	0x00000000 0
x8	0x00000000 0
x9	0x00000000 0
x10	0x00000000 0
x11	0x00000000 0
x12	0x00000000 0
x13	0x00000000 0
x14	0x00000000 0
x15	0x00000000 0
x16	0x00000000 0
x17	0x00000000 0