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ESC201
Total Marks: 8

Major Quiz-II

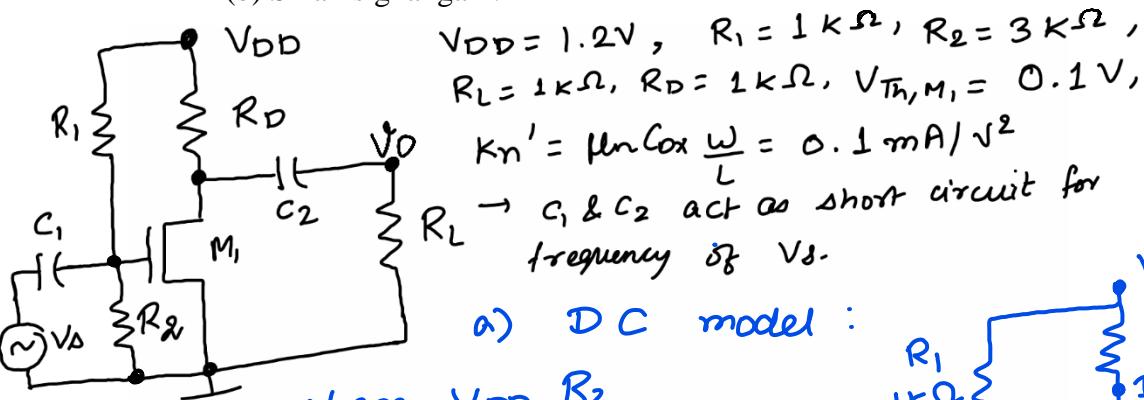
08/04/2025
Time: 30 minutes

Instructions

- Please write your name and roll number first.
- Read the question carefully and answer it in the question paper itself.

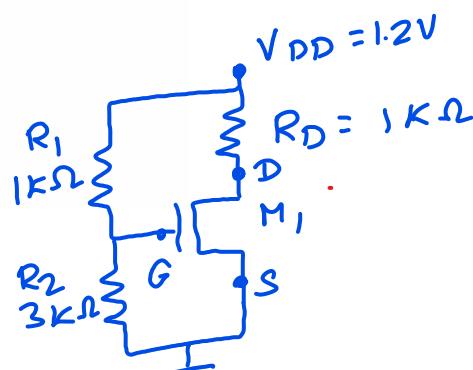
1) For the given circuit, find out:

- (a) The DC operating point (I_{DSQ} , V_{DSQ}) for the MOSFET (M_1). (1 mark)
- (b) Small signal gain. (2 marks)



a) DC model :

$$V_{GSQ} = V_{DD} \frac{R_2}{R_1 + R_2} = 1.2 \times \frac{3}{4} = 0.9V$$



Assuming M_1 is in saturation,

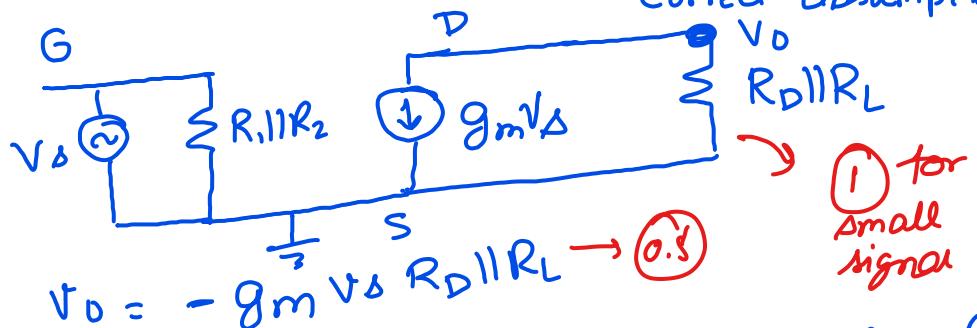
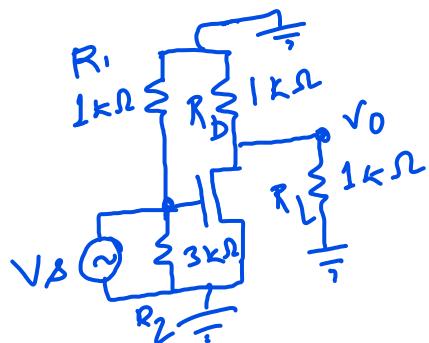
$$I_{DSQ} = \frac{1}{2} k_n' [V_{GSQ} - V_{Th}]^2 = 0.5 \times 0.1 \text{ mA/V}^2 \times (0.8)^2 \text{ V}^2$$

$$I_{DSQ} = 0.032 \text{ mA} \quad \text{circled 0.5}$$

$$V_{PSQ} = V_{DD} - R_D \cdot I_{DSQ} = 1.2 - 0.032 \times 1 = 1.168V \quad \text{circled 0.5}$$

Revisiting the assumption $\rightarrow V_{DSQ} > V_{GSQ} - V_{Th,M_1}$ (hence, saturation)

b) AC model :



$$g_m = k_n' [V_{GSQ} - V_{Th}] = 0.1 \text{ mA/V}^2 \cdot 0.8V = 0.08 \text{ mS}$$

$$\Rightarrow \frac{V_O}{V_S} = A_V = -g_m R_D || R_L = -0.08 \times 0.5 = -0.04 \quad \text{circled 0.5}$$

Very Bad amplifier: Should have used high R_D & R_L . 0.5

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- 2) Design a three-input Majority logic gate which outputs '1' if a majority (two or more) of its three inputs are '1', and outputs '0' otherwise.

(a) Write the truth table. (0.5 mark)

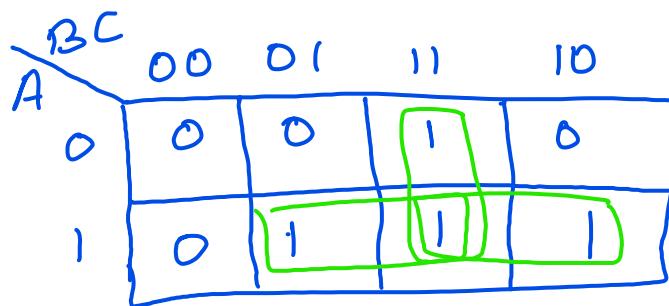
(b) Find the optimized Boolean expression for the output of the Majority logic gate using Karnaugh-map. (1.5 marks)

(c) Show the implementation of this Boolean expression using **complementary CMOS Design** (using both n-MOSFETs and p-MOSFETs). (3 marks)

Q.5

Truth Table			Out
A	B	C	
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

∴ No. of "1" entries = No. of "0" entries,
one may use either POS or SOP.



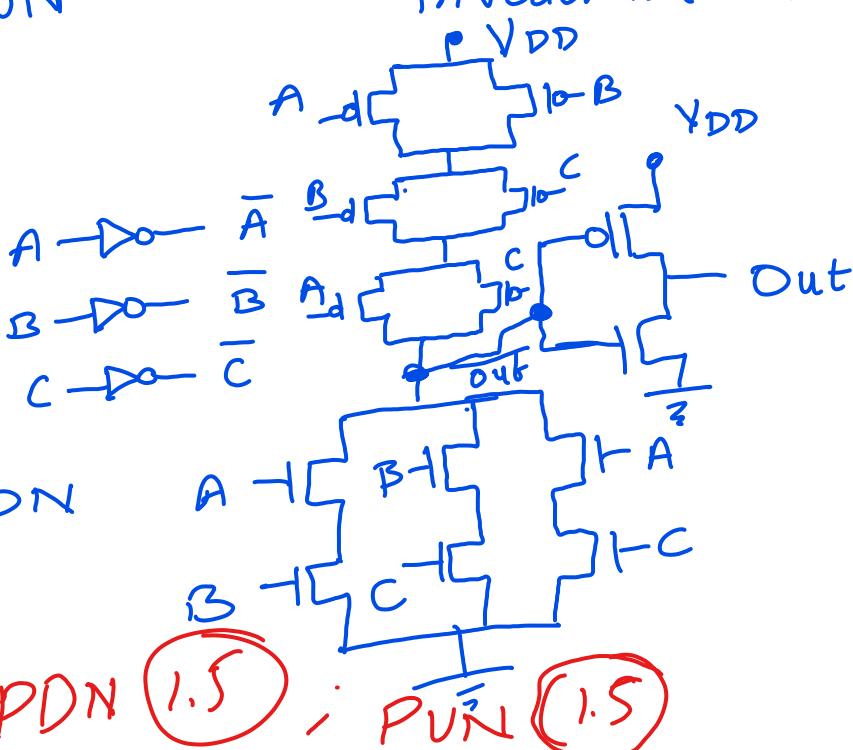
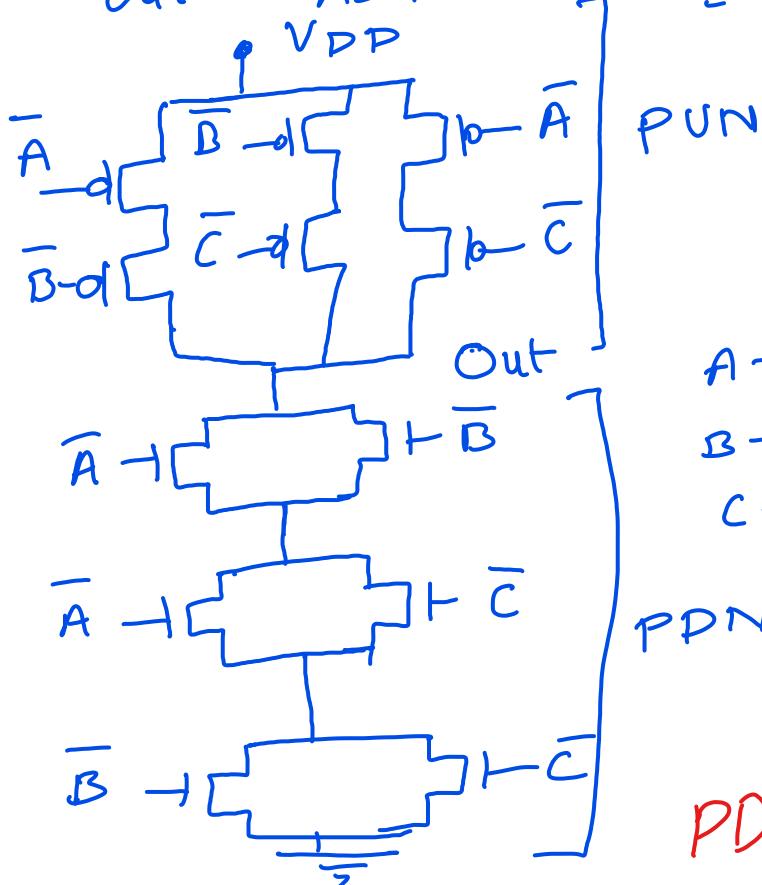
$$\text{Out} = AB + AC + BC$$

→ A lot of ways to realize this even using complementary CMOS. Please consider alternate solutions

→ PDN realizes Out ; PUN realizes Out

$$\overline{\text{Out}} = \overline{AB + BC + AC} = (\overline{A} + \overline{B}) \cdot (\overline{B} + \overline{C}) \cdot (\overline{C} + \overline{A})$$

→ Even $\overline{\text{Out}}$ followed by inverter is correct.



PDN

1.5

; PUN

1.5

Correct
K-Map
grey code +
entries

0.5