ESC201 Introduction to Electronics Lab 9 Handout for Lab Experiments
Combinational Circuit Design using ICs

Aim: In this lab, you will study the characteristics of basic logic gates, implement some combinatorial circuits using the ICs provided to you, and test the functionality of the digital circuit that you have implemented.

Introduction: Logic gates are the basic building blocks in digital circuits. Logic gates and several other digital functions are available in the form of IC (Integrated Circuit) chips. These ICs belong to several *Logic Families*: TTL (Transistor Transistor Logic based on Bipolar Junction Transistors i.e., BJTs), CMOS (complementary MOS based logic using NMOSs and PMOSs). The basic differences between several logic families are in speed and power consumption. The commercial versions of the TTL ICs belong to the 7400 series and those of the CMOS ICs belong to the CD4000 series. All TTL and CMOS ICs use +5 V as the power supply. Voltages above 2.5 V are taken as logic 1 and voltages below 2.5 V are taken as logic 0. For wiring purposes, you will use +5 V as logic 1 and the ground as logic 0. You must connect the power supply and ground pins of an IC to those of the DC power supply for proper working. You will use the following CMOS ICs and TTL ICs:

CD4007: Contains multiple n-channel and p-channel MOSFETs (NMOSs and PMOSs)
CD4069: Hex Inverters (6 NOT gates), each NOT gate is built using NMOSs and PMOSs
CD4001: Quad 2-input NOR gates (4 NOR gates), each NOR gate is built using NMOSs and PMOSs
CD4011: Quad 2-input NAND gates (4 NAND gates), each NAND gate is built using NMOSs and PMOSs
CD4070: Quad 2-input XOR gates (4 XOR gates), each XOR gate is built using NMOSs and PMOSs
TTL IC 74153: Dual 4-to-1 line Multiplexer (MUX) with enable inputs (enables are active LOW)

You will use the Digital Test Board for the experiments on digital circuits. You must connect V_{CC} (+5 V) and GND of the Digital Test Board to those of the DC power supply for proper working. You will wire the digital circuit designed using transistors or gates from the indicated ICs. The circuit diagram showing the transistors or gates and indicating the pin numbers of the ICs against all the input and output connections of the transistors or gates are given. Then, you have to connect required number of the data switches from the Digital Test Board to the inputs and the Logic Probe (LP) to the output of the digital circuit under consideration. You will test the output of the circuit for each input combination by toggling the data switches. You will verify that the logic implementation is working properly by obtaining the Truth Table (observing the outputs for given inputs).

Experiment 1: Familiarization with the Digital Test Board and ICs (*5 × 4 = 20 marks*)
The diagram for the Digital Test Board and the pin diagrams of ICs are shown in Fig. E1a and E1b.

1. Verify the working of all the data switches by connecting their outputs individually to the Logic Probe (LP) input. For each of the data switches, check that both logic low ‘0’ and logic high ‘1’ level can be obtained by toggling the switch. For Logic ‘0’: Green LED will be OFF; for Logic ‘1’: Green LED will be ON; and for Open connection of the LP (neither ‘1’ nor ‘0’): Green LED will flicker.

2. Connect any 4 data switch outputs to the 7-segment display driver inputs. Check the display for all the 16 input combinations. Note that for binary inputs 0000 to 0111, the display should show the corresponding decimal numbers from 0 to 7. For binary inputs 1000 to 1111, the decimal point at the top left corner of the display would also light up in addition to the numerals 0 to 7.

3. Test the functionality of Inverter (from IC CD4069), NAND gate (from IC CD4011), NOR gate (from IC CD4001) and XOR gate (from IC CD4070), one by one, using the Digital Test Board with required number of the data switches connected to the inputs and the LP connected to the output of the logic gate under test.

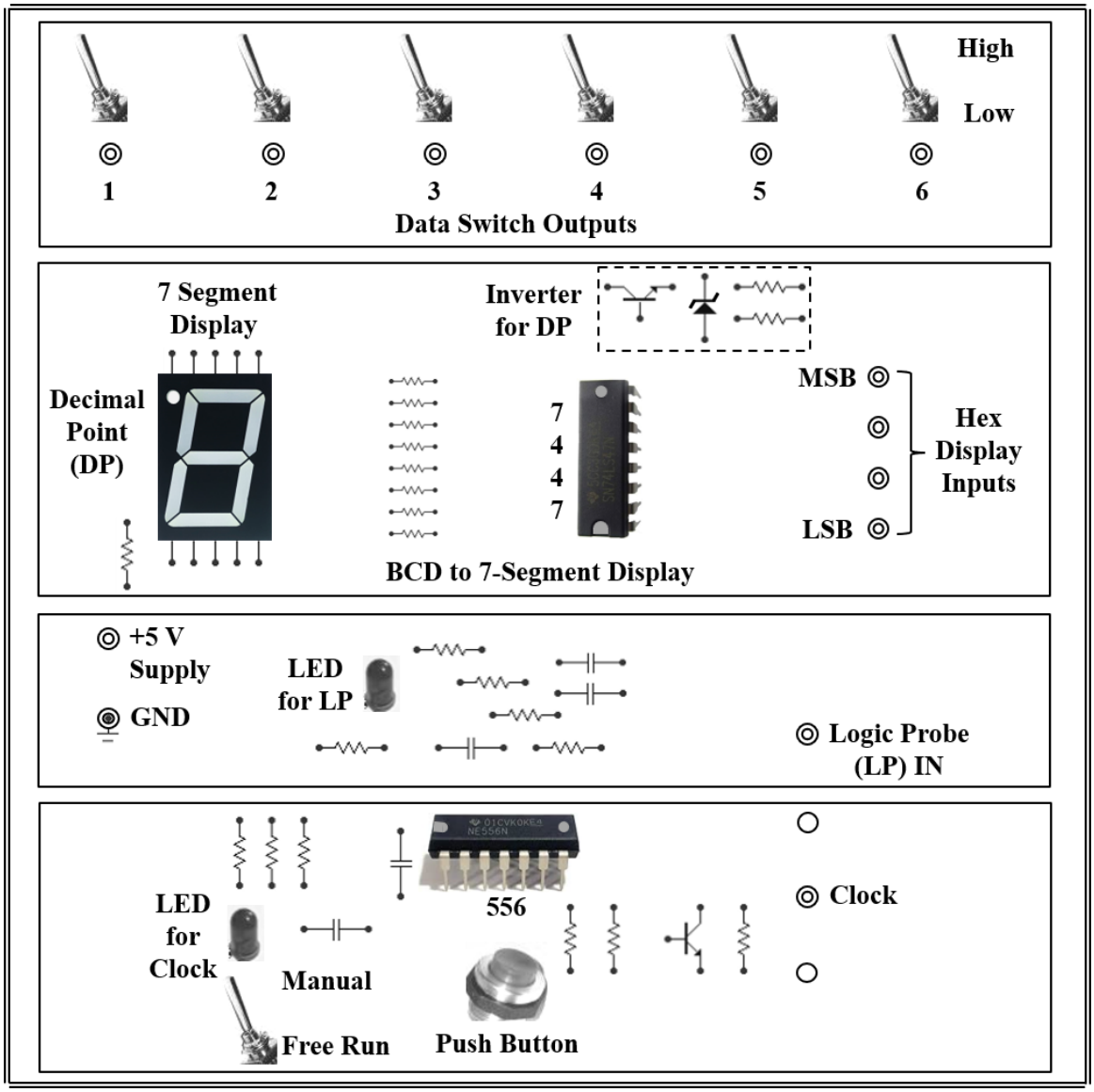

Figure E1a: Digital Test Board

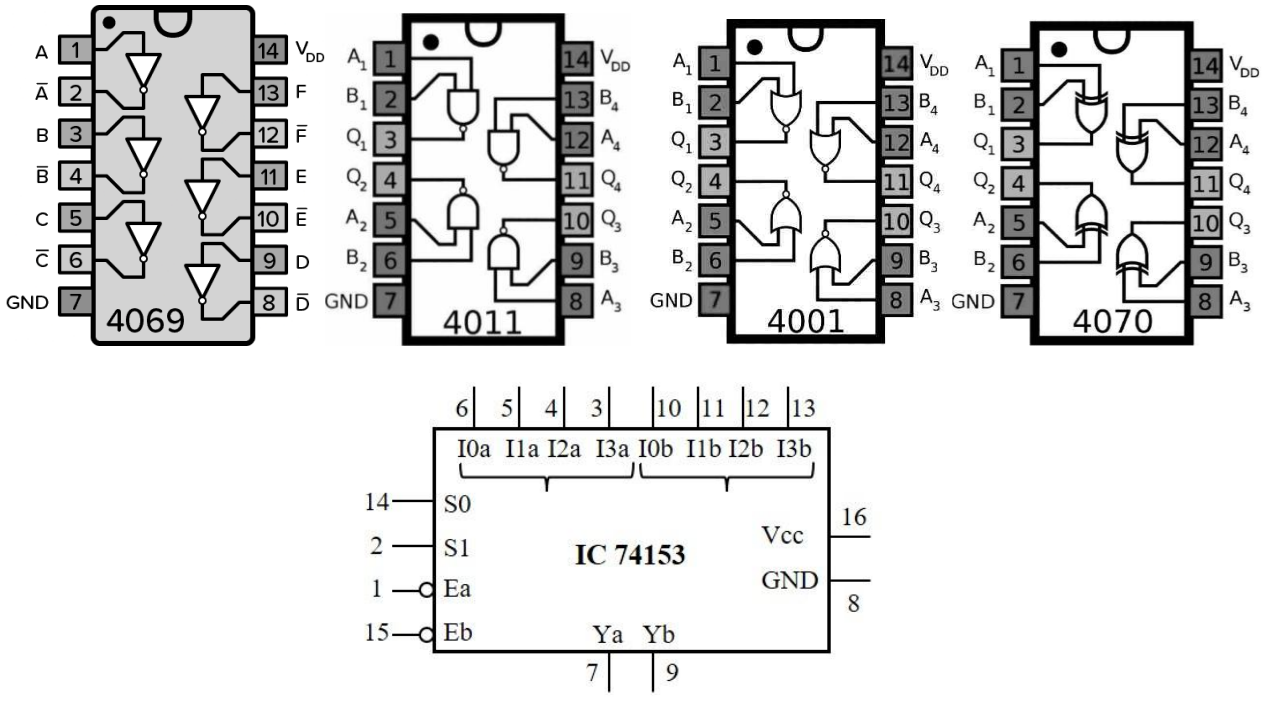

Figure E1b: Pin Diagrams of ICs

4. Test the functionality of the dual 4-to-1 MUX (IC 74153) by connecting two data switches to two select lines, one data switch and its complemented output (use an inverter from CD4069 IC) to two enable inputs (enables are active LOW). One by one, select each of 8 input lines using the three data switches connected to select lines and enable inputs. In each case, connect the remaining data switch to that selected input line, and test the output by connecting LP to the corresponding output of the MUX and toggling the data switch.

Experiment 2: Realization of Full-Adder Circuits (*5 × 2 = 10 marks*)

You will design and test a full-adder circuit using two different methods. If A and B are the two input bits and C is the carry in bit of the full adder, then the um is $S = A \oplus B \oplus C$ and the carry out is $C_{out} = (A \oplus B)C + AB$. The full adder can be designed using two half adders and additional gates as shown in Fig. E3a. For a half-adder circuit, if X and Y are two input bits, then the sum output is $S_H = X \oplus Y$ and the carry output is $C_H = XY$.

1. Set up the circuit for each half adder first as shown in Fig. E2a. For each half adder circuit, the pin numbers for the XOR and NAND gates in CD4070 IC and CD4011 IC, respectively, are given in Fig. E2a. Connect the power supply and ground pins of the ICs too. Using two data switches as the inputs and the LP as the output, test both the sum and carry outputs of each of the half adder, one by one, for all input combination and write down the full Truth table of the half adder from your observation.

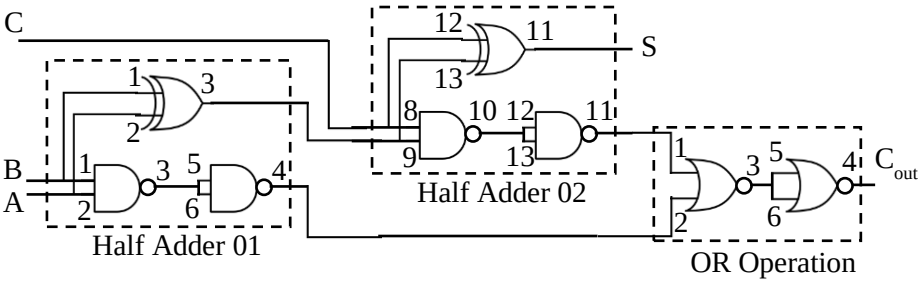

Figure E2a: Full Adder Circuit using Two Half Adders

Then, set up the circuit for the full adder. The pin numbers for the NOR gates in CD4001 IC are given in Fig. E2a. Connect the power supply and ground pins of the IC too. Using three data switches as the inputs and the LP as the output, test both the sum and carry outputs of the full adder, one by one, for all input combination and write down the full Truth table from your observation.

2. To design the full adder only, the number of gates can be reduced as shown in Fig. E2b. The pin numbers for the XOR and NAND gates in CD4070 IC and CD4011 IC, respectively, are given in Fig. E2b. Set up the circuit shown in Fig. E2b. Connect the power supply and ground pins of the ICs too. Using three data switches as the inputs and the LP as the output, test both the sum and carry outputs of the full adder, one by one, for all input combination and write down the full Truth table from your observation.

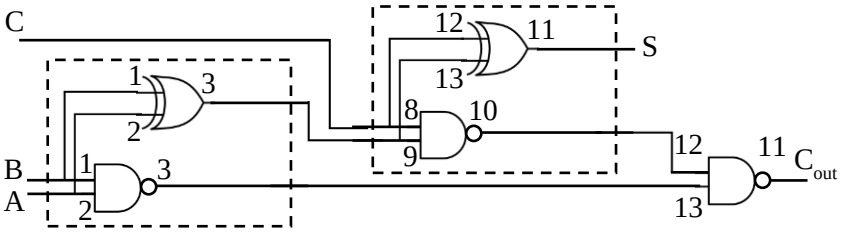

Figure E2b: Full Adder Circuit Design Alternative

Experiment 3: Realization of Decoder Circuits (*5 × 2 = 10 marks*)

You will design three 3-bit decoders capable of decoding the following 3-bit words (CBA) as follows:

The decoder should give logical '1' output only when the specified input word is 001, 101, or 111. For other input combinations, the output should be logical '0'. The Boolean function for the output F can be written as: $F = \bar{C}\bar{B}A + C\bar{B}A + CBA = (\bar{B} + C)A$ after minimization and grouping terms.

1. The function *F* can be realized using the circuit shown in Fig. E3a using only NAND gates. Set up the circuit shown in Fig. E3a. The pin numbers for the NAND gates in CD4011 IC are given in Fig. E3a. Connect the power supply and ground pins of the ICs too. Using three data switches as the inputs *A*, *B*, *C*, and the LP as the output *F*, test the output of the circuit for all input combination and write down the full Truth table from your observation.

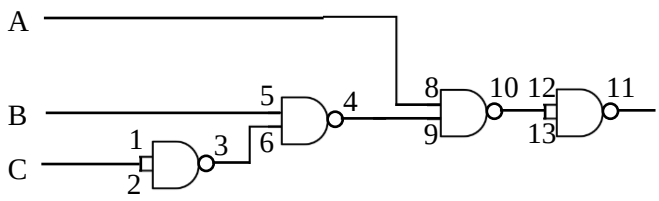

Figure E3a: NAND-based Realization

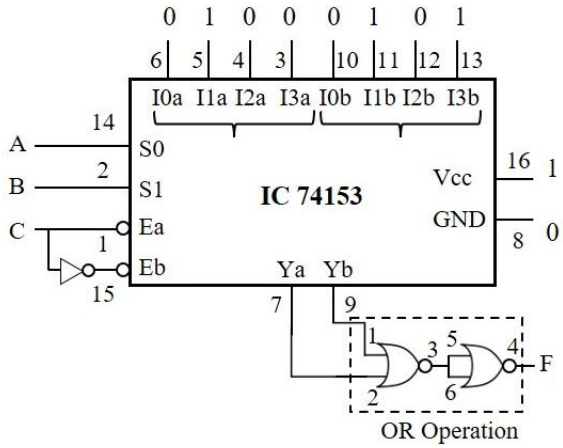

Figure E3b: MUX-based Realization

2. The same function *F* has been realized using a dual 4-to-1 MUX after converting it to an 8-to-1 line MUX with *B* and *A* as the two select lines, and *C* and $\bar{C}$ (using an inverter in CD 4069 IC) connected to the enable inputs, and taking the output from the OR gate (implemented using NOR gates in CD 4001 IC) as shown in Fig. 3b. Since, $F(C, B, A) = \Sigma m(1,5,7)$, all 8 input lines are connected to the corresponding logic '0' and '1' as shown in Fig. E3b. Set up the circuit shown in Fig. E3b. The pin numbers for the dual 4-to-1 MUX in IC 74153 are given Fig. E3b. Connect the power supply and ground pins of the ICs too. Using three data switches as inputs *A*, *B*, *C* and LP as the output *F*, test the output of the circuit for all input combination and write down the full Truth table from your observation.