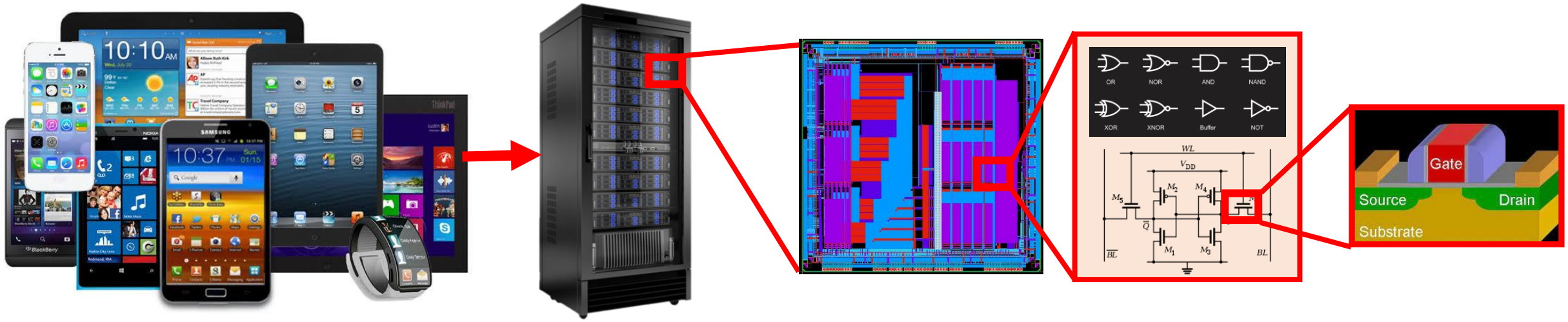

ESC201: Introduction to Electronics

Module 6: Digital Circuits

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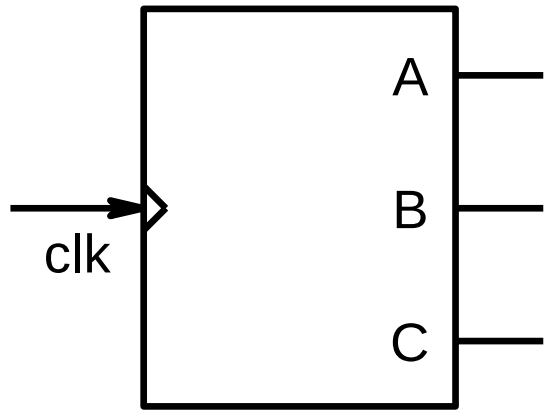
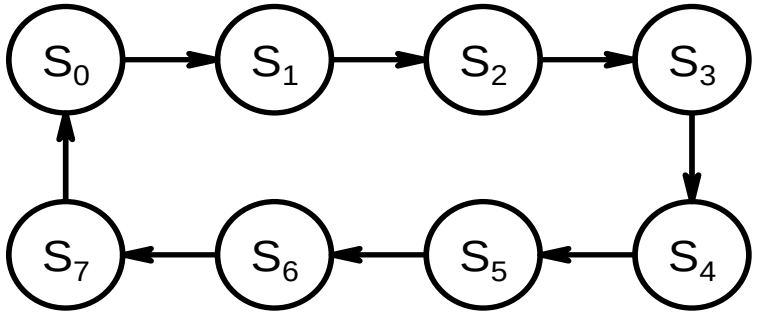
Counters

- Counters are sequential circuits.
- They traverse a set of states in a sequence.
- They keep repeating the cycle of states.
- There need be no input to counters.
- Output may be the state value itself.

Sequential Binary Counter



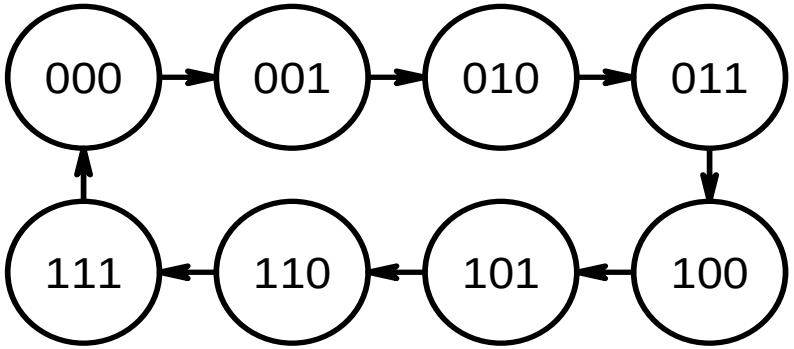


A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

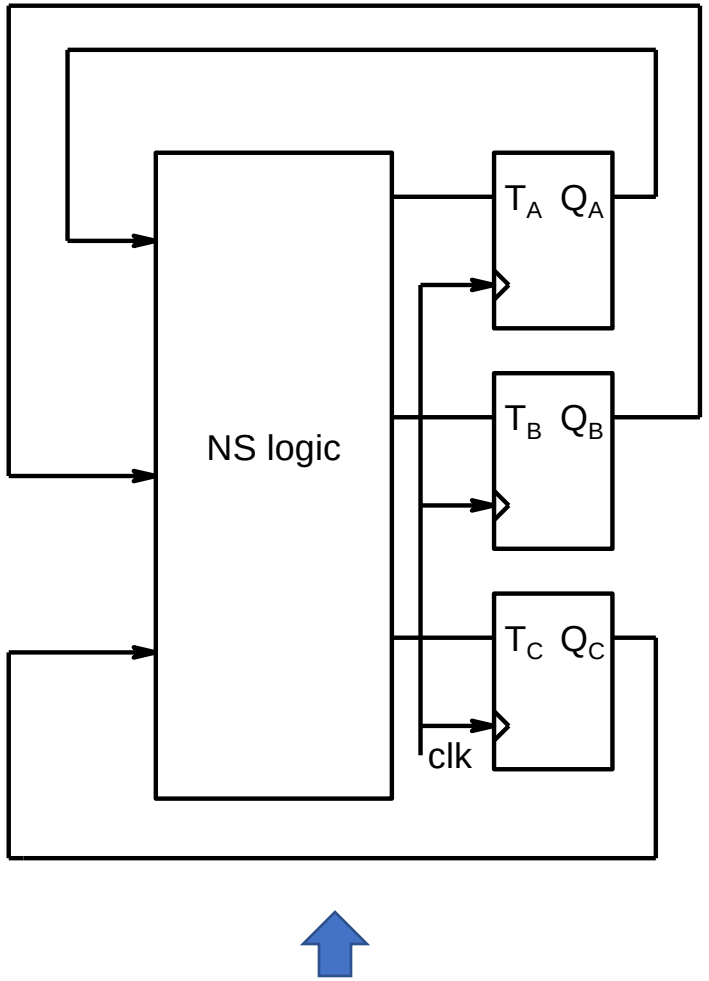
In state S_0, the output ABC is 000, in S_1 001 and so on

There are 8 states so 3 Registers are at least required. Let us choose T FF.

Design with T-Register

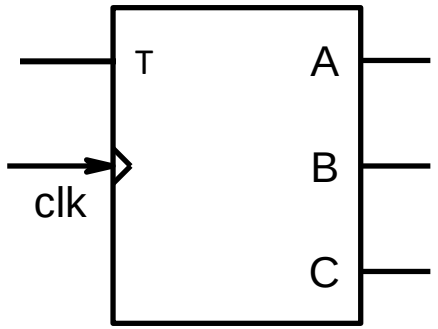


PS (*t*) A B C	NS (*t*+1) A B C	T_A T_B T_C
0 0 0	0 0 1	0 0 1
0 0 1	0 1 0	0 1 1
0 1 0	0 1 1	0 0 1
0 1 1	1 0 0	1 1 1
1 0 0	1 0 1	0 0 1
1 0 1	1 1 0	0 1 1
1 1 0	1 1 1	0 0 1
1 1 1	0 0 0	1 1 1



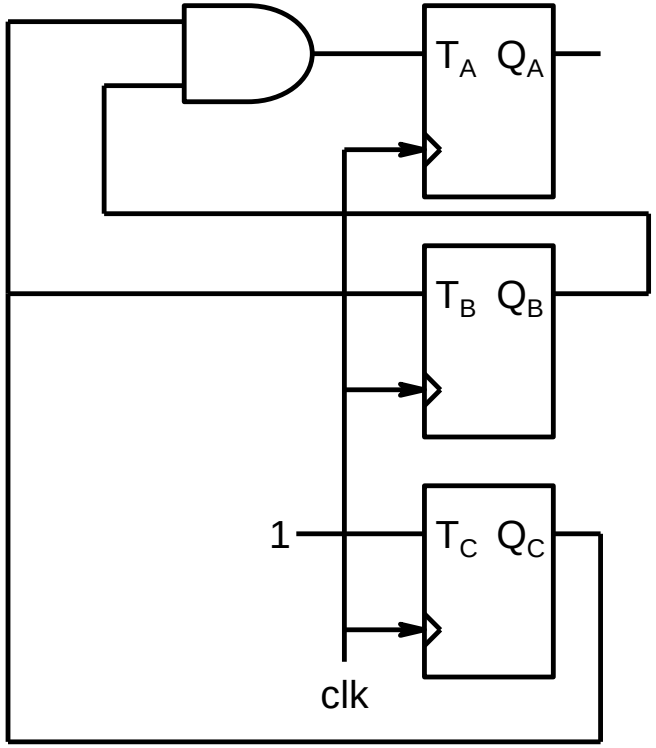
$$T_A = B.C \; ; \; T_B = C \; ; \; T_C = 1$$

Binary Counter



A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

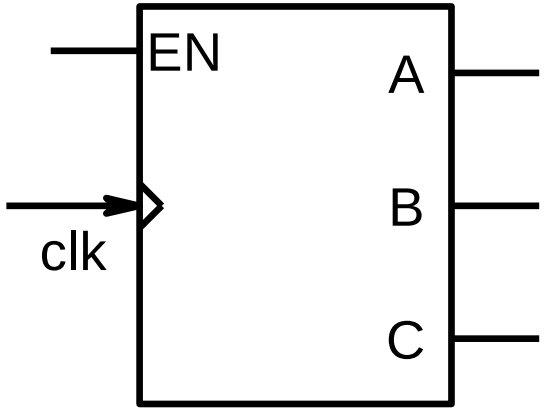
Based on
next state table



$$T_A = B.C \; ; \; T_B = C \; ; \; T_C = 1$$

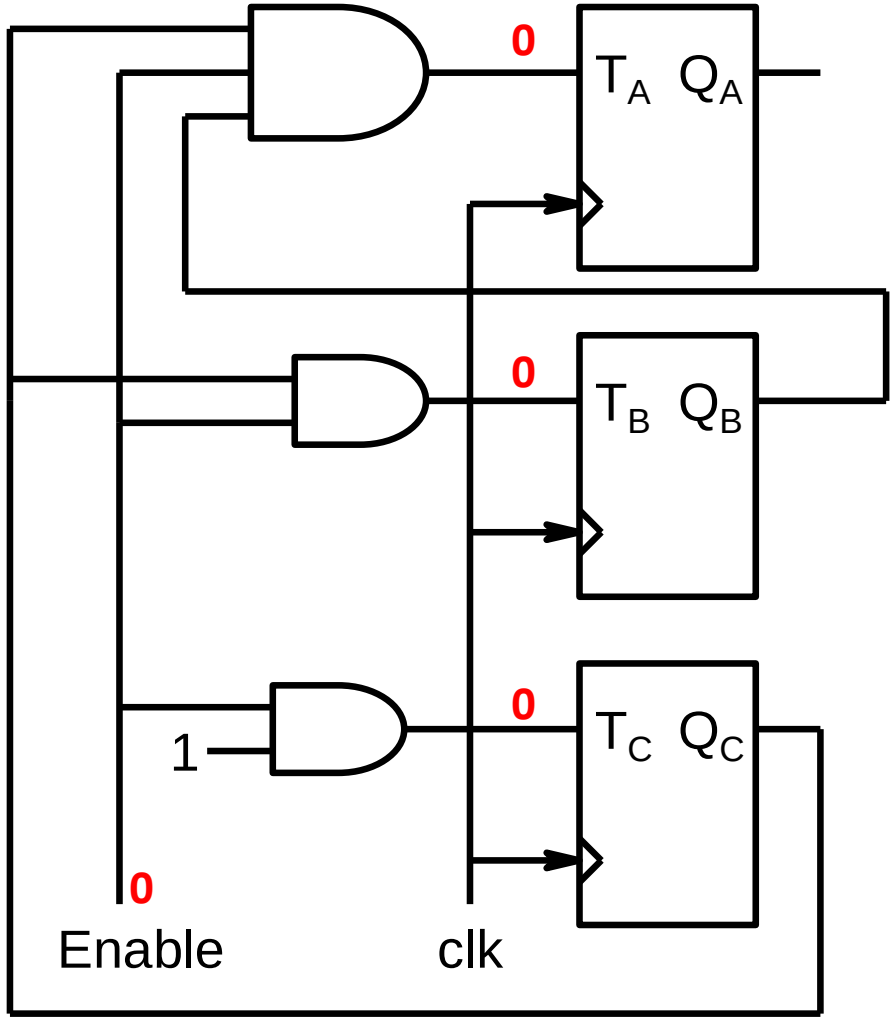
Binary Up Counter – Another Version

Counter with Enable

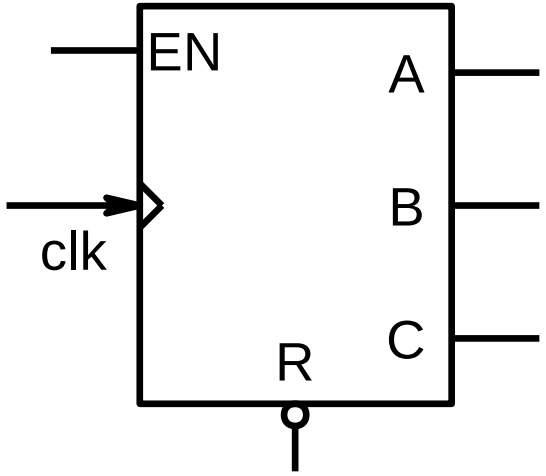


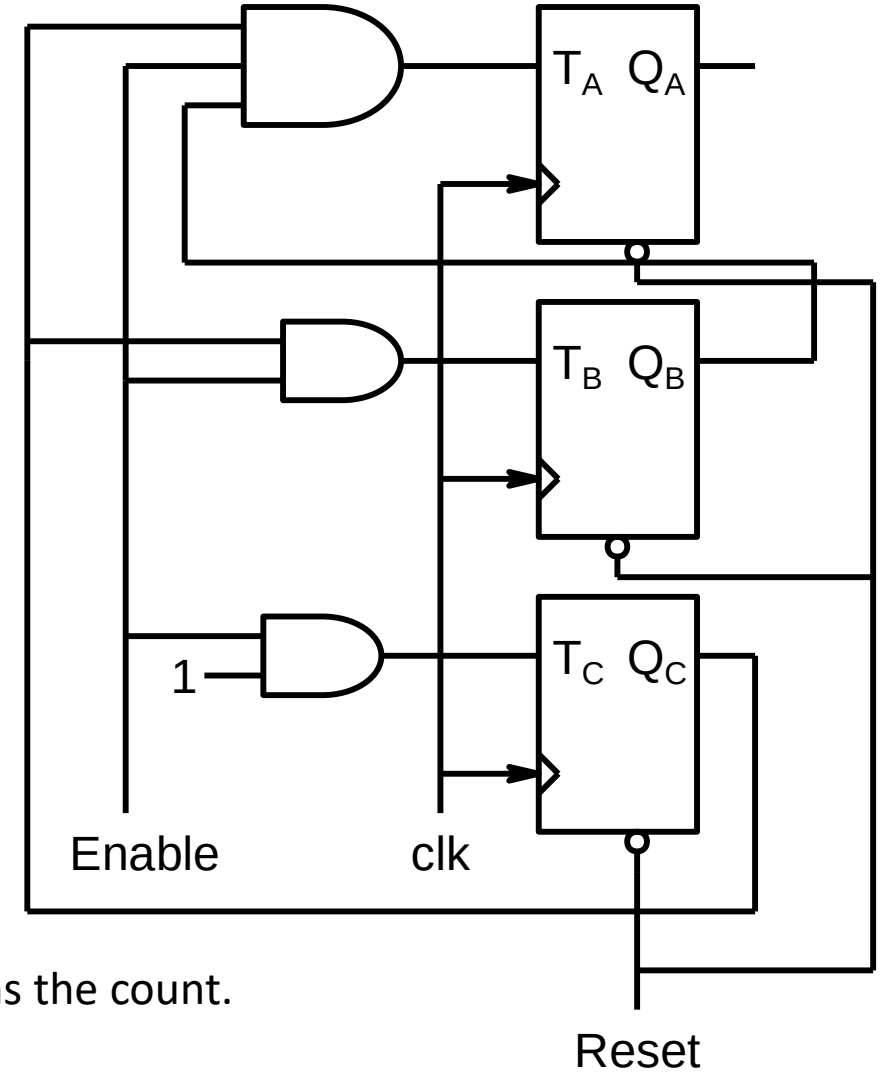
Counter is in Hold state.

When Enable = 1,
the counter begins the count.



Counter with Asynchronous Reset





When Enable = 1, the counter begins the count.

4 Bit Up Counter

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0

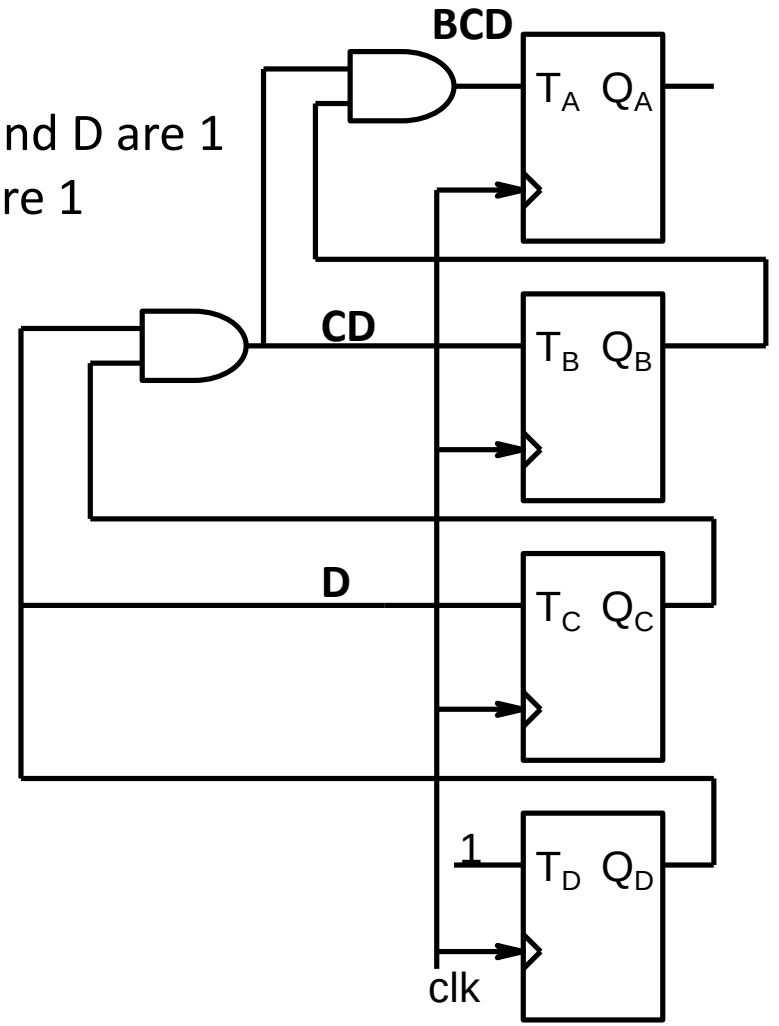
-D toggles every clock cycle

-C toggles only when D is 1

-B toggles only when both C and D are 1

-A toggles only when B C D are 1

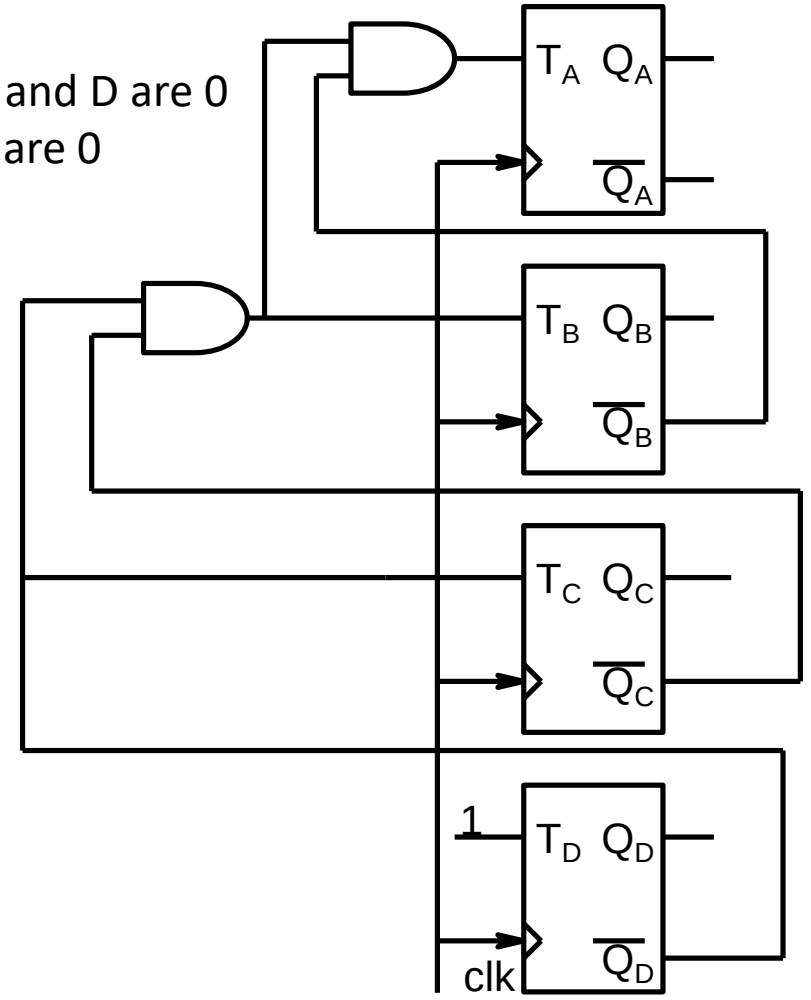
T FF toggles when T=1



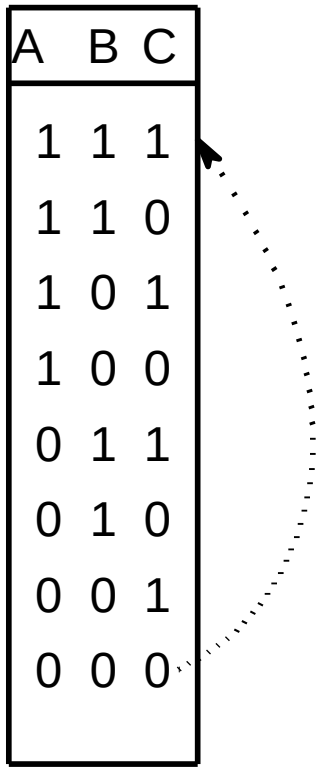
4-bit Down Counter

A	B	C	D
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0
1	1	1	1

-D toggles every clock cycle
-C toggles only when D is 0
-B toggles only when both C and D are 0
-A toggles only when D C B are 0

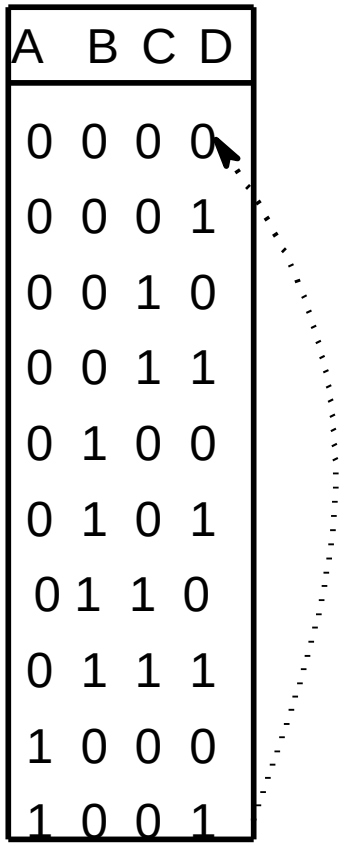


Some Other Types of Counters



A	B	C
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

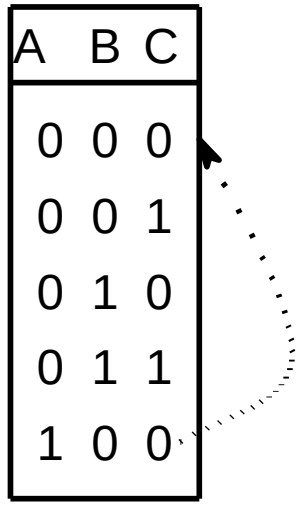
Binary down counter



A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Decade counter

Modulo-10 Counter



A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

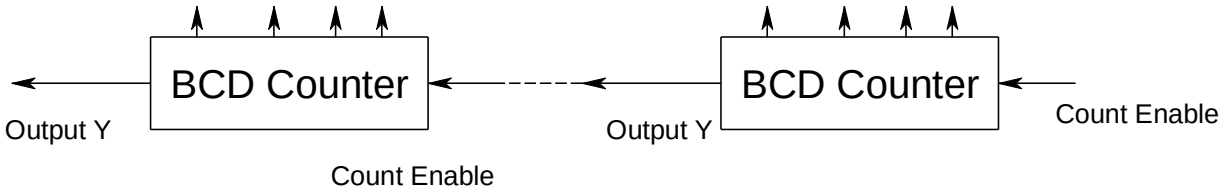
Modulo-5 Counter

BCD Counter

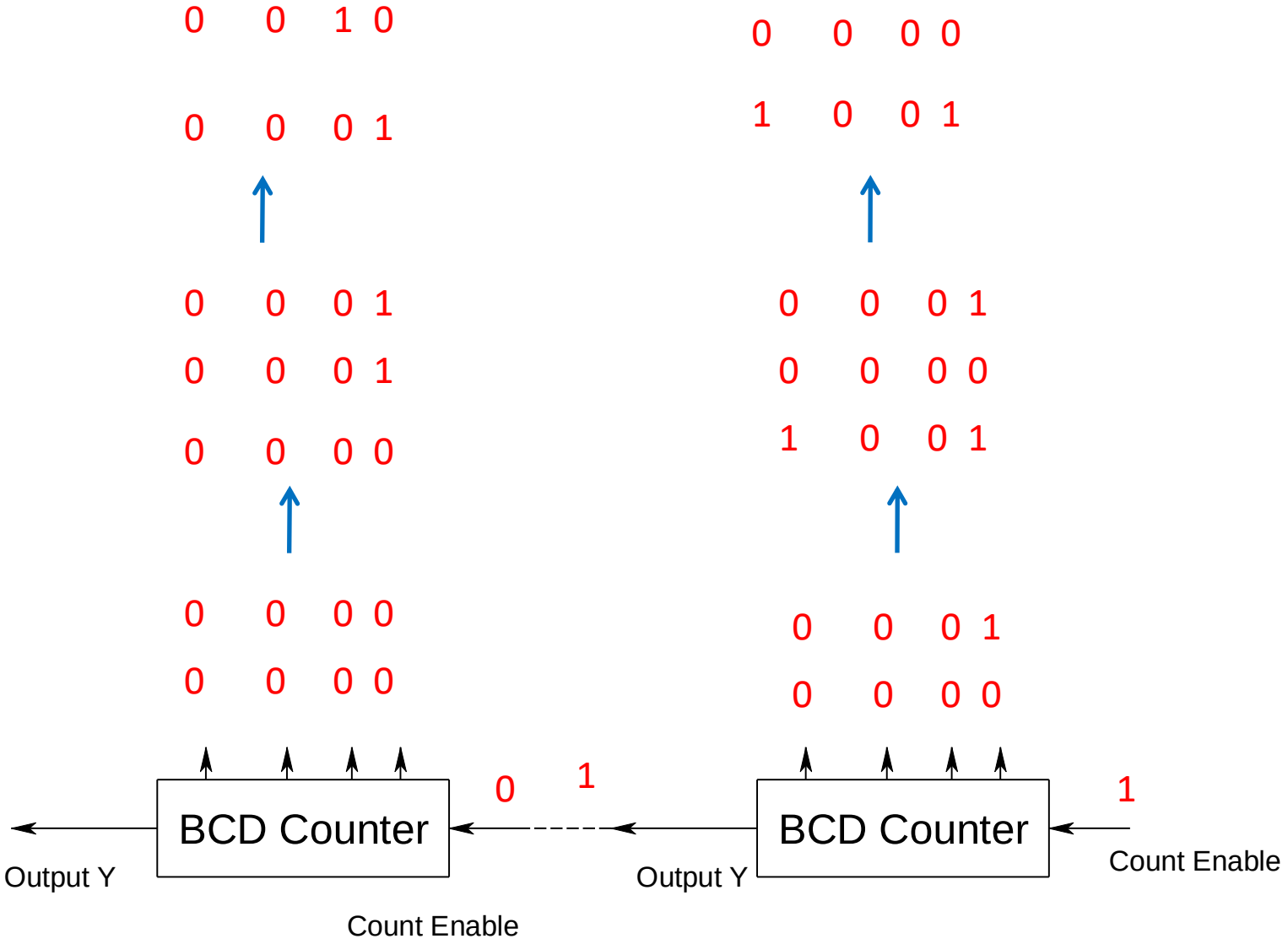
Binary Coded Decimal (BCD): each decimal digit is coded as a 4-bit binary number

25 = 0010 0101

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1



BCD counter from 0 to 99



Counter with Unused States!

Arbitrary sequence, 6 states

PS	NS						
A B C	A B C	J_A	K_A	J_B	K_B	J_C	K_C
0 0 0	0 0 1	0	X	0	X	1	X
0 0 1	0 1 0	0	X	1	X	X	1
0 1 0	1 0 0	1	X	X	1	0	X
1 0 0	1 0 1	X	0	0	X	1	X
1 0 1	1 1 0	X	0	1	X	X	1
1 1 0	0 0 0	X	1	X	1	0	X

There are two unused states 011 and 111. one approach to handle this situation is that, while evaluating expressions for J K , we use don’t care conditions corresponding to these unused states

Continued…

PS			NS			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A	B	C						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

A \ BC	00	01	11	10
0	0	0	X	1
1	X	X	X	X

$J_A = B$

Continued…

PS			NS								
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

$$J_A = B \qquad K_A = B$$

$$J_B = C \qquad K_B = 1$$

$$J_C = \overline{B} \qquad K_C = 1$$

After synthesizing the circuit, one needs to check that if by chance the counter goes into one of the unused states, after one or more clock cycles, it enters a used state and then remains among the used states