Performance Metrics: Mathematical Representation

CPU Clock Cycles

Let:

- $C_{\text{cpu\_core}}$ represent the CPU clock cycles.
- C_{counted} represent the number of clock cycles counted.
- C_{missed} represent the number of clock cycles not counted.

We can express the total clock cycles as:

$$C_{\text{cpu\_core}} = C_{\text{counted}} + C_{\text{missed}}$$

If some cycles are not counted, the reported value is C_{counted}, and we can infer:

$$C_{\text{cpu\_core}} > C_{\text{counted}}$$

Latency

Latency (L) is influenced by context switches (CS) and page faults (PF):

$$L \propto CS + PF$$

This indicates that as the number of context switches and page faults increases, latency tends to increase due to the additional overhead.

Branch Misses and Cache Misses

Branch misses can be represented by BM, where high values of BM indicate inefficiency in branch prediction, potentially increasing execution time.

Let T_{exec} represent the execution time, then:

$$T_{\text{exec}} \propto BM$$

Overall Performance Summary

The total execution time can be modeled as:

$$T_{\text{exec}} = f(C_{\text{cpu\_core}}, L, BM)$$

Where:

- T_{exec} depends on the number of CPU clock cycles ($C_{\text{cpu\_core}}$),
- Latency (L), which is influenced by context switches and page faults,
- Branch misses (BM).

Increases in any of these components negatively affect the overall performance.