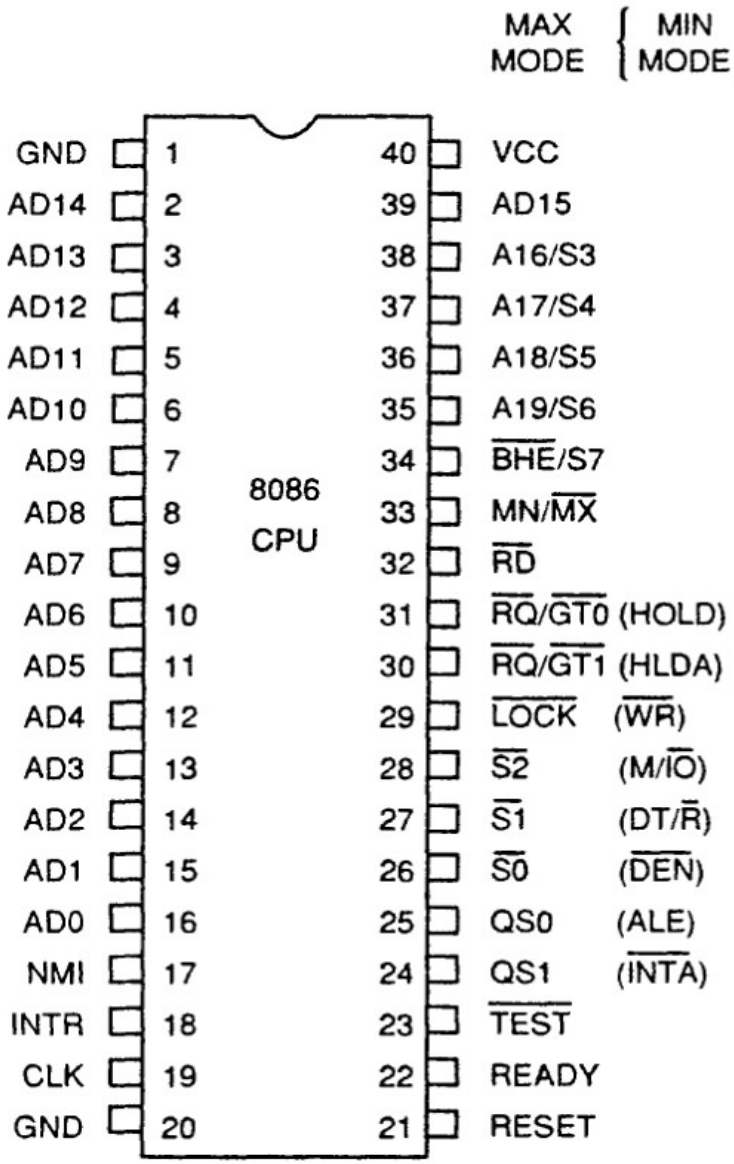
UNIT – 6

Contents

- Pin Diagram of 8086
- Minimum mode of Operation
- Maximum mode of Operation
- Timing Diagram
- 8255 PPI various modes of operation

INTEL 8086 - Pin Diagram



Pin Definitions

Pin(s)	symbol	Description
1&20	GND	ground
2-16	AD14-AD0	multiplexed address and data bus. it is separated by ALE pin. when it is high address bus is selected & low data bus is selected.
17	NMI	Non-maskable interrupt .it is not maskable by software
18	INTR	interrupt request. It specifies the availability of request. if any request is pending processor gives the acknowledgement by resetting IF flag(IF=0)
19	CLK	It is a timing signal. which is asymmetric square wave with 33%duty cycle.

Pin Definitions

21	RESET	It terminates the current activity & starts execution
22	READY	Indicates the trasfer of data which is ready
23	$\overline{\text{TEST}}$	when it is zero ,execution will continues. when it is one processor is in idle state
24-31	--	defined for minimum and maximum mode

Pin Definitions

32	**RD**	indicates a memory or I/O read is to be performed.
33	MN / $\overline{MX}$	CPU is in minimum mode when strapped to +5V and maximum mode when grounded.
34	**BHE'/S7**	It is used to indicate the transfer of data over higher order bus(D15-D8).

Pin Definitions

35-38 A19/S6 - A16/S3 — during the first part of the bus cycle the upper 4 bits of the address are output and

During the remainder of the bus cycle status is output. S3 & S4 indicate the segment register being used as follows:

S4	S3	Register
0	0	ES
0	1	SS
1	0	CS or none
0	0	DS

S5 gives the current setting of IF.

S6 is always 0.

39 AD15 — same as AD14-AD0

40 VCC — supply voltage +5V ±10%.

Minimum mode 8086 system

- 8086 operated in minimum mode when MN/MX'=1
- In this all the control signals are given out by microprocessor chip itself.
- There is a single microprocessor in minimum mode.

Minimum mode system

24	$\overline{INTA}$	Indicates recognition of an interrupt request.
25	ALE	outputs a pulse at the beginning of bus cycle and is to indicate an address is available on the address pins.
26	$\overline{DEN}$	output during the latter portion of bus cycle and is to inform the transceiver that CPU is ready to send or receive data.
26	DT / $\overline{R}$	indicates to the set of transceivers whether they are to transmit or receive data.
26	M / $\overline{IO}$	distinguish memory transfer (logic 1) from an I/O transfer (logic 0).
26	$\overline{WR}$	when 0, it indicates a write operation is being performed.
27	HOLD	Receives a bus request from bus masters.
28	HLDA	outputs a bus grant to a requesting master.

Maximum Mode 8086 System

- Here, either a numeric coprocessor of the type 8087 or another processor is interfaced with 8086.The Memory, Address Bus, Data Buses are shared resources between the two processors.
- The control signals for Maximum mode of operation are generated by the Bus Controller chip 8288. The three status outputs S0*, S1*, S2* from the processor are input to 8288.
- The outputs of the bus controller are the Control Signals, namely DEN, DT/R*, IORC*, IOWTC*, MWTC*, MRDC*, ALE etc.

Maximum mode system

24,25 QS1,QS0 — Reflects the status of the instruction queue.

26 – 28 S0,S1,S2 — Indicates the type of transfer to take place during the current bus cycle.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Inactive – passive

QS1	QS0	Indication
0	0	No operation
0	1	First byte of op-code from the queue
1	0	Empty Queue
1	1	Subsequent byte from the queue.

29 $\overline{LOCK}$ — Indicates the bus will not be released to other potential bus masters until the instruction with prefix LOCK is executed.

30 RQ / $\overline{GT1}$ — for inputting bus requests and outputting bus grants.

31 RQ / $\overline{GT0}$ — same as that RQ / $\overline{GT1}$ except that a request on RQ / $\overline{GT0}$ has higher priority.

Maximum mode system

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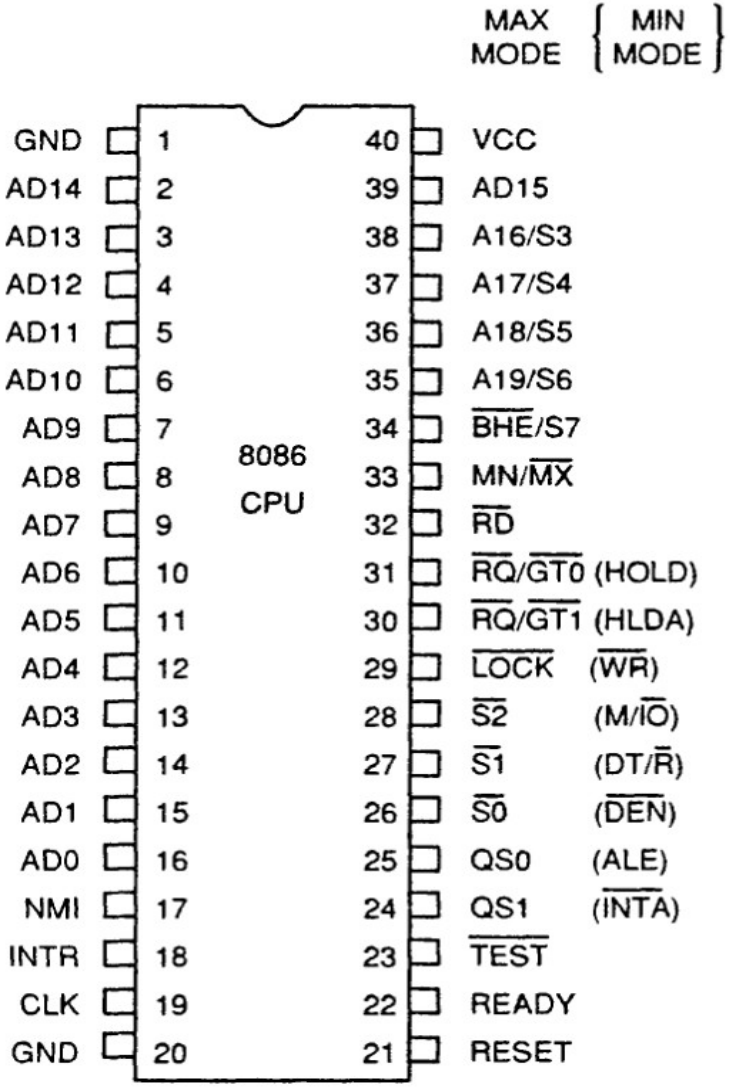
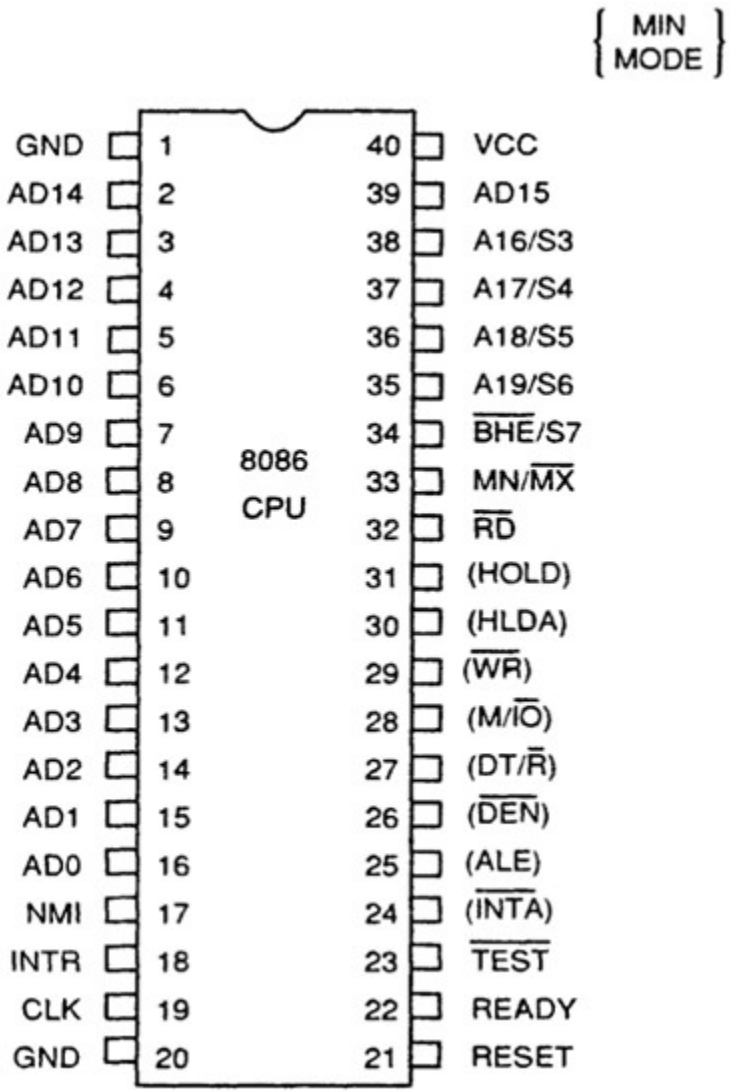
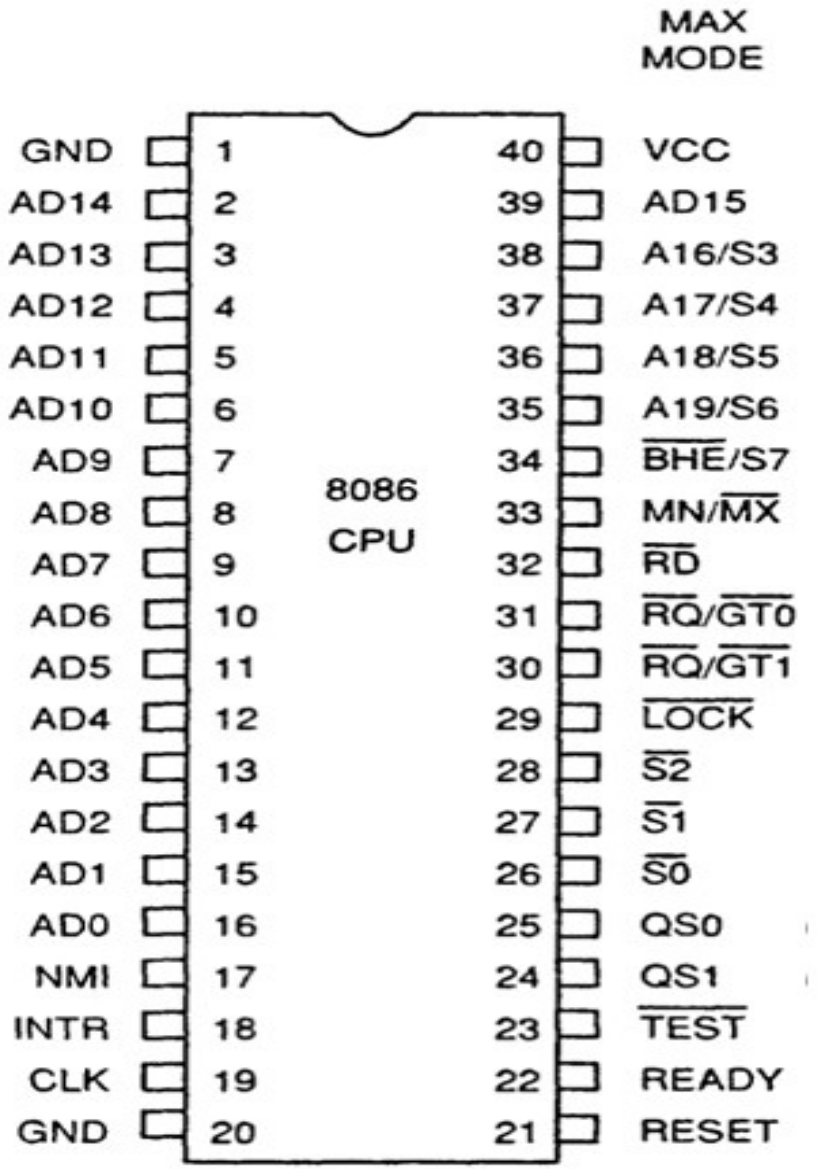
- Draw the pin diagram of 8086
- Draw the pin diagram of 8086 in minimum mode
- Draw the pin diagram of 8086 in maximum mode
- Explain about minimum mode signal
- Explain about maximum mode signal
- Draw the block diagram of 8255.
- Draw and explain the block diagram of 8255

INTEL 8086 - Pin Diagram




MIN
MODE
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8086
CPU
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 (HOLD)
30 (HLDA)
29 (WR)
28 (M/IO)
27 (DT/R)
26 (DEN)
25 (ALE)
24 (INTA)
23 TEST
22 READY
21 RESET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AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
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8086
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40 VCC
39 AD15
38 A16/S3
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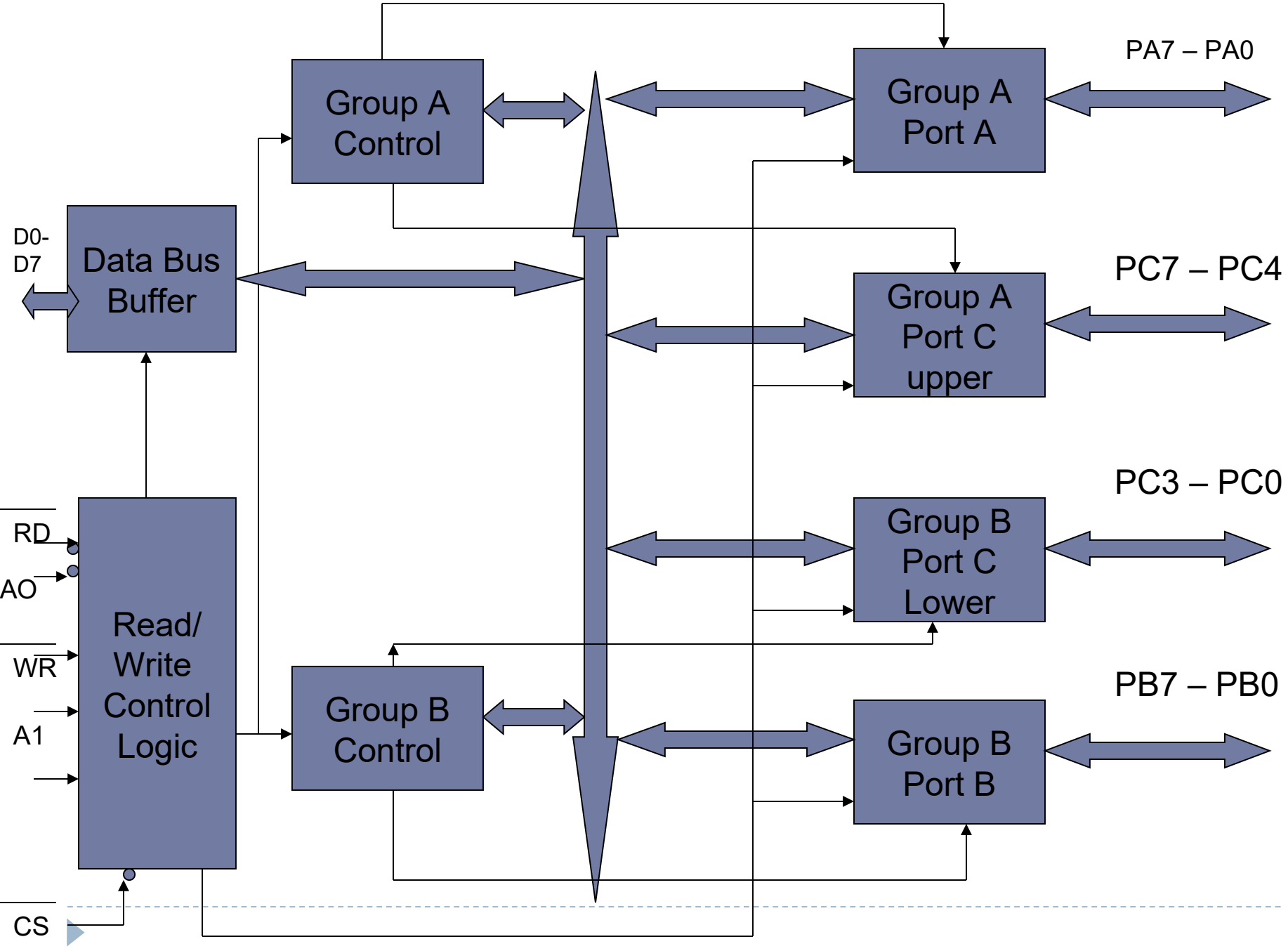
33 MN/MX
32 RD
31 RQ/GT0
30 RQ/GT1
29 LOCK
28 S2
27 S1
26 S0
25 QS0
24 QS1
23 TEST
22 READY
21 RESET

8255 PPI

Programmable peripheral interface

(or)

Architecture of Programmable I/O Port 8255


Group A Control
Group A Port A
PA7 – PA0
D0-
D7
Data Bus Buffer
Group A Port C upper
PC7 – PC4
Group B Port C Lower
PC3 – PC0
RD
AO
Read/ Write Control Logic
WR
A1
Group B Control
Group B Port B
PB7 – PB0
CS

Pin Description

PA(0-7): Port A is an I/O port. Its an 8-bit data output latch/buffer and an 8-bit data input latch.

RD': Read Control is an Active low input pin. RD is LOW when CPU reads data.

CS': Chip Select is an Active low input pin. A LOW on this pin selects 8255.

GND: This provides the ground for the IC

A0,A1: These pins along with RD',WR', CS' pins control the operation of 8255.

Pin Description (Accessing 8255 using A0, A1 ,RD ,WR ,CS pins)

A1	A0	RD	WR	CS	Operation Performed
X	X	X	X	1	Chip Disabled i.e. Chip not Selected
Chip is selected when CS = 0					
Input(Read) Operation.					
0	0	0	1	0	Read Port A- Data bus
0	1	0	1	0	Read Port B- Data bus
1	0	0	1	0	Read Port C- Data bus
1	1	0	1	0	Control Word Register- Data bus
			Output(write) Operation.		
0	0	1	0	0	Write Port A-data bus
0	1	1	0	0	Write Port B-data bus
1	0	1	0	0	Write Port C-data bus
1	1	1	0	0	Data bus-Control

Pin Description

PC(0-7): Port C is an 8-bit I/O port. Its lower 4-bits can be programmed to work in conjunction with PortB and the upper 4-bits can be programmed to work in conjunction with Port A separately.

PB(0-7): Port B is an 8-bit I/O port used for 8-bit output data latch/buffer or input data buffer

Vcc: +5V power supply.

D7-D0: Data bus, bidirectional, tristate lines connected to system data lines

RESET: input pin which resets the control word register.

WR': Write Enable is an active low input pin.it indicates the write operation.

Modes of Operation in 8255

- There are two basic modes of operation of 8255.

  1. I/O mode 2. Bit set-reset mode

- In the I/O mode, 8255 ports works as programmable I/O ports, while in BSR mode only port-c(pc0-pc7) cab be used to set or reset its individual port bits.
- Under the I/O mode of operation, further there are three modes. they are mode0,mode1,mode2.