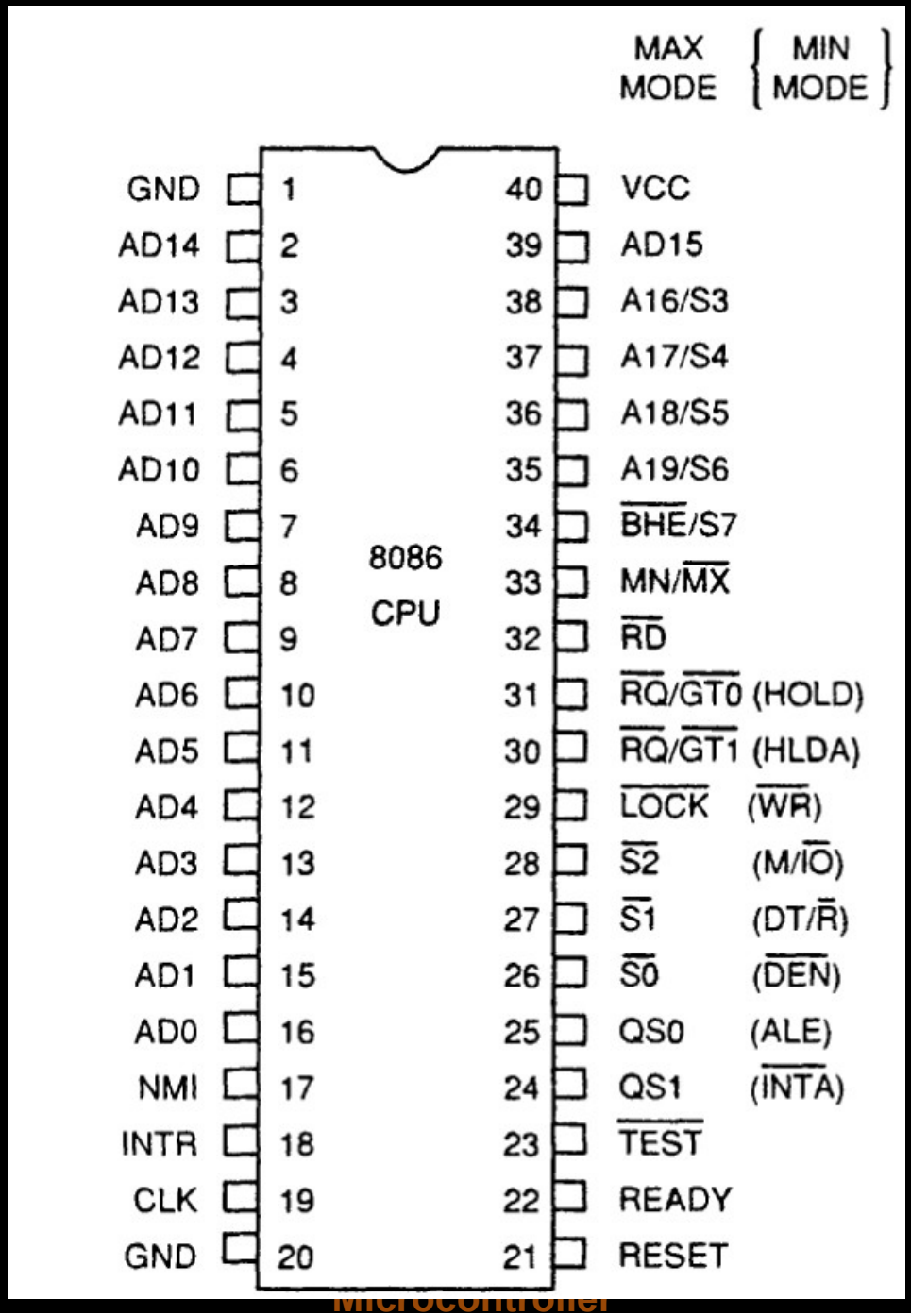
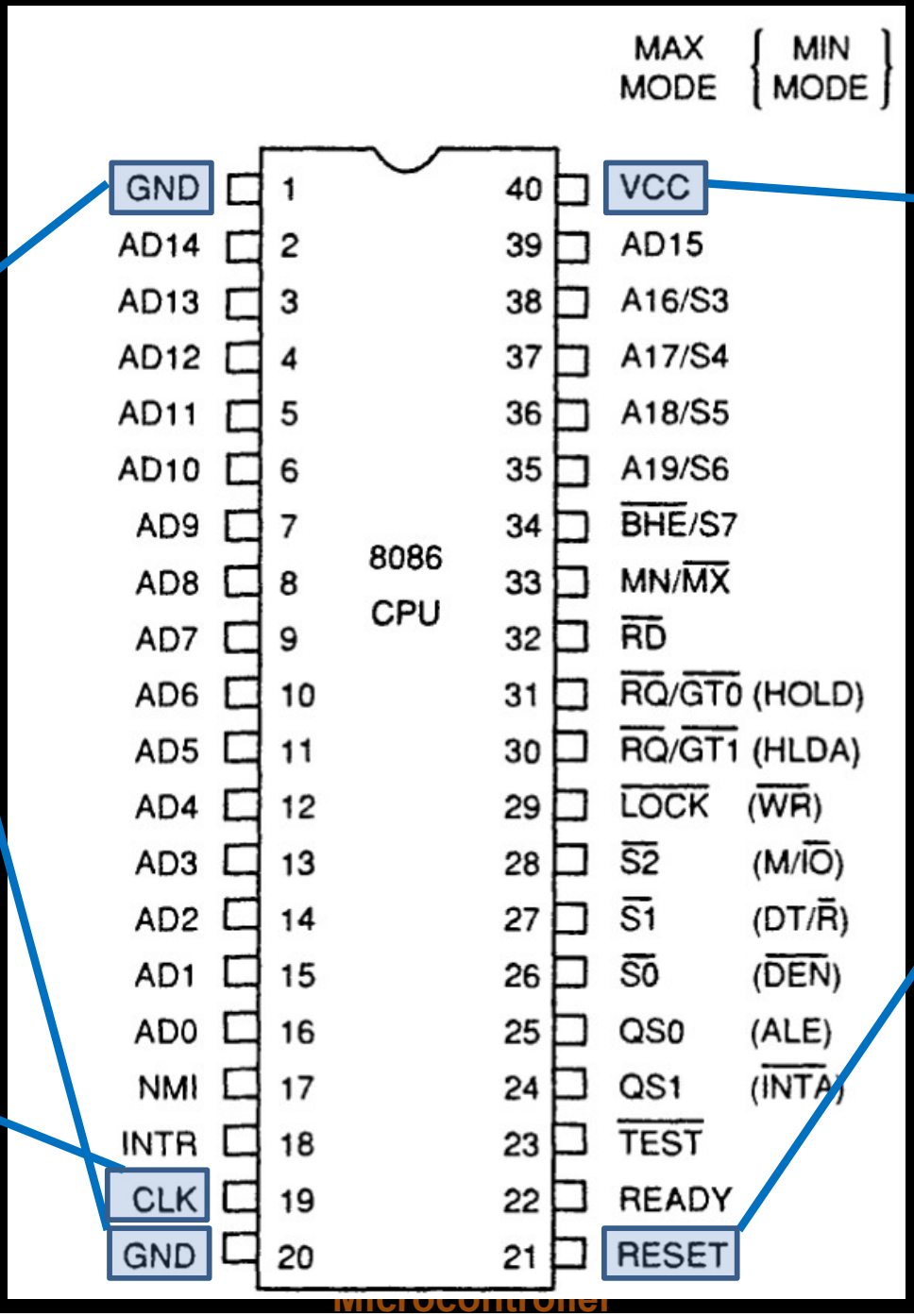
UNIT :5

INTEL 8086 - Pin Diagram



INTEL 8086 - Pin Details



Ground

Power Supply

5V ± 10%

Reset

Terminate the current activity & starts execution

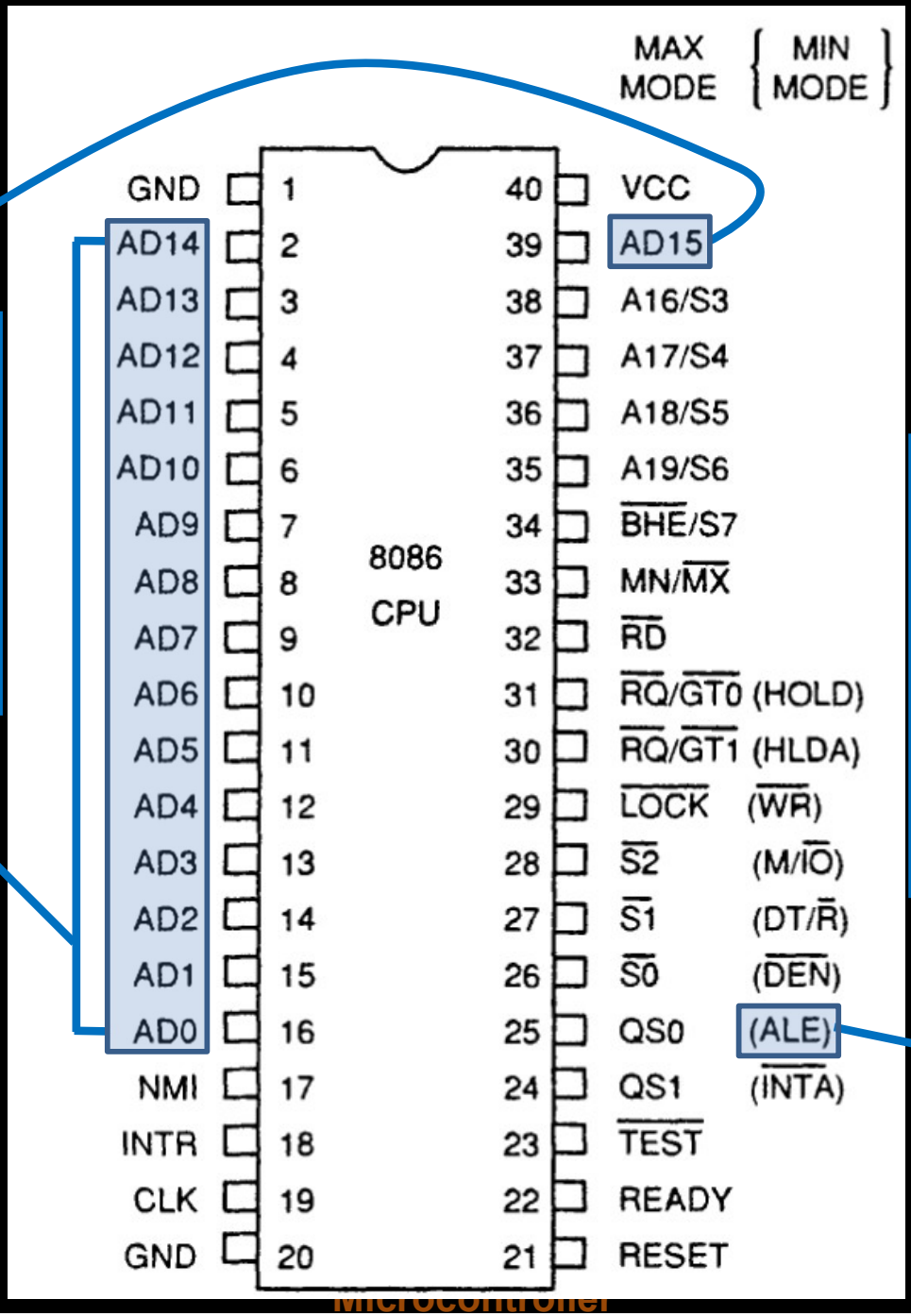
Clock

Timing signal

INTEL 8086 - Pin Details

Address/Data Bus:

Contains address bits A_{15}-A_0 when ALE is 1 & data bits D_{15} – D_0 when ALE is 0.

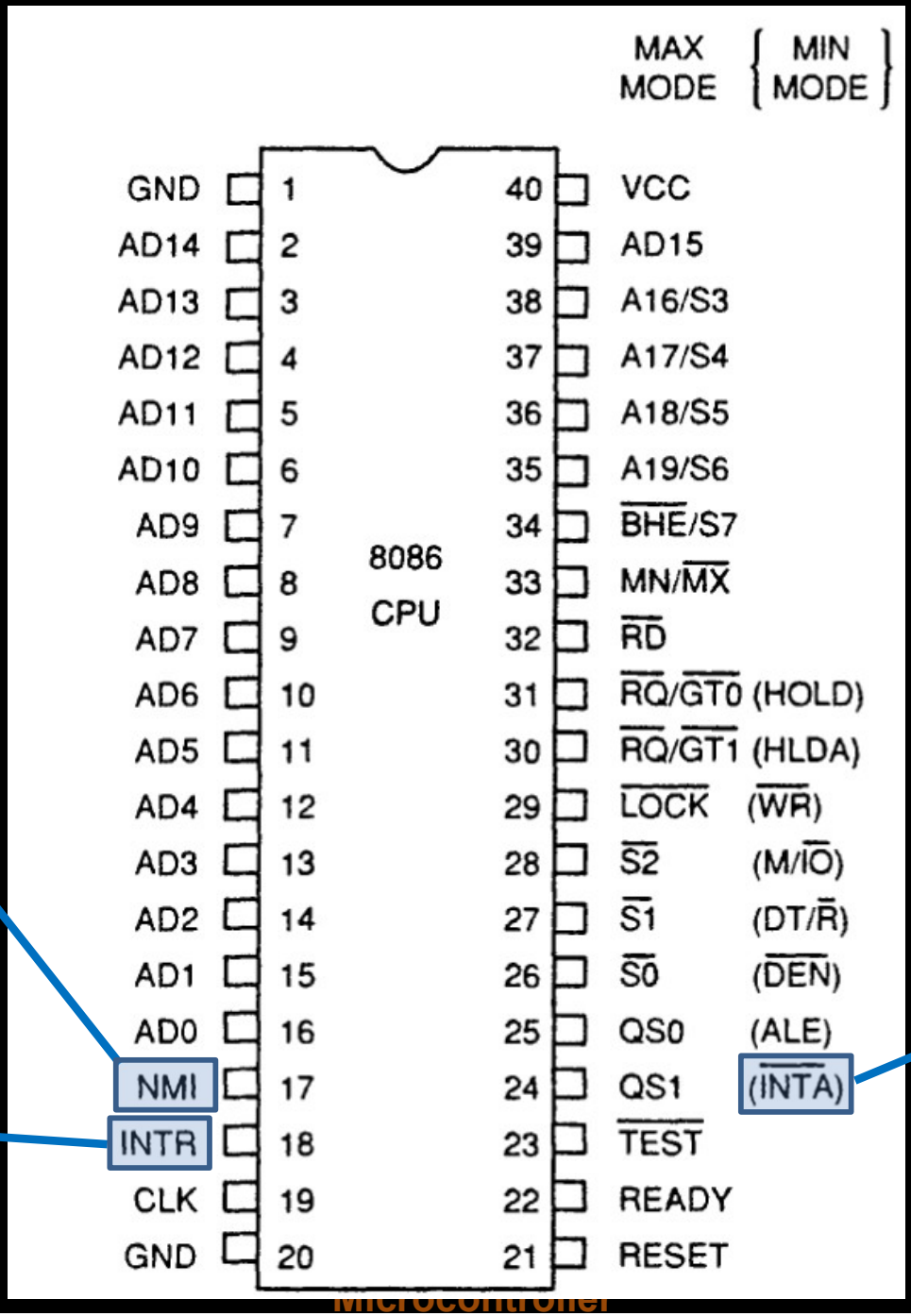


Address Latch Enable:

When high, multiplexed address/data bus contains address information.

INTEL 8086 - Pin Details

INTERRUPT

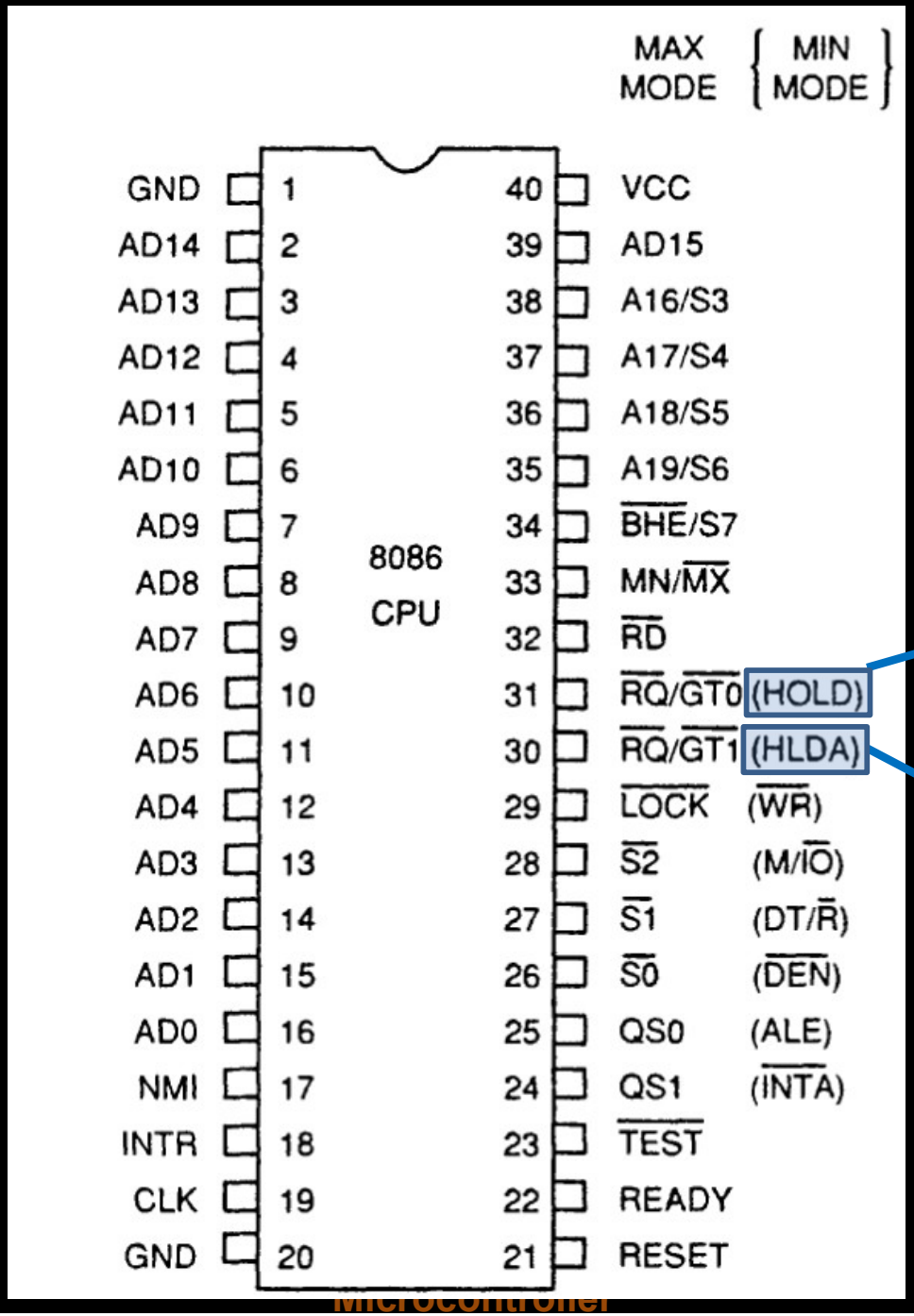


Non - maskable interrupt

Interrupt request

Interrupt acknowledge

INTEL 8086 - Pin Details



Direct Memory Access

Hold

Indicates the other master requesting for bus access

Hold acknowledge

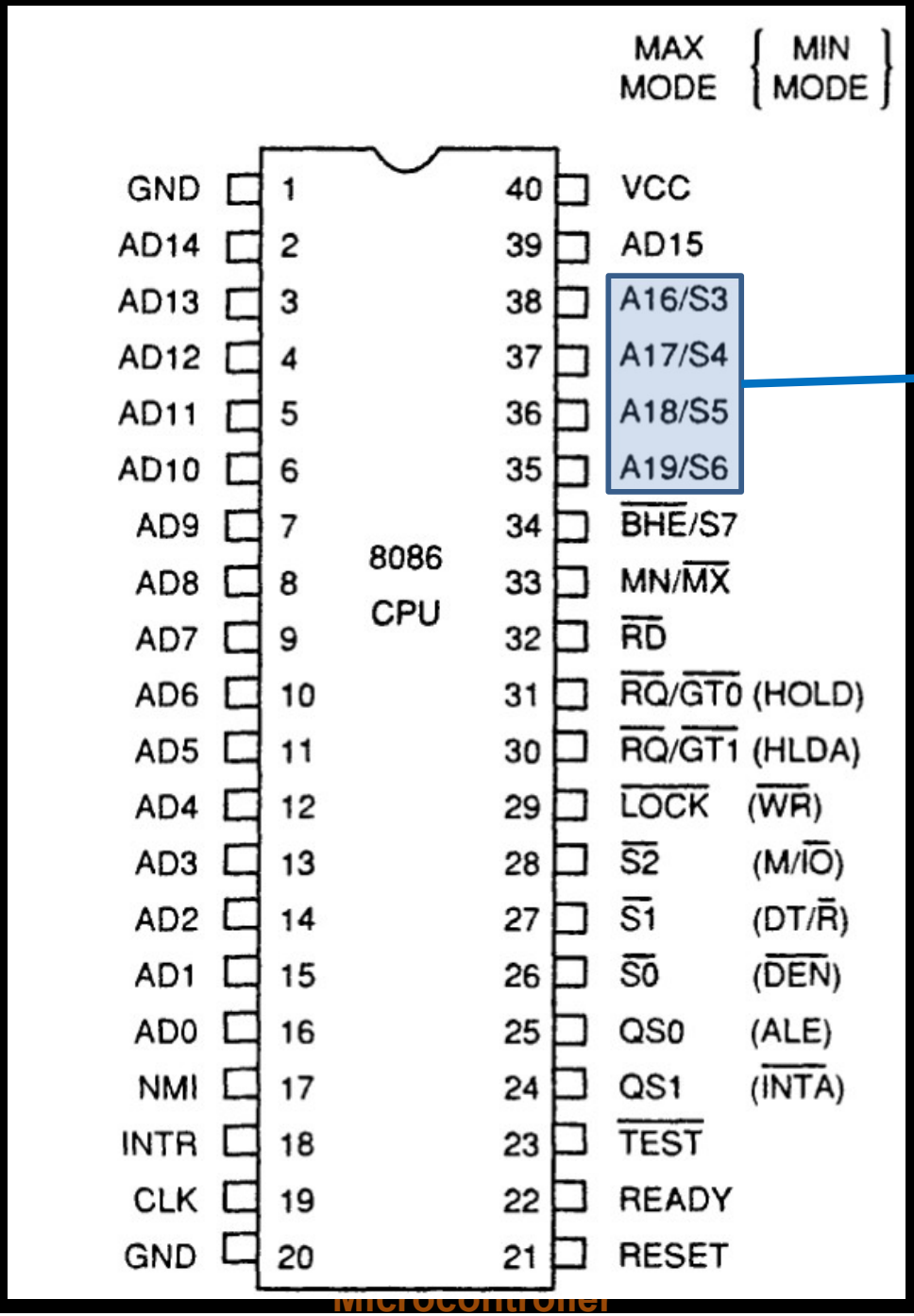
INTEL 8086 - Pin Details

S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:

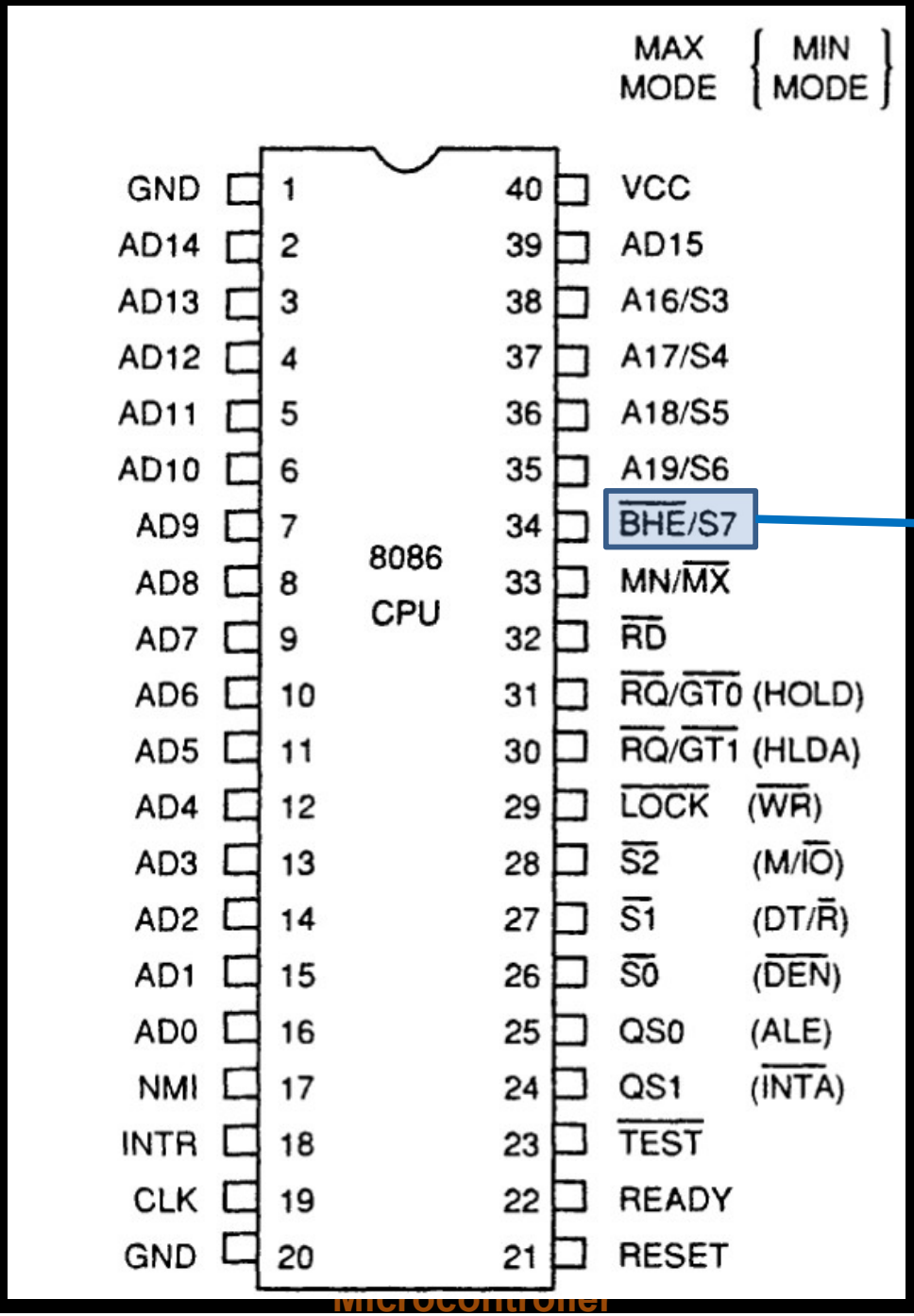
S4	S3	Function
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



Address/Status Bus

Address bits A_{19} – A_{16} & Status bits S_6 – S_3

INTEL 8086 - Pin Details

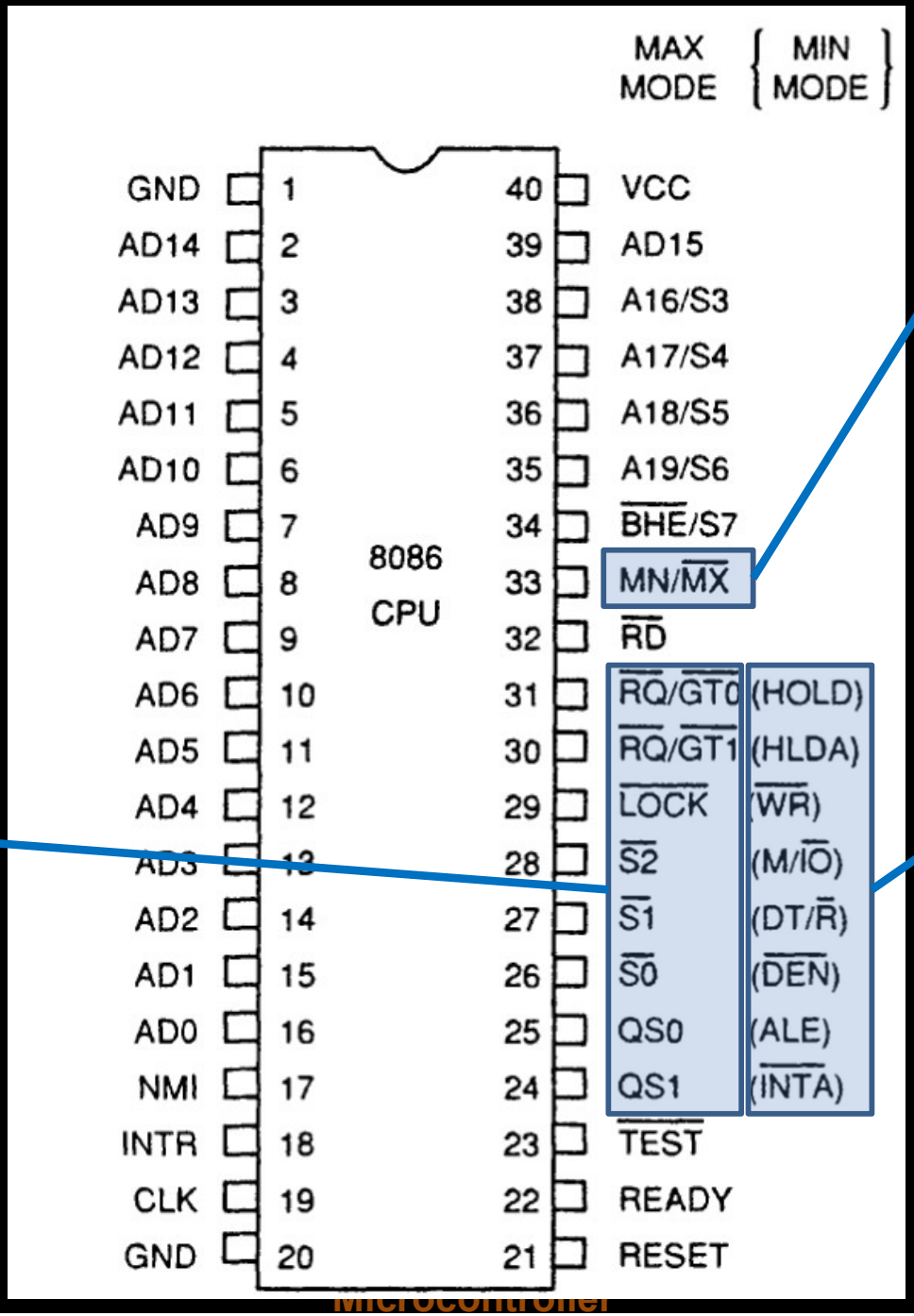


Bus High Enable/S7

Enables most significant data bits $D_{15} – D_8$ during read or write operation.

S_7: Always 1.

INTEL 8086 - Pin Details



Min/Max mode

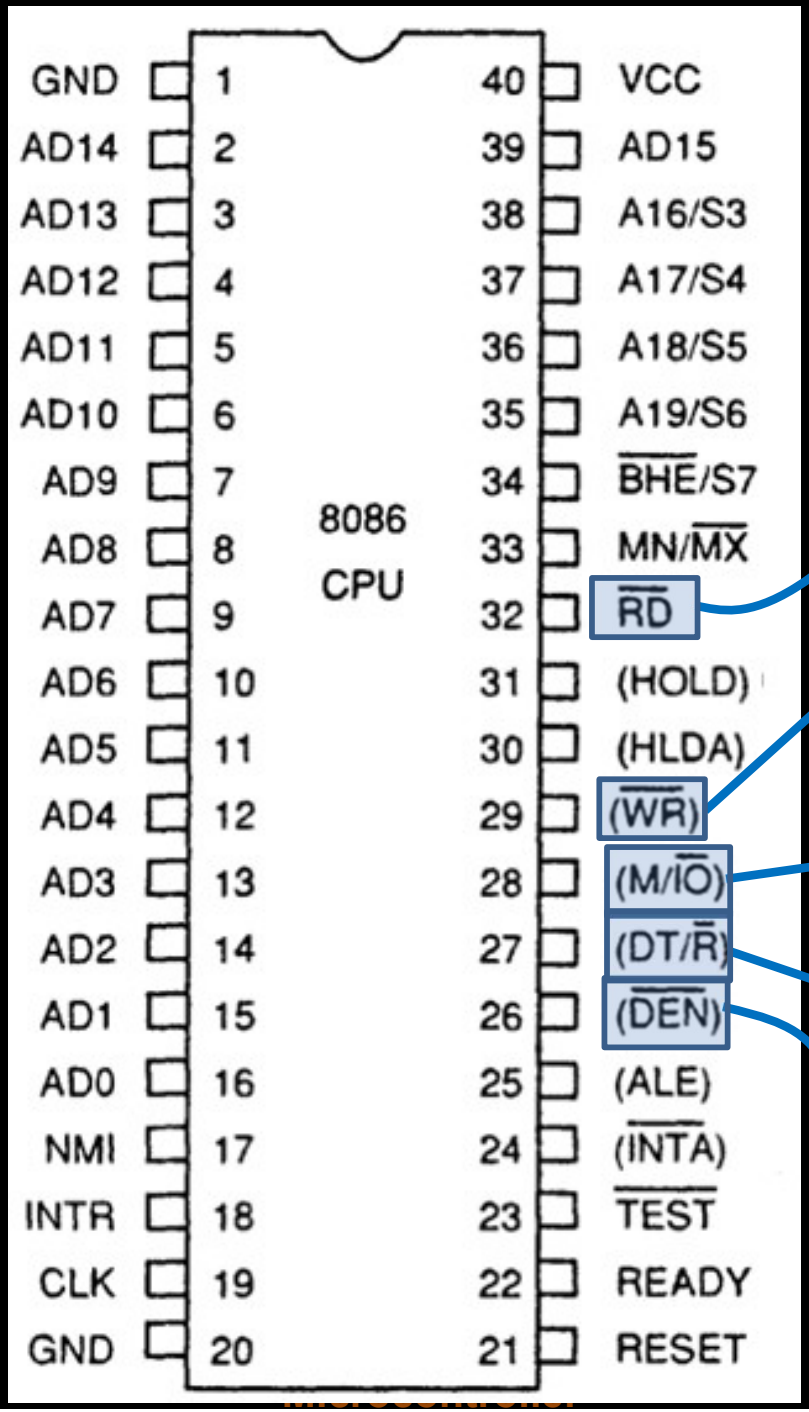
Minimum Mode: +5V

Maximum Mode: 0V

Minimum Mode Pins

Maximum Mode Pins

Minimum Mode- Pin Details



Read Signal

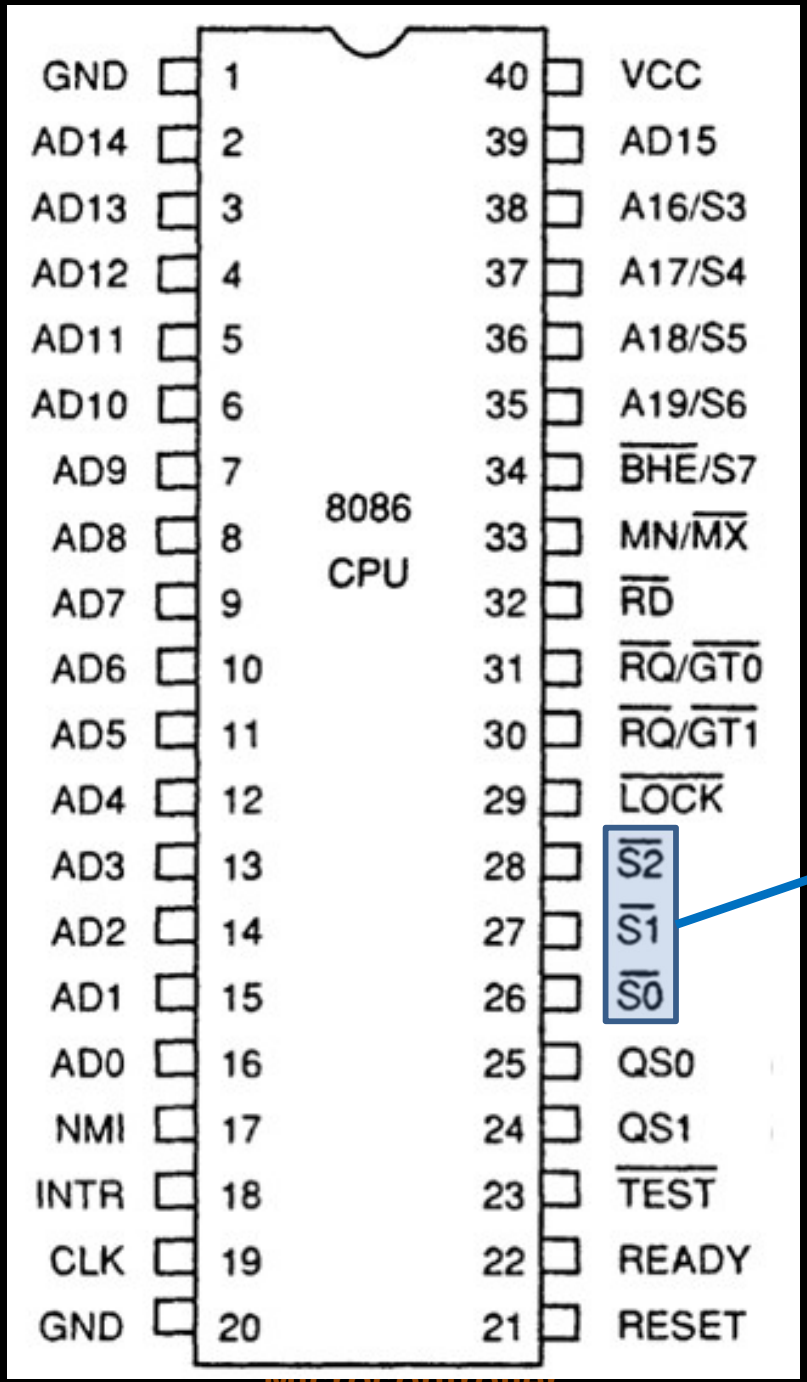
Write Signal

Memory or I/0

Data Transmit/Recei

Data Bus

Maximum Mode - Pin Details



S2 S1 S0

000: INTA
001: read I/O port
010: write I/O port
011: halt
100: code access
101: read memory
110: write memory
111: none -passive

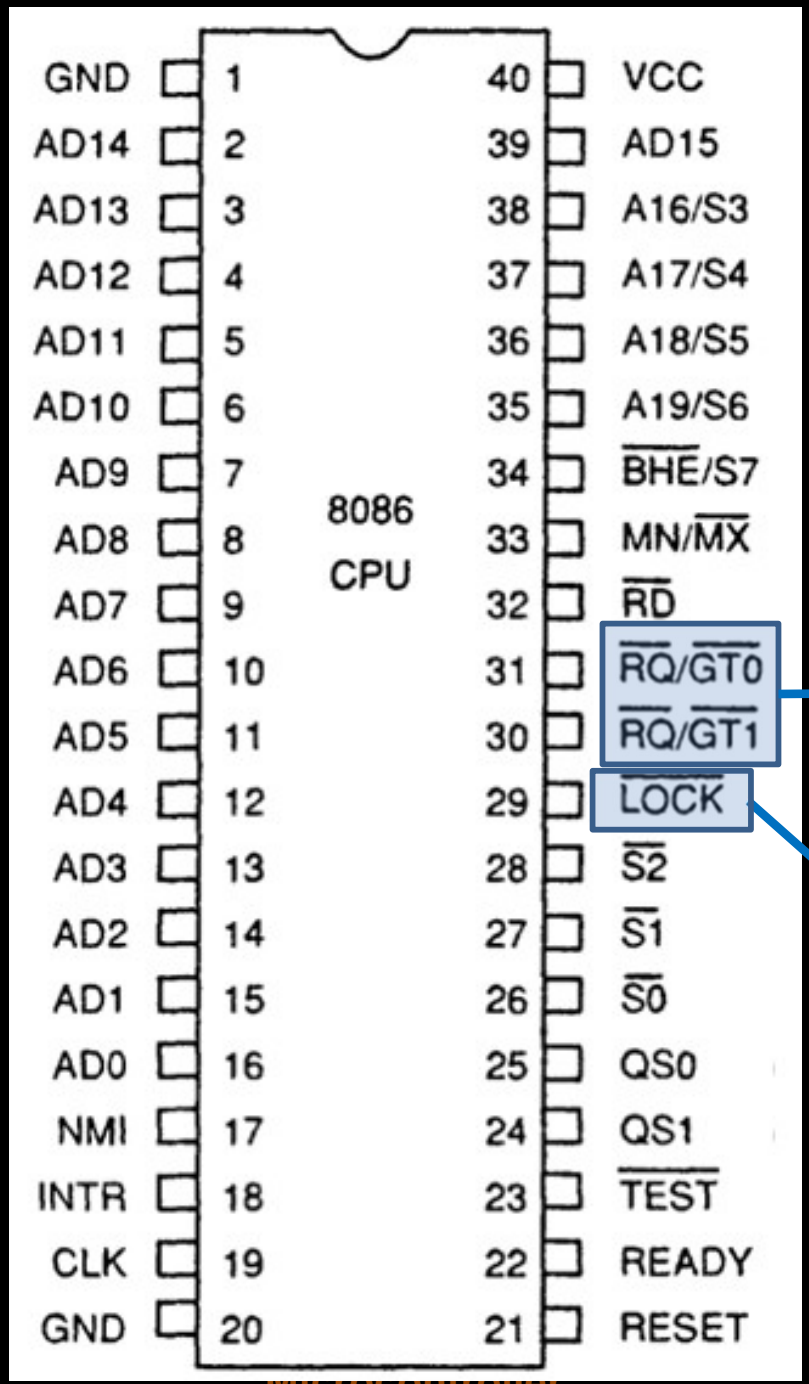
Status Signal

Type of operation being carried out by the processor.

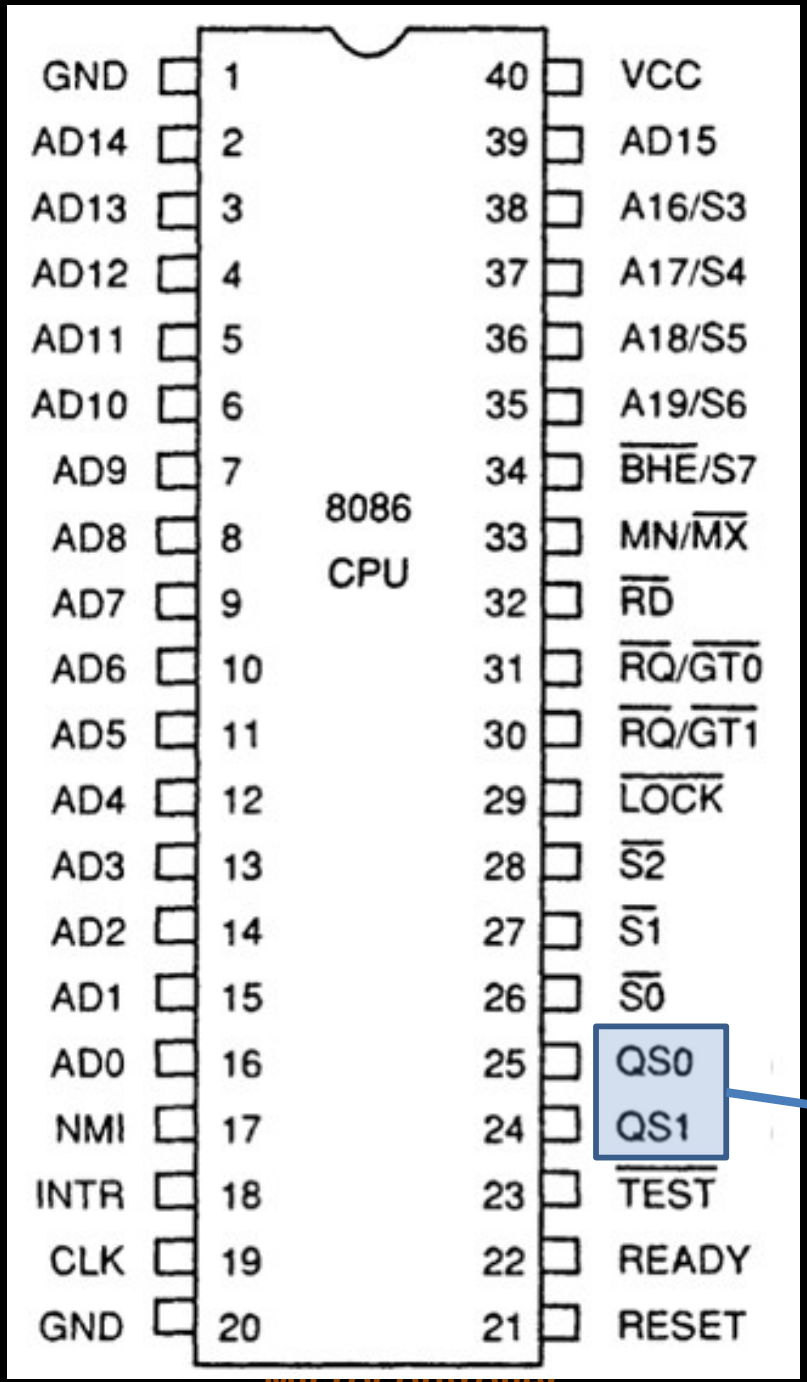
Maximum Mode - Pin Details

Lock Output

Used to lock the peripherals from gaining the system bus, when it is 0.



Maximum Mode - Pin Details



QS1 QS0

00: Queue is idle

01: First byte of opcode

10: Queue is empty

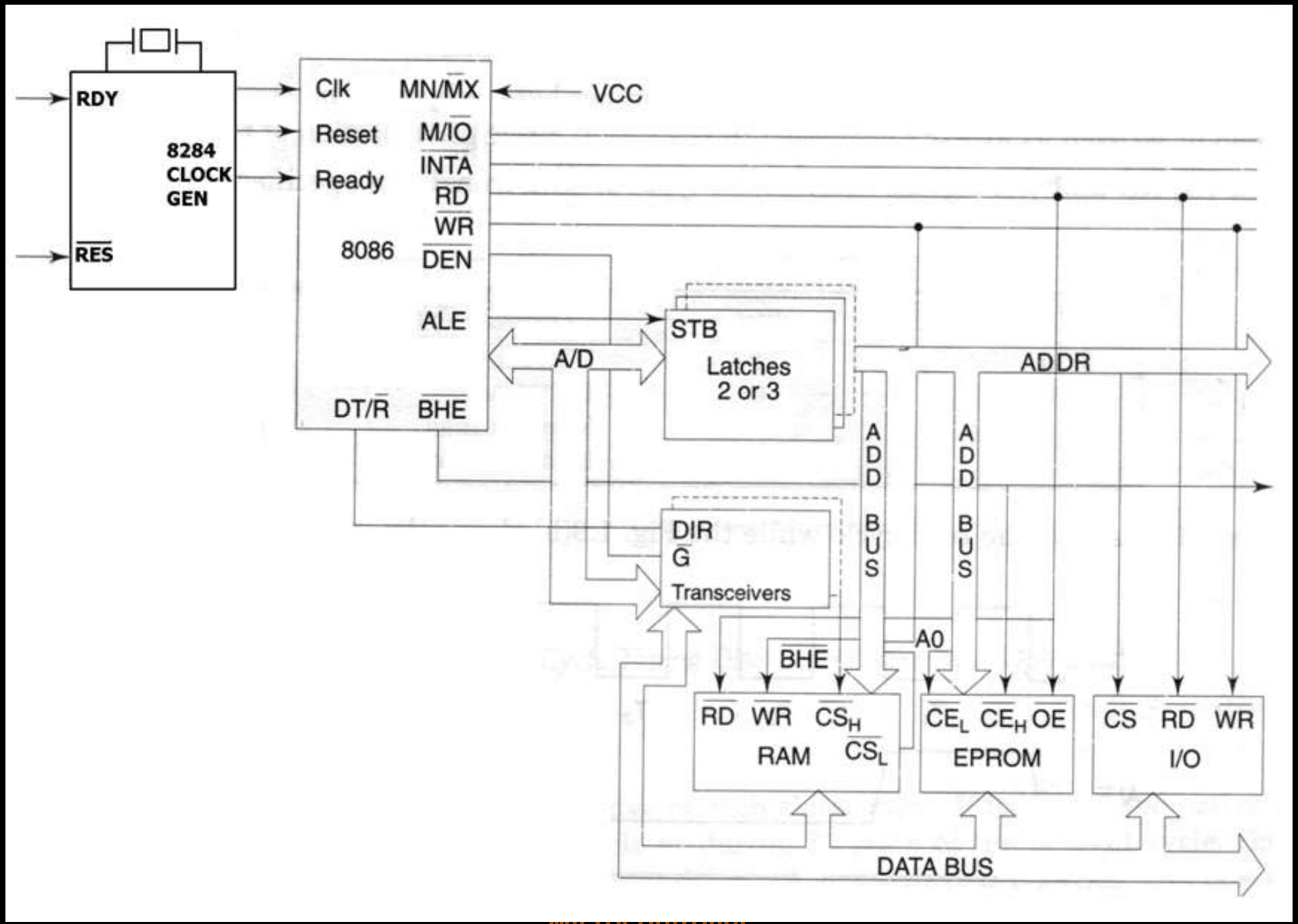
11: Subsequent byte of opcode

Queue Status

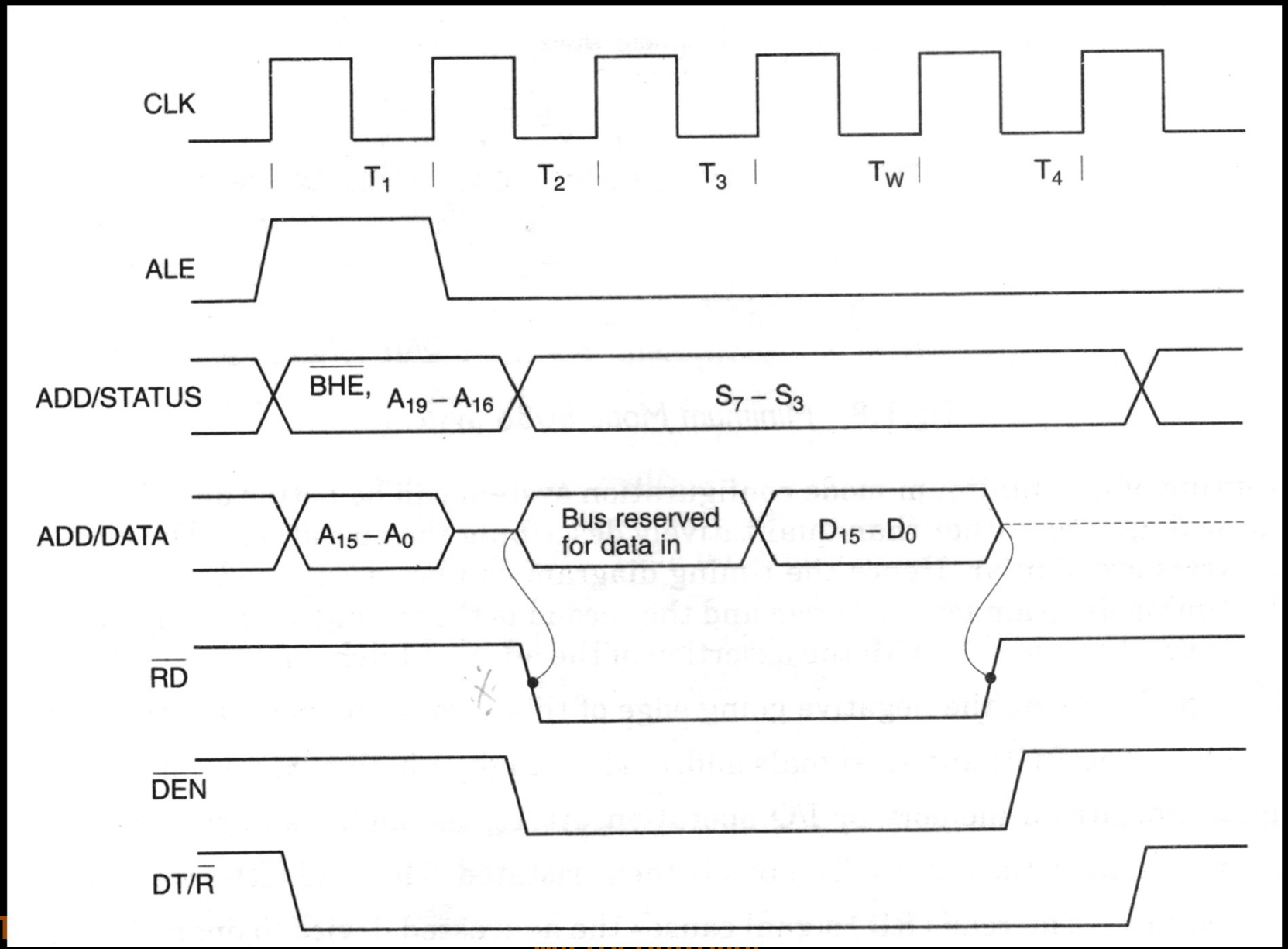
Indicates the status of code-prefetch queue

- TEST’: If this pin is 0,execution will continue, else, processor is in idle state. it is a active low signal.
- READY:it is a active high signal.it indicates ready for data transfer,when this pin is high.

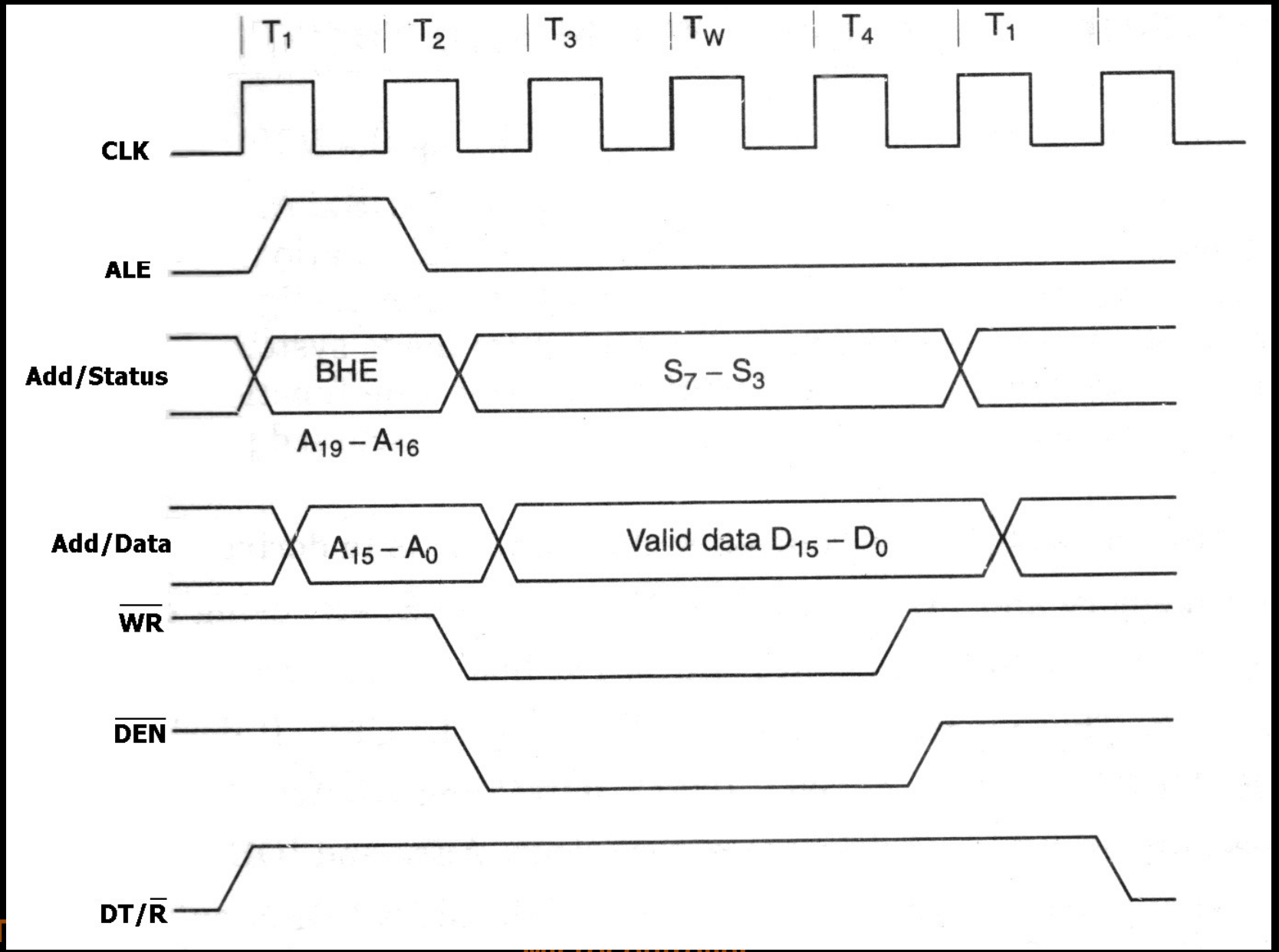
Minimum Mode 8086 System



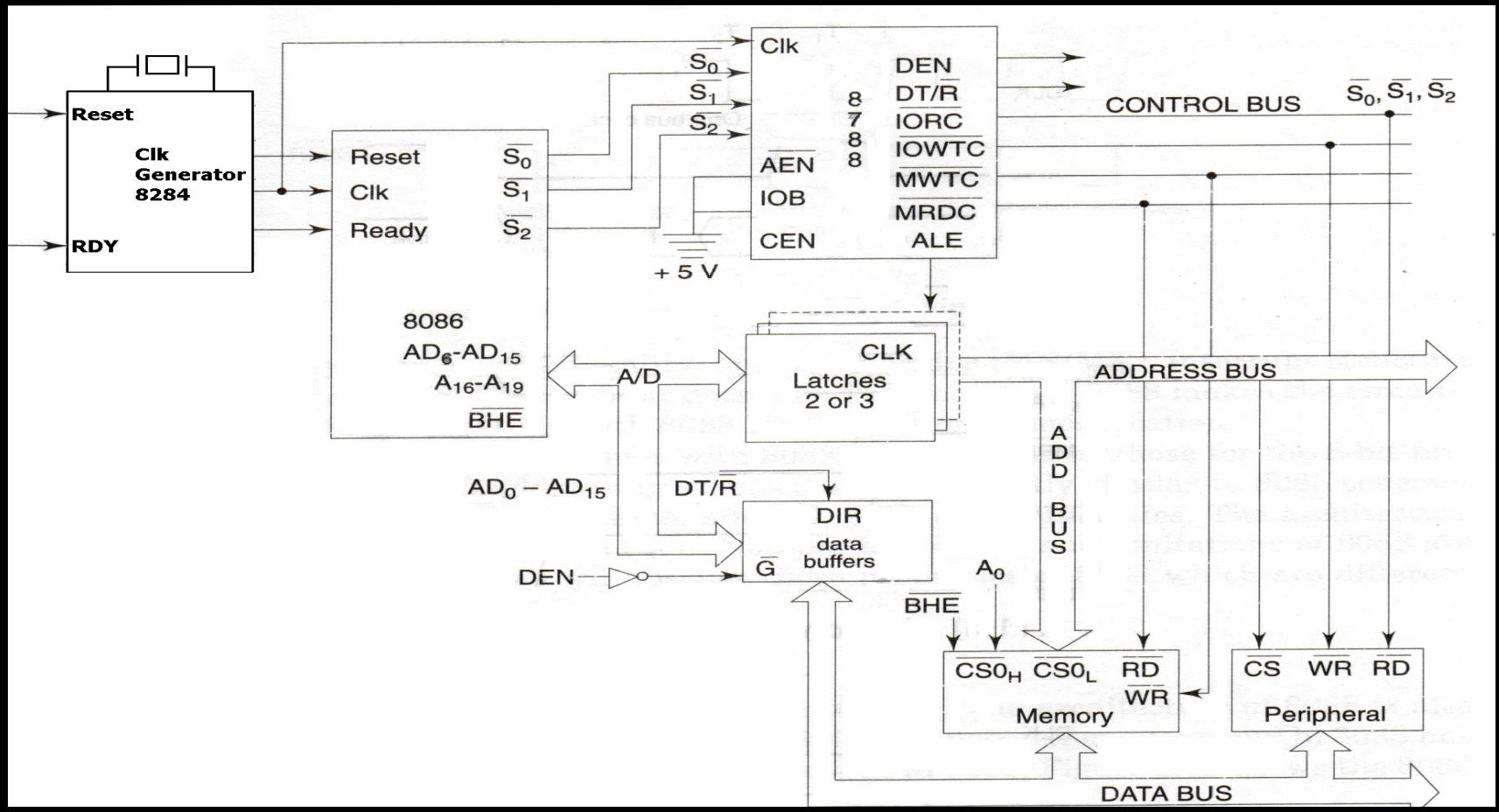
‘Read’ Cycle timing Diagram for Minimum Mode



‘Write’ Cycle timing Diagram for Minimum Mode



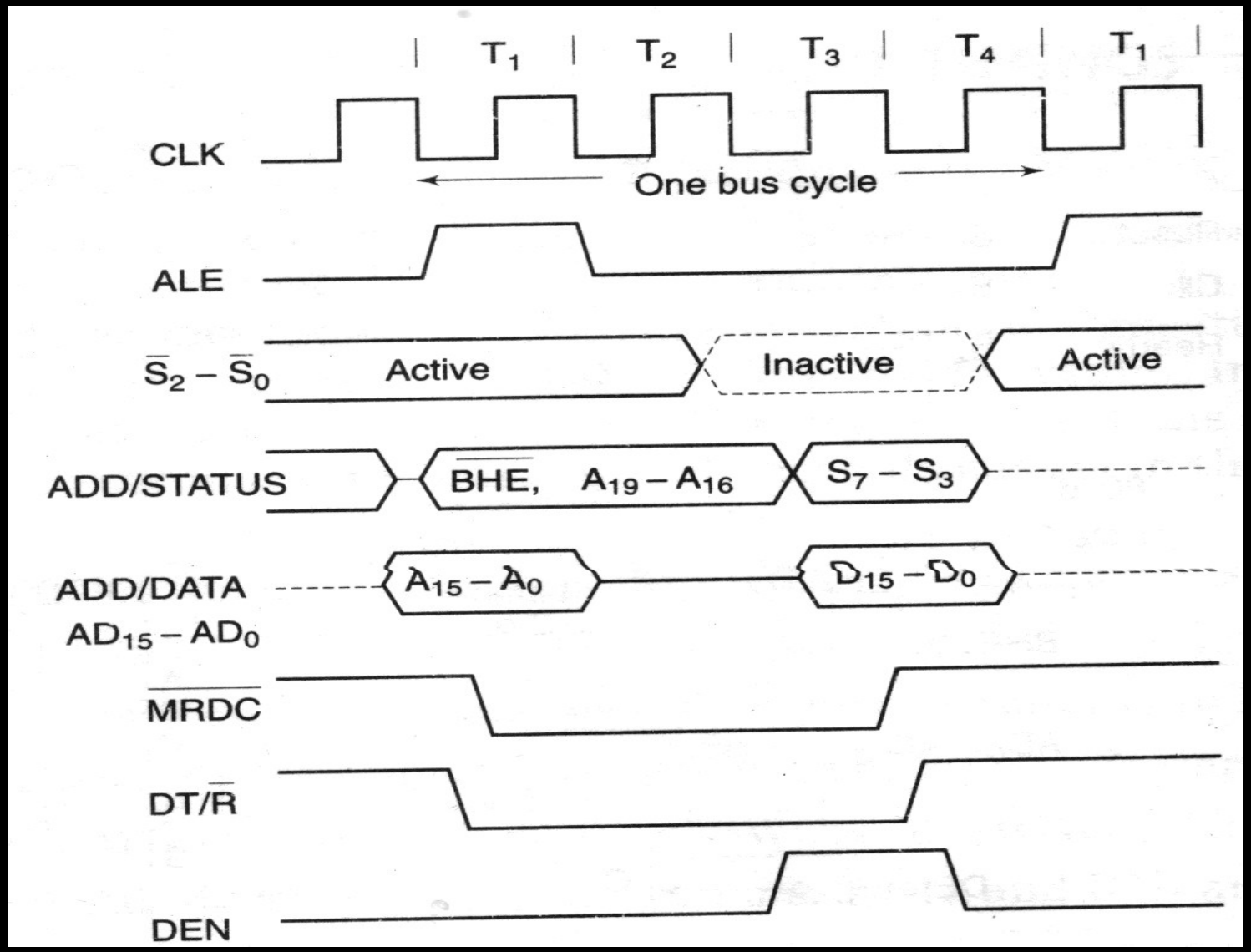
Maximum Mode 8086 System



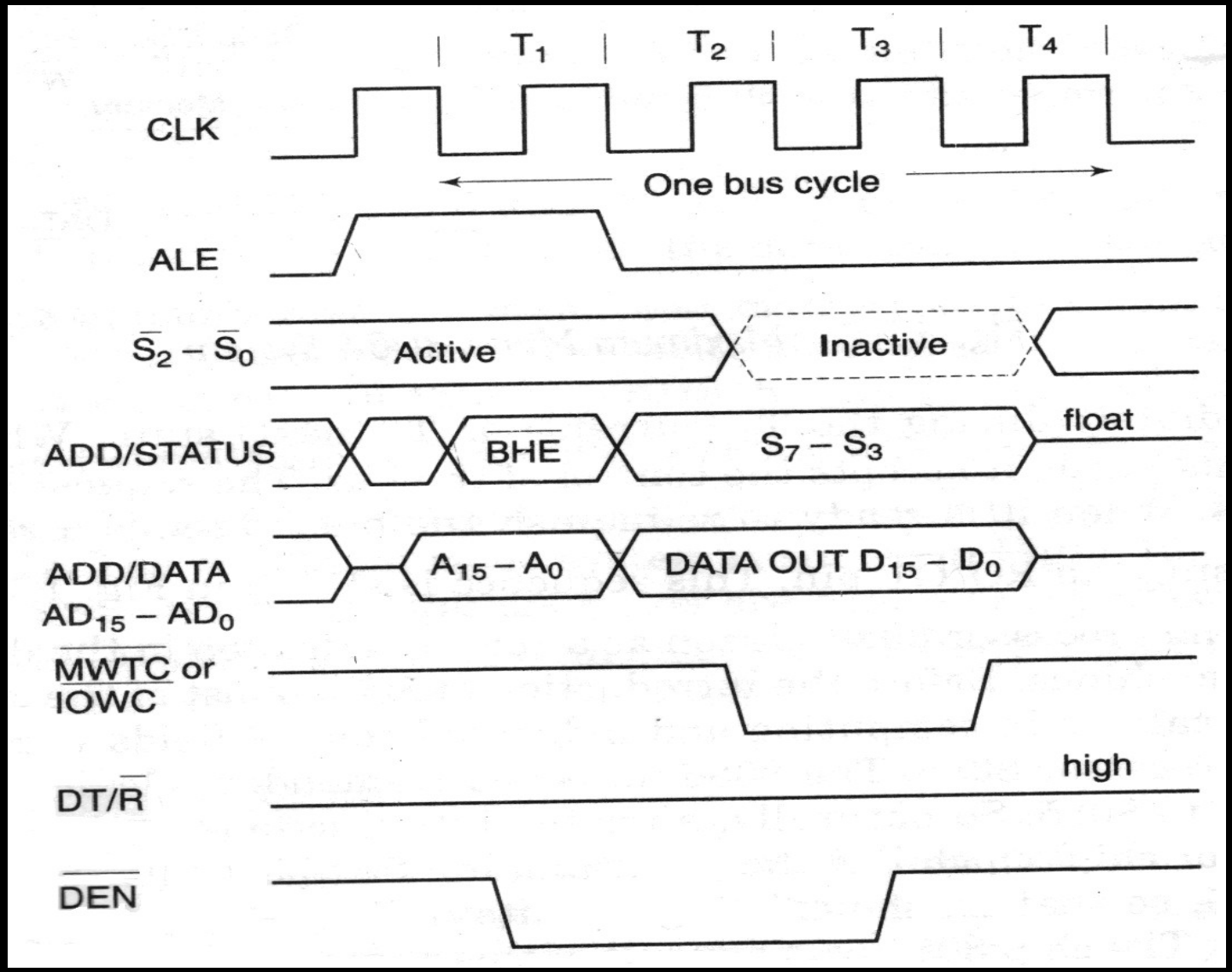
Maximum Mode 8086 System

- Here, either a numeric coprocessor of the type 8087 or another processor is interfaced with 8086.The Memory, Address Bus, Data Buses are shared resources between the two processors.
- The control signals for Maximum mode of operation are generated by the Bus Controller chip 8788. The three status outputs S0', S1', S2' from the processor are input to 8788.
- The outputs of the bus controller are the Control Signals, namely DEN, DT/R', IORC', IOWTC', MWTC', MRDC', ALE etc.

Memory Read timing in Maximum Mode



Memory Write timing in Maximum Mode



Memory Interfacing

Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{09}	A_{08}	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
						EPROM						8K × 8								
FE000H	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
FDFFFH	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
						RAM						8K × 8								
FC000H	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Memory Interfacing

Table 5.2 *Memory Chip Selection for Problem 5.1*

Decoder I/P → *Address/$\overline{BHE}$ →*	A_2 A_{13}	A_1 A_0	A_0 $\overline{BHE}$	*Selection/ Comment*
Word transfer on $D_0 - D_{15}$	0	0	0	Even and odd addresses in RAM
Byte transfer on $D_7 - D_0$	0	0	1	Only even address in RAM
Byte transfer on $D_8 - D_{15}$	0	1	0	Only odd address in RAM
Word transfer on $D_0 - D_{15}$	1	0	0	Even and odd addresses in ROM
Byte transfer on $D_0 - D_7$	1	0	1	Only even address in ROM
Byte transfer on $D_8 - D_{15}$	1	1	0	Only odd address in ROM

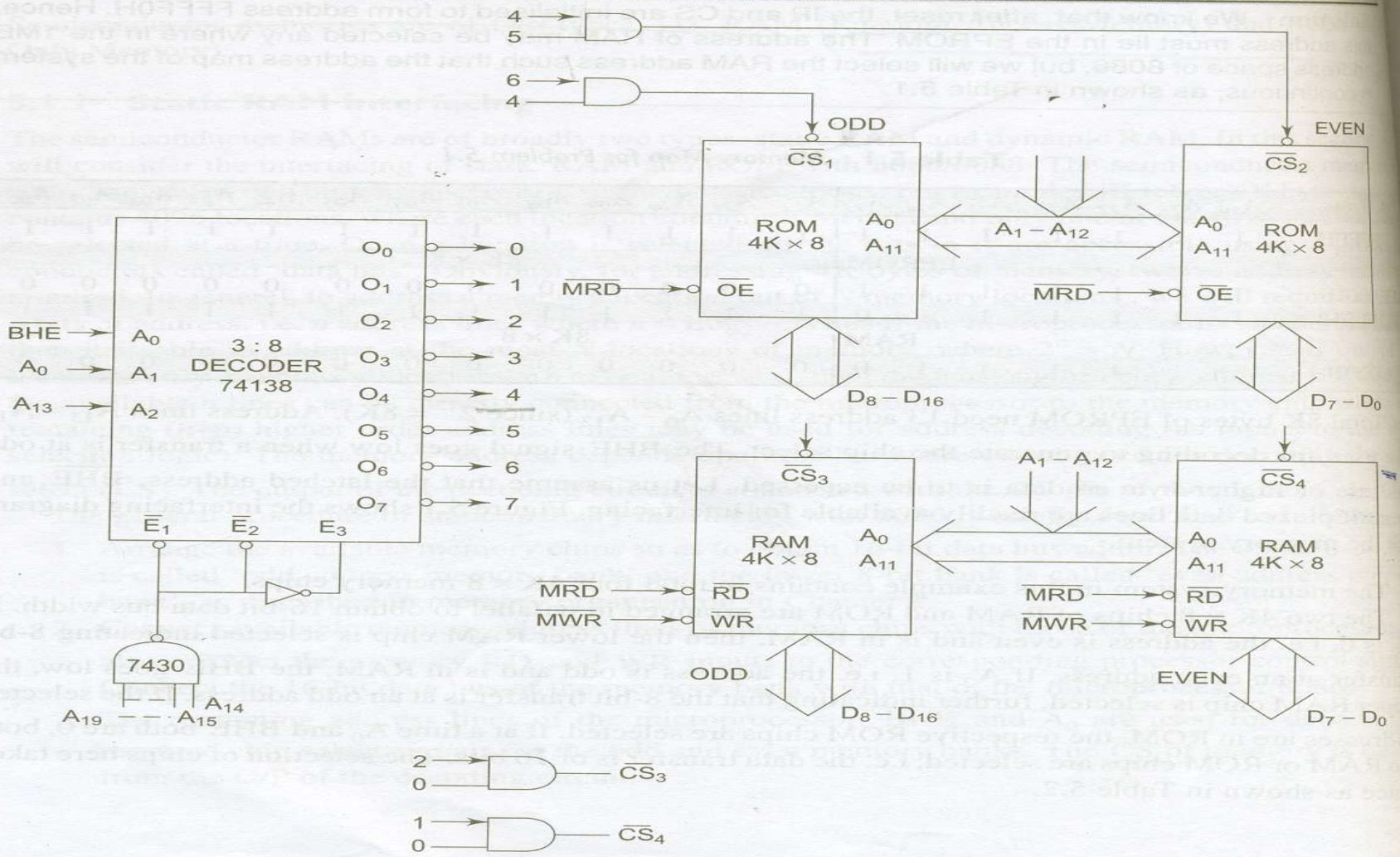


Fig. 5.1 *Interfacing Problem 5.1*

Memory Interfacing

Table 5.3 *Address Map for Problem 5.2*

Addresses	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{09}	A_{08}	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
						32KB EPROM														
F8000H	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0FFFFH	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
						64KB RAM														
00000H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

It is better not to use a decoder to implement the above map because it is not continuous, i.e. there is some unused address space between the last RAM address (0FFFFH) and the first EPROM address (F8000H). Hence the logic is implemented using logic gates, as shown in Fig. 5.2.

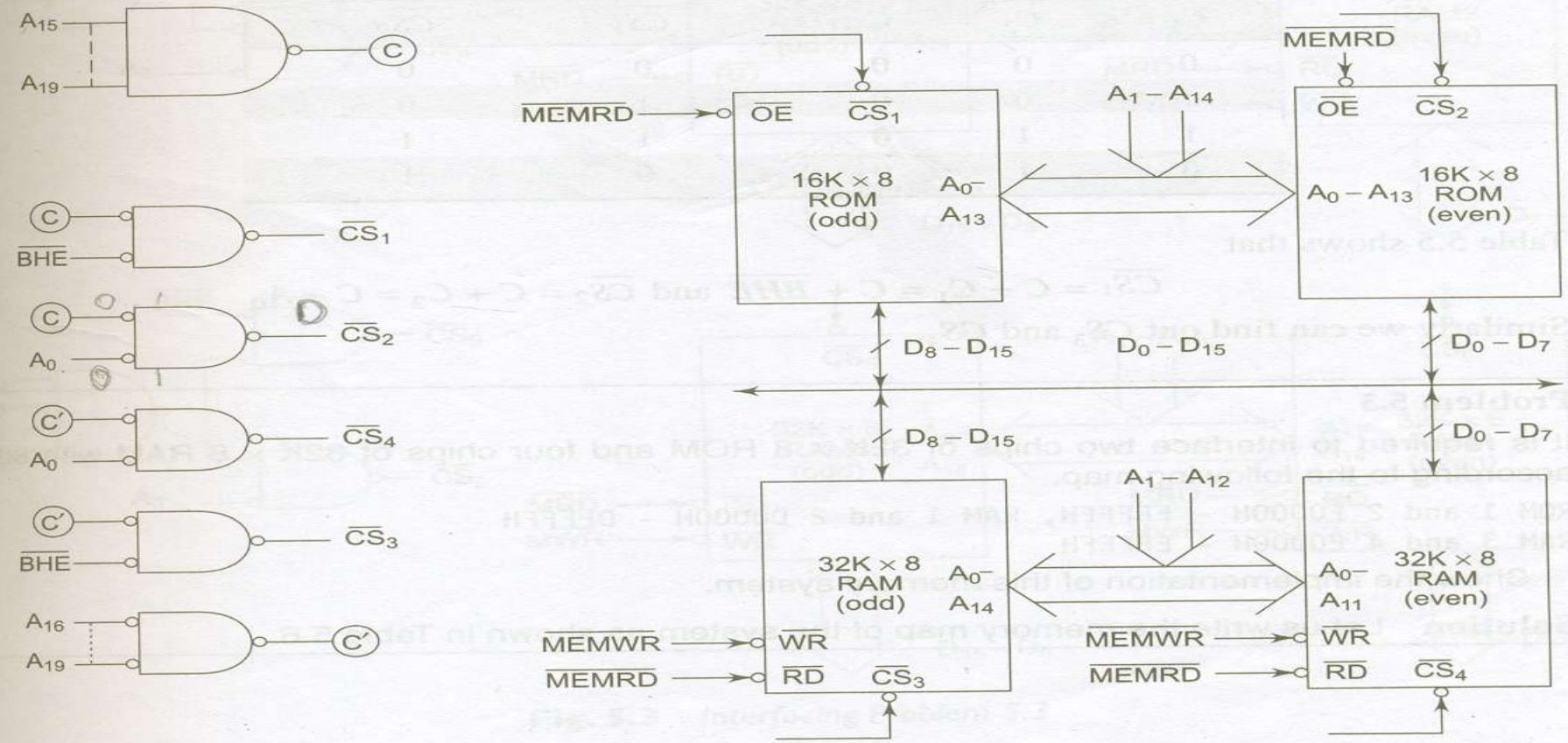


Fig. 5.2 *Interfacing Problem 5.2*

Memory Interfacing

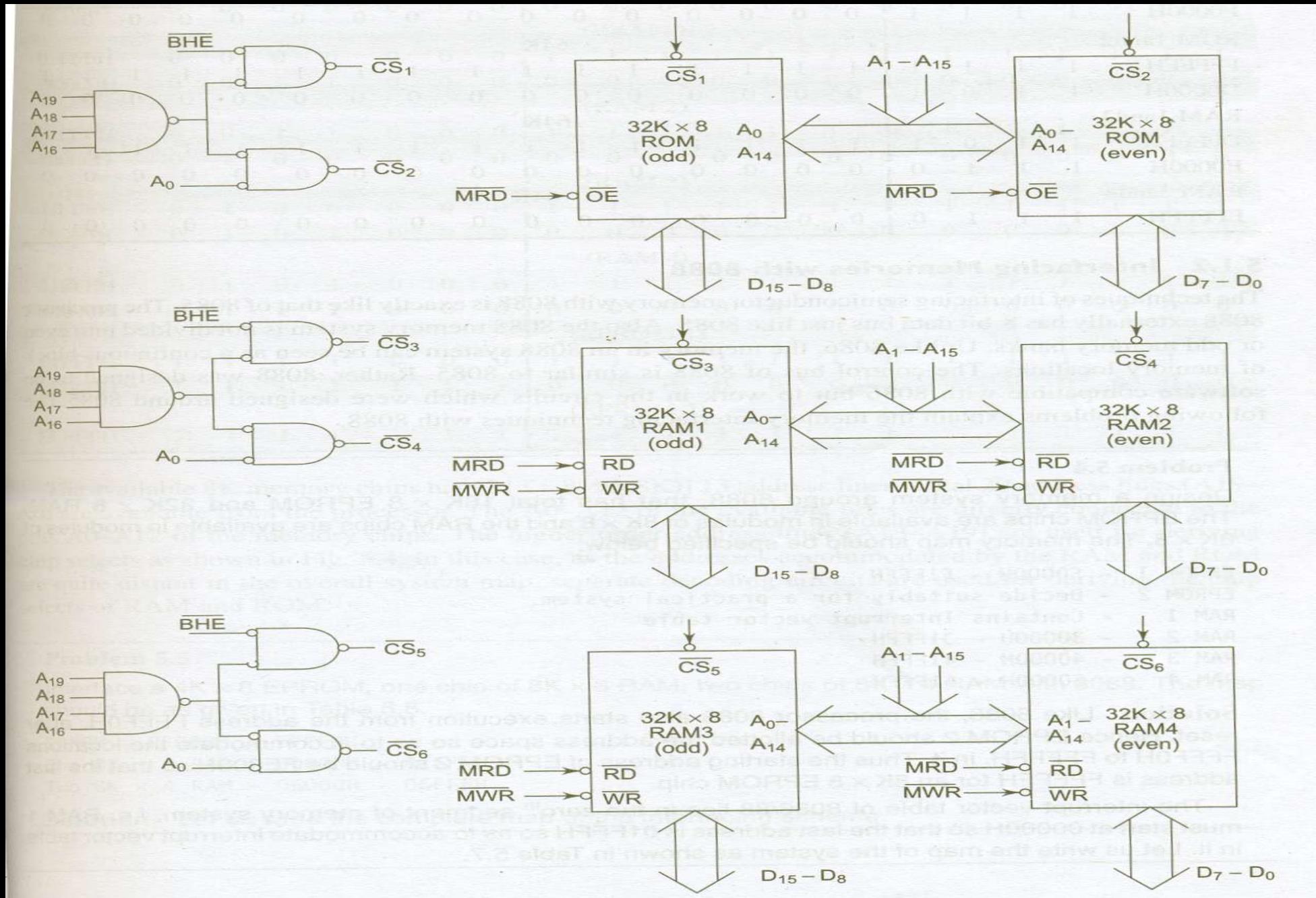


Fig. 5.3 *Interfacing Problem 5.3*