TCON Register in 8051 Microprocessor

The **TCON (Timer Control)** register in the 8051 microprocessor is an 8-bit register used to control and monitor the operation of the two timers/counters (Timer 0 and Timer 1) and the external interrupts (INT0 and INT1). It is a bit-addressable register, meaning each bit can be individually accessed and modified.

TCON Register Structure

The TCON register is organized as follows:

Bit	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware when Timer 1 overflows. Cleared by software or hardware.
6	TR1	Timer 1 Run Control Bit. Set to start Timer 1, cleared to stop Timer 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware when Timer 0 overflows. Cleared by software or hardware.
4	TR0	Timer 0 Run Control Bit. Set to start Timer 0, cleared to stop Timer 0.
3	IE1	External Interrupt 1 Edge Flag. Set by hardware when a falling edge is detected on INT1. Cleared by hardware when the interrupt is processed.
2	IT1	Interrupt 1 Type Control Bit. Set to enable edge-triggered interrupt on INT1, cleared for level-triggered interrupt.
1	IE0	External Interrupt 0 Edge Flag. Set by hardware when a falling edge is detected on INT0. Cleared by hardware when the interrupt is processed.
0	IT0	Interrupt 0 Type Control Bit. Set to enable edge-triggered interrupt on INT0, cleared for level-triggered interrupt.

Detailed Description of Each Bit

- **TF1 (Timer 1 Overflow Flag - Bit 7)**:
  - Set by hardware when Timer 1 overflows (i.e., when it rolls over from all 1s to all 0s).
  - Cleared by software or hardware when the interrupt is serviced.
- **TR1 (Timer 1 Run Control Bit - Bit 6)**:
  - Set to 1 to start Timer 1.
  - Cleared to 0 to stop Timer 1.
- **TF0 (Timer 0 Overflow Flag - Bit 5)**:

  - Set by hardware when Timer 0 overflows.
  - Cleared by software or hardware when the interrupt is serviced.

- **TR0 (Timer 0 Run Control Bit - Bit 4)**:
  - Set to 1 to start Timer 0.
  - Cleared to 0 to stop Timer 0.

- **IE1 (External Interrupt 1 Edge Flag - Bit 3)**:
  - Set by hardware when a falling edge is detected on the INT1 pin.
  - Cleared by hardware when the interrupt is processed.

- **IT1 (Interrupt 1 Type Control Bit - Bit 2)**:
  - Set to 1 to enable edge-triggered interrupt on INT1.
  - Cleared to 0 for level-triggered interrupt on INT1.

- **IE0 (External Interrupt 0 Edge Flag - Bit 1)**:
  - Set by hardware when a falling edge is detected on the INT0 pin.
  - Cleared by hardware when the interrupt is processed.

- **IT0 (Interrupt 0 Type Control Bit - Bit 0)**:
  - Set to 1 to enable edge-triggered interrupt on INT0.
  - Cleared to 0 for level-triggered interrupt on INT0.

Usage of TCON Register

- **Timer Control**: The TR0 and TR1 bits are used to start or stop Timer 0 and Timer 1, respectively. The TF0 and TF1 bits indicate overflow conditions for the timers.
- **Interrupt Control**: The IT0 and IT1 bits determine whether the external interrupts (INT0 and INT1) are edge-triggered or level-triggered. The IE0 and IE1 flags indicate the occurrence of an interrupt.

In summary, the TCON register is a critical control register in the 8051 microprocessor for managing timers and external interrupts. It allows the programmer to control the operation of timers and configure the behavior of external interrupts.