JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

Homework 10

Assigned: July 27, 2017

Due: August 3, 2017, at the beginning of the class.

The homework should be submitted in hard copies.

1. Problem 5.26 (10+5+5 points)

5.26 (a) Convert the laser-based distance measurer's FSM in Figure 5.26 to a state register and logic. (b) Assuming all gates have a delay of 2 ns and the 16-bit up-counter has a delay of 5 ns, and wires have no delay, determine the critical path for the laser-based distance measurer. (c) Calculate the corresponding maximum clock frequency for the circuit.

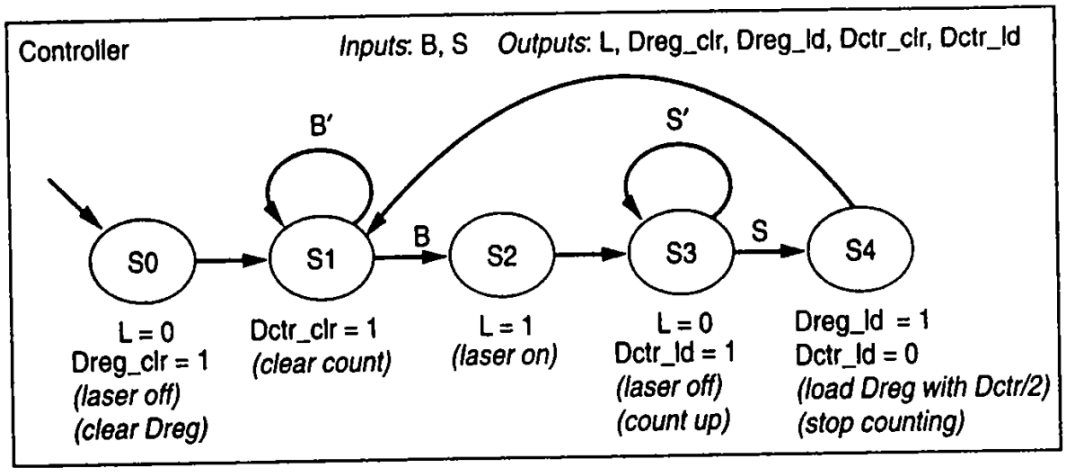
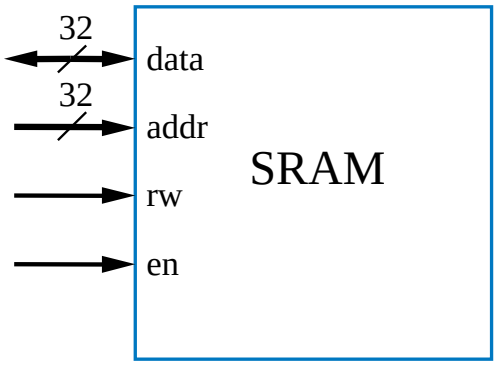


Figure 5.26 FSM description of the controller for the laser-based distance measurer, using the convention that FSM outputs not explicitly assigned a value in a state are implicitly assigned 0.

2. Given an SRAM block,



If the memory is byte addressable (each byte has an address), how many **bits** in maximum can the SRAM block have? (10 points)

3. Problem 5.37 (5 points)

5.37 Calculate the approximate number of SRAM bit storage cells that will fit on an IC with a capacity of 10 million transistors.

4. Problem 5.38 (5 points)

5.38 Summarize the main differences between DRAM and SRAM memories.

5. Problem 5.42 (5 points)

5.42 Summarize the main differences between EEPROM and flash memories.

6. Problem 5.43 (30 points)

5.43 Use an HLSM to capture the design of a system that can save data samples and then play them back. The system has an 8-bit input D where data appears. A single-bit input S changing from 0 to 1 requests that the current value on D (i.e., a sample) be saved in a nonvolatile memory. Sample requests will not arrive faster than once per 10 clock cycles. Up to 10,000 samples can be saved, after which sampling requests are ignored. A single-bit input P changing from 0 to 1 causes all recorded samples to be played back—i.e., to be written to an output Q one sample at a time in the order they were saved at a rate of one sample per clock cycle. A single-bit input R resets the system, clearing all recorded samples. During playback, any sample or reset request is ignored. At other times, reset has priority over a sample request. Choose an appropriate size and type of memory, and declare and use that memory in your HLSM.

7. Problem 7.20 (15 points)

7.20 Show how to implement on two 3-input 2-output lookup tables the following function: `F(a, b, c, d) = a'bd + b'cd'`. Assume the two lookup tables are connected in the manner shown in Figure 7.47. You may not need to use every lookup table output.

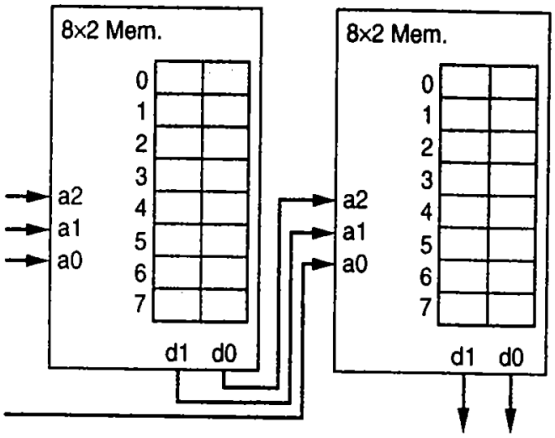


Figure 7.47 Two 3-input 2-output lookup tables implemented using 8x2 memory.

8. Use one 4-input LUT to implement the following Boolean function (10 points)

f = x2x3'x4' + x1'x2x4 + x1'x2x3 + x1x2x3