JOINT INSTITUTE
交大密西根学院

**Ve270 Introduction to Logic Design**

# Homework 6

**Assigned: June 22, 2017**

**Due: June 29, 2017, at the beginning of the class.**

**The homework should be submitted in hard copies.**

1. Problem 4.2 (10 points)

4.2 Trace the behavior of an 8-bit parallel-load register with 8-bit input *I*, 8-bit output *Q*, load control input `ld`, and synchronous clear input `clr` by completing the timing diagram in Figure 4.96.

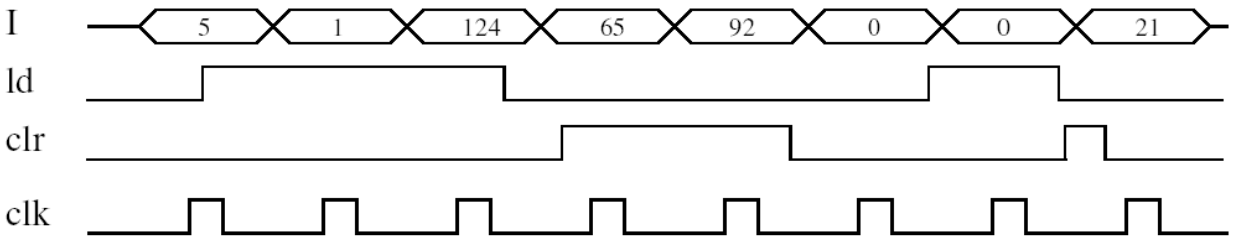


Figure 4.96

2. Problem 4.3, using components to draw schematic (20 points)

4.3 Design a 4-bit register with 2 control inputs `s1` and `s0`; 4 data inputs `I3`, `I2`, `I1`, and `I0`; and 4 data outputs `Q3`, `Q2`, `Q1`, and `Q0`. When `s1s0=00`, the register maintains its value. When `s1s0=01`, the register loads `I3...I0`. When `s1s0=10`, the register clears itself to `0000`. When `s1s0=11`, the register complements itself, so for example, `0000` would become `1111`, and `1010` would become `0101`. (*Component design problem.*)

3. Problem 4.46. Draw schematic. (20 Points).

4.46 Design a special multiplier circuit that can multiply its 16-bit input by 2, 4, 8, 16, or 32, specified by three inputs `a`, `b`, `c` (`abc=000` means no multiply, `abc=001` means multiply by 2, `abc=010` means by 4, `abc=011` means by 8, `abc=100` means by 16, `abc=101` means by 32). *Hint:* A simple solution consists entirely of just one copy of a component from this chapter. *(Component use problem.)*

4. Problem 4.57. Draw schematic (a), (b). (20 points)

4.57 Design a circuit that outputs a 1 every 99 clock cycles:
(a) Using an up-counter with a synchronous clear control input, and using extra logic,
(b) Using a down-counter with parallel load, and using extra logic.

5. Design a circuit called Receiver that receives two single bit signals, **Valid** and **Data_in**, from another device called Transmitter. The **Valid** signal sent from the Transmitter will be a 1-clock cycle pulse. The first bit of **Data_in** comes at the same time as **Valid**. Once the Receiver detects the **Valid** pulse, it will start receiving 8 bits through port **Data_in**, bit by bit. After the 8 bits of information is received, it should be copied into another 8-bit register called **RxReg**. Draw the schematic on component level (30 Points).