JOINT INSTITUTE
交大密西根学院

Ve 270 Introduction to Logic Design

Lab 4
Design of a Counter

UM-SJTU Joint Institute
Shanghai Jiao Tong University
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1. Objective

- To understand and design a special FSM – Counter.
- To design the counter by drawing schematics
- To design the counter by HDL modeling
- To experience the development process of an FPGA based digital device using HDL.

2. Requirement

In this lab, you are to design a device commonly used in modern computers, a 4-bit up/down synchronous binary counter. The counter is defined as follows:

- A 4-bit binary counter uses 4 flip-flop outputs to represent a binary number. It is capable of counting from 0 to 15.
- A synchronous counter implies that all flip-flops are sharing the same clock signal.
- An up/down counter is capable of counting up (incrementing) or down (decrementing).

The counter has two 1-bit control inputs called "Up/Down" and "Reset". The counter is to increment if "Up/Down" is 1 and decrement if "Up/Down" is 0. When "Reset" is 1 the counter should go to 0 no matter what the other inputs might be. "Up/Down" input can be provided with a toggle switch. The "Reset" input can be provided with a push button.

Another input to the counter is "Clock". Rising edges of "Clock" should trigger increment or decrement of the counter. "Clock" can be provided with a push button. Thus, each button press produces a rising edge. **NOTE**: sometimes the Xilinx ISE software doesn't accept a regular input port used for a clock signal. In that case, a special buffer "ibufg" in the "IO" category needs to be inserted in between the I/O Marker and the input of a device.

The outputs of 4 flip-flops should be used to show the binary number the counter is counting to. They should be connected to 4 LEDs on the FPGA board. Each time the button for "Clock" is pushed, the output number is incremented or decremented by one.

3. Draw Schematics

Draw the circuitry for the counter using Xilinx ISE schematic capture tool. It's highly suggested to use Macro for each functional block.

4. Simulation, Synthesis, and FPGA Implementation

Simulate your circuit using Xilinx ISE. Synthesize and implement your design on the Nexys2 FPGA board.

5. HDL Modeling

Now you are to repeat the design of the same 4-bit up/down synchronous binary counter. But the entire circuit must be modeled with Verilog HDL.

NOTE: the "Clock" signal can be connected to a push button or any other regular input source directly, if the circuit is modeled in HDL.

The outputs of the counter should be captured with 4 LEDs on the FPGA board, **and also supplied to an SSD Driver modeled with Verilog HDL so that the binary number is displayed in its hexadecimal equivalent**. Each time the button for "Clock" is pushed, the output number is incremented or decremented by one.

6. Simulation, Synthesis, and FPGA Implementation

Simulate and synthesize your circuit using Xilinx ISE. The procedures for simulation and synthesis are exactly the same as in Section 4, except the source files now become Verilog module(s) instead of schematics. The file name for a Verilog module must have an extension of .v so that it can be recognized by Xilinx ISE.

REQUIREMENT: The Xilinx ISE tool is able to generate a schematic synthesized from the source Verilog file(s). The block level (a.k.a. Register Transfer Level) schematic can be generated by double clicking Synthesis – XST → View RTL Schematic in the Processes window. You may double click on a block to view detailed design of the block. Include all the RTL schematics in your lab report.

7. Deliverables

Write a lab report to capture different aspects of your design including but not limited to design procedure, schematics, Verilog code, simulation and testing results, discussions, and conclusion. Only one report is required for each team. Electronic submission is required. Report is due by **10:00pm June 24, 2017**.

The full score for this lab is 200 points: 160 points for the experiment and 40 points for the lab report.