VE270 Homework 7

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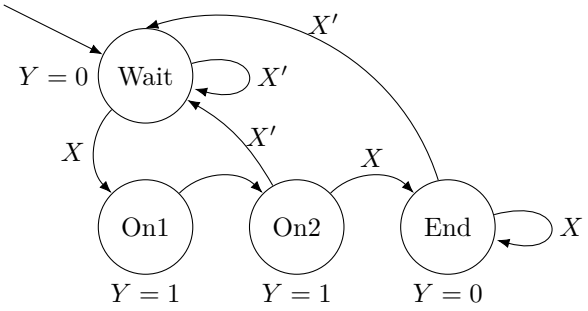
Problem 1.

Inputs: X; Outputs: Y



Problem 2.

Encode the states ($s_1 s_0$): Wait: 00, On1: 10, On2: 11, End: 01.

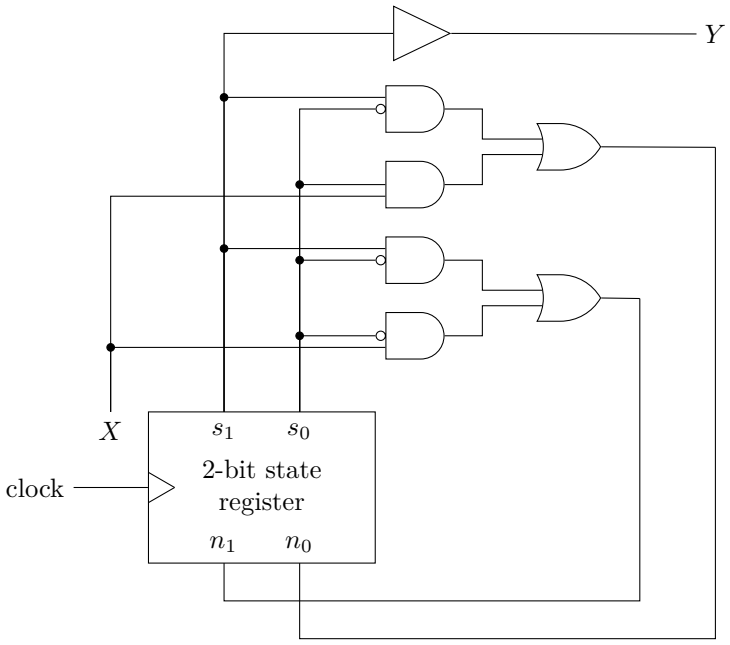
The truth table is

s_1	s_0	X	n_1	n_0	Y
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	1	1

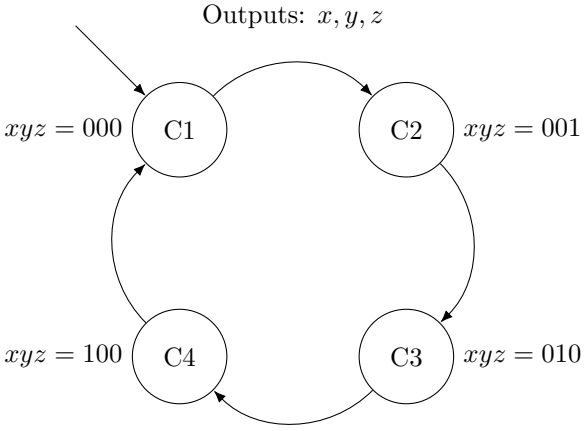
The euqations are

$$n_1 = s_0' X + s_1 s_0'$$
$$n_0 = s_0 X + s_1 s_0'$$
$$Y = s_1$$

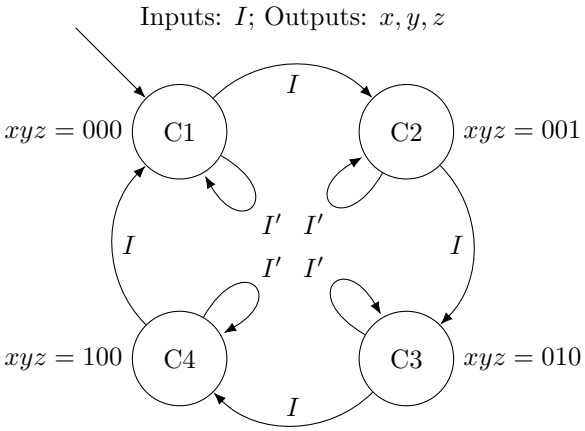
The schematics is


Y
X
s_1
s_0
clock
2-bit state
register
n_1
n_0

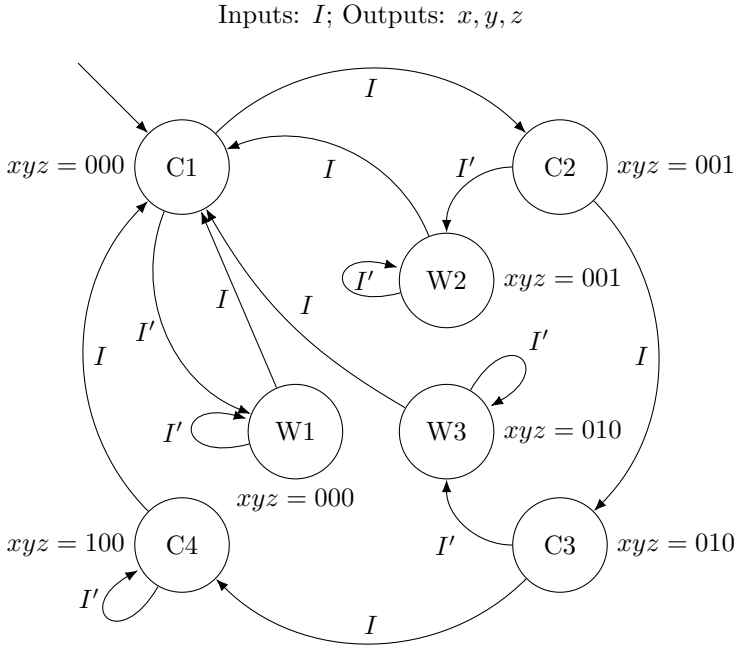
Problem 3.


Outputs: x, y, z
$xyz = 000$
C1
C2
$xyz = 001$
$xyz = 100$
C4
C3
$xyz = 010$

Problem 4.



Problem 5.



Problem 6.

Encode the states ($s_2 a_1 s_0$): C1: 000, W1: 001, C2: 010, W2: 011, C3: 100, W3: 101, C4: 110.

The truth table is

s_2	s_1	s_0	I	n_2	n_1	n_0	X	Y	Z
0	0	0	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	0	0
0	0	1	0	0	0	1	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	1	0	0	1
0	1	1	1	0	0	0	0	0	1
1	0	0	0	1	0	1	0	1	0
1	0	0	1	1	1	0	0	1	0
1	0	1	0	1	0	1	0	1	0
1	0	1	1	0	0	0	0	1	0
1	1	0	0	1	1	0	1	0	0
1	1	0	1	0	0	0	1	0	0
1	1	1	0	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X

The euqations are

$$n_2 = s_2' s_1 s_0' I + s_2 s_1' s_0' + s_2 I'$$

$$n_1 = s_1' s_0' I + s_1 I'$$

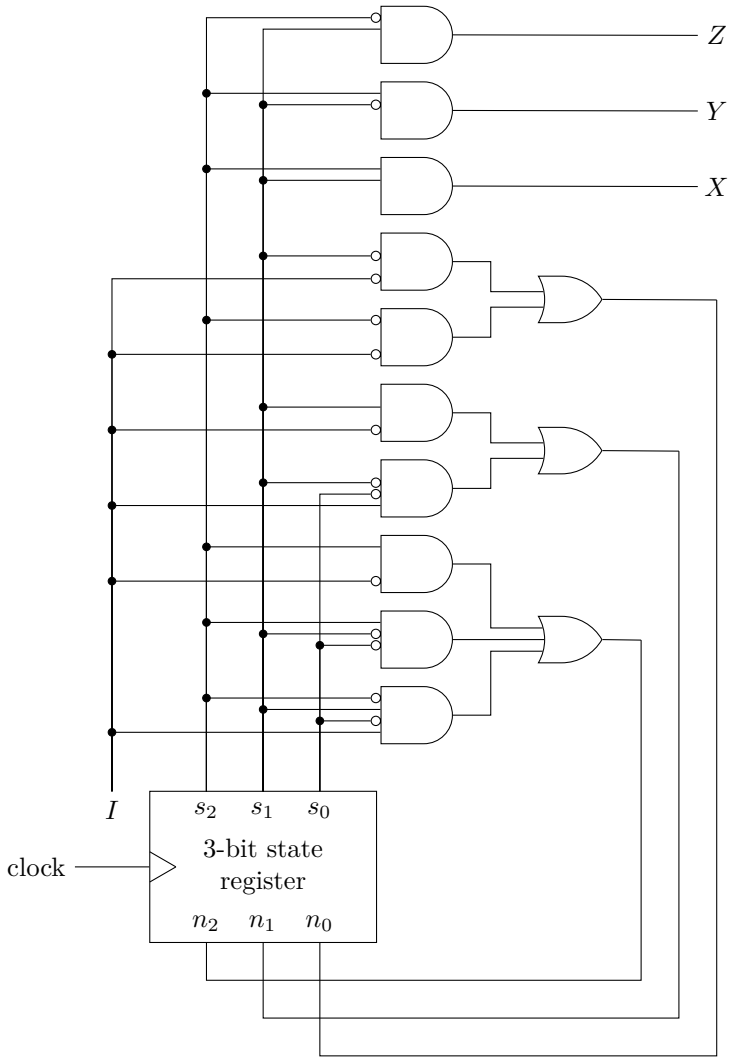
$$n_0 = s_2' I' + s_1' I'$$

$$X = s_2 s_1$$

$$Y = s_2 s_1'$$

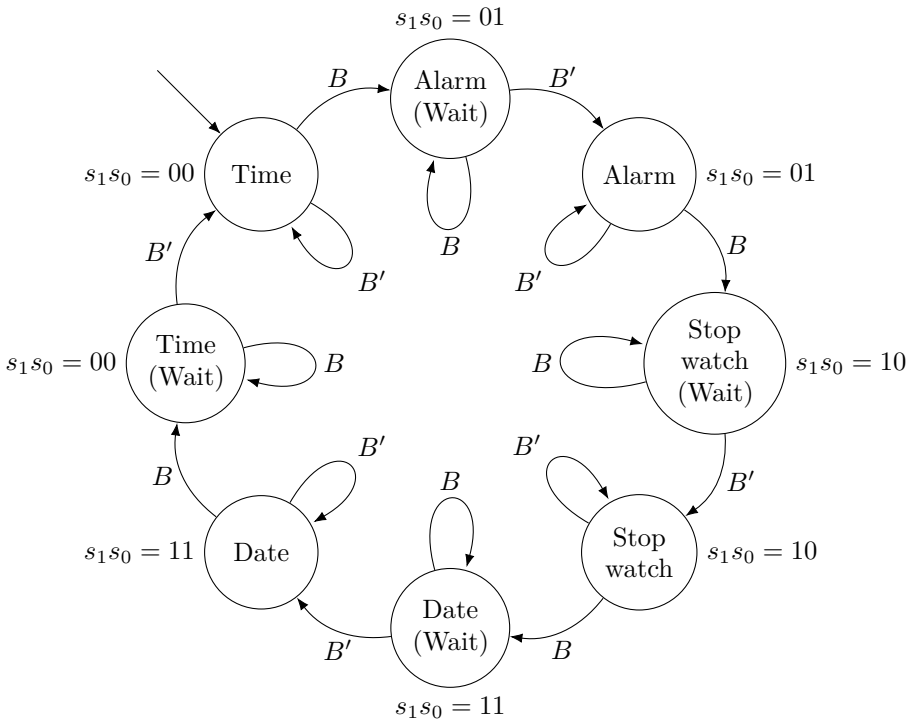
$$Z = s_2' s_1$$

The schematics is


Z
Y
X
I
s_2 s_1 s_0
clock
3-bit state register
n_2 n_1 n_0

Problem 7.

Inputs: B; Outputs: s_1, s_0



Encode the states ($s_2s_1s_0$): Time (Wait): 000, Time: 001, Alarm (Wait): 010, Alarm: 011, Stopwatch (wait): 100, Stopwatch: 101, Date (Wait): 110, Date (Wait): 111.

The truth table is

s_2	s_1	s_0	B	n_2	n_1	n_0	s_1	s_0
0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	1	0	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	1	1	0	1
0	1	0	1	0	1	0	0	1
0	1	1	0	0	1	1	0	1
0	1	1	1	1	0	0	0	1
1	0	0	0	1	0	1	1	0
1	0	0	1	1	0	0	1	0
1	0	1	0	1	0	1	1	0
1	0	1	1	1	1	0	1	0
1	1	0	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1
1	1	1	1	0	0	0	1	1

The euqations are

$$n_2 = s_2' s_1 s_0 B + s_2 s_1' + s_2 s_0' + s_2 B'$$

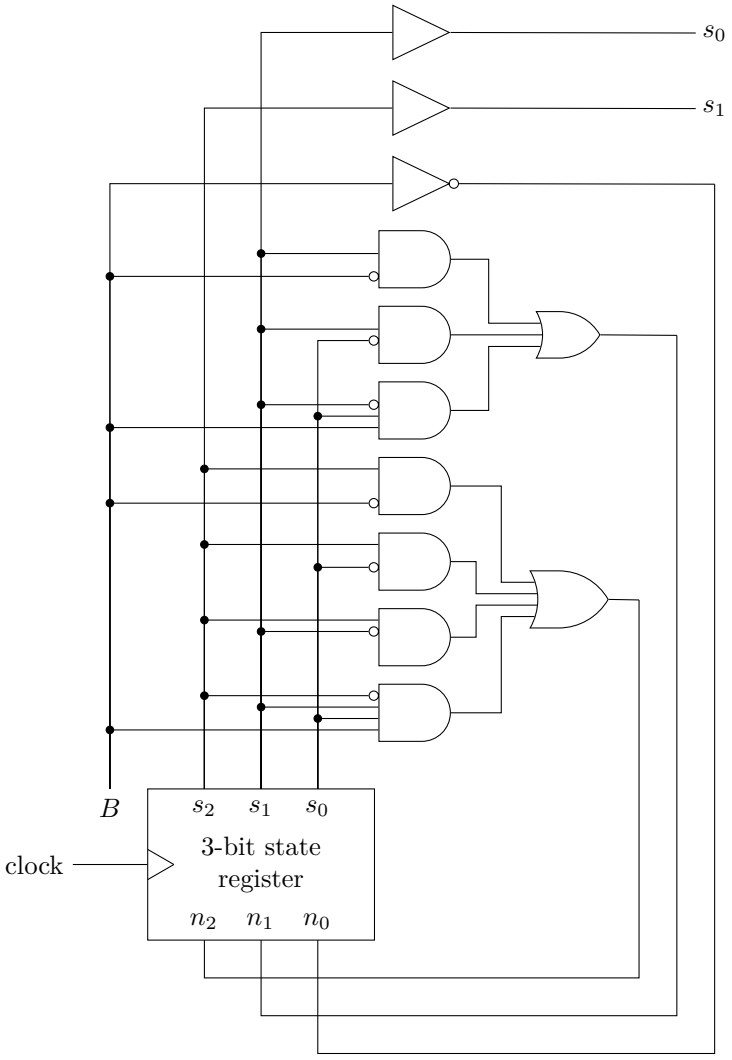
$$n_1 = s_1' s_0 B + s_1 s_0' + s_1 B'$$

$$n_0 = B'$$

$$s_1 = s_2$$

$$s_0 = s_1$$

The schematics is



Problem 8.

Same as Problem 7.