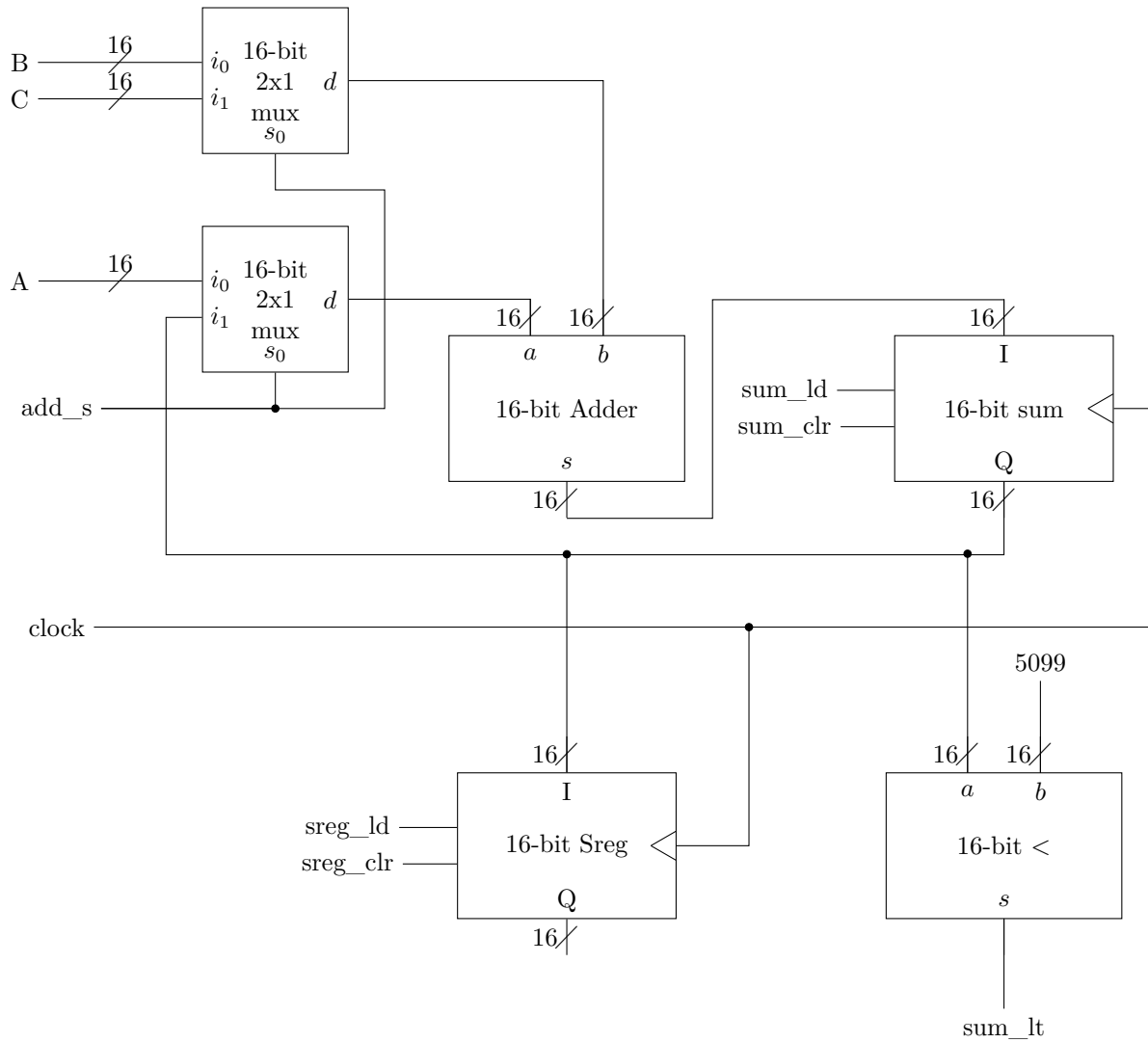# VE270 Homework 9

Liu Yihao 515370910207

Problem 1.

Inputs: A, B, C, add_s (0 for sum:=A+B and 1 for sum:=sum+C), sum_ld, sum_clr, sreg_ld, sreg_clr, clock

Outputs: sum_lt (whether sum<5099)

Problem 2.

Init

ld

clr

CT

32

I

32-bit
register

Q

clock

WT

32

32

I

32-bit
register

Q

32

32

a   b

32-bit Adder

s

32

32

a   b

32-bit <

s

32

32

I

32-bit
register

Q

32

32

32-bit >> 1

32

avg_lt_wt

32

32

I

32-bit
register

Q

32

32

32

a   b

32-bit Adder

s

32

32

32

32

a   b

32-bit Adder

s

32

32

32-bit >> 1

32

32-bit >> 1

32