交大密西根学院

UM-SJTU Joint Institute

Lab Report

2

UM-SJTU Joint Institute

Ve270 Introduction to Logic Design

by

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Design of an SSD Driver

1 Objectives

To design a Seven-Segment Display (SSD) driver using Xilinx ISE, and to implement the circuit in an FPGA chip.

2 Problem Definition

To form SSD as a digit-display system. By inputting 4-bit binary number, seven cathode will receive a 7-bit binary digit for the seven segments of the LED, then the corresponding parts of the LED will illuminate to form the correct decimal digit. When the cathode receives a "0" and the anode receives an "1"", the LED is turned on. The input of this system is a 4-bit binary number, the output is the corresponding decimal digit displayed by LED. As an example, when the driver receives "0101"" as input, the decimal number "5"" will be displayed.

3 System Partitioning

1. Switch and driver: switches and driver are used to input 4-bit binary digit signal. By toggling different switches, the driver will receive the binary digit inputted, then convert it to anodes and cathodes.
2. Anodes and cathodes: used for receiving the signal from driver, and controlling the LED segments.
3. LED segments: to receive the signal converted fro the anodes and cathodes, and illuminate to form the corresponding decimal digit.

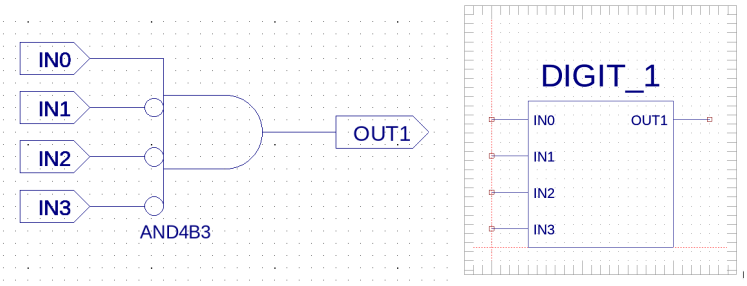
4 Design Entry

The overall truth table was shown in Table 1.

Input	Outputs(LED segments)						
	CA	CB	CC	CD	CE	CF	CG
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	1	0	1	1

Table 1: Overall truth table

First, we designed some macros to translate different inputs into numbers, for example, the schematics design and symbol for input number 1 (0001) was shown in Figure 1.

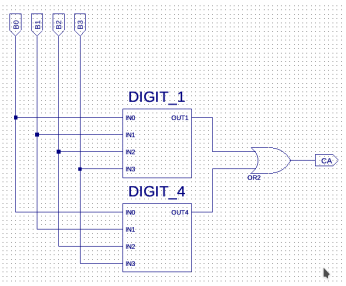


(a) Schematics design (b) Symbol

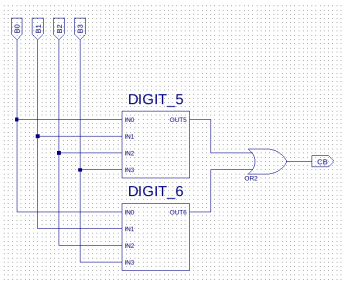
Figure 1: Schematics design and symbol for input number 1

According to this truth table, we designed a circuit for each input segment, shown in Figure 2.

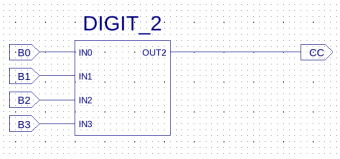
At last, we build the symbols for the seven input segments and designed a final circuit of SSD, shown in Figure 4.



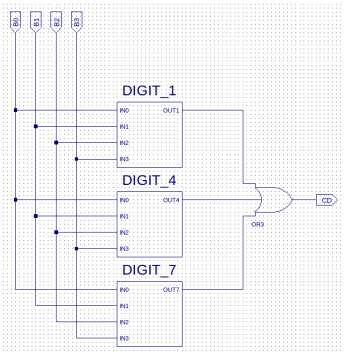
(a) CA



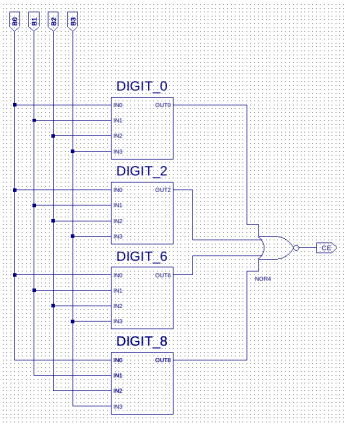
(b) CB



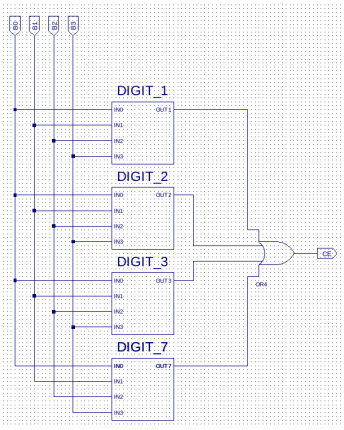
(c) CC



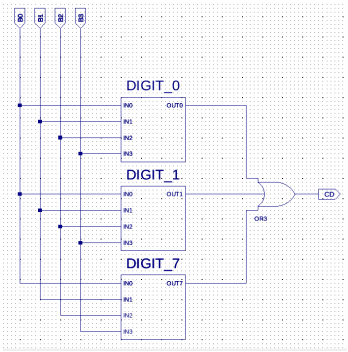
(d) CD



(e) CE



(f) CF



(g) CG

Figure 2: Schematics design for input segments

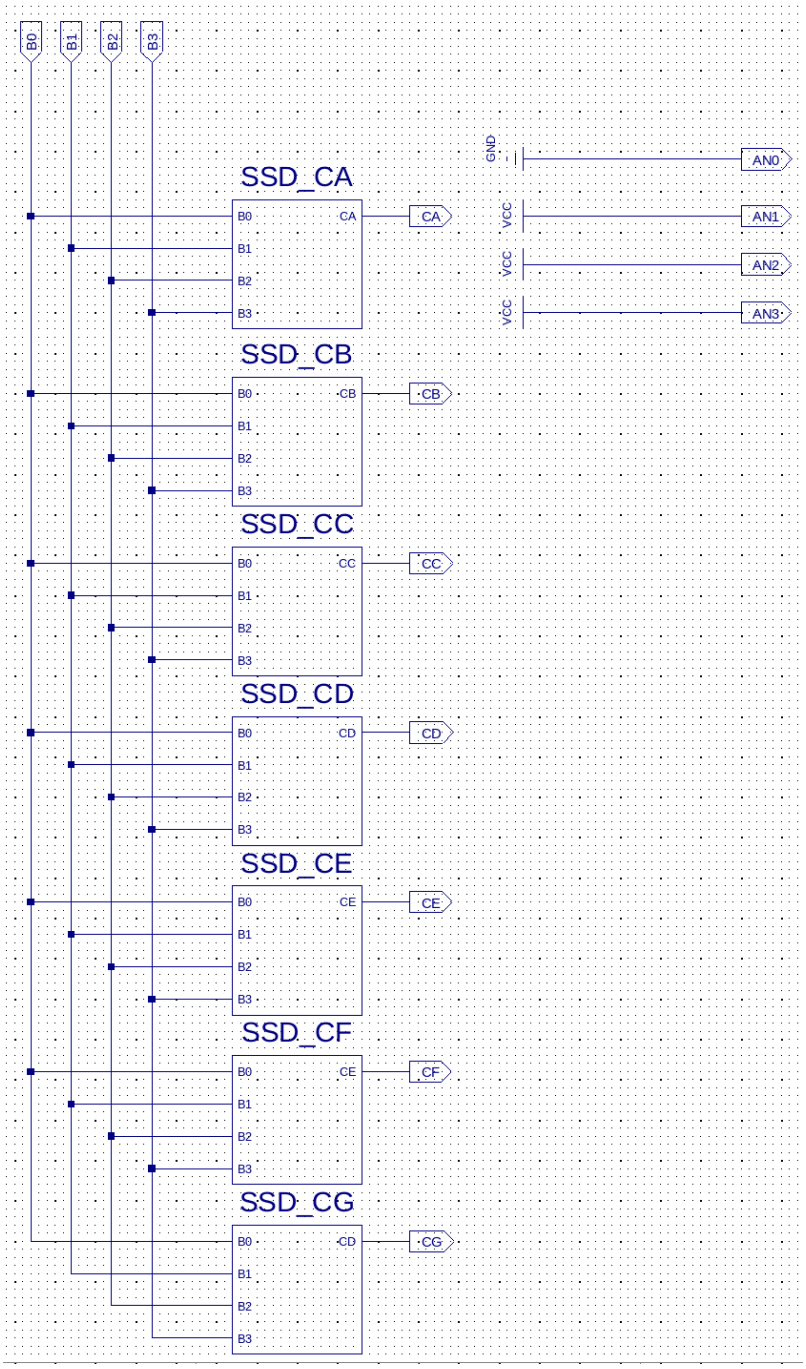


Figure 3: Schematics design for SSD

5 Test Plan

Test content	Test method
CA	Input signal that needs corresponding LED segment to illuminate, then observe if it illuminates. If it illuminates when corresponding signal inputted, this subsystem passes the test; otherwise it fails.
CB	
CC	
CD	
CE	
CF	
CG	
The overall system	Input every kind of the 4-bit binary digit signal: 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, then observe if LED displays the corresponding decimal digit:1,2,3,4,5,6,7,8,9. If so, the system passes the test; otherwise it fails.

6 Simulation Results

We simulated the result of the overall system with input values B0,B1,B2,B3 as 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001. The result was shown in Figure **??**.

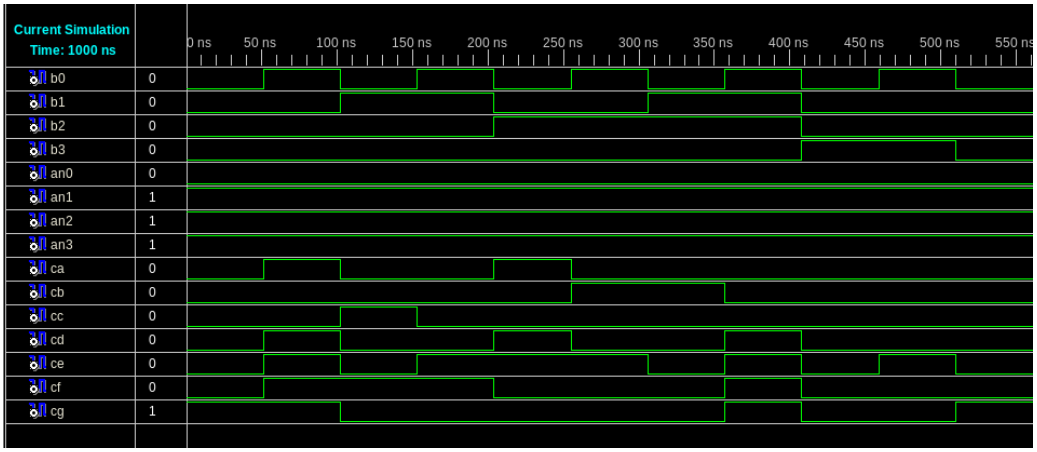


Figure 4: Simulation of SSD

We found the values in the simulation identical to the truth table we built as Table 1, which proved that our design was right.

7 Conclusion

8 Appendix

The schematics of our design, as well as the TEX source code, were attached to the report.