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Lab Report

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Ve270 Introduction to Logic Design

by

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Design of a Simple ALU



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1 Objectives

To design a simple datapath using combinational building blocks in Xilinx ISE, and to implement the circuit in an FPGA chip.

2 Problem Definition

To form a Arithmetic and Logic Unit (ALU) which takes 4-bit input data and outputs the result(F and Cout). The algorithm being used is decided on the 2-input select signal. The algorithms are shown in Table 1.

S0	S1	F	Cout	Example
0	0	A+B	Carry out	A=1100, B=1110, F=1010, Cout=1
0	1	A-B	Carry out	A=1100, B=1110, F=1110, Cout=0
1	0	A and B	0	A=1100, B=1110, F=1100, Cout=0
1	1	A or B	0	A=1100, B=1110, F=1110, Cout=0

Table 1: Overall truth table

3 System Partitioning

1. 8 Switches and 2 select signal buttons. Switches are used to input two 4-bit binary input A and B. The buttons are used to select the algorithm to be executed. Then the input signals will be transmitted to the inside circuit to calculate and come up with the result.
2. Inside circuit. To receive the input signals and get the result. It will outputs some signals that controls the LED to illuminate.
3. LED. LED is used as the output indicator. The illumination of different LED can indicate different different binary digit as the output F and Cout.

4 Design Entry

The algorithm in this system was shown in Table 2.

Select signal		Algorithm	Output	
S0	S1		F	Cout
0	0	Add	A+B	Carry out
0	1	Subtract	A-B	Carry out
1	0	And	A and B	0
1	1	Or	A or B	0

Table 2: Algorithm table

According to the Table 2, we designed the ALU circuit, shown in Figure 1.



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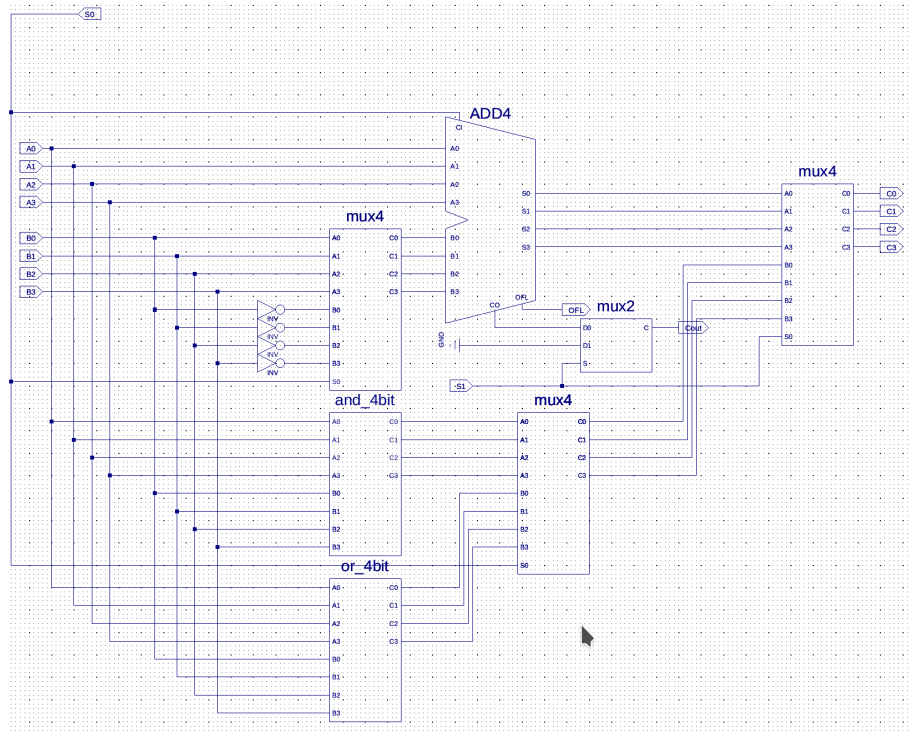


Figure 1: Schematics design of ALU



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The inner design of several symbols were shown in Figure 2.

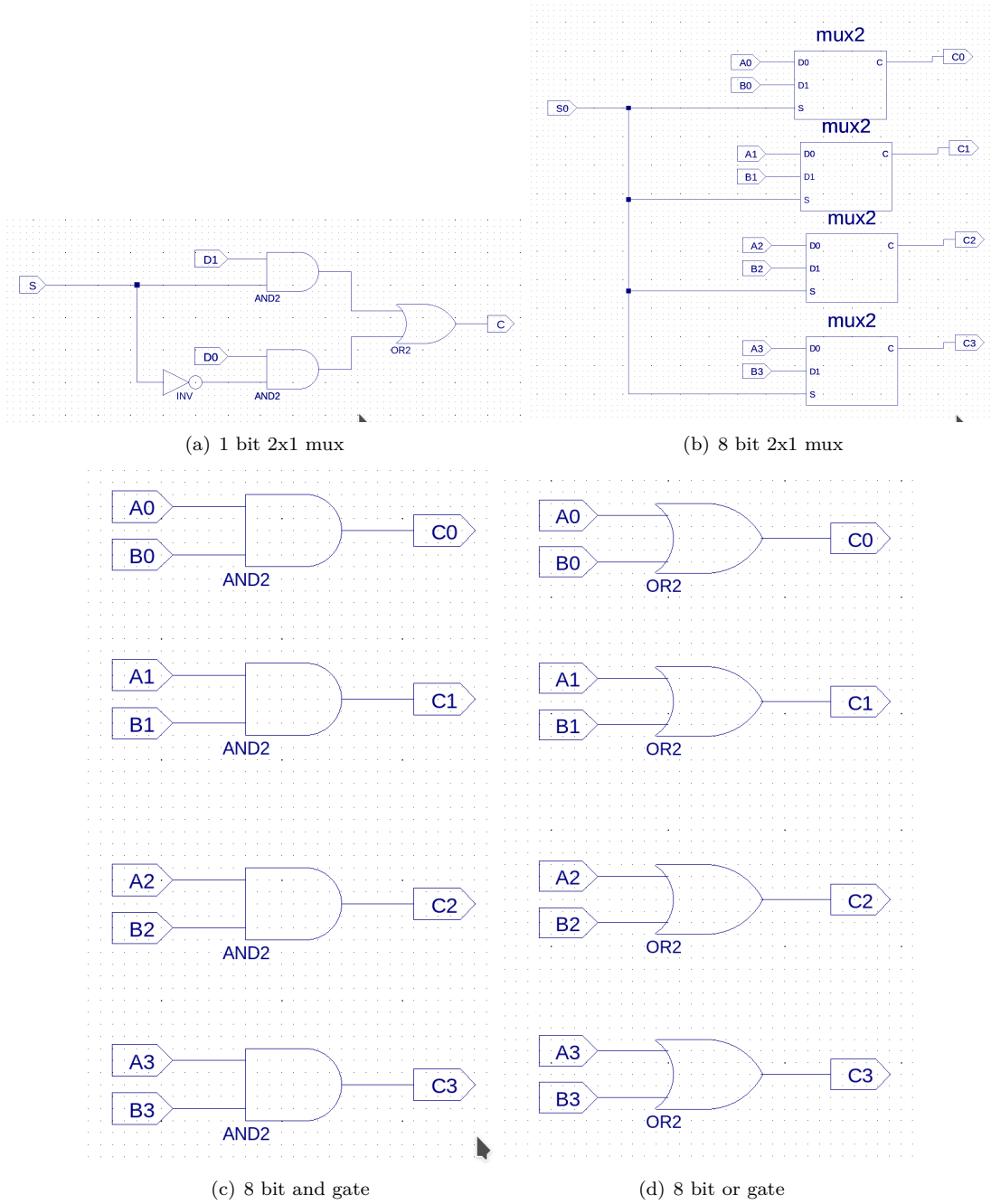


Figure 2: Schematics design of symbols



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5 Test Plan

Test content	Test method
CA	Input signal that needs corresponding LED segment to illuminate, then observe if it illuminates. If it illuminates when corresponding signal inputted, this subsystem passes the test; otherwise it fails.
CB	
CC	
CD	
CE	
CF	
CG	
The overall system	Input every kind of the 4-bit binary digit signal: 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, then observe if LED displays the corresponding decimal digit: 1, 2, 3, 4, 5, 6, 7, 8, 9. If so, the system passes the test; otherwise it fails.

6 Simulation Results

We simulated the result of the overall system with input values in Table 1, shown in Figure 3.

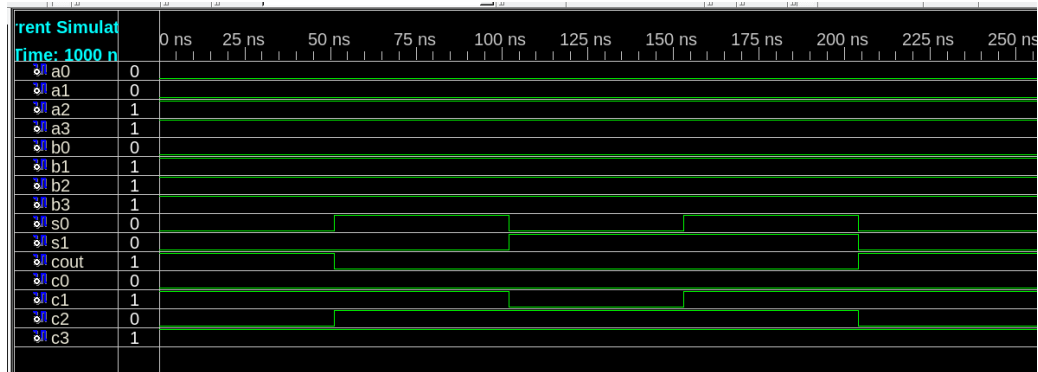


Figure 3: Simulation of ALU

We found the values in the simulation identical to Table 1.



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7 Conclusion

In this lab, we successfully finished it finally, but we also met with some problems in the process. Some existing modules in ISE will cause error in the simulation and pace process, such as the inverse-4 and mux-4, so we have to build a new module ourselves. We practiced build a ALU with 2-bit select input signal and four kinds of algorithms.

8 Appendix

The schematics of our design had been submitted to canvas before.