JOINT INSTITUTE
交大密西根学院

Ve 270 Introduction to Logic Design

Lab 3
Design of a Simple ALU

UM-SJTU Joint Institute
Shanghai Jiao Tong University
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1. Objective

To design a simple datapath using combinational building blocks in Xilinx ISE, and to implement the circuit in an FPGA chip.

2. Design Specification

The purpose of datapaths is to provide routes for data to travel between functional units. Datapaths can be joined together to make bigger datapaths using multiplexers [wikipedia.org].

In this lab, you are asked to design a simple Arithmetic and Logic Unit (ALU) that takes two 4-bit input data (A and B) and outputs the results (F and Cout) depending on the select signal S according to Table 1. The block diagram of the design is shown in Figure 1.

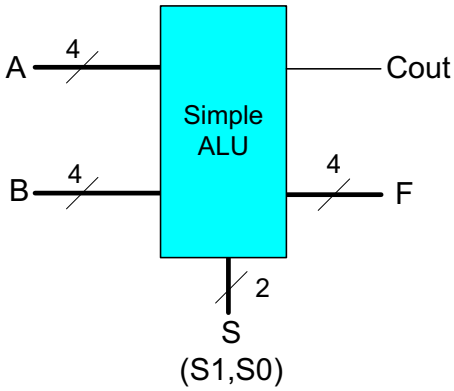


Figure 1 Block Diagram of ALU

Table 1 ALU Functions

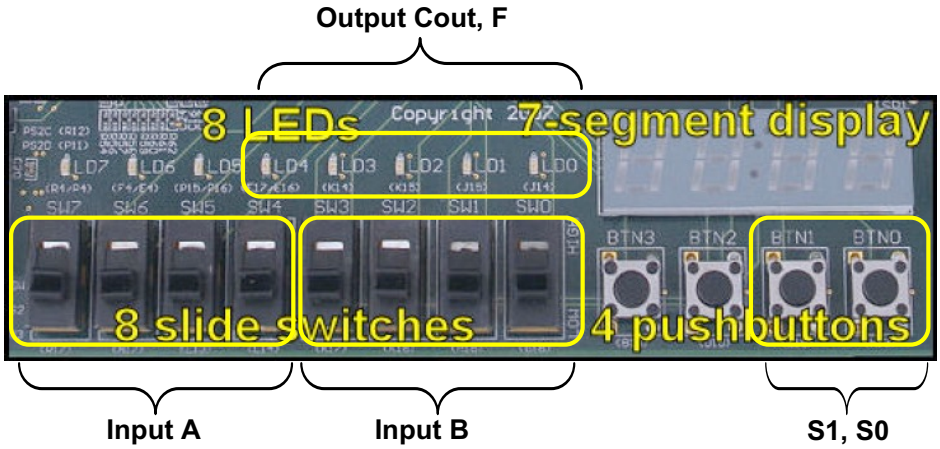
S1	S0	F	Cout	Example
0	0	A+B	Carry out	A=1100, B=1110, F=1010, Cout=1
0	1	A-B	Carry out	A=1100, B=1110, F=1110, Cout=0
1	0	A and B	0	A=1100, B=1110, F=1100, Cout=0
1	1	A or B	0	A=1100, B=1110, F=1110, Cout=0

3. Drawing Schematics and Simulation

Draw the circuitry for the ALU using Xilinx ISE schematic capture tool. Make sure the inputs are labeled correctly. Simulate the top-level integrated circuit using HDL Bencher.

4. Synthesis and FPGA Implementation

Synthesize and implement your design on the Nexys2 FPGA board. Use switches SW7~SW4 for input A, SW3~SW0 for input B, push button BTN1 for S1 and BTN0 for S0, LEDs LD3~LD0 for output F, and LD4 for output Cout, as shown in following figure. Toggle input switches to observe changes on the output LEDs. Try different inputs and verify your results.



5. Deliverable

1) Demonstrate your board to the lab instructor before you sign out.
2) Write a lab report to capture different aspects of your design including but not limited to design procedure, schematics, simulation and testing results, discussions, and conclusion. Only one report is required for each team. Electronic submission is required. Report is due by **10:00pm June 17, 2017**.