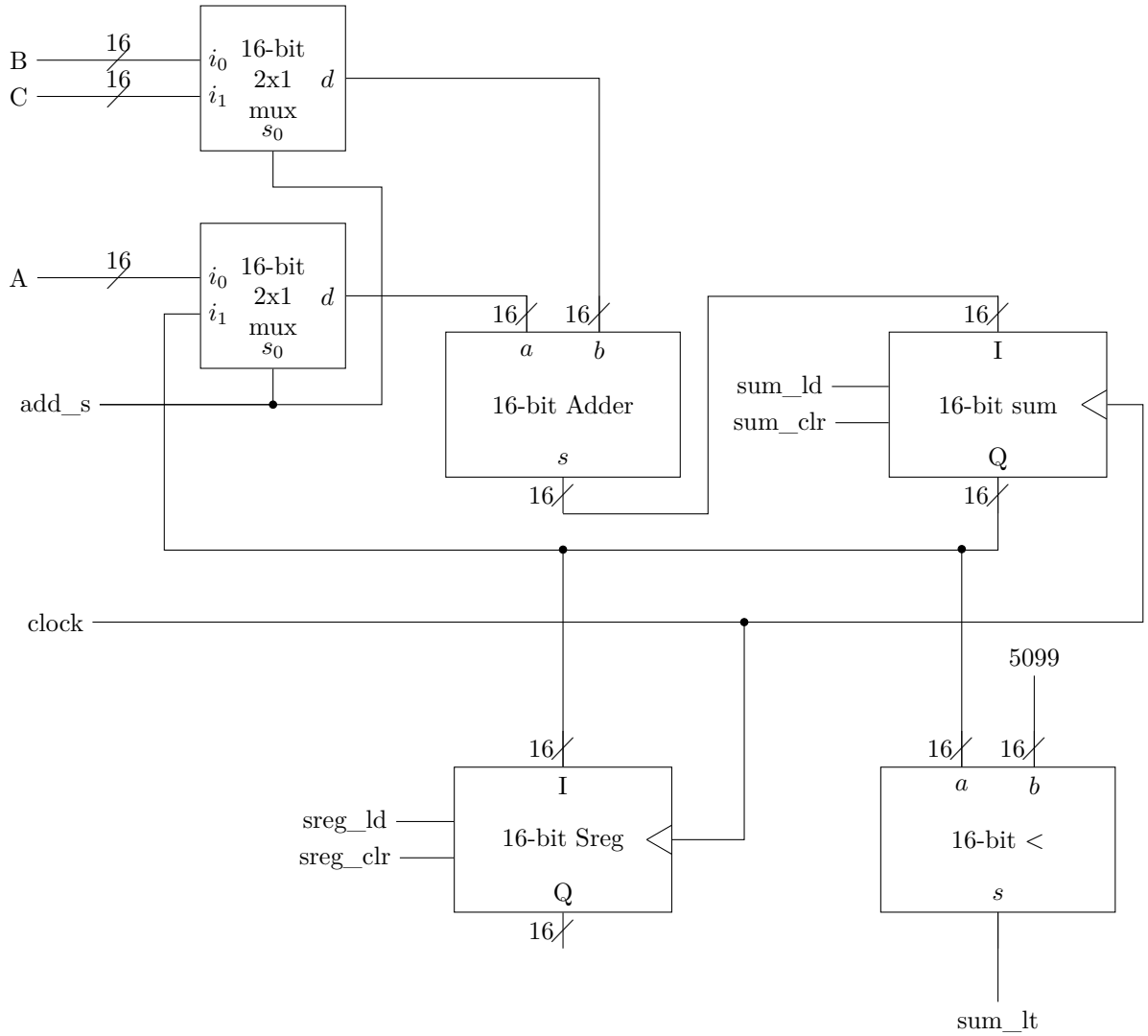
VE270 Homework 9

Liu Yihao 515370910207

Problem 1.

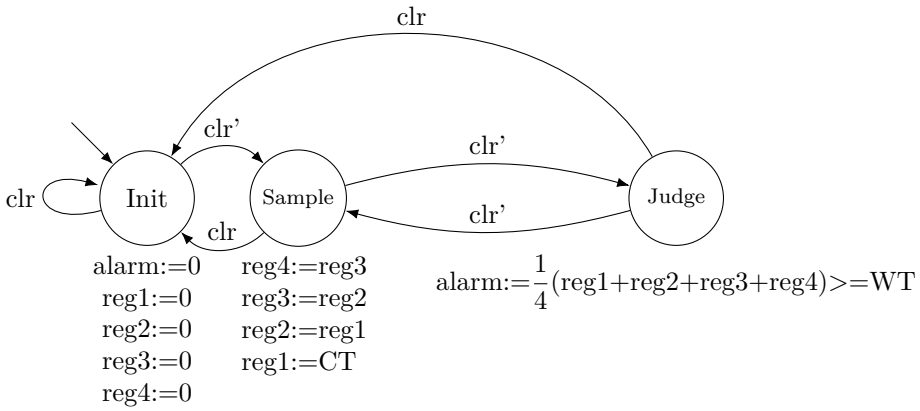
Inputs: A, B, C, add_s (0 for sum:=A+B and 1 for sum:=sum+C), sum_ld, sum_clr, sreg_ld, sreg_clr, clock

Outputs: sum_lt (whether sum<5099)

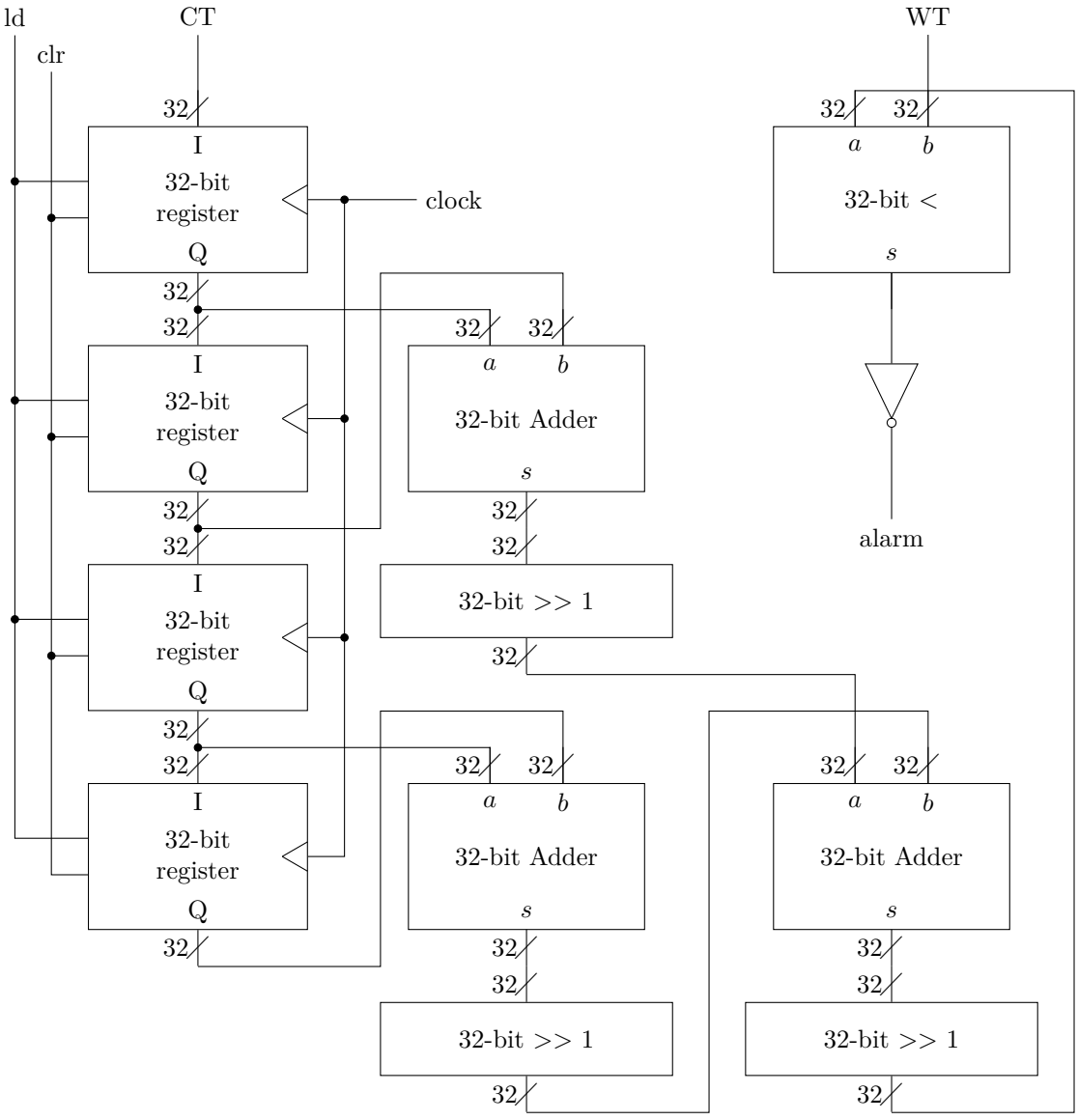


Problem 2.

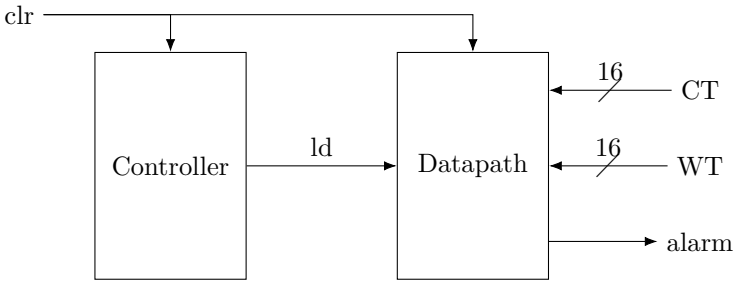
Step 1: HLSM Design
Inputs: clr, CT, WT
Outputs: alarm
Local registers: reg1, reg2, reg3 reg4



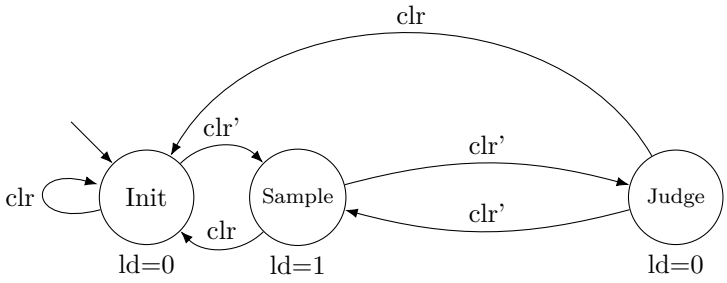
Step 2: Datapath Design



Step 3: Connect the datapath to a controller

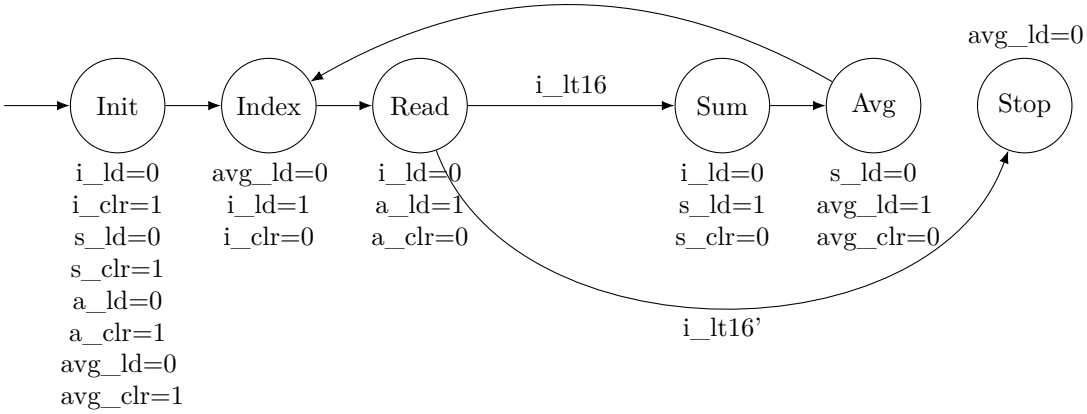


Step 4: FSM Design
Inputs: clr
Outputs: ld



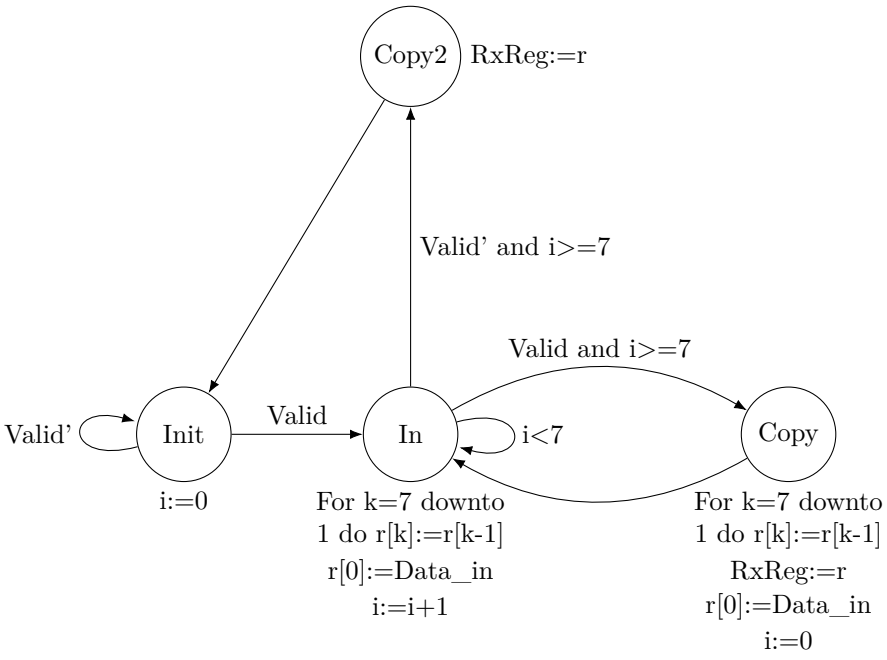
Problem 3.

Inputs: i_lt16
Outputs: i_ld, i_clr, s_ld, s_clr, a_ld, a_clr, avg_ld, avg_clr



Problem 4.

Step 1: HLSM Design
Inputs: Valid (bit), Data_in (bit)
Outputs: RxReg (8 bits)
Local registers: i (3 bits), r (8 bits)


Copy2
RxReg:=r
Valid' and i>=7
Valid and i>=7
Valid'
Init
Valid
In
i<7
Copy
i:=0
For k=7 downto
1 do r[k]:=r[k-1]
r[0]:=Data_in
i:=i+1
For k=7 downto
1 do r[k]:=r[k-1]
RxReg:=r
r[0]:=Data_in
i:=0