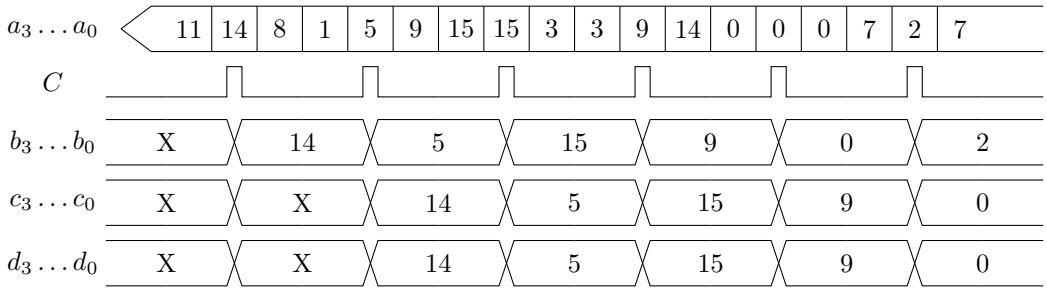
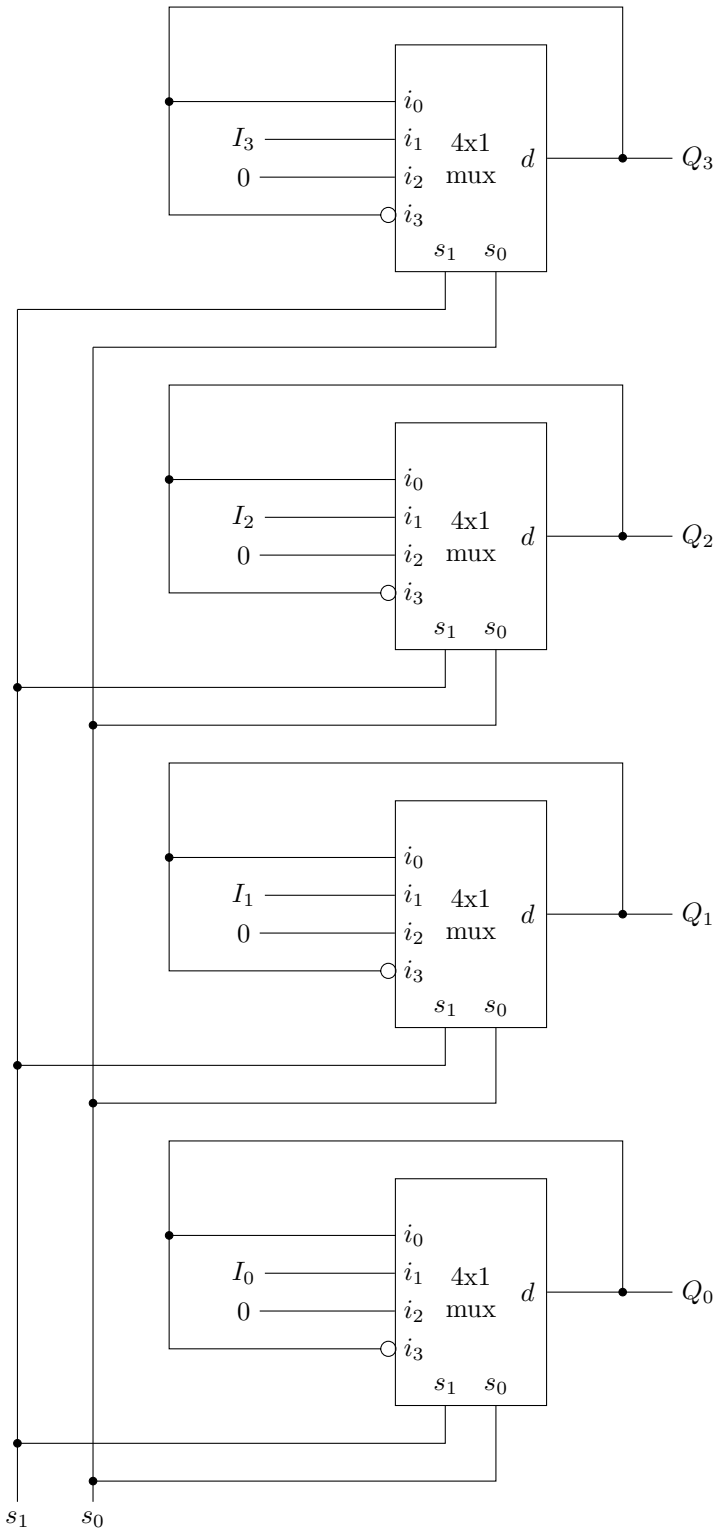
VE270 Homework 6

Liu Yihao 515370910207

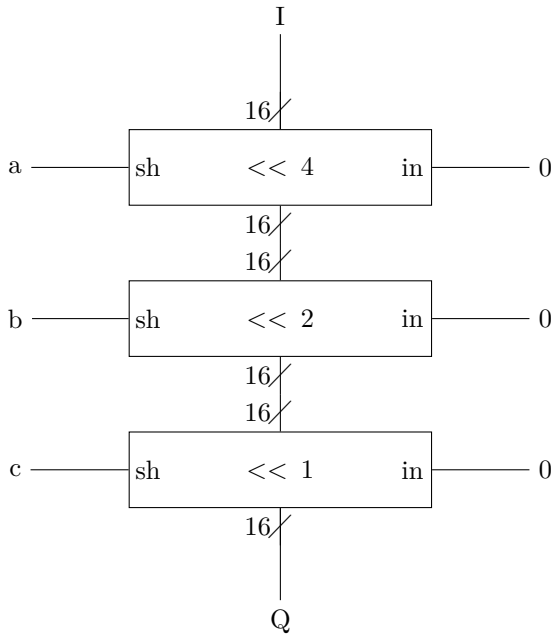
Problem 1.



Problem 2.

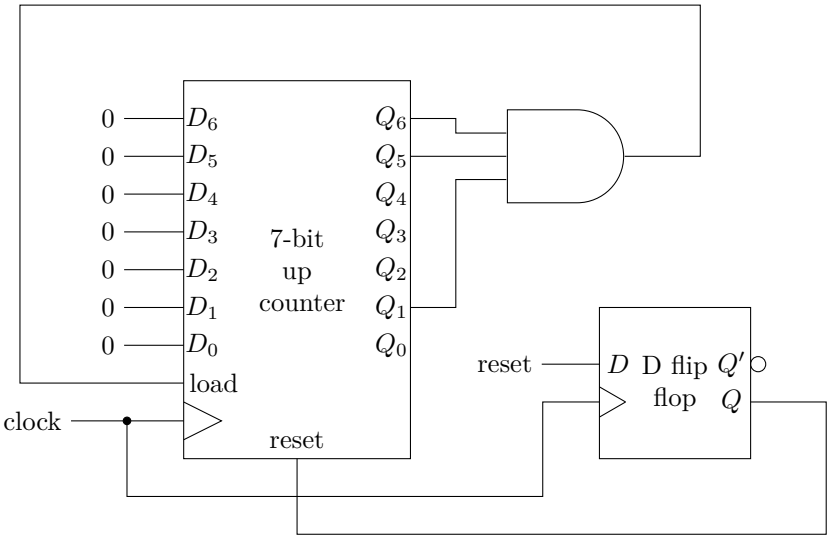

i_0
I_3
i_1
4x1
d
Q_3
0
i_2
mux
i_3
s_1 s_0
i_0
I_2
i_1
4x1
d
Q_2
0
i_2
mux
i_3
s_1 s_0
i_0
I_1
i_1
4x1
d
Q_1
0
i_2
mux
i_3
s_1 s_0
i_0
I_0
i_1
4x1
d
Q_0
0
i_2
mux
i_3
s_1 s_0
s_1
s_0

Problem 3.

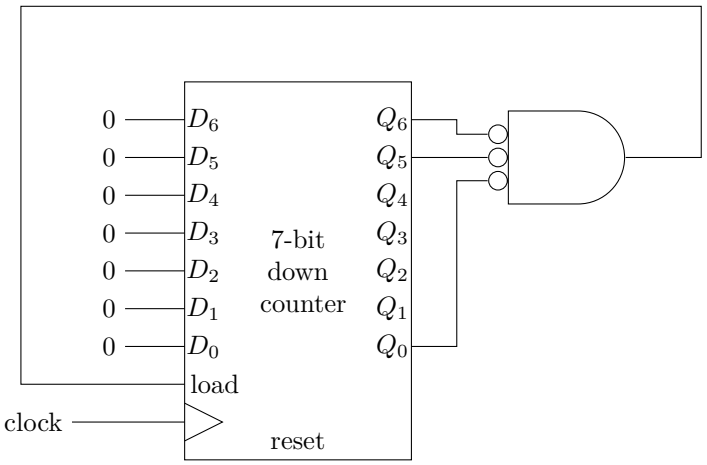


Problem 4.

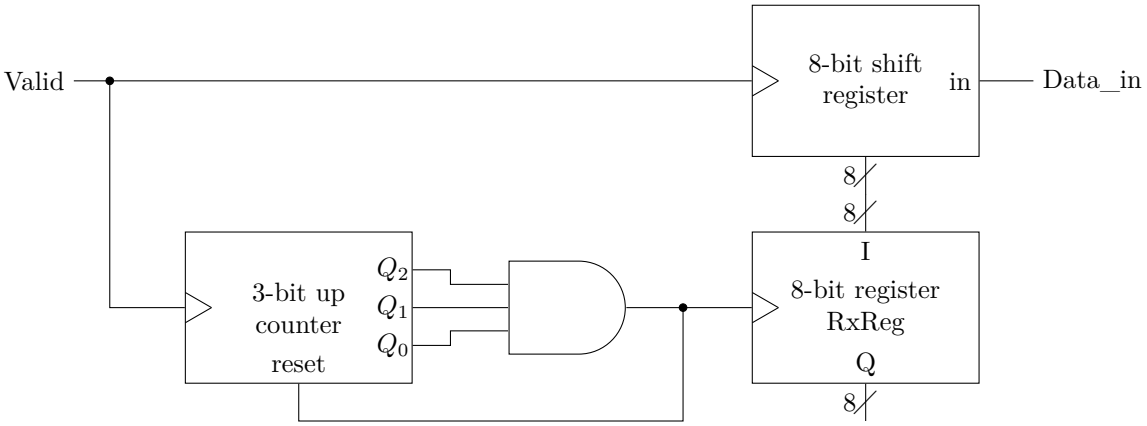
(a)



(b)


0
0
0
0
0
0
0
D_6
D_5
D_4
D_3
D_2
D_1
D_0
load
clock
7-bit
down
counter
reset
Q_6
Q_5
Q_4
Q_3
Q_2
Q_1
Q_0

Problem 5.


Valid
8-bit shift
register
in
Data_in
8
8
I
3-bit up
counter
reset
Q_2
Q_1
Q_0
8-bit register
RxReg
Q
8