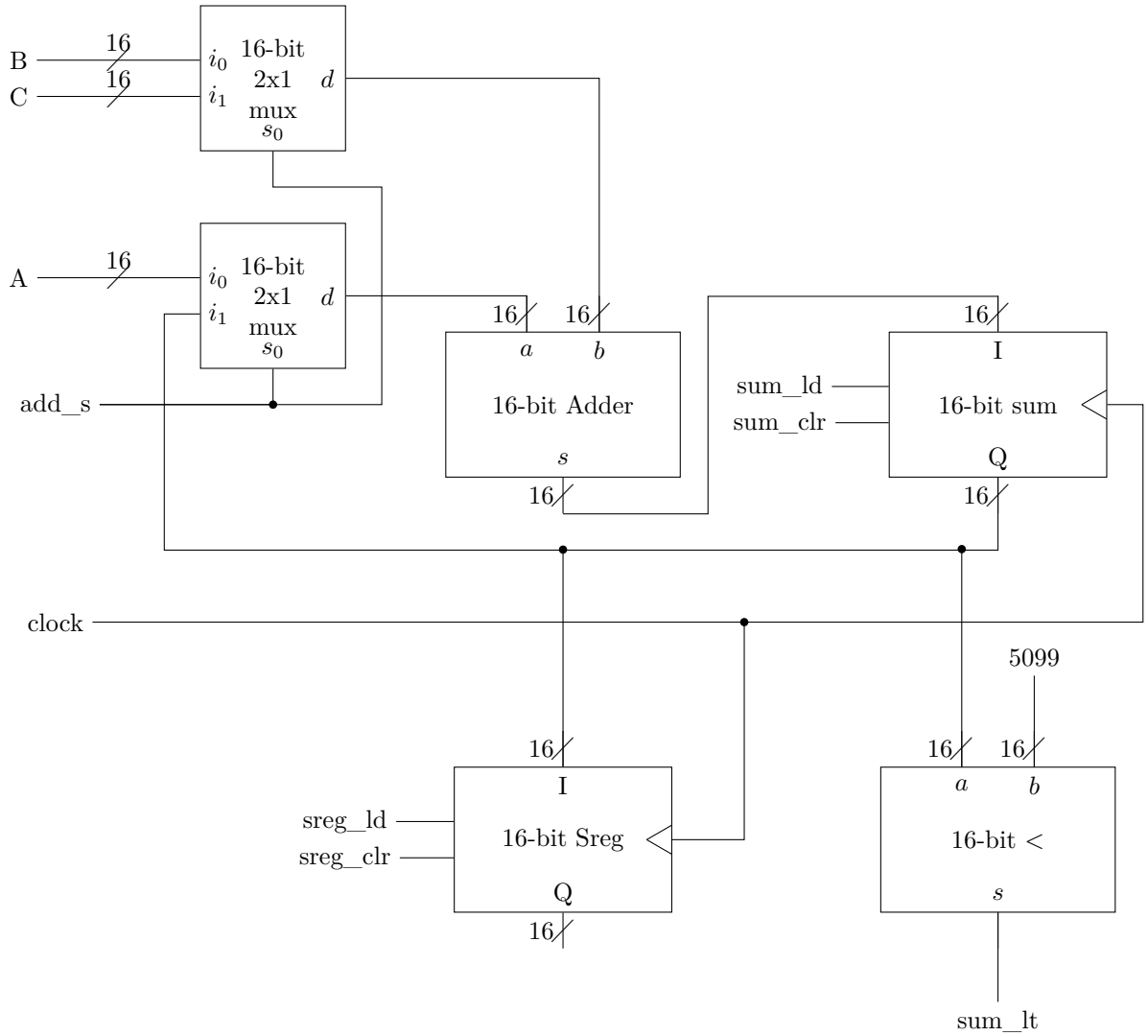
# VE270 Homework 9

Liu Yihao 515370910207

## Problem 1.

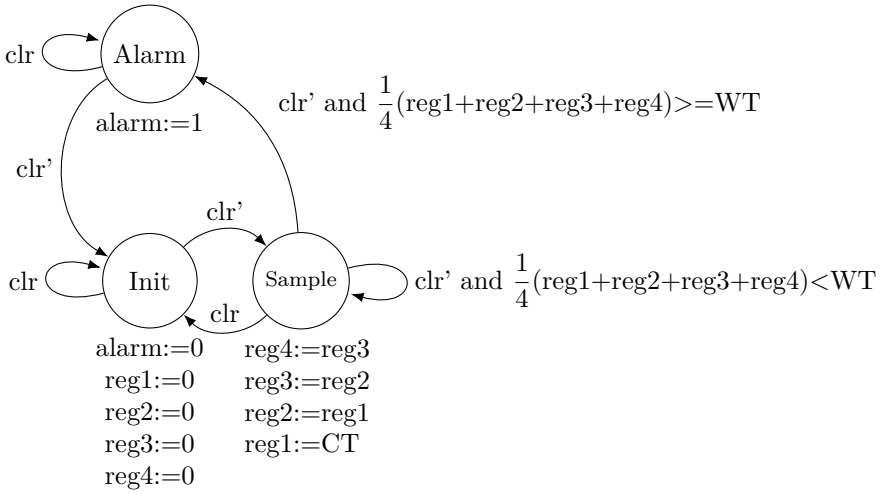
Inputs: A, B, C, add_s (0 for sum:=A+B and 1 for sum:=sum+C), sum_ld, sum_clr, sreg_ld, sreg_clr, clock

Outputs: sum_lt (whether sum<5099)

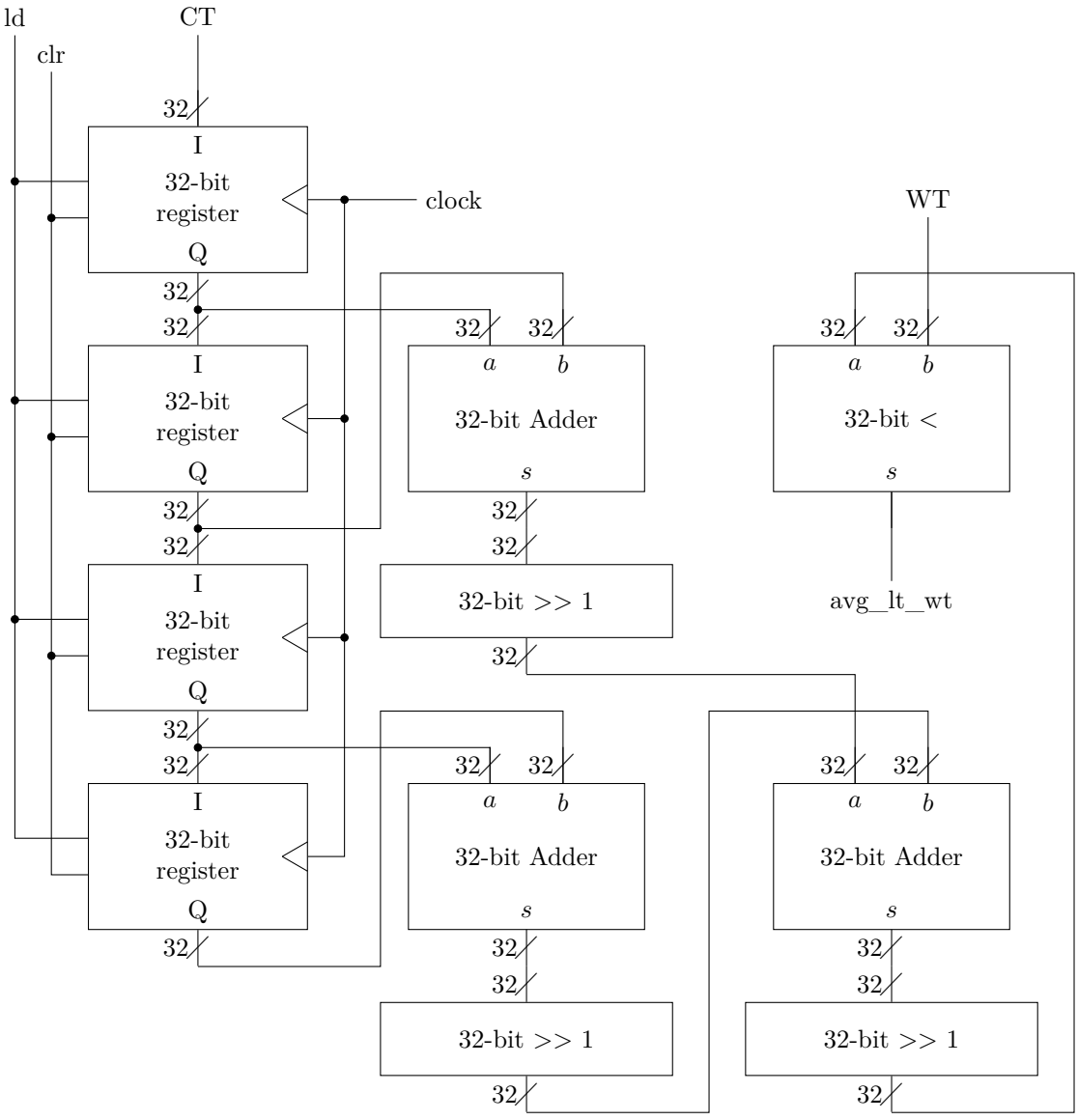


# Problem 2.

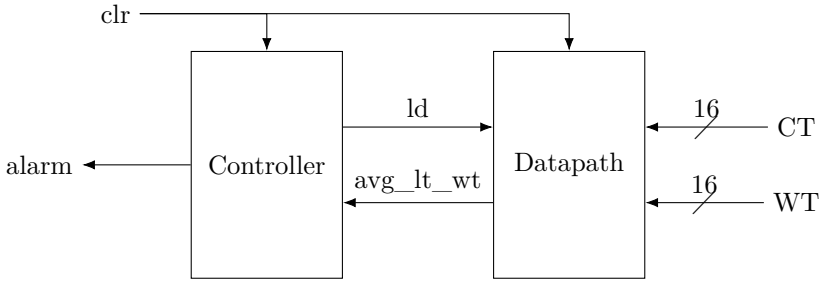
Step 1: HLSM Design
Inputs: clr, CT, WT
Outputs: alarm
Local registers: reg1, reg2, reg3 reg4



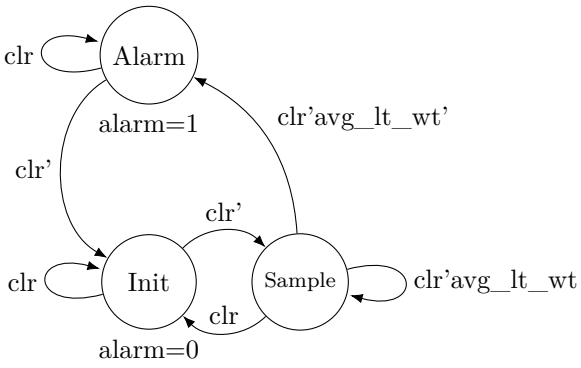

Step 2: Datapath Design




Step 3: Connect the datapath to a controller




Step 4: FSM Design
Inputs: clr
Outputs: alarm


Alarm
clr
alarm=1
clr'avg_lt_wt'
clr'
clr'
Init
Sample
clr
clr'avg_lt_wt
clr
alarm=0

## Problem 3.