VE270 Homework 9

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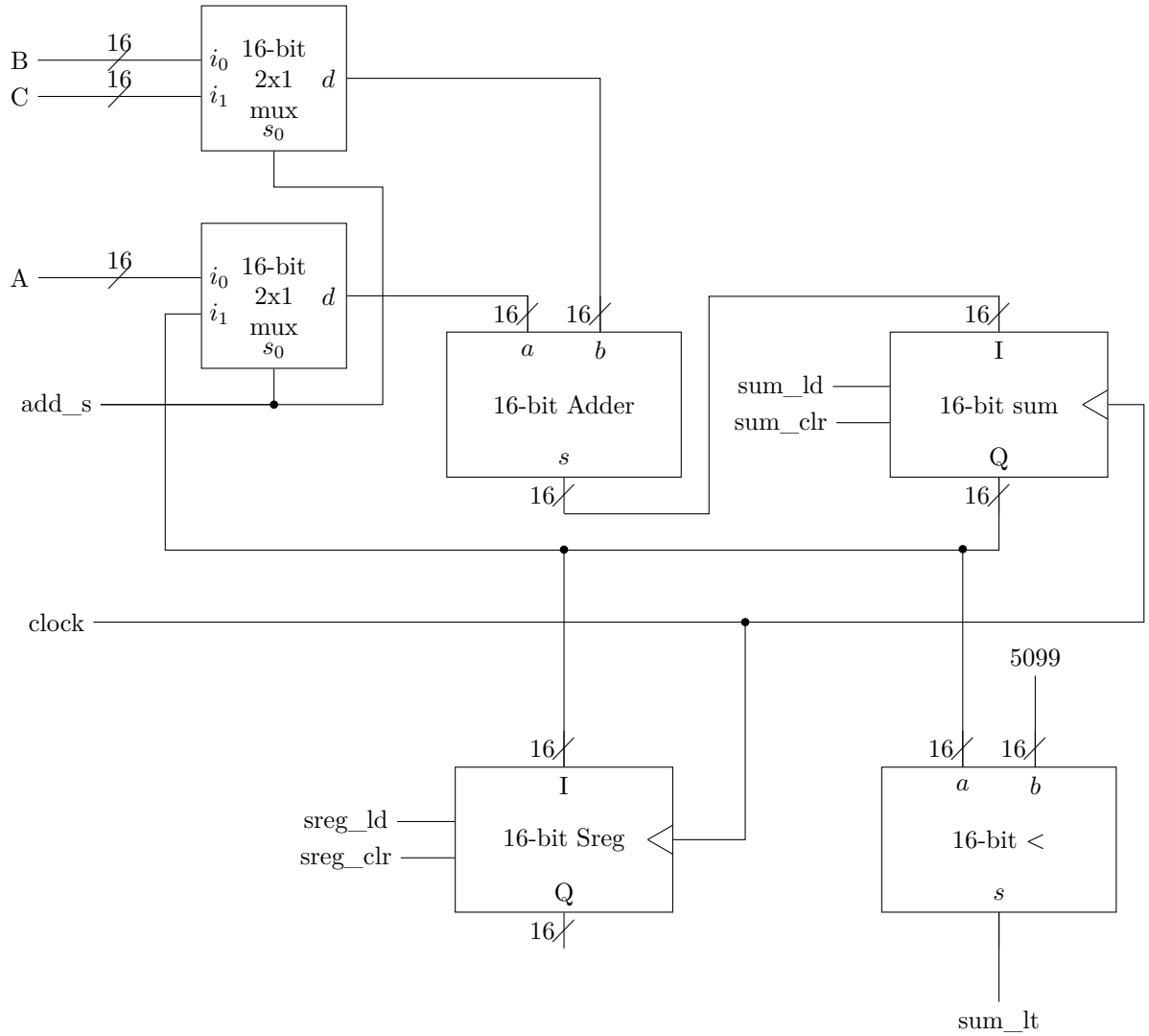
Problem 1.

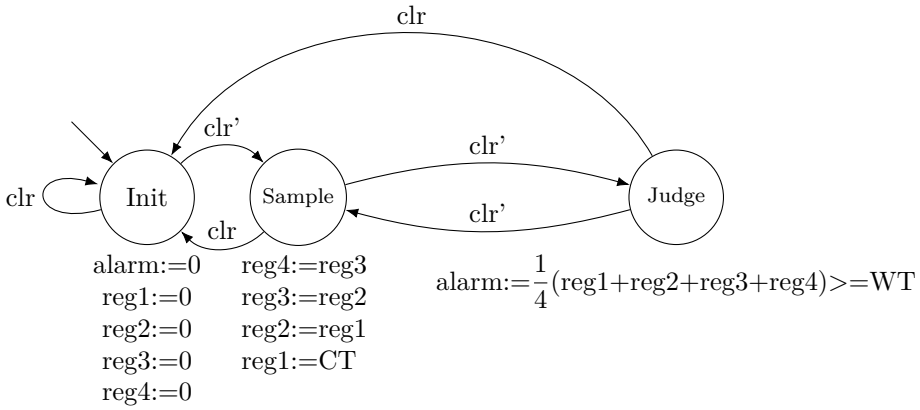
Inputs: A (16 bits), B (16 bits), C (16 bits), add_s (bit, 0 for sum:=A+B and 1 for sum:=sum+C), sum_ld (bit), sum_clr (bit), sreg_ld (bit), sreg_clr (bit), clock (bit)

Outputs: sum_lt (bit, whether sum<5099)

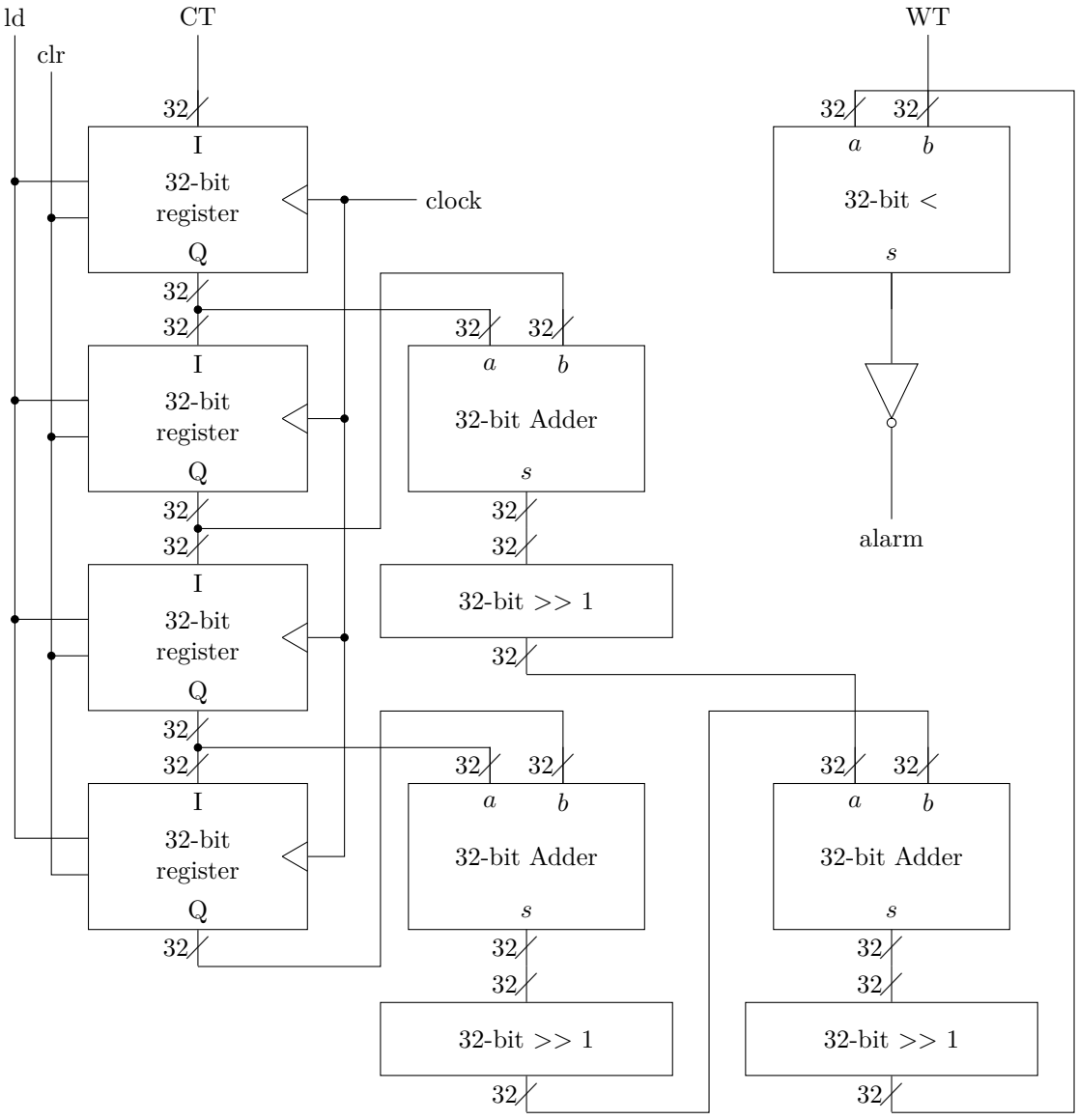


Problem 2.

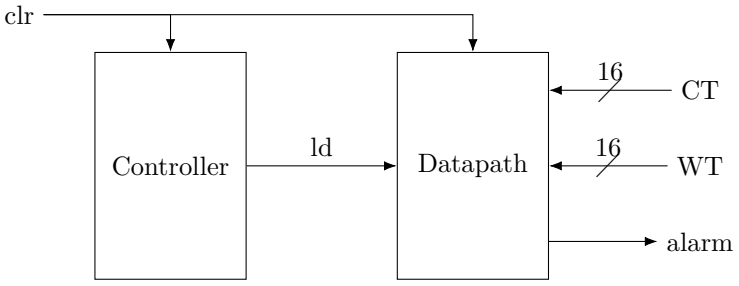
Step 1: HLSM Design
Inputs: clr (bit), CT (32 bits), WT (32 bits)
Outputs: alarm (bit)
Local registers: reg1, reg2, reg3, reg4 (all 32 bits)



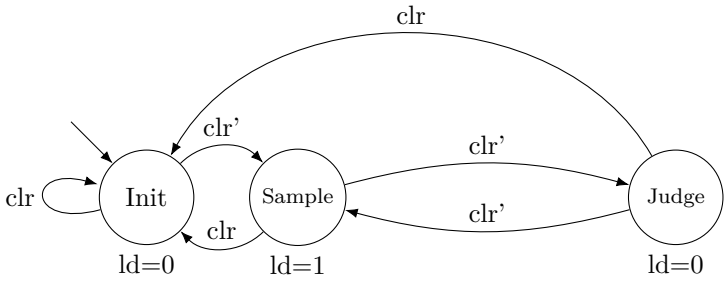
Step 2: Datapath Design



Step 3: Connect the datapath to a controller

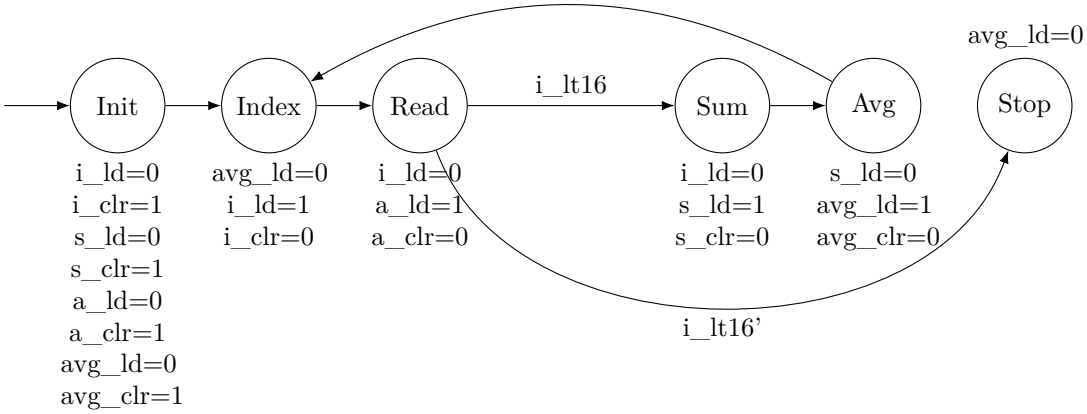


Step 4: FSM Design
Inputs: clr
Outputs: ld



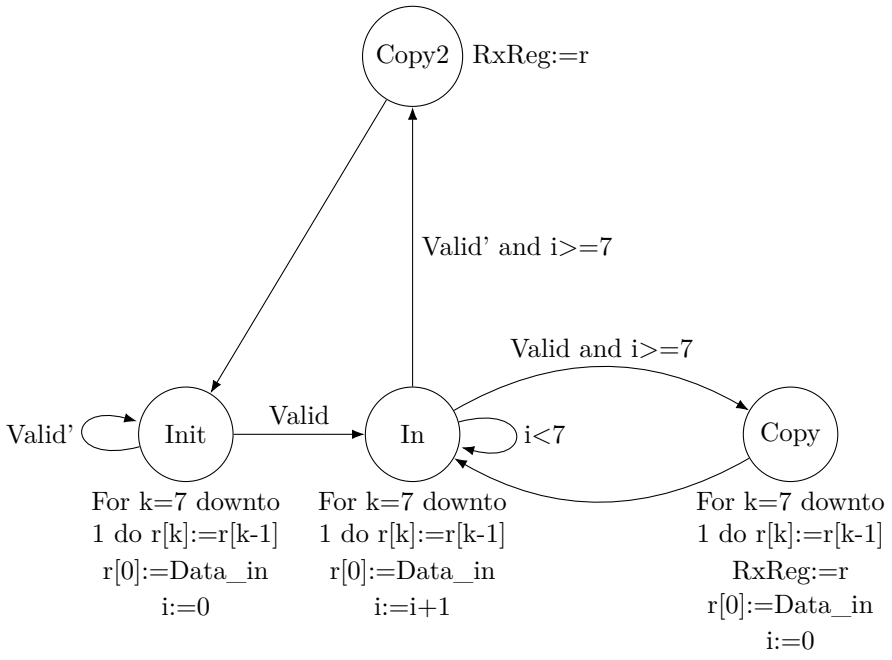
Problem 3.

Inputs: i_lt16
Outputs: i_ld, i_clr, s_ld, s_clr, a_ld, a_clr, avg_ld, avg_clr

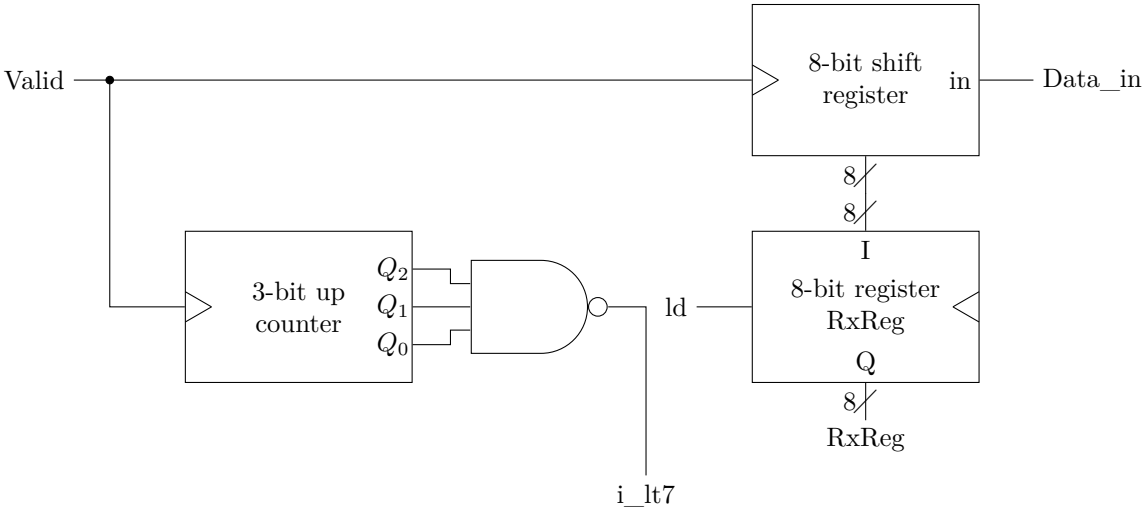


Problem 4.

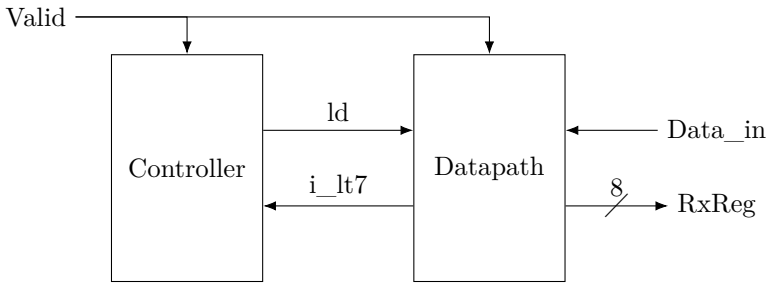
Step 1: HLSM Design
Inputs: Valid (bit), Data_in (bit)
Outputs: RxReg (8 bits)
Local registers: i (3 bits), r (8 bits)



Step 2: Datapath Design



Step 3: Connect the datapath to a controller



Step 4: FSM Design
Inputs: Valid, i_lt7
Outputs: ld