

# VE270 Homework 8

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## Problem 1.

1. The truth table is

$s_2$	$s_1$	$s_0$	$X$	$n_2$	$n_1$	$n_0$	$Y$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

The equations are

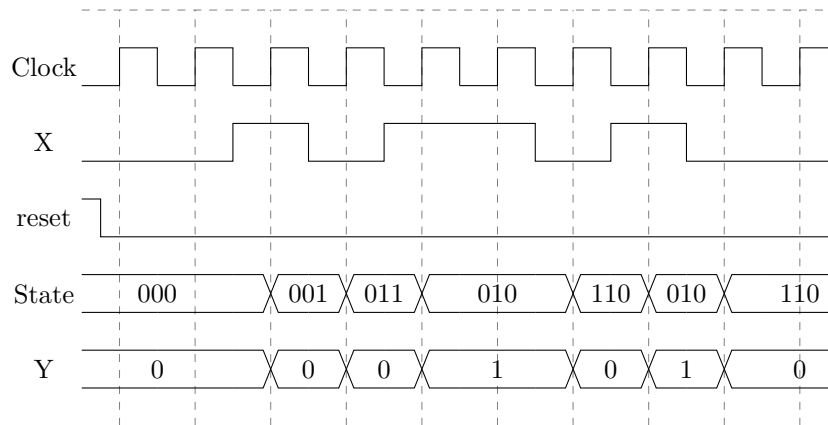
$$n_2 = s'_2 s_1 s'_0 X'$$

$$n_1 = s'_2 s_1 s'_0 + s'_1 s_0 + s_1 X$$

$$n_0 = s'_1 s'_0 X + s'_1 s_0 X'$$

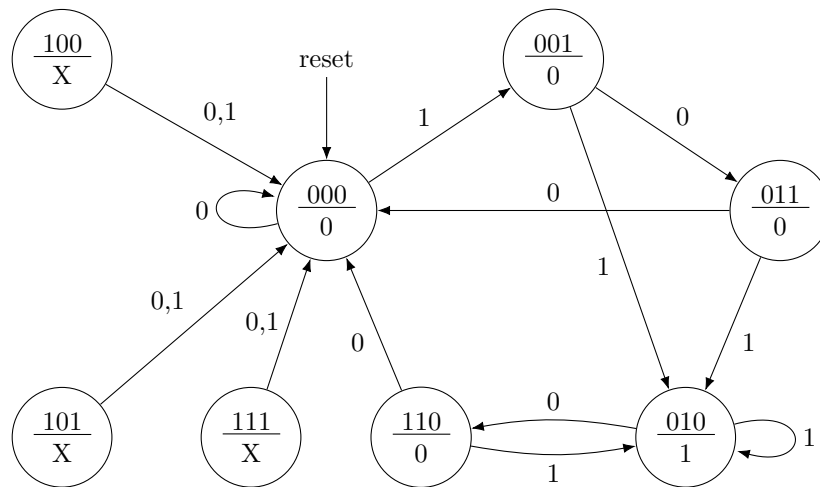
$$Y = s'_2 s_1 s'_0$$

2.



3. The state diagram is

Inputs:  $X$ ; Outputs:  $Y$



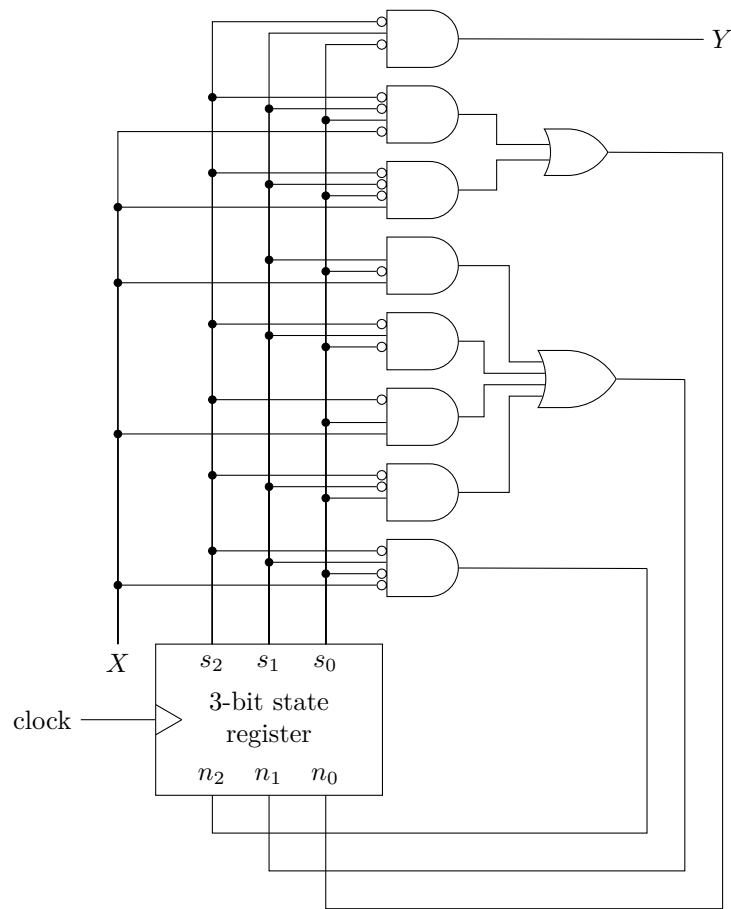
The truth table is

$s_2$	$s_1$	$s_0$	$X$	$n_2$	$n_1$	$n_0$	$Y$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

The euqations are

$$\begin{aligned}
n_2 &= s'_2 s_1 s'_0 X' \\
n_1 &= s'_2 s'_1 s_0 + s'_2 s_0 X + s'_2 s_1 s'_0 + s_1 s'_0 X \\
n_0 &= s'_2 s'_1 s'_0 X + s'_2 s'_1 s_0 X' \\
Y &= s'_2 s_1 s'_0
\end{aligned}$$

The schematics is



## Problem 2.

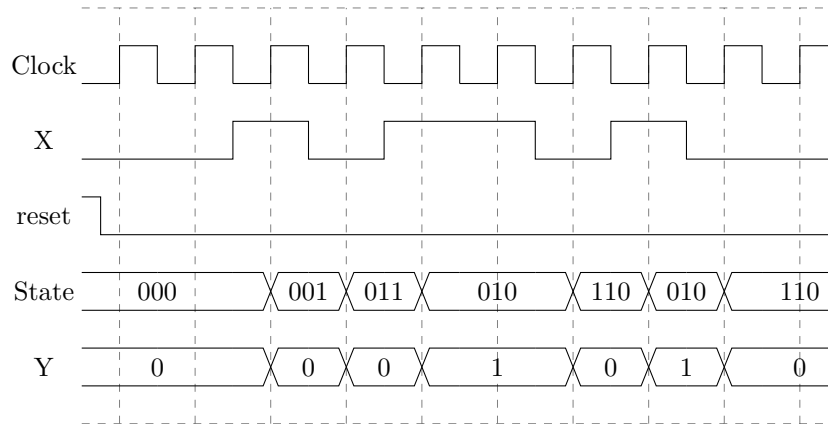
1. The truth table is

$s_2$	$s_1$	$s_0$	$X$	$n_2$	$n_1$	$n_0$	$Y$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

The euqations are

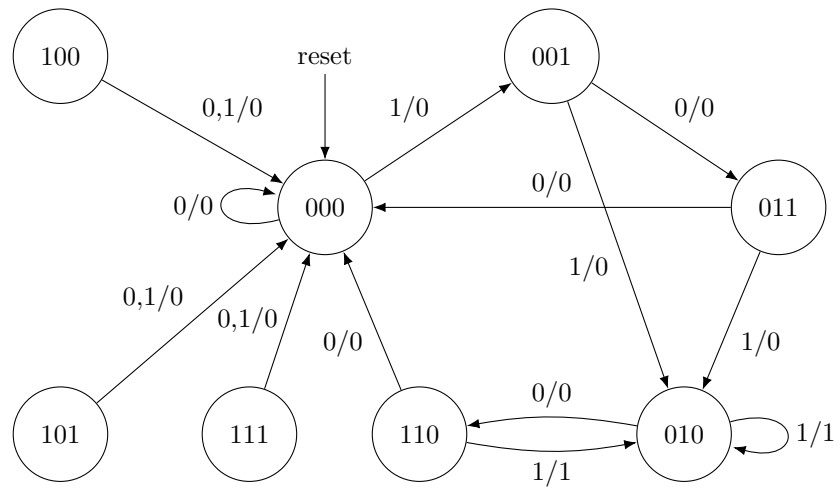
$$\begin{aligned}
n_2 &= s'_2 s_1 s'_0 X' \\
n_1 &= s'_2 s_1 s'_0 + s'_1 s_0 + s_1 X \\
n_0 &= s'_1 s'_0 X + s'_1 s_0 X' \\
Y &= s_1 s'_0 X
\end{aligned}$$

2.



3. The state diagram is

Inputs:  $X$ ; Outputs:  $Y$



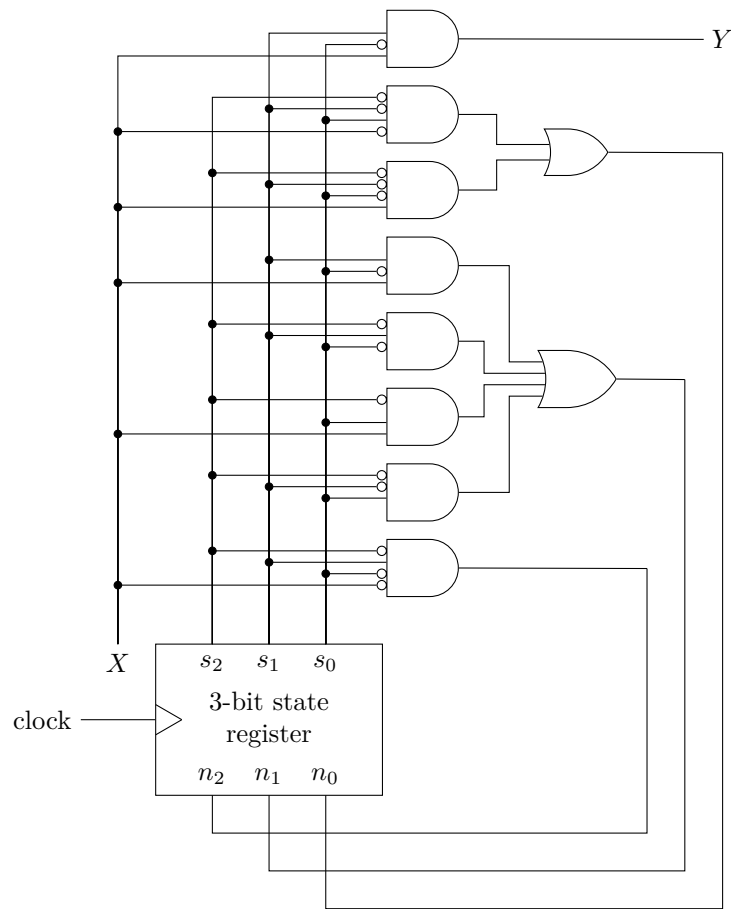
The truth table is

$s_2$	$s_1$	$s_0$	$X$	$n_2$	$n_1$	$n_0$	$Y$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

The euqations are

$$\begin{aligned}
n_2 &= s'_2 s_1 s'_0 X' \\
n_1 &= s'_2 s'_1 s_0 + s'_2 s_0 X + s'_2 s_1 s'_0 + s_1 s'_0 X \\
n_0 &= s'_2 s'_1 s'_0 X + s'_2 s'_1 s_0 X' \\
Y &= s_1 s'_0 X
\end{aligned}$$

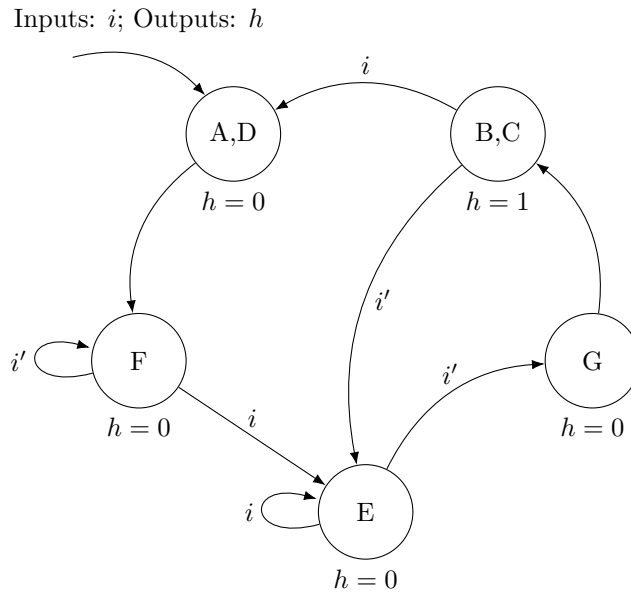
The schematics is



### Problem 3.

B	<del>X</del>					
C	<del>X</del>	(E,E) (D,A)				
D	(F,F)	<del>X</del>	<del>X</del>			
E	(G,F) (E,F)	<del>X</del>	<del>X</del>	(G,F) (E,F)		
F	(F,F) (E,F)	<del>X</del>	<del>X</del>	(F,F) (E,F)	(F,G) (E,E)	
G	(C,F) (B,F)	<del>X</del>	<del>X</del>	(C,F) (B,F)	(C,G) (B,E)	(C,F) (B,E)
	A	B	C	D	E	F

So we can find that (A,D) and (B,C) are two pairs of equivalent state. The optimized FSM diagram is



#### Problem 4.

Straightforward 2-bit binary encoding:

The truth table is

$s_1$	$s_0$	$n_1$	$n_0$	$W$	$X$	$Y$
0	0	0	1	1	0	0
0	1	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	0	0	0

The equations are

$$n_1 = s'_1 s_0 + s_1 s'_0$$

$$n_0 = s'_0$$

$$W = s'_1 s'_0$$

$$X = s'_1 s_0$$

$$Y = s_1 s'_0$$

The logic size is 8, the delay is 1.

3-bit output encoding:

The truth table is

$s_2$	$s_1$	$s_0$	$n_2$	$n_1$	$n_0$	$W$	$X$	$Y$
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	0
0	1	1	X	X	X	X	X	X
1	0	0	0	1	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X



The euqations are

$$n_2 = s_2' s_1' s_0'$$

$$n_1 = s_2$$

$$n_0 = s_1$$

$$W = s_2$$

$$X = s_1$$

$$Y = s_0$$

The logic size is 3, the delay is 1.

One-hot encoding:

The truth table is

$s_3$	$s_2$	$s_1$	$s_0$	$n_3$	$n_2$	$n_1$	$n_0$	$W$	$X$	$Y$
0	0	0	0	X	X	X	X	X	X	X
0	0	0	1	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0	0	1	0
0	0	1	1	X	X	X	X	X	X	X
0	1	0	0	1	0	0	0	0	0	1
0	1	0	1	X	X	X	X	X	X	X
0	1	1	0	X	X	X	X	X	X	X
0	1	1	1	X	X	X	X	X	X	X
1	0	0	0	0	0	0	1	0	0	0
1	0	0	1	X	X	X	X	X	X	X
1	0	1	0	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X

The euqations are

$$n_3 = s_2$$

$$n_2 = s_1$$

$$n_1 = s_0$$

$$n_0 = s_3$$

$$W = s_0$$

$$X = s_1$$

$$Y = s_2$$

The logic size is 0, the delay is 0.