VE270 Homework 8

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Problem 1.

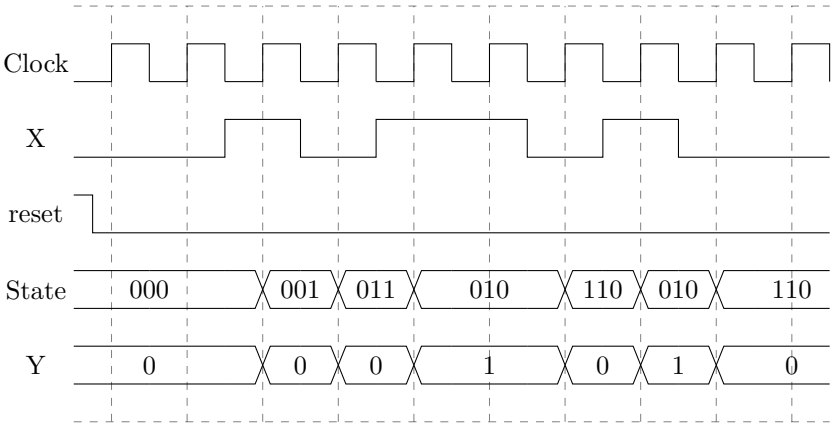
1. The truth table is

s_2	s_1	s_0	X	n_2	n_1	n_0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

   The euqations are

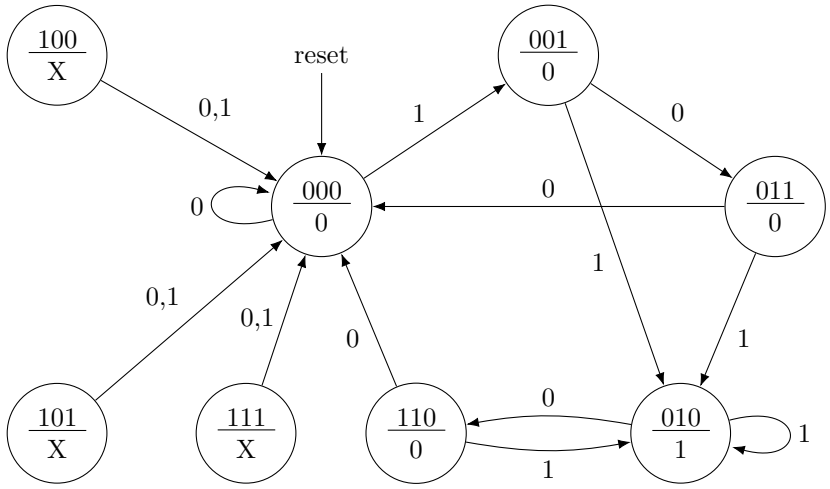
$$n_2 = s_2' s_1 s_0' X'$$
$$n_1 = s_2' s_1 s_0' + s_1' s_0 + s_1 X$$
$$n_0 = s_1' s_0' X + s_1' s_0 X'$$
$$Y = s_2' s_1 s_0'$$

2.



3. The state diagram is

Inputs: X; Outputs: Y



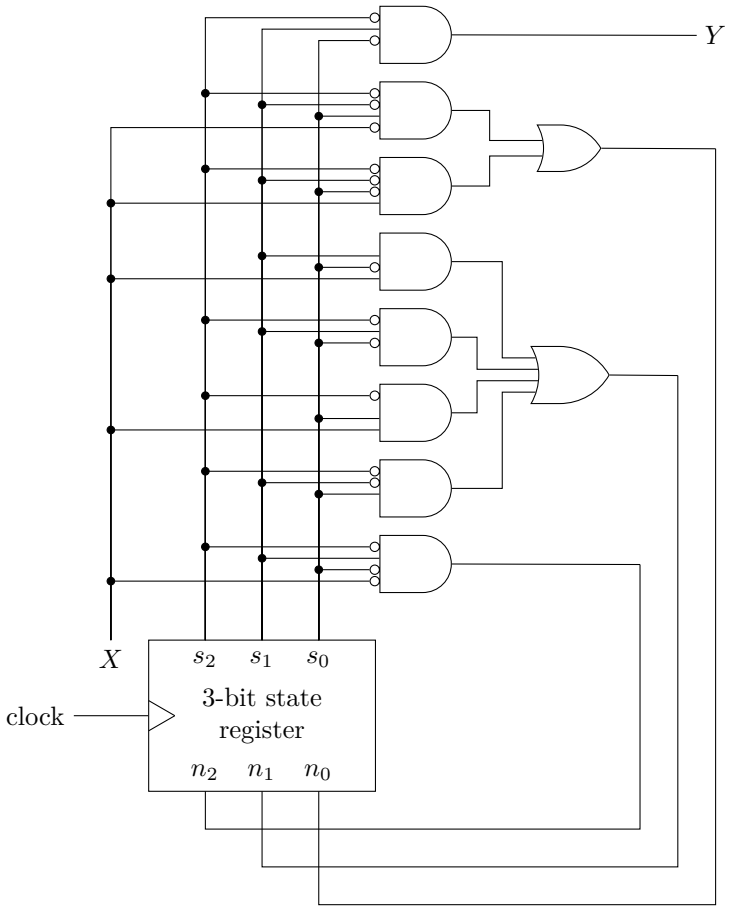
The truth table is

s_2	s_1	s_0	X	n_2	n_1	n_0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

The euqations are

$$n_2 = s_2' s_1 s_0' X'$$
$$n_1 = s_2' s_1' s_0 + s_2' s_0 X + s_2' s_1 s_0' + s_1 s_0' X$$
$$n_0 = s_2' s_1' s_0' X + s_2' s_1' s_0 X'$$
$$Y = s_2' s_1 s_0'$$

The schematics is



Problem 2.

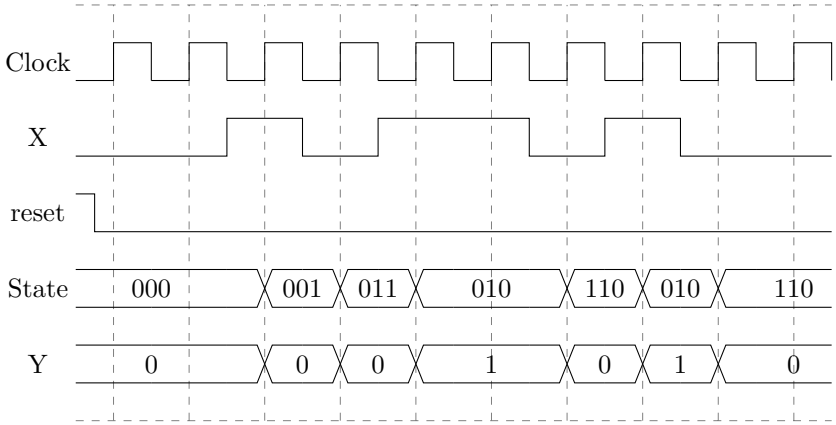
1. The truth table is

s_2	s_1	s_0	X	n_2	n_1	n_0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

The euqations are

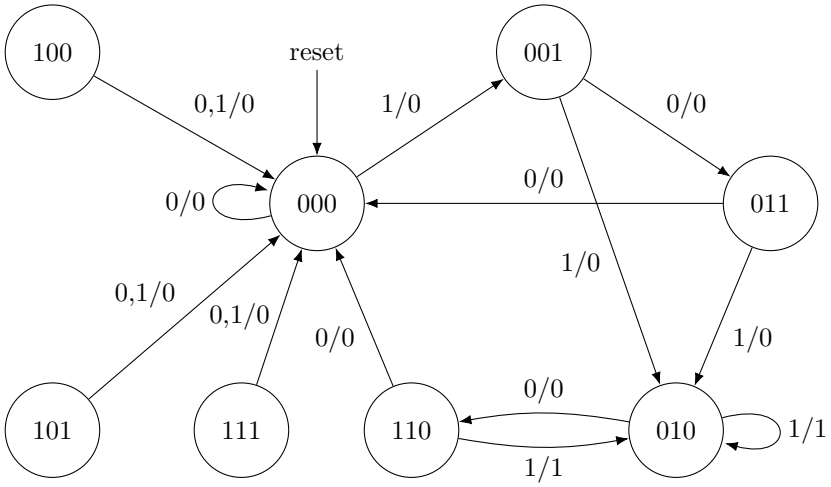
$$n_2 = s_2' s_1 s_0' X'$$
$$n_1 = s_2' s_1 s_0' + s_1' s_0 + s_1 X$$
$$n_0 = s_1' s_0' X + s_1' s_0 X'$$
$$Y = s_1 s_0' X$$

2.



3. The state diagram is

Inputs: X; Outputs: Y



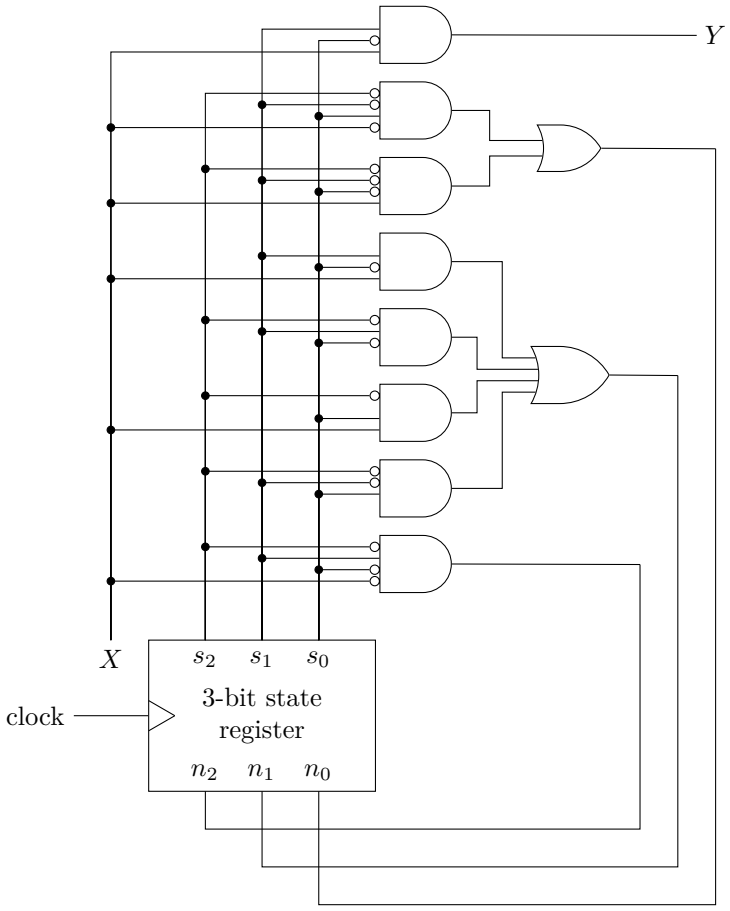
The truth table is

s_2	s_1	s_0	X	n_2	n_1	n_0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

The euqations are

$$n_2 = s_2' s_1 s_0' X'$$
$$n_1 = s_2' s_1' s_0 + s_2' s_0 X + s_2' s_1 s_0' + s_1 s_0' X$$
$$n_0 = s_2' s_1' s_0' X + s_2' s_1' s_0 X'$$
$$Y = s_1 s_0' X$$

The schematics is

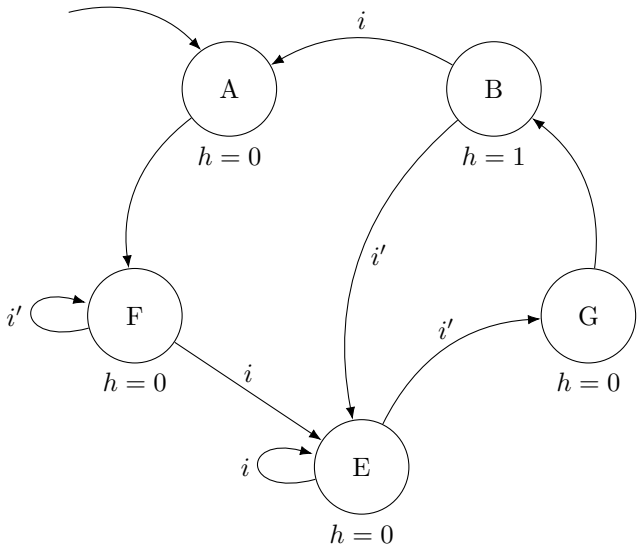


Problem 3.

	A	B	C	D	E	F
B	~~(A,B)~~					
C	~~(A,C)~~	(E,E) (D,A)				
D	(F,F)	~~(B,D)~~	~~(C,D)~~			
E	~~(G,F)~~ (E,F)	~~(B,E)~~	~~(C,E)~~	~~(G,F)~~ (E,F)		
F	~~(F,F)~~ (E,F)	~~(B,F)~~	~~(C,F)~~	~~(F,F)~~ (E,F)	~~(F,G)~~ (E,E)	
G	~~(C,F)~~ (B,F)	~~(B,G)~~	~~(C,G)~~	~~(C,F)~~ (B,F)	(C,G) (B,E)	~~(C,F)~~ (B,E)

So we can find that (A,D) and (B,C) are two pairs of equivalent state.
The optimized FSM diagram is

Inputs: i; Outputs: h



Problem 4.

Straightforward 2-bit binary encoding:
The truth table is

s_1	s_0	n_1	n_0	W	X	Y
0	0	0	1	1	0	0
0	1	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	0	0	0

The euqations are

$$n_1 = s_1' s_0 + s_1 s_0'$$
$$n_0 = s_0'$$
$$W = s_1' s_0'$$
$$X = s_1' s_0$$
$$Y = s_1 s_0'$$

The logic size is 8, the delay is 1.

3-bit output encoding:
The truth table is

s_2	s_1	s_0	n_2	n_1	n_0	W	X	Y
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	0
0	1	1	X	X	X	X	X	X
1	0	0	0	1	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X

The euqations are

$$n_2 = s_2' s_1' s_0'$$

$$n_1 = s_2$$

$$n_0 = s_1$$

$$W = s_2$$

$$X = s_1$$

$$Y = s_0$$

The logic size is 3, the delay is 1.

One-hot encoding:
The truth table is

s_3	s_2	s_1	s_0	n_3	n_2	n_1	n_0	W	X	Y
0	0	0	0	X	X	X	X	X	X	X
0	0	0	1	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0	0	1	0
0	0	1	1	X	X	X	X	X	X	X
0	1	0	0	1	0	0	0	0	0	1
0	1	0	1	X	X	X	X	X	X	X
0	1	1	0	X	X	X	X	X	X	X
0	1	1	1	X	X	X	X	X	X	X
1	0	0	0	0	0	0	1	0	0	0
1	0	0	1	X	X	X	X	X	X	X
1	0	1	0	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X

The euqations are

$$n_3 = s_2$$

$$n_2 = s_1$$

$$n_1 = s_0$$

$$n_0 = s_3$$

$$W = s_0$$

$$X = s_1$$

$$Y = s_2$$

The logic size is 0, the delay is 0.