VE270 Homework 10

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Problem 1.

(a) The truth table is

s_2	s_1	s_0	B	S	n_2	n_1	n_0	L	$Dreg\_clr$	$Dreg\_ld$	$Dctr\_clr$	$Dctr\_ld$
0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	1	0	0	1	0	1	0	0	0
0	0	0	1	0	0	0	1	0	1	0	0	0
0	0	0	1	1	0	0	1	0	1	0	0	0
0	0	1	0	0	0	1	0	0	0	0	1	0
0	0	1	0	1	0	1	0	0	0	0	1	0
0	0	1	1	0	0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1	0	0	0	1	0
0	1	0	0	0	0	1	1	1	0	0	0	0
0	1	0	0	1	0	1	1	1	0	0	0	0
0	1	0	1	0	0	1	1	1	0	0	0	0
0	1	0	1	1	0	1	1	1	0	0	0	0
0	1	1	0	0	0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	0	0	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0	0	1
0	1	1	1	1	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	0	0	1	0	0
1	0	0	0	1	0	0	1	0	0	1	0	0
1	0	0	1	0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	0	1	0	0	1	0	0
1	0	1	0	0	X	X	X	X	X	X	X	X
1	0	1	0	1	X	X	X	X	X	X	X	X
1	0	1	1	0	X	X	X	X	X	X	X	X
1	0	1	1	1	X	X	X	X	X	X	X	X
1	1	0	0	0	X	X	X	X	X	X	X	X
1	1	0	0	1	X	X	X	X	X	X	X	X
1	1	0	1	0	X	X	X	X	X	X	X	X
1	1	0	1	1	X	X	X	X	X	X	X	X
1	1	1	0	0	X	X	X	X	X	X	X	X
1	1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	1	X	X	X	X	X	X	X	X

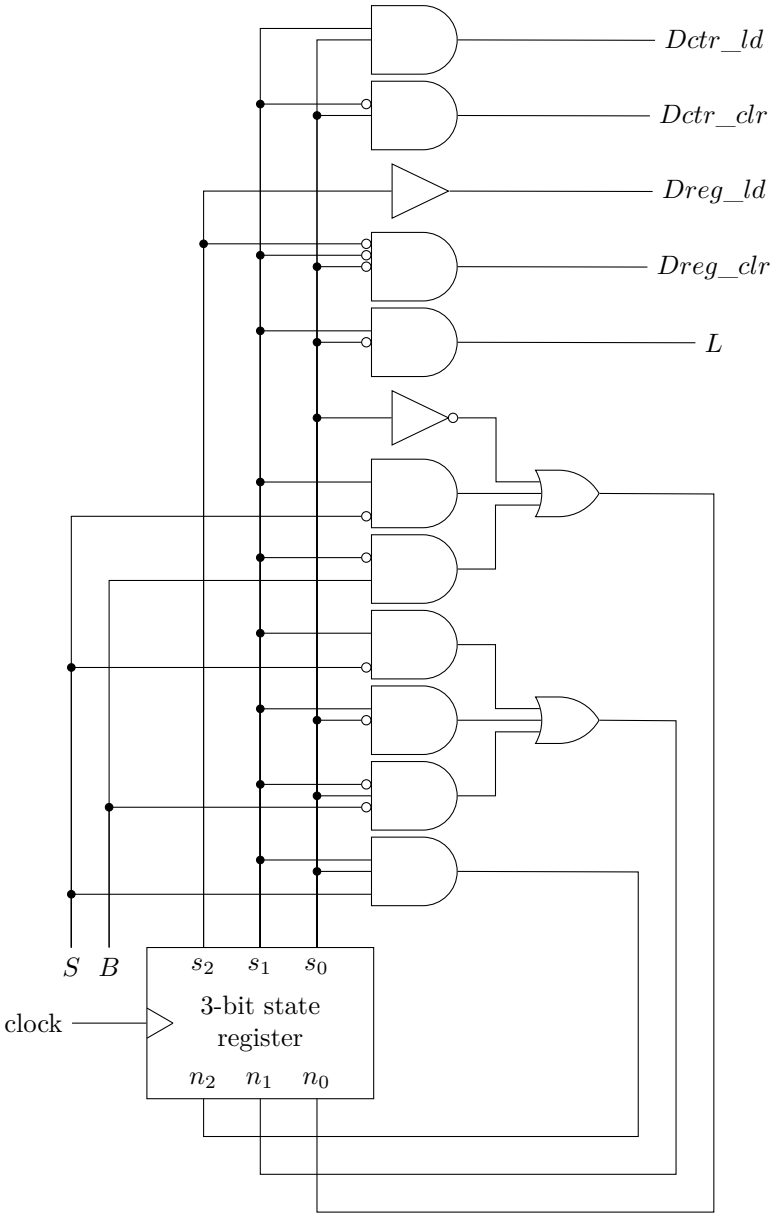
The euqations are

$$n_2 = s_1 s_0 S$$

$$n_1 = s_1' s_0 B' + s_1 s_0' + s_1 S'$$

$$n_0 = s_1' B + s_1 S' + s_0'$$
$$L = s_1 s_0'$$
$$Dreg\_clr = s_2' s_1' s_0'$$
$$Dreg\_ld = s_2$$
$$Dctr\_clr = s_1' s_0$$
$$Dctr\_ld = s_1 s_0$$

The schematics is



(b) The critical path is the 16-bit up counter, so the delay is 5 ns.

(c) The maximum clock frequency is $1/5\,\text{ns} = 200\,\text{MHz}$.

Problem 2.

The SRAM block can have $2^{32} \times 8 = 34359738368$ bits in maximum.

Problem 3.

The approximate number of SRAM bit storage cells is $\lfloor 10000000/6 \rfloor = 1666666$.

Problem 4.

SRAM cells have 6 transistors and is faster but DRAM cells have only 1 transistor and is slower. What's more, DRAM uses capacitor which discharges overtime so that it must be refreshed regularly, but SRAM needn't.

Problem 5.

EEPROMs are erased electronically, but flash memories can be erased simultaneously.

Problem 6.