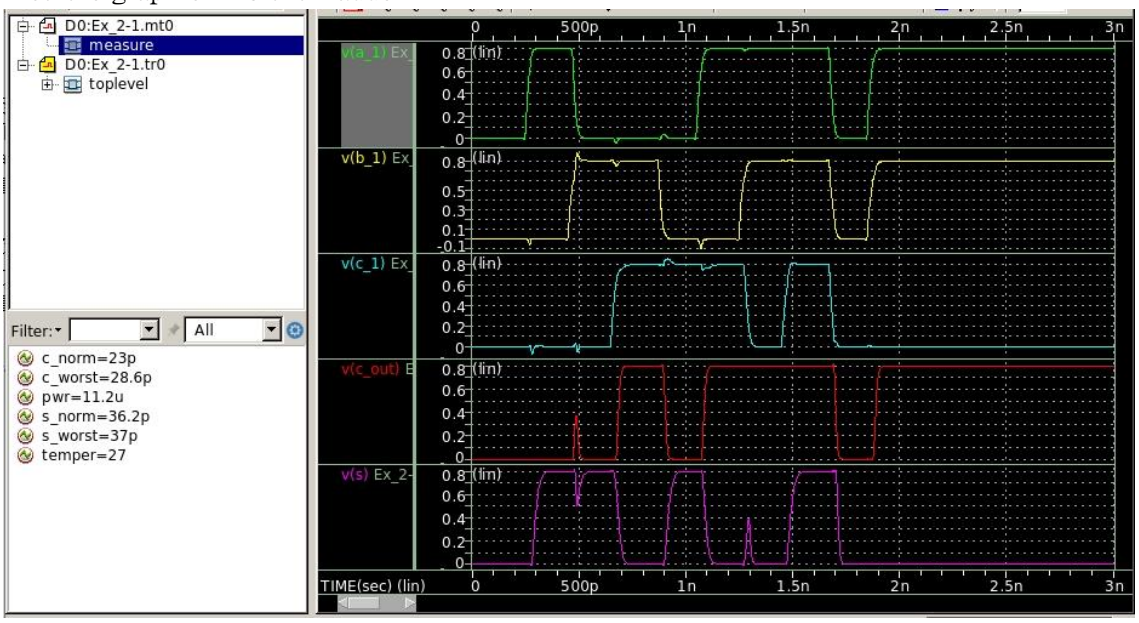
Exercise 2-1:

- Plot the graph of 1-bit full adder

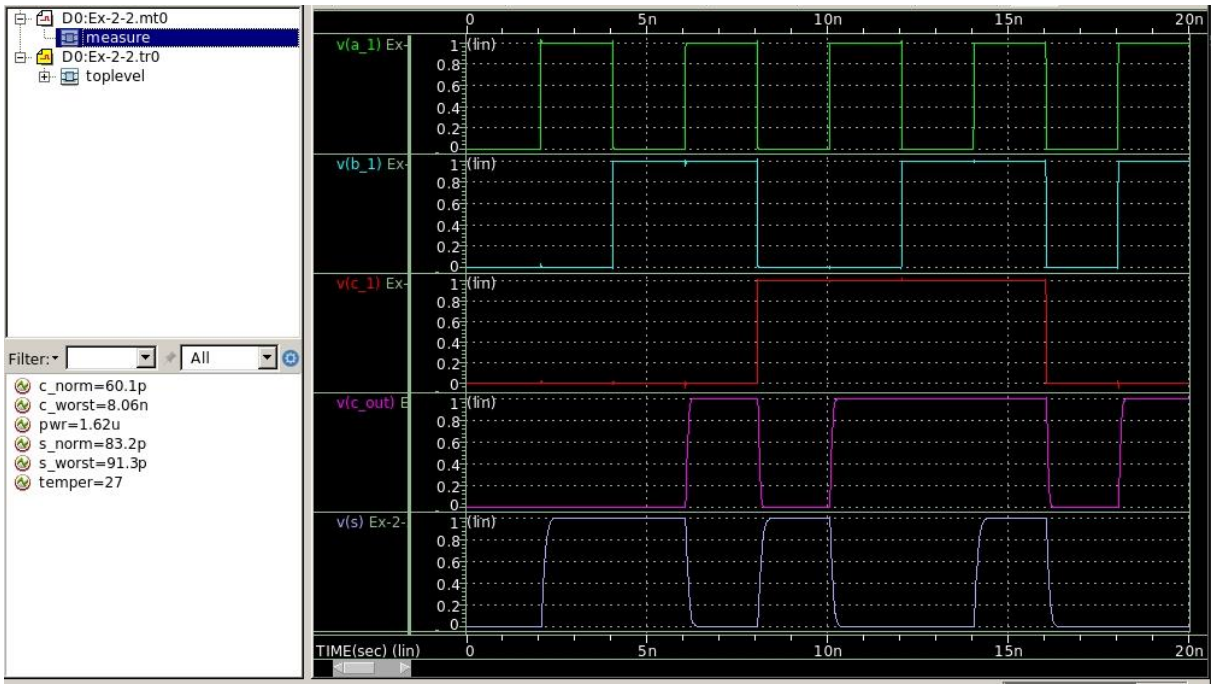


-

為了找到 worst case delay，我們必須先找到電路的 critical path 是哪一條，可以透過發送兩個測試訊號，這兩個訊號可以使 critical path 上的一個 gate 改變其初始值。根據觀察， critical path 必定從 input ‘a_1’ 或 ‘b_1’ 開始，而 S 的 worst case transition delay 是從 000 到 001，c_out 的 worst case transition delay 是從 000 到 011。

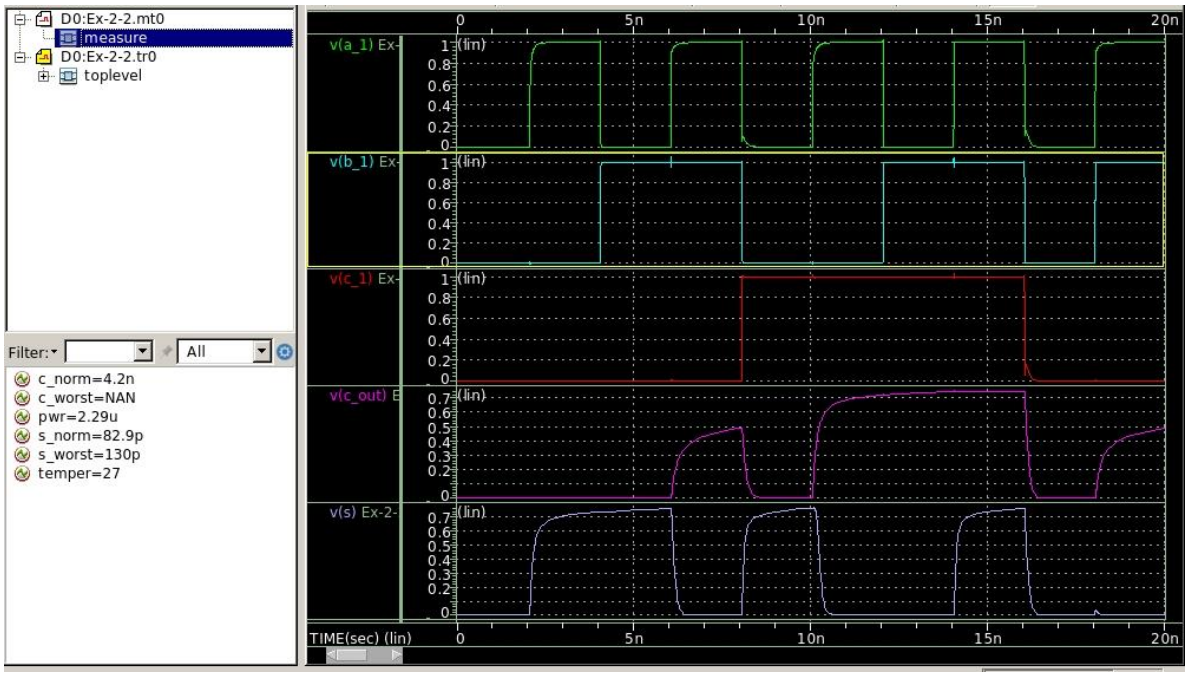
Exercise 2-2:

- CMOS



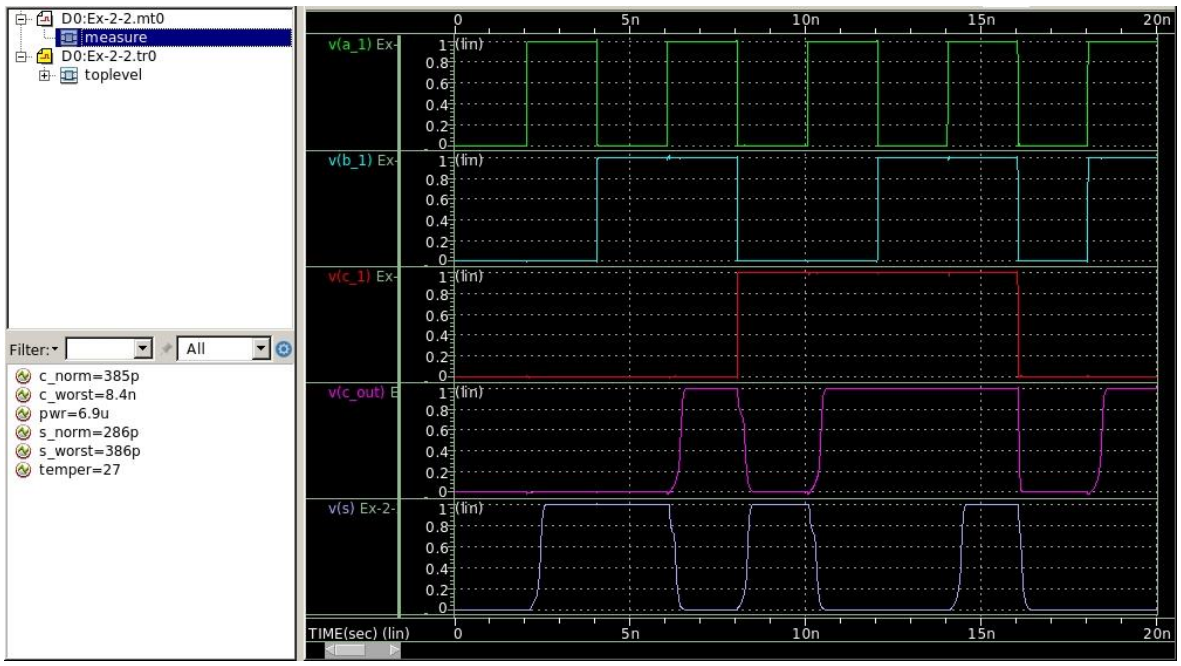
Average Power = 1.62uW, Delay = 91.3ps, Area = 28 transistors.

➢ CPL



Average Power = 2.29uW, Delay = 130ps, Area = 20 transistors.

➢ DVCS



Average Power = 6.9uW, Delay = 385ps, Area = 30 transistors.

Exercise 2-3:

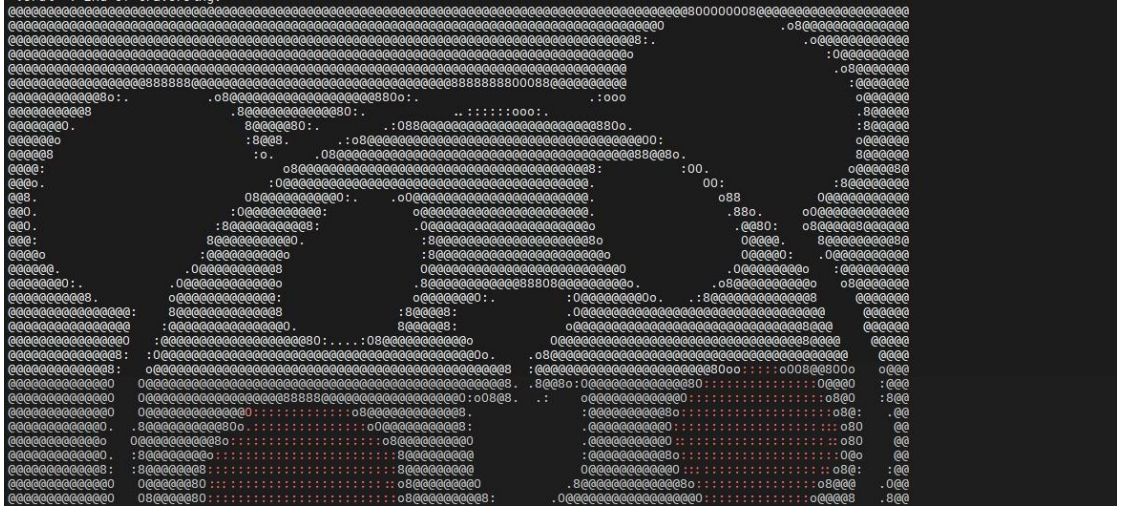
- 電路的 delay time 分析

```
****************************************

Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_08302018
Wire Load Model Mode: top

  Startpoint: B[0] (input port)
  Endpoint: Output[4] (output port)
  Path Group: default
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  B[0] (in)                                0.00       0.00 r
  U4/Y (NAND2xp5_ASAP7_75t_R)             17.78      17.78 f
  U16/Y (NAND3xp33_ASAP7_75t_R)           15.20      32.98 r
  U17/Y (NAND3xp33_ASAP7_75t_R)           22.36      55.34 f
  U20/Y (INVx1_ASAP7_75t_R)               12.23      67.57 r
  U22/Y (NAND2xp5_ASAP7_75t_R)             8.95      76.53 f
  U24/Y (NAND2xp5_ASAP7_75t_R)             6.63      83.16 r
  Output[4] (out)                          0.00      83.16 r
  data arrival time                                  83.16

  max_delay                               90.00      90.00
  output external delay                    0.00      90.00
  data required time                                 90.00
  -----------------------------------------------------------
  data required time                                 90.00
  data arrival time                                 -83.16
  -----------------------------------------------------------
  slack (MET)                                         6.84


1
exit

Memory usage for this session 168 Mbytes.
Memory usage for this session including child processes 168 Mbytes.
CPU usage for this session 2 seconds ( 0.00 hours ).
Elapsed time for this session 9 seconds ( 0.00 hours ).

Thank you ...
```

The critical paths : B[0] -> NAND2xp5 -> NAND3xp33 -> NAND3xp33 -> INVx1 -> NAND2xp5 -> NAND2xp5 -> output[4]

- Verify in gate leve
-

```
21:02 dic290@ee21[~/Hw2/Ex_2-3_and_2-4/supplement]$ irun TESTBED_Adder_4bit.v -define RTL -debug -notimingchecks -loadpli1 debpli:novas_pli_boot
irun(64): 15.20-s084: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
Loading snapshot worklib.TESTBED:v ..... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/INCISIVE_15.20.084/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi_P-2019.06, Linux x86_64/64bit, 05/26/2019
(C) 1996 - 2019 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'Adder_4bit.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
```



- 電路的 delay time 分析

```
Number of ports:                           13
Number of nets:                            30
Number of cells:                           22
Number of combinational cells:             22
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          2
Number of references:                       7

Combinational area:                30.093120
Buf/Inv area:                       1.399680
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   30.093120
Total area:                 undefined
1
report_timing
```

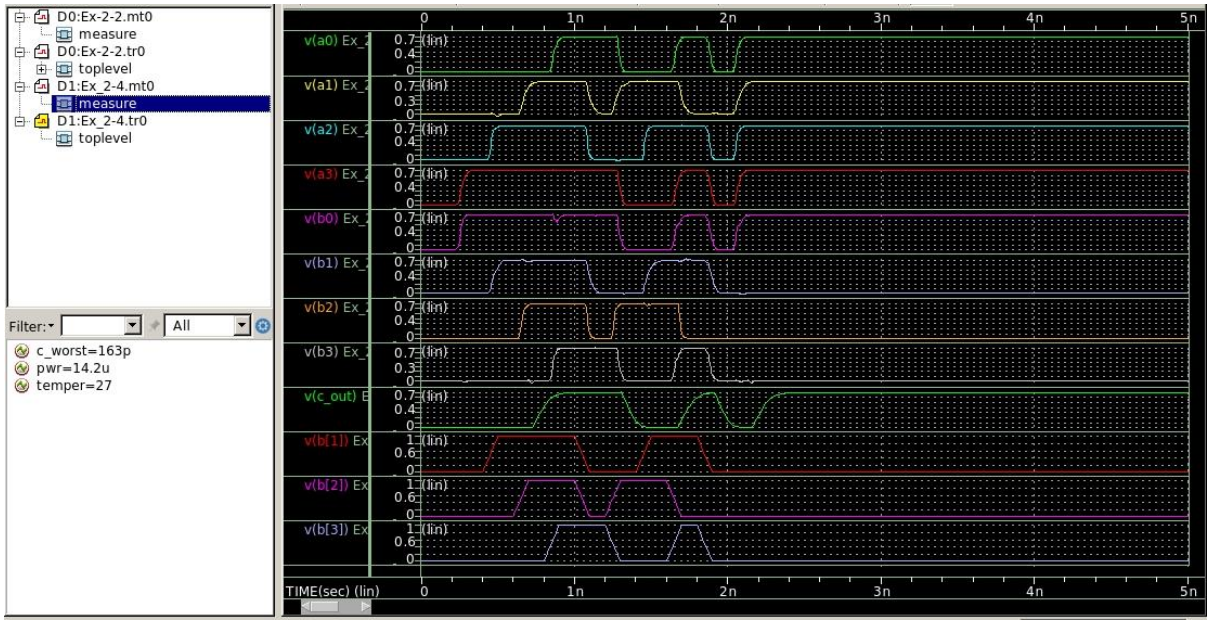
描述該電路所使用的 port 數、net 數、cell 數，代表該電路所用的面積大 小，通常要做面積優化或比較時會以此報告為依據，不論是 combination circuit 還是 sequence circuit，電路優化時最重要的就是 critical path 的時間，因為其代表花費最多時間的那條路徑，如圖二所示， design compiler 會自動從元件庫中選擇適合的邏輯閘來合成，因此，report 中所 顯示的是 critical path 上的邏輯閘延遲時間。

Exercise 2-4:

- CMOS Logics for 4-bit Adder

透過.vec 檔撰寫波形，舉例來說，0 到 200ps 的波形，A 的 input 訊號 是 1110、B 的 input 訊號是 0001，得到的 Output + carry out 訊號是 10000，確實能執行 4 位元的加法功能，而接下來會利用 Hspice 去對 critical path 的 delay 和 power 做測量，做出較為精確的分析。

➢ Waveform



{C_out, S} = A+B, so result is correct.

The worst delay = 163ps, average power = 14.2uW