DIC HW3

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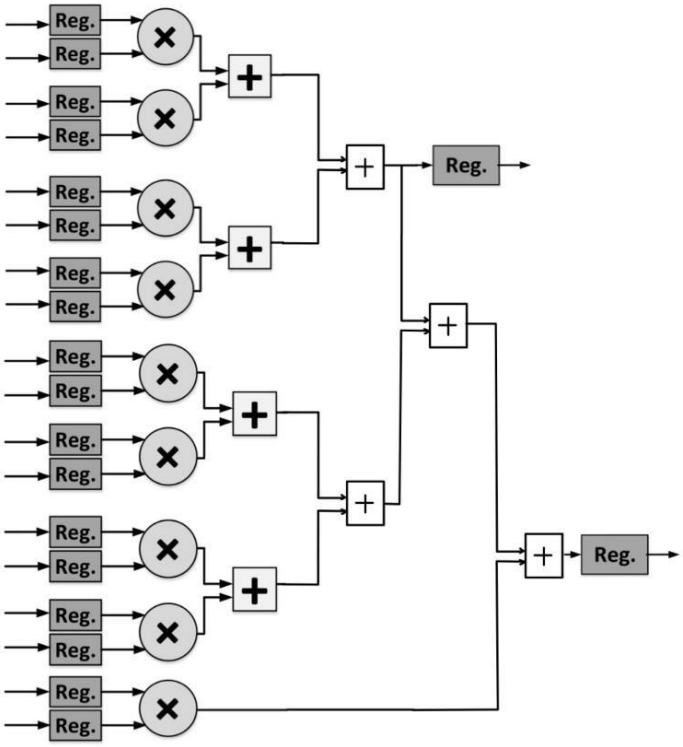
➢ Time/Area Analysis of Sequential Circuits

1. without pipeline techniques



Clock period = 1.5 ns

Timing report :

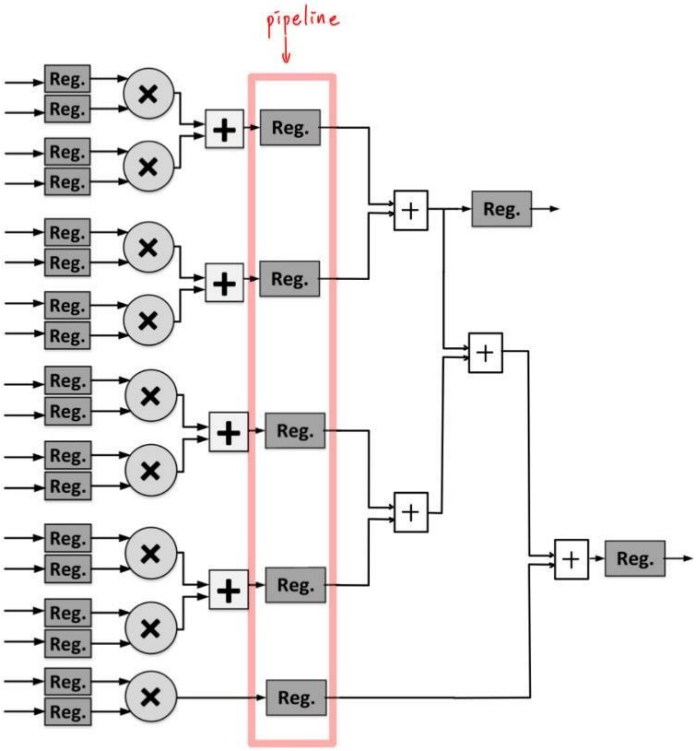
```
clock clk (rise edge)                                  1500.00    1500.00
clock network delay (ideal)                               0.00    1500.00
Out_OFM_reg_33_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    1500.00 r
library setup time                                      -19.09    1480.91
data required time                                                1480.91
-------------------------------------------------------------------------
data required time                                                1480.91
data arrival time                                                -1480.78
-------------------------------------------------------------------------
slack (MET)                                                          0.14
```

Throughput: 450/(50*1500) * 10^12= 6*10^9 (ops/s)

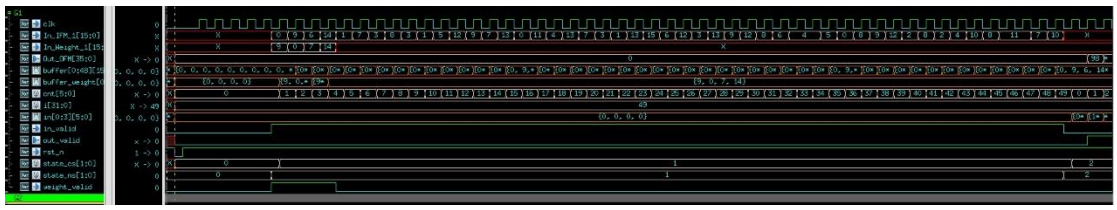
Area:

```
Number of ports:                         1578
Number of nets:                         28119
Number of cells:                        25341
Number of combinational cells:          24340
Number of sequential cells:               981
Number of macros/black boxes:               0
Number of buf/inv:                       3260
Number of references:                      68

Combinational area:              30145.374775
Buf/Inv area:                     2795.627532
Noncombinational area:            5950.039641
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 36095.414416
Total area:                 undefined
1
```

2. with pipeline techniques



Clock period = 0.9 ns



Timing report :

```
clock clk (rise edge)                                    900.00     900.00
clock network delay (ideal)                                0.00     900.00
pipe1_reg_3__31_/CLK (DFFHQx4_ASAP7_75t_R)                 0.00     900.00 r
library setup time                                       -14.26     885.74
data required time                                                  885.74
-------------------------------------------------------------------------
data required time                                                  885.74
data arrival time                                                  -885.73
-------------------------------------------------------------------------
slack (MET)                                                           0.00
```

Throughput: 450/(55*900) * 10^12= 9.09*10^9 (ops/s)

Area:

```
Number of ports:                        1533
Number of nets:                        28974
Number of cells:                       26467
Number of combinational cells:         24847
Number of sequential cells:             1600
Number of macros/black boxes:              0
Number of buf/inv:                      4296
Number of references:                     65

Combinational area:              29939.621817
Buf/Inv area:                     3348.267870
Noncombinational area:            9095.120482
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 39034.742299
Total area:                 undefined
1
```

3. Optimize

Clock period = 0.548 ns

Timing report :

```
clock clk (rise edge)                                    548.00     548.00
clock network delay (ideal)                                0.00     548.00
multi_out_reg_3__27_/CLK (DFFHQx4_ASAP7_75t_R)             0.00     548.00 r
library setup time                                       -15.53     532.47
data required time                                                  532.47
-------------------------------------------------------------------------
data required time                                                  532.47
data arrival time                                                  -532.45
-------------------------------------------------------------------------
slack (MET)                                                          0.02
```

Area:

```
Number of ports:                         1493
Number of nets:                         27529
Number of cells:                        25136
Number of combinational cells:          23615
Number of sequential cells:              1504
Number of macros/black boxes:               0
Number of buf/inv:                       4375
Number of references:                      46

Combinational area:              28429.833688
Buf/Inv area:                     3545.856025
Noncombinational area:            8493.724667
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 36923.558355
Total area:                 undefined
1
```

Area efficiency: 450/((36923*10^-6)*54*548*(10^-12)) = 412 GOPS/mm2 > 400 GOPS/mm2