DIC HW5

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1. Implement a 3x3 convolution kernel without clock gating

Area analysis (4957 < 5100 μm^2)

```
****************************************
Report : area
Design : Convolution
Version: T-2022.03
Date   : Mon Dec 25 21:13:00 2023
****************************************

Library(s) Used:

    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic290/Hw5/Ex5/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic290/Hw5/Ex5/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic290/Hw5/Ex5/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          830
Number of nets:                          4119
Number of cells:                         2947
Number of combinational cells:           2766
Number of sequential cells:               166
Number of macros/black boxes:               0
Number of buf/inv:                        546
Number of references:                      27

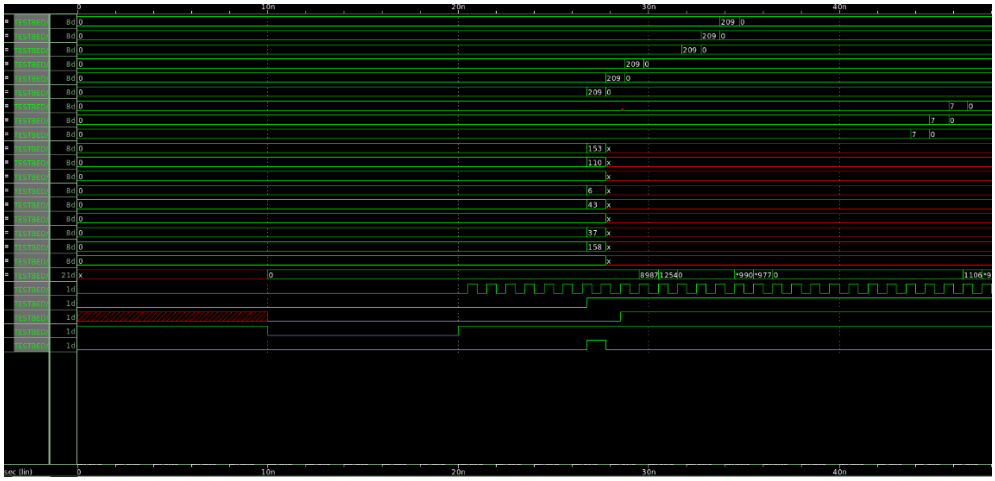
Combinational area:               3951.063341
Buf/Inv area:                      383.045765
Noncombinational area:            1006.836473
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  4957.899814
Total area:                 undefined
1
```

Clock period:

```
set DESIGN "Convolution"
set CLK_period 1000.0
set IN_DLY  [expr 0.5*$CLK_period]
set OUT_DLY [expr 0.5*$CLK_period]
```

Waveform:



Timing analysis:

```
  add_3_root_add_0_root_add_145_8/U7/Y (INVx1_ASAP7_75t_R)
                                                  15.50     692.14 f
  add_3_root_add_0_root_add_145_8/U1_14/CON (FAx1_ASAP7_75t_R)
                                                  20.36     712.50 r
  add_3_root_add_0_root_add_145_8/U6/Y (INVx1_ASAP7_75t_R)
                                                  15.50     728.00 f
  add_3_root_add_0_root_add_145_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                  37.56     765.56 f
  add_3_root_add_0_root_add_145_8/U29/Y (INVx1_ASAP7_75t_R)
                                                  18.83     784.39 r
  add_3_root_add_0_root_add_145_8/SUM[15] (Convolution_DW01_add_5)
                                                   0.00     784.39 r
  add_2_root_add_0_root_add_145_8/B[15] (Convolution_DW01_add_4)
                                                   0.00     784.39 r
  add_2_root_add_0_root_add_145_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                  35.94     820.34 r
  add_2_root_add_0_root_add_145_8/U32/Y (INVx1_ASAP7_75t_R)
                                                  17.51     837.84 f
  add_2_root_add_0_root_add_145_8/SUM[15] (Convolution_DW01_add_4)
                                                   0.00     837.84 f
  add_0_root_add_0_root_add_145_8/B[15] (Convolution_DW01_add_0)
                                                   0.00     837.84 f
  add_0_root_add_0_root_add_145_8/U1_15/CON (FAx1_ASAP7_75t_R)
                                                  22.82     860.66 r
  add_0_root_add_0_root_add_145_8/U8/Y (INVx1_ASAP7_75t_R)
                                                  15.27     875.93 f
  add_0_root_add_0_root_add_145_8/U1_16/CON (FAx1_ASAP7_75t_R)
                                                  20.30     896.23 r
  add_0_root_add_0_root_add_145_8/U7/Y (INVx1_ASAP7_75t_R)
                                                  15.27     911.50 f
  add_0_root_add_0_root_add_145_8/U1_17/CON (FAx1_ASAP7_75t_R)
                                                  20.30     931.80 r
  add_0_root_add_0_root_add_145_8/U6/Y (INVx1_ASAP7_75t_R)
                                                  15.59     947.39 f
  add_0_root_add_0_root_add_145_8/U4/Y (XOR2xp5_ASAP7_75t_R)
                                                  19.98     967.37 f
  add_0_root_add_0_root_add_145_8/SUM[18] (Convolution_DW01_add_0)
                                                   0.00     967.37 f
  U314/Y (NAND2xp5_ASAP7_75t_R)                   11.33     978.70 r
  Out_OFM_reg_18_/D (ASYNC_DFFHx1_ASAP7_75t_R)     0.00     978.70 r
  data arrival time                                         978.70

  clock clk (rise edge)                         1000.00    1000.00
  clock network delay (ideal)                      0.00    1000.00
  Out_OFM_reg_18_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)   0.00    1000.00 r
  library setup time                             -20.79     979.21
  data required time                                        979.21
  ------------------------------------------------------------------------
  data required time                                        979.21
  data arrival time                                        -978.70
  ------------------------------------------------------------------------
  slack (MET)                                                 0.50


1
```

Power Analysis:

```
Report : Time Based Power
Design : Convolution
Version: P-2019.03-SP5-1
Date   : Mon Dec 18 18:05:32 2023
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network                0.0000    0.0000    0.0000    0.0000 ( 0.00%)
register                  2.148e-04 1.566e-06 4.796e-08 2.164e-04 (85.73%)  i
combinational             1.429e-05 2.150e-05 2.271e-07 3.601e-05 (14.27%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.306e-05   ( 9.14%)
  Cell Internal Power  = 2.290e-04   (90.75%)
  Cell Leakage Power   = 2.751e-07   ( 0.11%)
    Intrinsic Leakage  = 2.751e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 2.524e-04  (100.00%)

X Transition Power     = -1.175e-08
Glitching Power        =    0.0000

Peak Power             = 6.440e-04
Peak Time              =      1169
```

(Power = 252.4 μ**W** > 150 μ**W)**

2. Implement a 3x3 convolution kernel with clock gating

Area analysis (4810 μm**^2**)

```
1
2  ****************************************
3  Report : area
4  Design : Convolution
5  Version: T-2022.03
6  Date   : Mon Dec 25 21:19:39 2023
7  ****************************************
8
9  Library(s) Used:
10
11     asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic290/Hw5/Ex5_3111511057/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
12     asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic290/Hw5/Ex5_3111511057/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
13     asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic290/Hw5/Ex5_3111511057/asap7sc7p5t_SEQ_RVT_TT_08302018.db)
14
15 Number of ports:                          837
16 Number of nets:                         3928
17 Number of cells:                        2756
18 Number of combinational cells:          2564
19 Number of sequential cells:              177
20 Number of macros/black boxes:              0
21 Number of buf/inv:                       705
22 Number of references:                     29
23
24 Combinational area:              3752.075493
25 Buf/Inv area:                     494.087047
26 Noncombinational area:           1058.158072
27 Macro/Black Box area:               0.000000
28 Net Interconnect area:      undefined  (No wire load specified)
29
30 Total cell area:                 4810.233565
31 Total area:                 undefined
32 1
33
```

Clock period:

```
set DESIGN "Convolution"
set CLK_period 1000.0
set IN_DLY  [expr 0.5*$CLK_period]
set OUT_DLY [expr 0.5*$CLK_period]
```

Timing analysis:

```
  add_3_root_add_0_root_add_192_8/U1_13/CON (FAx1_ASAP7_75t_R)
                                                  20.36     681.71 r
  add_3_root_add_0_root_add_192_8/U7/Y (INVx1_ASAP7_75t_R)
                                                  15.50     697.21 f
  add_3_root_add_0_root_add_192_8/U1_14/CON (FAx1_ASAP7_75t_R)
                                                  20.36     717.56 r
  add_3_root_add_0_root_add_192_8/U6/Y (INVx1_ASAP7_75t_R)
                                                  15.50     733.06 f
  add_3_root_add_0_root_add_192_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                  37.56     770.62 f
  add_3_root_add_0_root_add_192_8/U29/Y (INVx1_ASAP7_75t_R)
                                                  18.83     789.45 r
  add_3_root_add_0_root_add_192_8/SUM[15] (Convolution_DW01_add_5)
                                                   0.00     789.45 r
  add_2_root_add_0_root_add_192_8/B[15] (Convolution_DW01_add_4)
                                                   0.00     789.45 r
  add_2_root_add_0_root_add_192_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                  35.94     825.40 r
  add_2_root_add_0_root_add_192_8/U31/Y (INVx1_ASAP7_75t_R)
                                                  17.51     842.90 f
  add_2_root_add_0_root_add_192_8/SUM[15] (Convolution_DW01_add_4)
                                                   0.00     842.90 f
  add_0_root_add_0_root_add_192_8/B[15] (Convolution_DW01_add_0)
                                                   0.00     842.90 f
  add_0_root_add_0_root_add_192_8/U1_15/CON (FAx1_ASAP7_75t_R)
                                                  22.82     865.73 r
  add_0_root_add_0_root_add_192_8/U7/Y (INVx1_ASAP7_75t_R)
                                                  15.27     881.00 f
  add_0_root_add_0_root_add_192_8/U1_16/CON (FAx1_ASAP7_75t_R)
                                                  20.30     901.29 r
  add_0_root_add_0_root_add_192_8/U6/Y (INVx1_ASAP7_75t_R)
                                                  15.27     916.56 f
  add_0_root_add_0_root_add_192_8/U1_17/CON (FAx1_ASAP7_75t_R)
                                                  20.30     936.86 r
  add_0_root_add_0_root_add_192_8/U5/Y (INVx1_ASAP7_75t_R)
                                                  15.59     952.45 f
  add_0_root_add_0_root_add_192_8/U4/Y (XOR2xp5_ASAP7_75t_R)
                                                  19.83     972.28 f
  add_0_root_add_0_root_add_192_8/SUM[18] (Convolution_DW01_add_0)
                                                   0.00     972.28 f
  U451/Y (INVxp67_ASAP7_75t_R)                     9.53     981.81 r
  Out_OFM_reg_18_/D (ASYNC_DFFHx1_ASAP7_75t_R)     0.00     981.81 r
  data arrival time                                         981.81

  clock clk (rise edge)                         1000.00    1000.00
  clock network delay (ideal)                      0.00    1000.00
  Out_OFM_reg_18_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)   0.00    1000.00 r
  library setup time                             -16.85     983.15
  data required time                                        983.15
  ------------------------------------------------------------------------
  data required time                                        983.15
  data arrival time                                        -981.81
  ------------------------------------------------------------------------
  slack (MET)                                                 1.34


1
```

Power Analysis:

```
                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network             6.502e-06 6.011e-06 4.526e-09 1.252e-05 (13.90%)
register                  4.207e-05 1.966e-06 5.238e-08 4.409e-05 (48.97%)  i
combinational             1.354e-05 1.967e-05 2.134e-07 3.342e-05 (37.13%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.765e-05   (30.71%)
  Cell Internal Power  = 6.211e-05   (68.99%)
  Cell Leakage Power   = 2.703e-07   ( 0.30%)
    Intrinsic Leakage  = 2.703e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 9.003e-05  (100.00%)

X Transition Power     = 1.169e-06
Glitching Power        =    0.0000

Peak Power             = 5.718e-04
Peak Time              =      1168

1
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(Power = 90.03 μW < 150 μW)

將 With clock gating 與 Without clock gating 的 power 作比較，可以發現加入 clock gating 的電路耗費 power 會減少 (252.4 μW > 90.03 μW)，原因是因為當輸入 IN_IFM=0，Latch 的 Enable=1，所以進入 D flip flop 的 clock gate 會被 fixed 住，因此 D flip flop 就不會被 trigger 而讓 power 的耗費降低