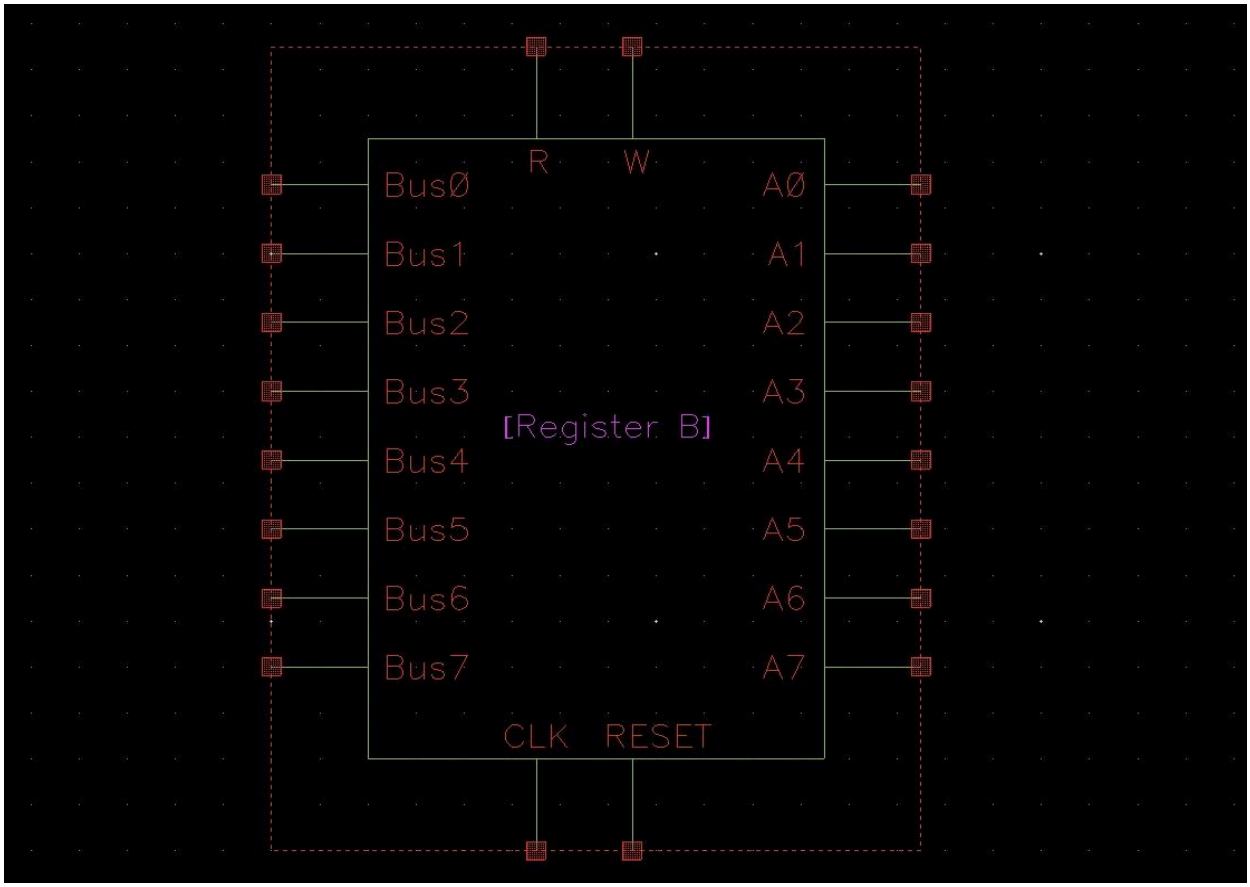
Register - B

TEAM 2 - (1) Aasha Chanpa - 202304001 (3) Divy Vasava - 202304028

(2) Astha Patel - 202304032 (4) Hiral Parmar - 202304004



8-BIT Register Symbol

TOTAL PINS - 20

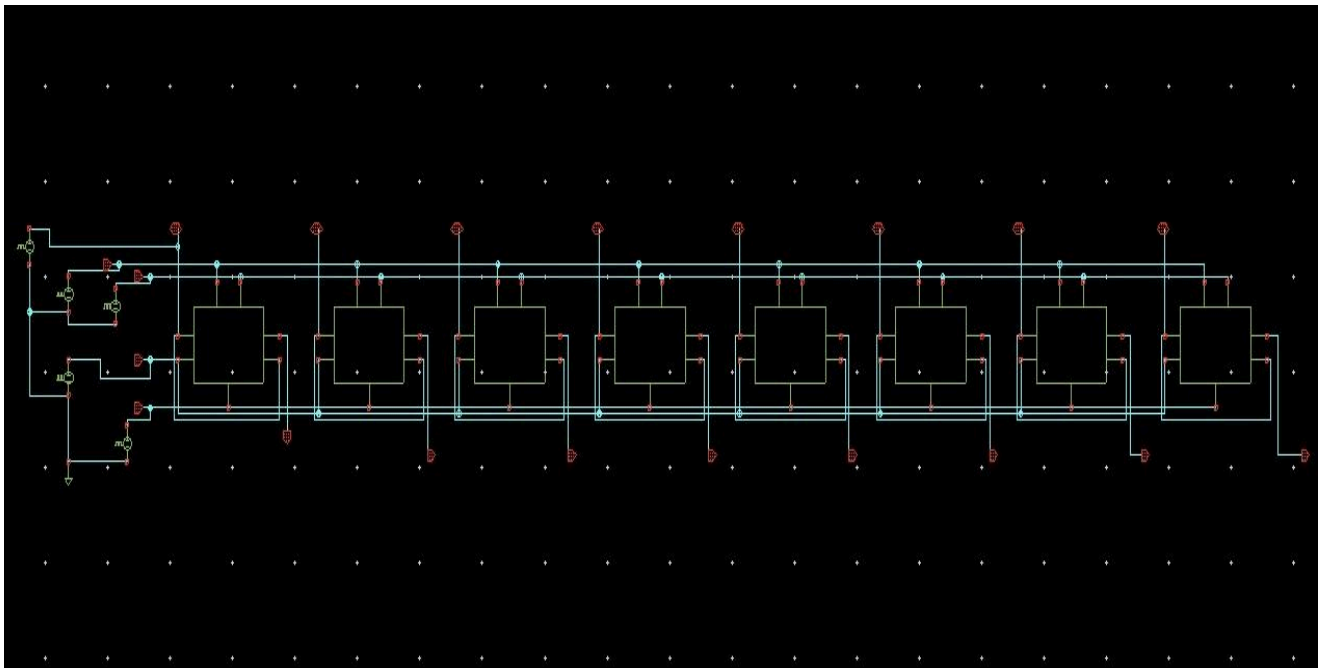
- InputOutput Pins BUS0 (LSB) to BUS7 (MSB) - Bus to register
- Output Pins A0 (LSB) to A7 (MSB) - Register to ALU
- Input Pin R and Input Pin W - to read or write the data
- Input Pin CLK and Input Pin RESET

Functionality:-

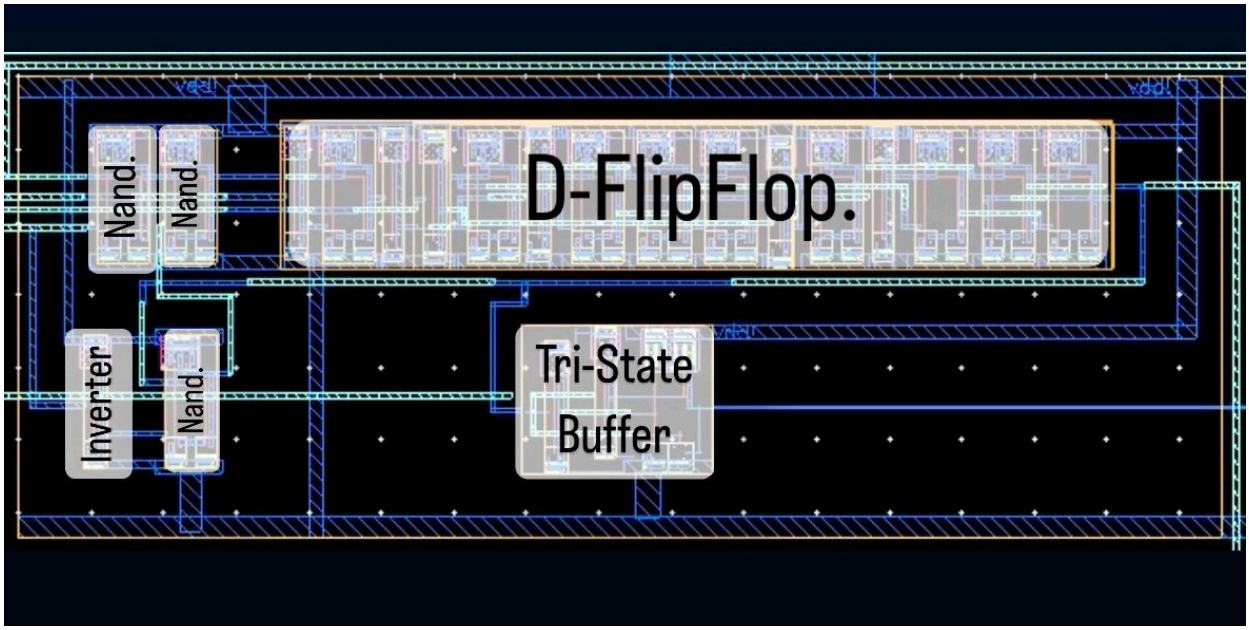
This register is built using D flip-flops made from D latches .The first latch is called the **master ,** The second latch is called the **slave**. Only when the clock changes from 0 to 1 does the value of D get passed to Q. Therefore , It acts like a rising-edge triggered flip-flop.

This register stores 8-bit of data and is designed to work as part of a larger system of 8-bit computer . It has three control lines:-

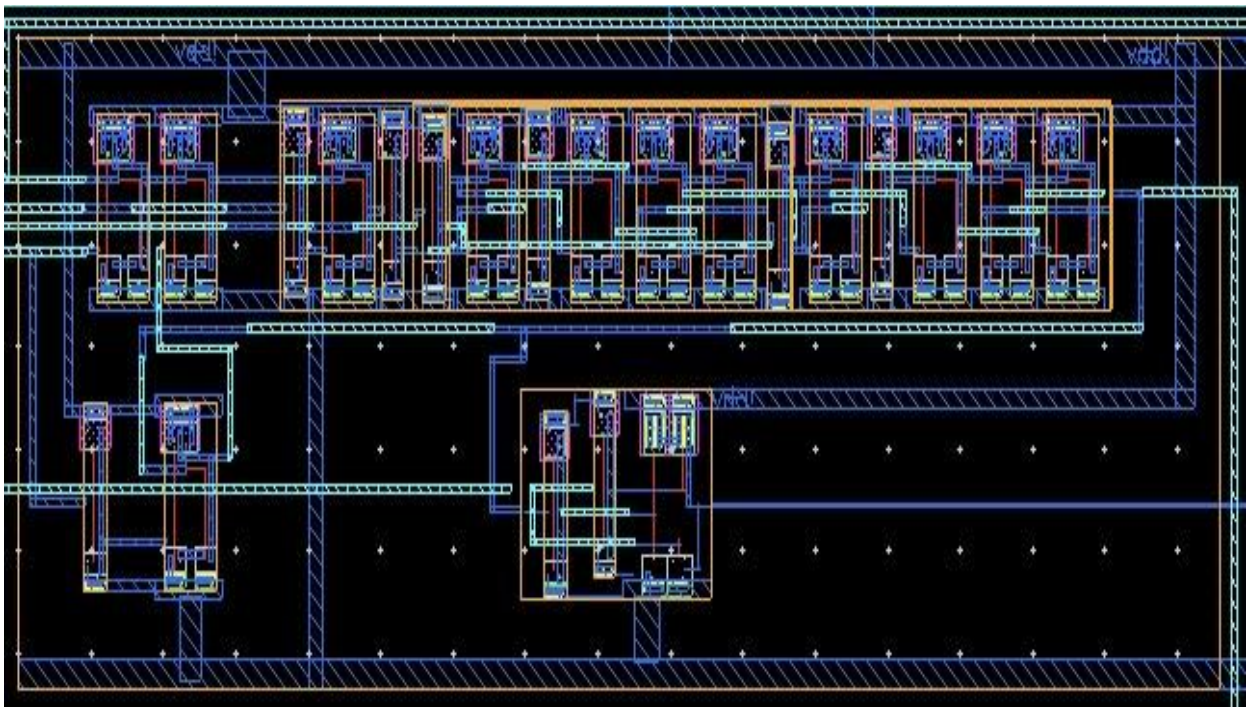
1. **W (Input Enable) :** Allows data from the bus to be loaded into the register only when it is active. When W pin is low , the register will hold the previous value
2. **R (Output Enable):** Allows the register to put the stored value back onto the shared bus when it is active. When R pin is low , the tri state buffer will open circuit the Bus and register's output (by giving high impedance as output)
3. **Clear (Reset):** A synchronous signal that resets the register output to zero when activated.



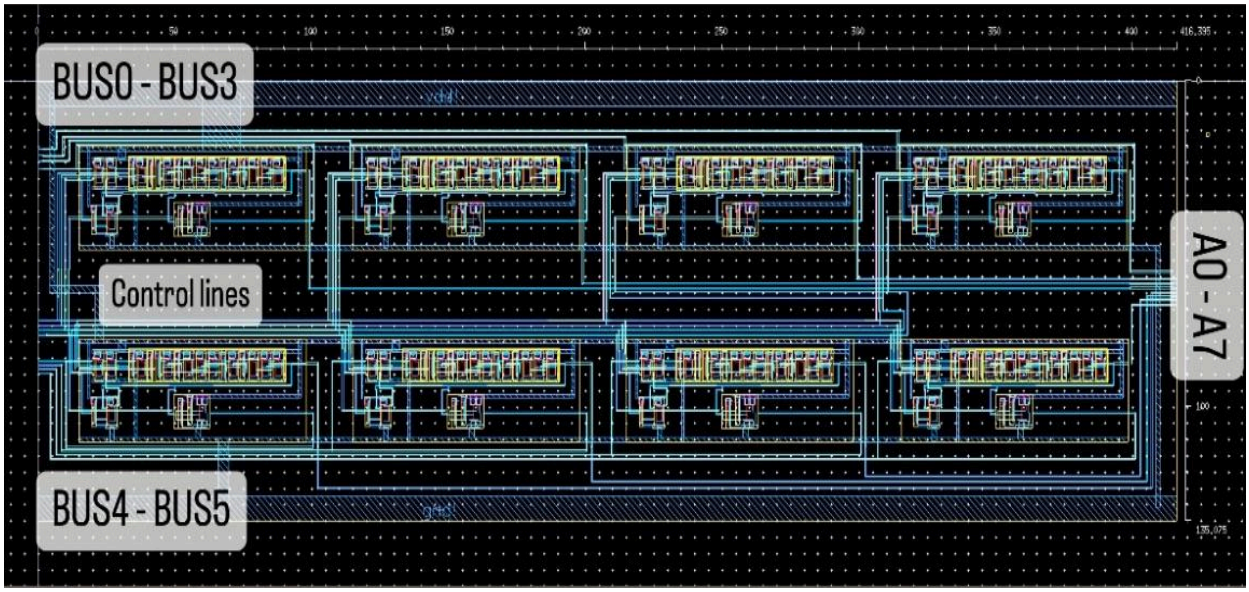
Schematic of 8 bit Register



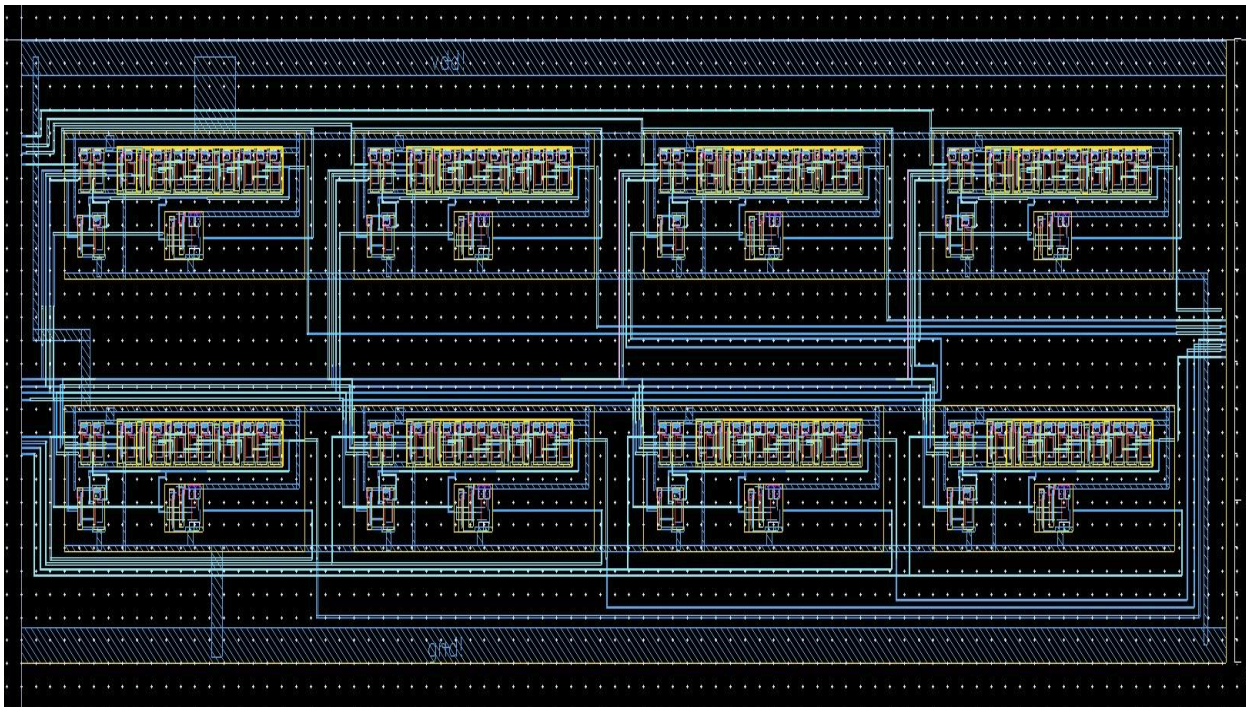
Layout Of 1 Bit Register



Layout Of 1 Bit Register



Layout Of 8 Bit Register



Layout Of 8 Bit Register

Hierarchy of Files used in 8bit_register :-

- aasha1_bit

1. D_ff_reset_up <= D_ff_using_latch_up <= D_latch_up
2. Tri_buffer_up
3. nand2_up
4. inv_up

Delay:-

5. Before Post Layout Simulation - 0.34 ns
6. After Post Layout Simulation - 0.81 ns