A Linear-Logarithmic CMOS Image Sensor With Pixel-FPN Reduction and Tunable Response Curve

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***Abstract*— This paper presents a high dynamic range (DR) linear-logarithmic (Lin-Log) CMOS image sensor (CIS) pixel with threshold voltage cancellation technique for pixel fixed pattern noise (PFPN) reduction. A tunable pixel response curve was applied for different environments. To avoid the gain loss of source follower in conventional APS structure, a column shared-amplifier with programmable gain was also applied. A prototype high DR Lin-Log CIS chip consisting of 100 × 100 5-T pixel array with n+/p-sub photodiode, a pixel area of 6 × 6 μm^2, and 3.3 V operation was designed and fabricated in TSMC 0.18 μm CMOS 1P6M standard process. The measured results achieved a DR of 143 dB, a PFPN related to sensitivity in logarithmic response (rms/log-sensitivity) of 1.96%, and a PFPN related to full-swing in logarithmic response (rms/$V_{log-swing}$) of 0.45%. Linear and logarithmic sensitivity were 651 mV/lux-s and 55 mV per decade of illumination, respectively, at 50 fps. The temporal noise and power consumption were 0.746 mV_{rms} and 1.88 mW, respectively.**

***Index Terms*— CMOS image sensor (CIS), high dynamic range (DR), linear-logarithmic response (Lin-Log), pixel fixed pattern noise (PFPN).**

I. Introduction

IN RECENT years, numerous high dynamic range (DR) CMOS image sensors (CISs) have been developed for applications as in biomedicine and machine vision because these sensors can display both bright and dark scenes clearly in the same frame [1]–[10]. To extend DR, pixel-level ADCs have been reported [1]–[3]. However, these techniques have a drawback of having large pixel size. To implement a high DR CIS with small pixel size, many ideas such as multiple exposure schemes [4], [5], well capacity adjustment schemes [6], dual-exposure schemes [7]–[10], and logarithmic/linear-logarithmic response schemes [11]–[22] have been published in the literature.

Among these high DR techniques, logarithmic response CIS can achieve high DR with simple operation and lower circuit complexity. The conventional three-transistor (3T) logarithmic CIS, shown in Fig. 1, is similar to conventional 3T linear CIS. In contrast to conventional 3T linear CIS which only provides a DR of about 60 dB, logarithmic response CIS can achieve a DR of around 120 dB. Although a logarithmic response CIS has a good DR performance, the pixel suffers limited voltage swing (only 0.2 ∼ 0.3 V), poor fixed pattern noise and serious image lag at low illumination. Limited voltage swing decreases signal-to-noise ratio (SNR) and poor pixel fixed pattern noise (PFPN) and image lag severely deteriorate the image quality.

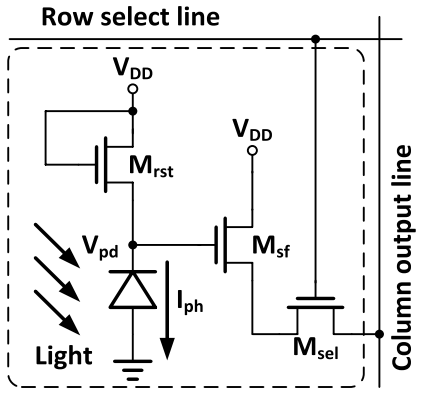

Fig. 1. Conventional logarithmic CMOS image sensor.

To improve voltage swing, linear-logarithmic (Lin-Log) architecture has been proposed. The Lin-Log sensor keeps sensitivity of low-illuminated image as linear response and compresses high-illuminated image with logarithmic response. It effectively prevents image lag at low illumination and also extends the dynamic range by conserving the detail in low-light and over-exposed area. The conventional high DR CIS suffers from large PFPN induced by the process-dependent logarithmic response. Off-chip compensation techniques are usually required to solve the PFPN issue with additional signal processing effort and cost. Conversely, on-chip calibration in logarithmic CIS provides an efficient solution for PFPN reduction. Therefore, Lin-Log CISs with threshold voltage cancellation and tunable linear region have been proposed to achieve a high dynamic DR imaging with on-chip PFPN compensation.

On the other hand, how to decide the switching point between linear and logarithmic response to obtain the best contrast under different imaging environments is also an important issue in this type of CIS. Some studies have used

Manuscript received July 25, 2013; revised October 26, 2013; accepted November 22, 2013. Date of publication December 12, 2013; date of current version March 24, 2014. This work was supported in part by the National Chip Implementation Center, Taiwan, and in part by the Signal Sensing and Application Laboratory, EECS, National Tsing Hua University. This is an expanded paper from the IEEE SENSORS 2012 Conference. The associate editor coordinating the review of this paper and approving it for publication was Dr. Shoushun Chen.

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Digital Object Identifier 10.1109/JSEN.2013.2294740

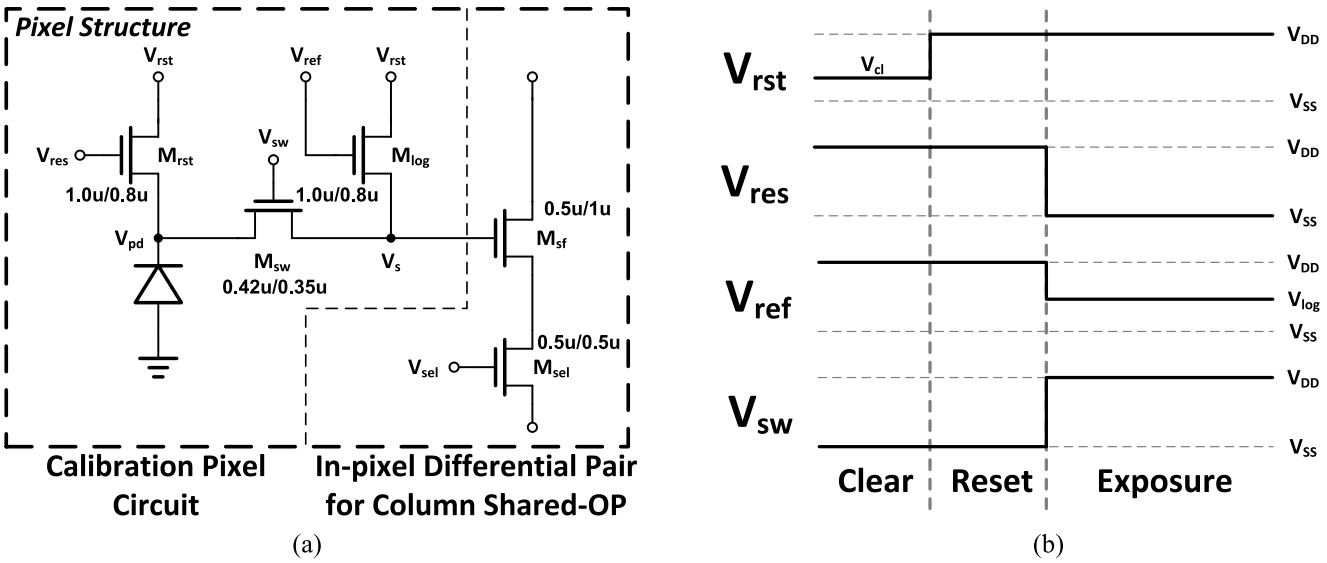

Fig. 2. (a) Proposed pixel structure. (b) Timing diagram for pixel operation in one row.

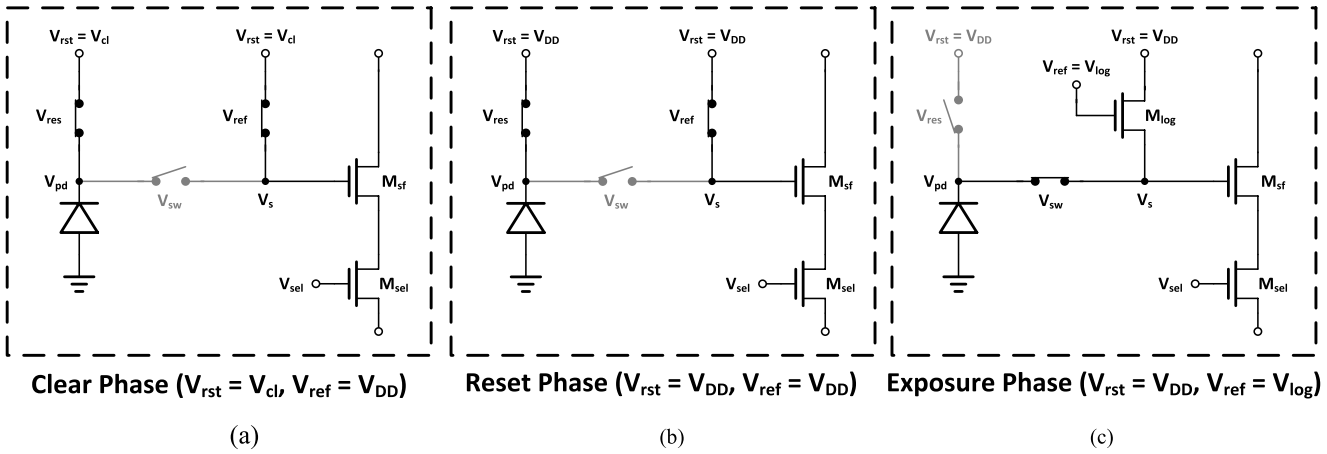

Fig. 3. Principle operation for the proposed pixel with threshold variation cancelling scheme in one row: (a) Clear phase. (b) Reset phase. (c) Exposure phase.

off-chip decision [13], but it requires more effort to fit linear and logarithmic curve. For the above-mentioned reason, on-chip decision has been developed [15], [16].

In this paper, a detailed description of the design of a high DR Lin-Log CIS with PFPN reduction by using threshold voltage cancellation scheme and tunable linear region is presented. In addition, this paper also applies column shared-amplifier [23] with programmable gain to reduce the gain loss of source follower in conventional APS structure.

The rest of this paper is organized as follows. The pixel circuit and column circuit designs are described in Section II. The experimental results of the realized prototype chip are presented in Section III. Finally, conclusions are drawn in Section IV.

II. Proposed High DR Lin-Log CIS

A. Conventional Logarithmic CIS Architecture

A conventional logarithmic CIS imager is shown in Fig. 1. In this circuit, M_{sf} and M_{sel} act as the source follower and select switch, respectively. The small current generated by photodiode makes M_{rst} to operate in subthreshold region. In subthreshold region, the gate-source voltage is proportional to the logarithm of current flowing into M_{rst}. The output voltage at node V_{pd} is determined by I–V equation in the sub-threshold region shown in (1)

$$V_{pd} = V_{DD} - V_{th,n} - nV_T \cdot \ln\left(\frac{I_{ph}}{I_0}\right) \tag{1}$$

where $V_{th,n}$ is the threshold voltage of M_{rst}, I_0 is the saturation current of M_{rst} in the subthreshold region, n is the body-effect coefficient, and V_T is the thermal voltage. The output voltage includes a process-dependent term $V_{th,n}$ from M_{rst} and causes a large PFPN in this type of sensor.

B. Proposed Lin-Log CIS Architecture

A new 5T Lin-Log pixel design and timing diagram with readout scheme to solve PFPN problem in conventional logarithmic CIS is shown in Fig. 2(a) and (b). When compared

with conventional logarithmic CIS in Fig. 1, M_{rst} and M_{sw} were implemented to achieve threshold voltage cancellation. The pixel operation in one row consists of three phases shown in Fig. 3, namely as clear phase, reset phase, and exposure phase.

Clear Phase: M_{rst} and M_{log} are ON, M_{sw} is OFF, and V_{pd} and V_s is charged to the voltage V_{rst}($V_{rst} = V_{cl}$ during the clear phase). The detailed circuit description is presented in Fig. 3(a). The main purpose in this phase is to eliminate the exposure value of the last frame which affects the reset voltage at reset phase.

Reset Phase: M_{rst} and M_{log} are still ON. M_{sw} remains OFF for isolating V_{pd} and V_s to prevent the I_{ph} induced logarithmic term in (1) being sampled at this phase. The detailed circuit description is presented in Fig. 3(b). The voltage V_{rst} is raised from $V_{cl}$to V_{DD}. V_s is pulled to a threshold voltage related term shown in (2)

$$V_1 = V_s = V_{DD} - V_{th,n} \tag{2}$$

where V_1 is a threshold voltage drop from V_{DD}.

Exposure Phase: The device M_{rst} is OFF and M_{sw} is ON. V_{ref} is changed from V_{DD} to V_{log}. The detailed circuit description is illustrated in Fig. 3(c). The photodiode starts the integration. At low-illumination condition, the behavior of the pixel similar to a conventional 3T-APS by keeping M_{log} OFF and V_s is discharged as linear response. At high-illumination condition, V_s is discharged below the threshold to turn ON M_{log} in the subthreshold region. Thus V_s is inversely proportional to photocurrent determined by I–V equation in the sub-threshold region of M_{log} shown in (3)

$$V_2 = V_s = V_{pd} = V_{log} - V_{th,n} - nV_T \cdot \ln\left(\frac{I_{ph}}{I_0}\right) \tag{3}$$

Equation (3) shows the signal voltage (V_s) in logarithmic response. By correlated double sampling (CDS), V_1 of (2) is subtracted from V_2 of (3) as shown in (4), and the processin-duced threshold voltage variation term ($V_{th,n}$) is canceled out.

$$\Delta V = V_1 - V_2 = V_{DD} - V_{log} + nV_T \cdot \ln\left(\frac{I_{ph}}{I_0}\right) \tag{4}$$

where ΔV is the output voltage after CDS operation, and V_{DD} - V_{log} is the preset linear range by tuning V_{log} depending on environment. The rest term in (4) is a logarithm related term. As shown in (4) first order PFPN at logarithmic mode can be easily reduced by CDS operation.

C. Column Circuit and Readout Scheme

Fig. 4 shows the used column shared-OP structure. M_{sf} is the input device of the column shared-OP enabled by M_{sel} and M_{sf} and M_{sel} are in the pixel. Fig 5 shows the column circuit and operation principle with column CDS. At the end of the exposure phase, the switches v1x and CE are ON and v2x is OFF [Fig. 5(b)]. The column shared-OP acts like a unity gain buffer, and the voltage at OP's output (V_{out_op1}) and CDS output (V_{out_col1}) is shown in (5) and (6), respectively

$$V_{out\_op1} = V_{sig} + V_{os\_op} \tag{5}$$

$$V_{out\_col1} = V_{com} \tag{6}$$

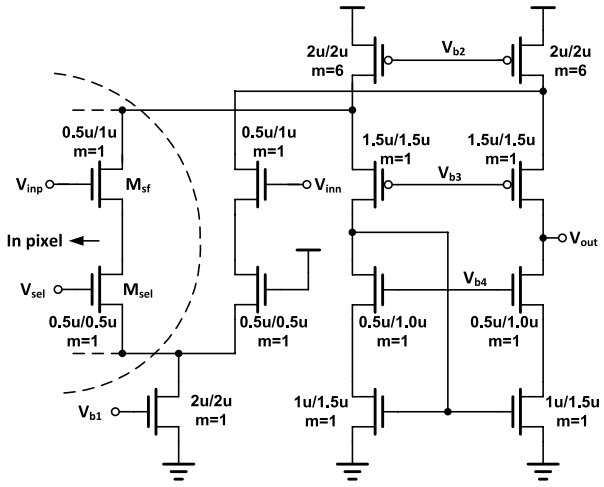

Fig. 4. Column shared-OP in column circuit.

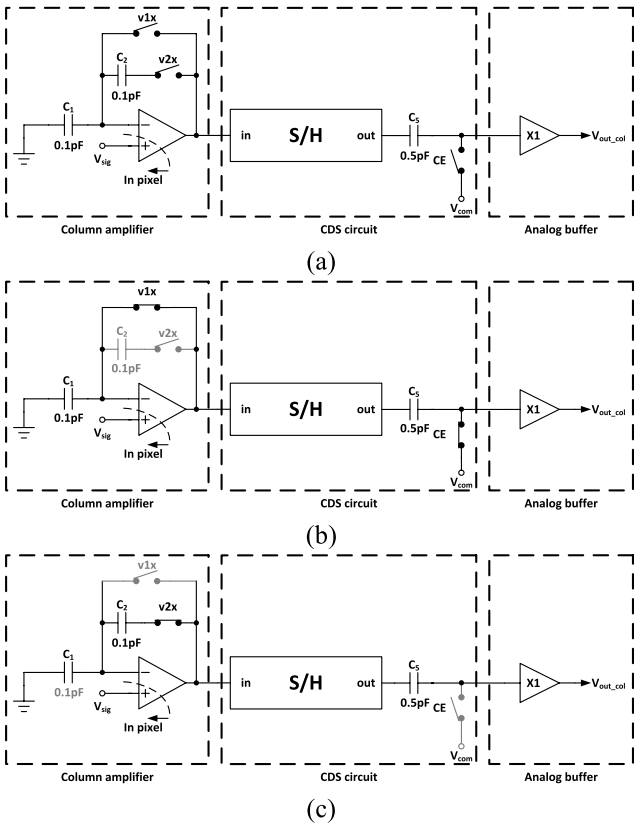

Fig. 5. Proposed column circuit and readout scheme. (a) Full column circuit. (b) Sample signal voltage. (c) Sample reset voltage and complete CDS operation.

where V_{os_op} is the offset voltage of column shared-OP due to differential pair's mismatch, V_{com} is an external voltage reference, and V_{sig} is pixel signal level.

Subsequently, the pixel goes into clear and reset phase, and the pixel reset level will be sampled by column CDS as shown in Fig. 5(c). The switches v1x and CE are OFF and v2x is ON.

At this phase, the column shared-OP with two capacitors (C_1 and C_2) provides a column gain of about (C_1+C_2)/C_2. The voltage of OP's output (V_{out_op2}) and CDS output (V_{out_col2}) are shown in (7) and (8), respectively By this operation, the

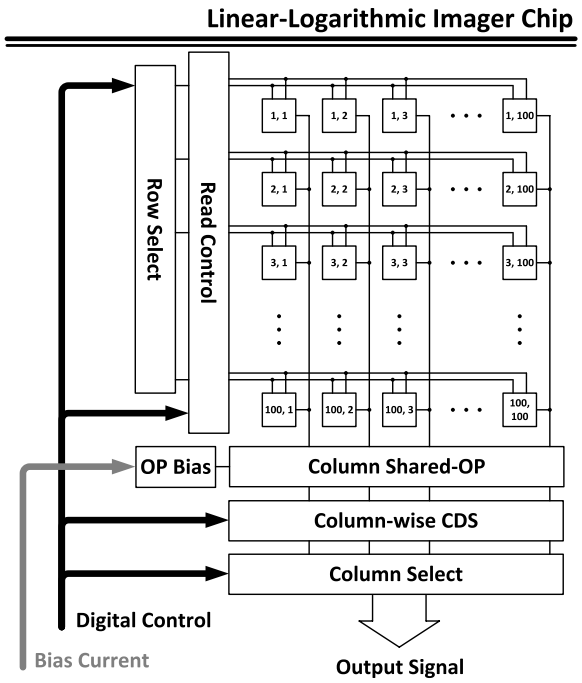

Fig. 6. System architecture of the proposed Lin-Log CMOS image sensor.

offset voltage (V_{os_op}) of column shared-OP is removed, and the voltage difference of pixel reset level (V_{rst}) and pixel signal level (V_{sig}) is delivered to the CDS circuit output.

$$V_{out\_op2} = V_{sig} + V_{os\_op} + \frac{C_1 + C_2}{C_2}\left(V_{rst} - V_{sig}\right) \quad (7)$$

$$V_{out\_col2} = V_{com} + \frac{C_1 + C_2}{C_2}\left(V_{rst} - V_{sig}\right) \quad (8)$$

where V_{rst} is the pixel reset level.

D. Chip Structure

Fig. 6 shows the system architecture. This chip consists of a pixel array, row select, read control, column shared-OP, OP bias, column-wise CDS and column select. Row select was implemented by shift register for scanning pixels' voltage of each row. Read control generates the control signals for pixels, which are gated by row select. OP bias and column shared-OP have already been described in the previous paragraph. Column CDS circuit achieves the subtraction of pixel reset and signal level, which is related to light intensity. Column select is used to select the column CDS out serially to I/O pins.

III. The Lin-Log Chip Measurements

Fig. 7 shows the chip microphotograph of the presented CMOS image sensor fabricated in TSMC 0.18 μm CMOS 1P6M standard process. The imager array has 100 × 100 pixels with a pixel size of 6 × 6 μm^2. A 16bits, ±5V full scale input range off-chip digitizer (NI PXI5922) is used for this sensor. The best frame rate in our testing system is 50 fps. A column shared-OP and CDS are integrated at the bottom side of the image array. The chip size is

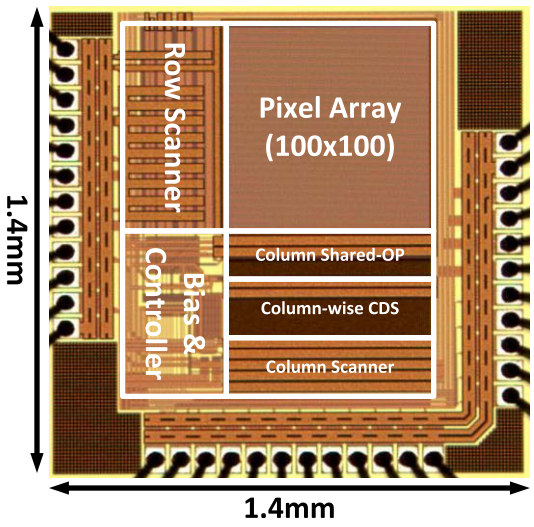

Fig. 7. Chip micrograph.

TABLE I
Sensor Measurement

Technology	0.18um 1P6M CMOS
Power supply	3.3V
Array size	100×100
Pixel level transistors	5
Pixel size	6µm × 6µm
Fill factor	32.54%
Dynamic range	143dB
Conversion Gain	13.9µV/e^-
Full Well Capacity	92.8 ke^-
Linear sensitivity	651mV/lux.s
Logarithmic sensitivity	55mV/dec
Temporal noise	0.746mV_{rms} (54e^-)
PFPN at linear	12mV
PFPN at log	1.08mV
PFPN at log [rms/(log sensitivity)]	1.96%
PFPN at log [$rms/V_{logswing}$]	0.45%
Power consumption	1.88mW @ 50 fps

1.4 × 1.4 mm^2. The measured performance of the developed CMOS image sensor is summarized in Table I. The achieved dynamic range and PFPN in logarithmic region is 143 dB and 1.96% respectively. Linear and logarithmic sensitivity are 651 mV/lux-s and 55 mV per decade of luminance, respectively. Furthermore, temporal noise is 746 μV_{rms}, and the average power consumption is 1.88 mW at 50 fps.

A. Photoelectric Conversion Characteristics

Fig. 8 shows the measured photoelectric conversion characteristics from 0.01 to 156500 lux with different V_{log} values. The cross and circle lines show the measurement results with V_{log} as 1.8 and 2.5 V, respectively. The zoom-in part

TABLE II
LOGARITHMIC AND LINEAR-LOGARITHM PIXEL APPROACH COMPARISON TABLE

	[11]	[12]	[13]	[14]	[15]	This work
Technology	0.8um	0.25um	0.18um	0.35um	0.5um	0.18um
Array size	160×120	N/A	352×288	640×480	16×16	100×100
Pixel level transistors	4	5	7	4	7	5
Pixel size (um^2)	30×30	10x10	5.6×5.6	7.5×7.5	23.4×27.15	6×6
Fill factor	N/A	43%	33%	37%	24.56%	32.54%
Dynamic range	>120dB	140dB	143dB	124dB	121.26dB	143dB
High dynamic range technique	Linear-Logarithmic	Logarithmic	Linear-Logarithmic	Linear-Logarithmic	Linear-Logarithmic	Linear-Logarithmic
Linear-logarithmic switching	On chip fixed	N/A	Off chip	On chip fixed	On chip adjustable	On chip adjustable
Logarithmic sensitivity (mV/dec)	53mV/dec	N/A	77mV/dec	66mV/dec	79.98mv/dec	55mV/dec
FPN at linear (mV)	N/A	N/A	N/A	N/A	13.8mV	12mV
FPN at log (mV)	6.5mV	32mV	3.08mV	5mV	19.1mV	1.08mV
FPN at log (%) [rms/(log sensitivity)]	12.26%rms	N/A	4.00%rms	7.57%rms	23.88%rms	1.96%rms
FPN at log (%) [rms/$V_{logswing}$]	N/A	2.46%rms	N/A	N/A	8.34% rms	0.45%rms

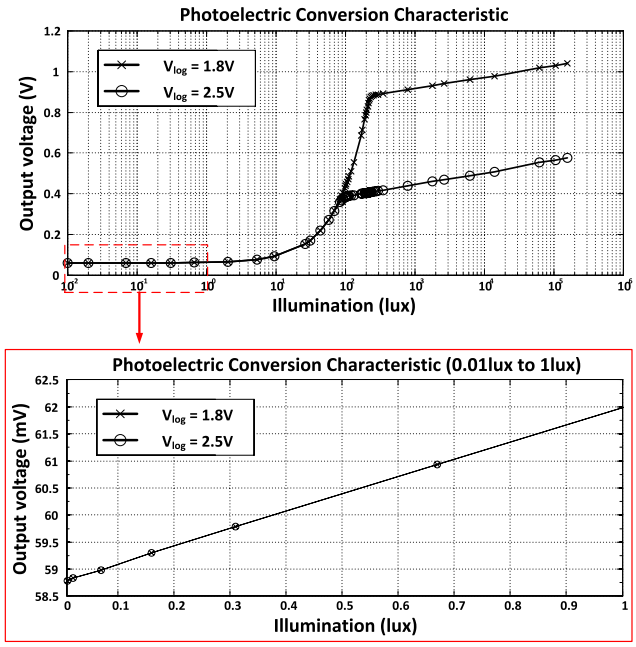

Fig. 8. Photoelectric conversion characteristic.

from 0.01lux to 1lux is also shown. The sensitivity in linear region and logarithmic region are 651mV/lux-sec and 55 mV per decade of luminance respecitvely. In the linear region, the voltage swing of V_{log} as 1.8 and 2.5 V are 0.4 V and 0.9 V, respectively. This shows that the swing in linear region is tunable by varying V_{log}, depending on different image environments. In the zoom-in image, the two curves (V_{log} = 1.8 V and 2.5 V) are very similar, which shows that, in low illumination testing, the proposed pixel has a linear response to light intensity, and the two different levels of V_{log} (1.8 V and 205 V) in this measurement don't affect the pixel output until to the turning point (linear region to logarithmic region). The dynamic range in this paper is defined as (9).

$$DR = DR_{Linear} + DR_{Log} = 20 * Log\left(\frac{V_{sw,linear}}{\sigma_{read}}\right) + 20 * \left(\frac{V_{sw,\log}}{Sen_{\log}}\right) \quad (9)$$

where $V_{sw,linear}$ and $V_{sw,log}$ are the voltage swing at linear mode and logarithmic mode, respectively. σ_{read} is the read noise and Sen_{log} is the logarithmic sensitivity. In our design, $V_{sw,linear}$ is tunable by adjusting V_{log} level. For example, when V_{log} is 1.8 V at 1x analog gain, $V_{sw,linear}$ and $V_{sw,log}$ are around 806 mV and 484 mV, respectively (total voltage swing is 1.29V). Since σ_{read} is 0.746 mV_{rms} and Sen_{log} is 55mV per decade, the theoretical DR_{Linear} and DR_{Log} are around 60 dB and 176 dB, respectively. It implies an achievable total DR of 236 dB. However, because of the restriction of our optical testing system, the reported DR in the measurement result is 143 dB.

B. Column Gain With Column Shared-OP

In this chip, the column shared-OP can be configured as unity gain buffer (v1x always ON) or column amplifier (v1x is ON at the end of pixel exposure phase). The gain of column amplifier is $(C_1+C_2)/C_2$. We designed $C_1 = C_2$ in this chip so that the ideal column-gain in column amplifier is two. To measure column gain, the pixel is operated in linear mode

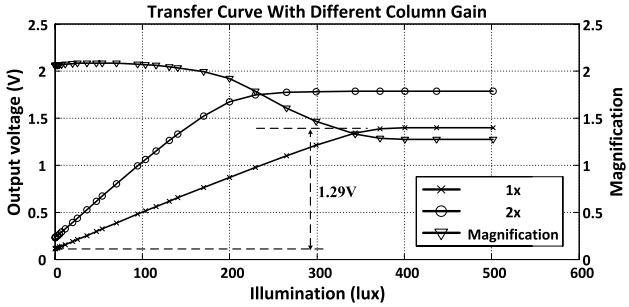

Fig. 9. Transfer curve with different column gain.

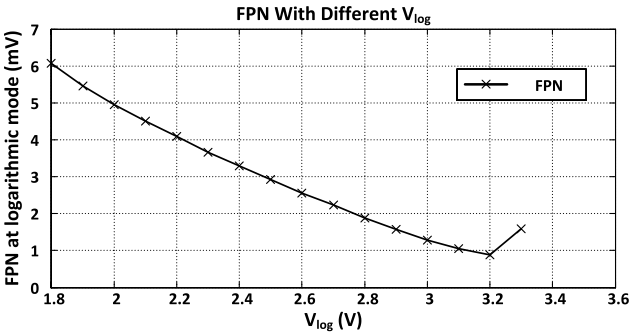

Fig. 10. Measured FPN with different Vlog.

(V_{log} = 0 V). The measurement result is shown in Fig. 9. The cross line shows the transfer curve with unity gain, and the circle line shows the transfer curve with column-gain of two. The measured gain between cross line and circle line is stated in triangle line. The trend of this line can be separated by three conditions.

In the region below about 80 lux, the magnification slowly increases as illumination. This is caused by signal-dependent parasitic capacitance of column shared-OP's negative input due to sample signal. According to Fig. 5(a), we can obtain (10) by adding parasitic term in (7)

$$V_{out\_op2} = V_{sig} + V_{os\_op} + \frac{C_1 + C_2}{C_2}\left(V_{rst} - V_{sig}\right) + \frac{C_{p1}V_{rst} - C_{p2}V_{sig}}{C_2} \quad (10)$$

where C_{p1} is the parasitic capacitance at column shared-OP's negative input during reset phase and C_{p2} is the parasitic capacitance at column shared-OP's negative input during exposure phase. From (10), we can observe that the parasitic term in (10) is increased by increasing illumination. Thus the magnification is slowly increased as illumination.

When the illumination is increased between 80 and 350 lux, the magnification decreases rapidly because some outputs of the column shared-OPs are saturated. If the illumination exceeds 350 lux, all column shared-OPs are saturated so that the magnification remains constant as the illumination increases.

C. Logarithmic Mode PFPN With Different V_{log}

To measure PFPN in logarithmic mode, the illumination of light source is about 3000 lux to make sure that our sensor is operated in logarithmic mode. We captured 100 frames at the same illumination and averaged 100 frames on pixel level. Then we obtain the standard deviation from the averaged pixels. The measurement result is shown in Fig. 10. From this figure, it can be noted that the PFPN decreases as V_{log} increases before V_{log} reaches 3.3 V. The major reason for this trend is that the threshold voltage saved in the reset phase and exposure phase is not exactly equivalent due to the body effect of the M_{log} in pixel shown in Fig. 2(a). The reset voltage is higher than the signal voltage, and thus, the V_{bs} of M_{log} is not equal to each other so that the threshold voltage $V_{th,n}$ cannot be cancelled clearly due to body effect term which is also process dependent. As V_{log} increases, the M_{log}'s V_{bs} between reset phase and exposure phase becomes closer. By the proposed threshold voltage cancellation scheme, the body effect term's influence can be mitigated. When V_{log} equals 3.3 V, the PFPN is increased because the signal voltage exceeds column shared-OP's input common mode range (ICMR).

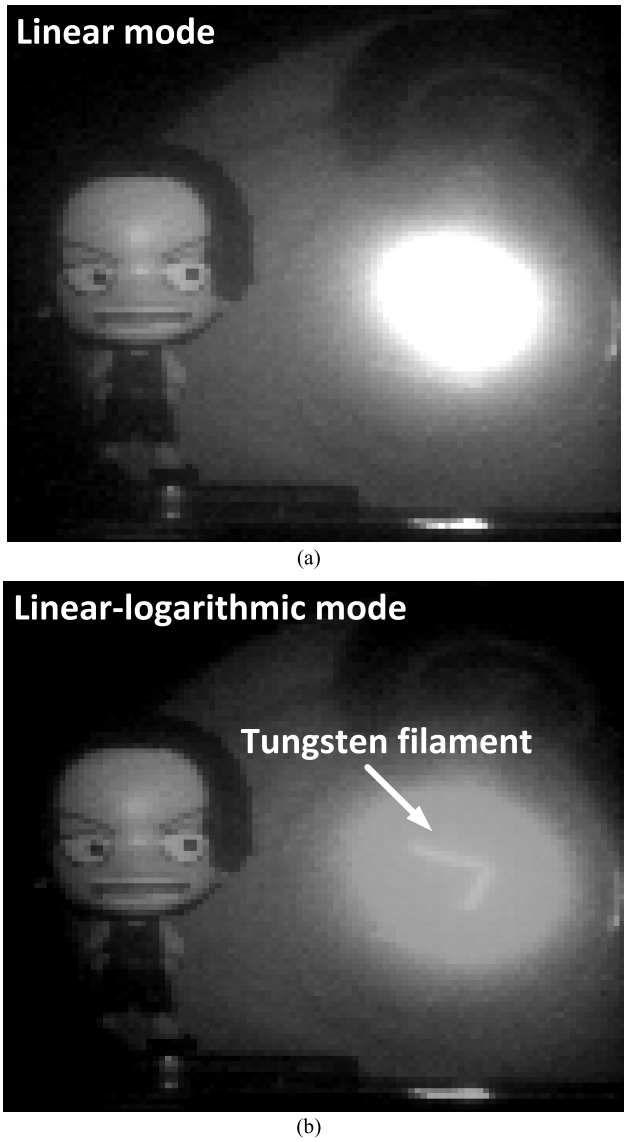

Fig. 11. Sample images. (a) Linear mode. (b) Linear-logarithmic mode.

D. Images

Fig. 11 shows the sample images captured from prototype without any post-processing. Fig. 11(a) is captured in linear response. The illuminated lamp creates an high dynamic range (HDR) scene but the tungsten filament is unrecognizable because the image around the tungsten filament is saturated so that it cannot display high- and low-light information at the same time with linear mode.

Fig. 11(b) shows that the doll and lamp's tungsten filament are cognoscible in Lin-Log response as expected. The doll is captured in linear region and the lamp is captured in logarithmic region. It shows a HDR scene that the detailed information of high light and low light can be displayed simultaneously with the proposed Lin-Log CIS. The measured performance comparison table of the proposed Lin-Log or logarithmic imager with state-of-the-art published works is summarized in Table II.

IV. Conclusion

This paper proposed a Lin-Log CIS with high DR. With threshold voltage cancellation for PFPN reduction and column shared-OP scheme, the imager achieves a dynamic range of 143dB, a PFPN related to sensitivity in log response (rms/log-sensitivity) of 1.96%, and a PFPN related to full-swing in log response (rms/$V_{log-swing}$) of 0.45%. On-chip tunable response curve is proposed to control Lin-Log switching point properly without post-processing effort and cost to achieve the best contrast with different image environments. It shows that the proposed design provides a promising solution of wide DR CIS chip.

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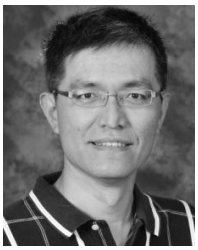

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