PIN-photodiode based active pixel in 0.35 µm high-voltage CMOS for optical coherence tomography

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Abstract - This paper presents an active pixel based on a PIN photodiode for application in Optical Coherence Tomography (OCT), where a high responsivity and low crosstalk is required. The proposed pixel is built on a wafer with a high-resistivity epitaxial silicon layer and optimized for high efficiency at 850 nm, low dark current, low crosstalk, and low noise operation. Advantages of this approach over conventional approaches such as the 3T active pixel in a standard CMOS process and over 4T pinned photodiode active pixel approaches for OCT applications are explained. A test chip was fabricated in 0.35 µm high-voltage CMOS. Three different epitaxial layer thicknesses are investigated. Measured results of the OCT PIN-photodiode pixel are presented.

Keywords - PIN photodiode; active pixel; high resistivity; waveguide coupling; 0.35 µm CMOS; low crosstalk; low noise;

I. INTRODUCTION

From day to day, the number of applications where electronics and photonics are integrated monolithically or in a 3-dimensional manner is increasing. This concept of integration is applied in many applications such as data communications [1], biosensing [2], transmitters [3], LIDAR systems [4] etc. For the spectral-domain optical coherence tomography (OCT) investigated here, an arrayed waveguide grating (AWG) separates the spectrum into 512 waveguides. The wavelength of the used light is determined by the application (ophthalmology) and lies in the near-infrared (NIR) spectral region (800-900 nm). Due to the limited optical power because of eye safety, an optical power on the order of nanowatts is expected per photodiode. Coupling the light effectively out from the waveguides into the photodiodes requires structures that are significantly larger than the used wavelength and this determines the size of the integrated photodetector. The grating coupler at the waveguide's end has a large length. The photodiode, therefore, needs a size of 50 µm×10 µm.

When light penetrates deeper (T_{pen} (850 nm)~25 µm) into the silicon (where the penetration depth is defined as the depth at which incoming radiation is attenuated for the factor of e) than the depth of the photodiode's space-charge region, a high probability of diffusion of photogenerated electrons to the neighboring photodetectors exists. Carrier diffusion occurs for 850 nm light and low or moderately increased supply voltages especially for homogenously doped substrates with usually a doping concentration of 10^{15} cm^{-3}. In applications where low crosstalk is demanded, photodiodes must be fully depleted. Instead of increasing the reverse bias voltage, a deeper depletion region can be achieved by use of a highly resistive (lowly doped) epitaxial (EPI) layer, which is obtained by lowering the doping concentration of acceptors in the EPI layer.

Nowadays most of the commercially available image sensors are CMOS image sensors. Active pixels, which exploit pinned photodiodes are known as very sensitive, low-noise and high conversion gain pixels [5]. It also should be mentioned that the good performance of the conversion gain of active pixel sensors relates to their small pixel area, i.e. to the small capacitance of the photodetector. Furthermore, image sensors are typically optimized for the visible spectrum and the photodetector's responsivity between 800 and 900 nm is low.

In applications, where these longer wavelengths are used, PIN photodiode based photodetectors could have many advantages over widely used conventional pinned photodiode based pixels or simple *p*/*n*-photodiode based pixels in a standard CMOS process. A pinned photodiode (which is practically a double photodiode with two vertically arranged *p*/*n* junctions leading to a high capacitance per µm²) with the large light-sensitive area needed for the OCT sensor would lead to a very long charge transfer time, when full charge transfer to the floating storage node in a 4T pixel is needed. The capacitance of a large-area PIN photodiode per µm² is much smaller than that of a pinned photodiode. The PIN photodiode, therefore, leads to a fast response in waveguide coupled OCT applications. This work presents the implementation of a PIN photodiode based active pixel on a *p*-/*p*+ epitaxial wafer. Its advantages and disadvantages are shown and a good basis for the development of a sensor for OCT is introduced.

II. PIN PHOTODIODE

The PIN photodiode is built of *n*+ (cathode), an intrinsic *p*- type silicon layer and *p*+ substrate (anode). The concept of spectral-domain OCT requires the implementation of up to 512 independent channels, each of them comprising one photodiode. The photodiodes are arranged either in an 1- or 2-dimensional array. To prevent electrical crosstalk between neighboring channels the photodiodes should be separated as far as possible from each other and/or each detector should comprise a guard ring. The PIN

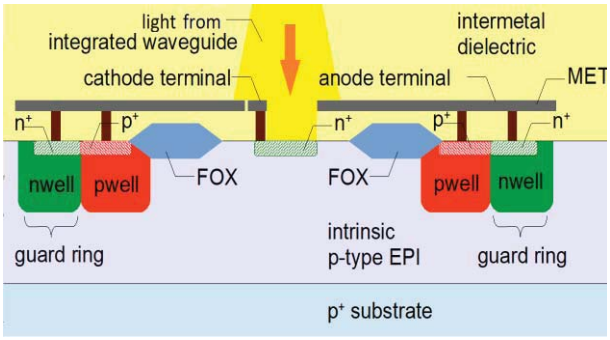

Figure 1. PIN photodiode cross section.

photodiode's cross section is depicted in Fig. 1. The photodiode's active area of 10×50 µm^2 is determined by the grating coupler's size, while the cathode to anode distance (25 µm) and the guard-ring width (15 µm) are chosen in a way to minimize the dark current and the crosstalk. The total pixel area is 290×250 µm^2.

By decreasing the doping concentration of the EPI silicon, the depletion region for the same reverse bias voltage extents deeper into the *p*- EPI. Ideally, all of the intrinsic EPI that is irradiated by incoming light should be depleted. Light that is absorbed within the space-charge region (SCR) will almost instantaneously contribute to the photocurrent due to carrier drift, light that penetrates through the SCR generating carriers in the *p*+ substrate will give a much slower photocurrent contribution due to carrier diffusion and it also raises the chance to give a current signal in one of the neighboring pixels due to 3-dimensional carrier diffusion. To suppress this crosstalk signal each pixel is surrounded by a short-circuited *p*/*n*-junction ring, a so-called "guard ring". The necessity of applying significant reverse biases for a fully depleted diode and the high-resistive EPI-type starting material both require a special isolation concept for the electronic circuits. Therefore we use for the circuit design solely isolated devices in the high-voltage CMOS technology that are isolated by deep *n*-wells.

We have tested three different EPI thicknesses (20, 30, 40 µm) for their spectral responsivity behavior. The measurement results are depicted in Fig. 2. The photodiodes were illuminated with light from a monochromator. The responsivity for 850 nm with 20 µm EPI layer thickness is 0.445 A/W increasing to 0.55 A/W for 40 µm EPI layer thickness, where *SRmax* is the maximal theoretical spectral responsivity of a device with the quantum efficiency of 100%.

If we compare obtained measurement results with the spectral responsivities of the photodiodes in standard CMOS, we see a significant increase of spectral responsivity in the spectral region of 800 to 900 nm. Koklu et al. [6] reports spectral responsivities of *p*+/*n*-well/*p*-sub, *n*-well/*p*-sub and *n*+/*p*-sub photodiodes in a 3T APS at different diffusion areas in standard 0.18 µm CMOS process. Obtained spectral responsivities in the wavelength range of 800 to 900 nm are from 0.02 to 0.35 A/W. These results match measured results obtained by Strle et al. [7] who measured spectral responsivities of *n*+/*p*-sub, *n*+/*p*-well, and *n*-well/*p*-sub photodiodes in 130 nm standard CMOS process.

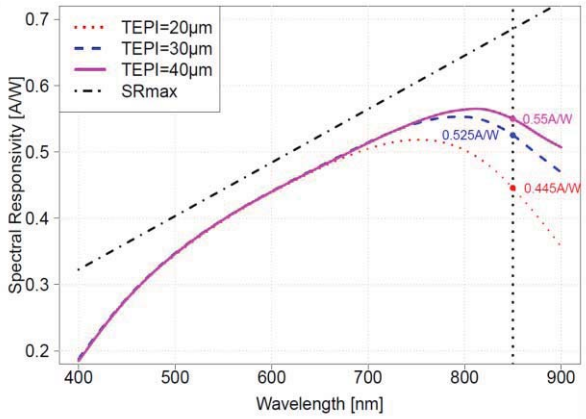

Figure 2. PIN photodiode spectral responsivity measurement results with different EPI layer thicknesses where comparison is made with the maximal theoretical spectral responsivity (*SRmax*).

Another benefit of low doped EPI is seen in cross talk measurements, where in the spectral region from 800 to 900 nm we obtain extremely low cross talk below -60 dB for a photodiode pitch of 140 µm and for all three epitaxial layer thicknesses, which fulfills the requirements of an OCT application. On the other hand we observed an increase of the dark current with increasing EPI thickness, $I_{dark}(TEPI = 20\ \mu m) = 0.556$ pA, $I_{dark}(TEPI = 30\ \mu m) = 1.53$ pA, and $I_{dark}(TEPI = 40\ \mu m) = 3.66$ pA where the reverse bias voltage is -10 V. Therefore, we chose 20 µm EPI thickness wafer as the most optimal starting material for an OCT pixel sensor.

III. PIXEL DESIGN

A. Conventional approaches

1) P/N-photodiode active pixel in a standard CMOS process

In a standard CMOS process photodiodes are usually formed of *n*+/*p*-well or *n*-well/*p*-well. Maximum allowed supply voltages in such processes, where the resistivity of the silicon is about 10 Ωcm [8], can barely deplete such photodiodes, therefore the probability of diffusion of photo-generated electrons to neighboring pixels is high, especially for longer wavelengths, which penetrate deeper into the silicon. Ref. [9] reports crosstalk of almost 25% for 850 nm wavelength, 8 µm thick epitaxial layer and 4 µm photodiode pitch. Due to this fact these pixels usually have high crosstalk and low efficiency for longer wavelengths, therefore this type of pixels doesn't suit well for OCT applications.

2) 4T pinned photodiode active pixel

Another conventional approach is the 4T pinned photodiode pixel. Key benefits of this approach are very low dark current, high conversion gain (only for small pixels), separate charge integration and storage regions, noiseless charge transfer and efficient suppression of reset (*kT/C*) noise, which is the major noise source in 3T pixels [10]. Charge transfer efficiency becomes more and more critical for larger pinned photodiodes when the transfer time dramatically increases. For example for a photodiode size of 40 µm × 40 µm for complete charge transfer 3 µs

to 6 µs are needed [11]. Electrical crosstalk also could be a problem at longer wavelengths. Ref. [12] reports crosstalk of almost 16% at 850 nm (TCAD simulations), while pixel pitch and technology are not mentioned. Even with many advantages, this type of pixel is not a good choice in applications where large photodiodes are required as well as in applications where long wavelengths are used. Since the pinning layer of the pinned photodiode is connected with the *p*-type substrate, negative voltages cannot be applied to the substrate to extend the SCR.

B. PIN photodiode based active pixel

The proposed pixel is based on the 3T architecture. The schematic of the test pixel and a timing diagram are shown in Fig. 3. This pixel consists of a PIN photodiode and three transistors. Transistors M1 and M2 form a source follower (gain less than unity) and the third transistor (M3) is used as a reset transistor. A select transistor was not needed in this pixel test structure.

Prior to integration, the photodiode is reset (RS signal is high for 1 µs). The supply voltage of 2.2 V together with the reset (RS) pulses of 3.3 V makes the pixel working in the hard reset mode ($V_{DD}<V_{G3}-V_{TH3}$), which means fast and complete removal of charges from the photodiode during the reset, where the final photodiode reset voltage fixes at V_{DD}. In this case, 2.2 V is the maximum supply voltage for which hard reset works. Benefits of a hard reset operation are elimination of image lag the and better linearity on one hand, but lower saturation level on the other hand [13], [14]. During the integration, which duration is fixed, the maximal exposure time is set to 190 µs.

The conversion gain of this architecture depends on the photodiode capacitance. Operating conditions are given in Table 1. The anode voltage is chosen in a manner to achieve the best performance of the photodiode (low dark current, low crosstalk, and the smallest possible photodiode capacitance). Load of the pixel is the impedance of the oscilloscope probe (C=20 pF, R=1 MΩ).

Main noise source in such a pixel is the reset (kT/C) noise and its rms noise is $\sqrt{kT/C}$ for hard-reset operation, where k is the Boltzmann constant, T the absolute temperature and C is the photodiode's capacitance. For

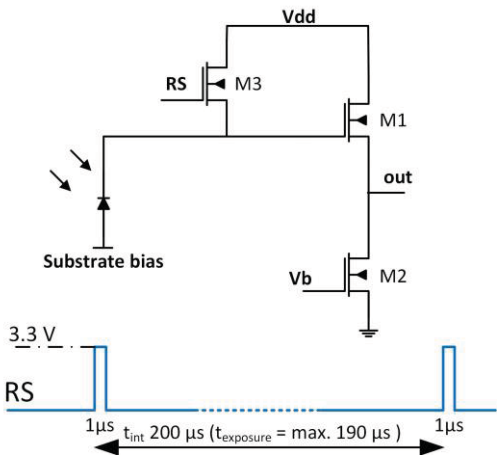

Figure 3. Schematic of test pixel and timing diagram.

Table 1. Pixel operating conditions.

Parameter	Value
V_{DD}	2.2 V
Substrate bias	-10 V
Bias current	3 µA
Load impedance	C=20 pF, R=1 MΩ

implemented photodiode, which has a capacitance of 149.9 fF at -10 V reverse bias, reset noise is 165.6 µV rms. Compared to the other reset possibilities, soft reset and so-called flushed reset [15], this reset operation is noisier but simpler to implement and image lag is eliminated in comparison to soft reset.

This pixel is optimized for low-noise operation. Input referred noise of a source follower amplifier is given by the following equation (flicker and thermal noise only) [16]:

$$\overline{V_{n,in}^2} = 4kT\frac{2}{3}\left(\frac{g_{m2}}{{g_{m1}}^2}+\frac{1}{g_{m1}}\right)+\frac{K}{C_{ox}}\left(\frac{{g_{m2}}^2}{W_2L_2{g_{m1}}^2}+\frac{1}{W_1L_1}\right)\frac{1}{f}$$

where g_m is the transconductance, K is technology parameter, Cox specific gate oxide capacitance, $W_{1,2}$ widths of the transistor gates, $L_{1,2}$ lengths of the transistor gates and f is the frequency. Since the readout circuit is located in a gap of a photodiode guard ring, to minimize crosstalk, values of transistors widths and lengths are chosen to meet minimal design rules.

IV. PIXEL CHARACTERIZATION

A test chip was fabricated in 0.35 µm high-voltage CMOS.

1) Measurement setup

One of the widely used methods for characterization of image sensors is a photon transfer curve (PTC) [17]. To obtain such a curve, mean values at each illumination level are needed. There are two ways of getting image sensor data. The first way is to keep the optical power constant and change the exposure time and the second is to sweep optical power while exposure time is constant. For the measurements, the first method was used. Exposure time was swept from zero (complete dark) to 190 µs, i. e. light pulses with a duration up to 190 µs were used, while integration time was constant (200 µs). Every sample is corrected afterwards for the dark current. Input optical power is chosen in the manner to lead pixel to saturation for an exposure time of 190 µs. Light is coupled to the photodiode via 850 nm single mode optical fiber. Measured optical power at the end of the optical fiber was 2.24 nW. Optical power at the photodiode surface is slightly lower than the power measured at the end of fiber due to the small width of the photodiode of 10 µm (few micrometers gap between the surface and the fiber). Analog output of the test pixel is taken via a probe with an input impedance of R = 1 MΩ and C = 20 pF and sampled by a LeCroy WaveRunner 6200A oscilloscope and further processed by software. Correlated double sampling circuit is not implemented on the chip, but this technique is used in post-processing of pixel data in order to isolate signal and remove FPN (fixed pattern noise). To obtain the PTC, averaging with the factor of 256 was done for each

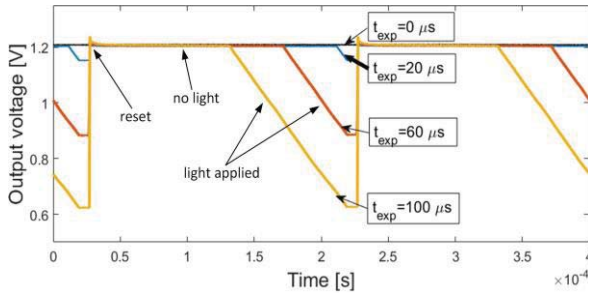

Figure 4. Pixel transient response for 4 different exposure times. After the reset, if there's no light, pixel output is steady. When the light is applied, photo-generated electrons store in the photodiode causing the drop on the output voltage.

exposure time and mean values and standard deviations were calculated. All measurements were made in a dark chamber.

2) Measured results

This section presents measured results of a pixel with 20 µm thick EPI layer, 10×50 µm² photodiode size, 15 µm guard ring width and 25 µm guard ring to cathode distance. Transient response for four different exposure times (0 µs, 20 µs, 60 µs, and 100 µs) is shown in Fig 4. Photon-transfer curve is shown in Fig 5. Measured pixel parameters are presented in Table 2. The pixel operates in a linear region for exposure times up to 180 µs. Conversion gain is expectedly low (1.316 µV/e^-) due to the photodiode capacitance of 149.9 fF. Mean noise is 273.9 µV (201 e^-) and it is calculated as the standard deviation of the pixel output in the dark. For this noise floor, the calculated dynamic range is 71.2 dB. Low conversion gain reflects in a relatively large full-well capacity of 842.7 ke^- which is a figure of merit for the signal-to-noise ratio (SNR). In OCT systems SNR is considered as one of the most important parameters that determine the imaging quality [18]. We measured SNR of 57.3 dB. The linear output voltage swing of the pixel is 1.109 V and it is determined with the photodiode reset voltage (upper boundary) and the saturation of the current mirror (lower boundary). The integral nonlinearity (INL) is 3.37 %.

V. Conclusion

The 3T active pixel is an old approach but in specific imaging applications in combination with a PIN photodiode gives better performance regarding crosstalk than approaches with standard substrates. The unmodified HV CMOS process with high resistive epitaxial layer and isolated electronics gives better results with respect to responsivity than a standard CMOS process. Even usage of a high resistivity epitaxial layer requires large negative substrate voltages for a fully depleted photodiode, which excludes the implementation of a pinned photodiode in waveguide coupled OCT pixels. Since the photodiode for an OCT application is very large in size and has a large capacitance (although the PIN photodiode has a much lower capacitance per µm² than a pinned photodiode), its conversion gain is low compared to known 4T pinned photodiode active pixels with a very small light-sensitive and floating storage node area. But the large photodiode capacitance, on the other hand, minimizes the contribution of reset noise to the total noise. It has been shown that this pixel approach successfully takes all benefits of both PIN photodiode and 3T pixel architecture, which makes it ready for the highly demanding OCT application.

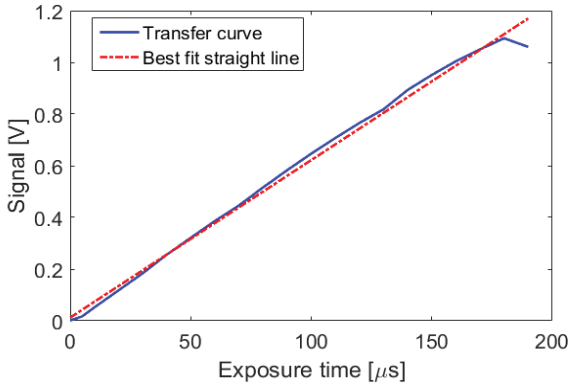

Figure 5. Transfer curve and best fit straight line. In order to get the curve, pixel outputs are taken in equidistant steps for exposure times from 0 µs (complete darkness) to 190 µs (saturation). The pixel output is linear for exposure times up to 180 µs, while for longer exposures it goes to saturation.

Table 2. Measured pixel parameters.

Parameter	**Value**
Pixel size	10×50 µm²
Linear full well capacity	842.7 ke^-
Mean noise (rms)	273.9 µV (201 e^-)
Conversion gain	1.316 µV/e^-
Linear output voltage swing	1.109 V
Integral nonlinearity (INL)	3.37 %
Dynamic range	71.2 dB
Signal-to-noise ratio	57.3 dB

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