Enhanced Near-Infrared Response CMOS Image Sensors Using High-Resistivity Substrate: Photodiodes Design Impact on Performances

Jean-Baptiste Lincelles, Olivier Marcelot, *Member, IEEE*, Pierre Magnan, *Member, IEEE*, Olivier Saint-Pé, and Michel Bréart de Boisanger

***Abstract*— A three-transistor pixel, front-side-illuminated CMOS image sensor is developed and realized using high-resistivity (HR) silicon ($N_a \approx 10^{12}$ cm^{-3}) to enhance its near-infrared response thanks to a large depleted depth. Both TCAD simulations and an analytical model are used to estimate the space-charge region extension of a photodiode. A strong 3-D geometrical variation with pixel design geometry is shown. Punchthrough current measurements in a pixel array are used to demonstrate these variations and their impact. The punchthrough and crosstalk measurements can provide an optimum pixel design on HR silicon. Electrooptical characterization demonstrates excellent quantum efficiency despite slightly degraded crosstalk performances for near-infrared wavelengths.**

***Index Terms*— Active pixel sensors (APSs), crosstalk, high resistivity (HR), near-infrared, p-n junctions, punchthrough.**

I. Introduction

STANDARD three-transistor (3T) active pixel sensors (APSs) [1] shown in Fig. 1 use a reverse-biased p-n junction for charge collection and 3 nMOS for pixel operation. Thanks to the CMOS technology improvement and the use of in-pixel transistors, APS are now competing with charge-coupled devices (CCDs) in many applications [2]. By extending the collecting field of CCDs through the use of high resistivity (HR) and high biasing voltages, excellent quantum efficiency (QE) and crosstalk performances for scientific instruments are achieved [3]. More recently, similar features in a CMOS image sensor have been implemented in hybrid devices [4] or monolithic devices [5], [6] to improve charge collection efficiency, but the pixel design restrictions are not assessed. This paper investigates the extension of the space-charge region (SCR) (Fig. 1) in a pixel array integrated into HR silicon, and studies the design restrictions and the electrooptical performances of 3T pixels on such substrates without backside bias. Section II discusses the SCR extension dependence on the pixel geometry of a single photodiode in HR silicon ($N_a \approx 10^{12}$ cm^{-3}) by means of the TCAD simulations and an analytical model. A method to study these variations based on punchthrough current is presented in Section III. A test vehicle (described in Section IV) has been designed to estimate the SCR variations with pixel design using the punchthrough effects in Section V, and to measure the electrooptical performances in Section VI.

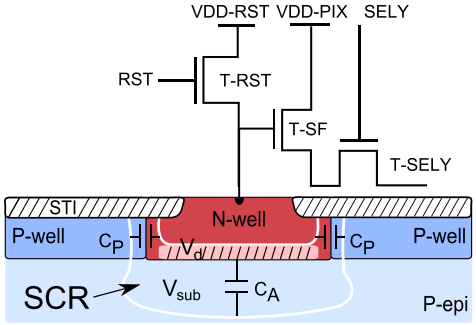

Fig. 1. Schematic cross section of a conventional 3T pixel with a p-n photodiode.

II. Depletion Dependence on Photodiode Design

Assuming an abrupt p-n junction approximation, the Poisson equation solution of a 1-D photodiode yields an SCR width expressed by [7, p. 165]

$$W = \sqrt{\frac{2\epsilon_{\mathrm{Si}}}{q} . \frac{N_{\mathrm{sub}} + N_d}{N_{\mathrm{sub}} N_d} . (V_r + V_{\mathrm{bi}})} \tag{1}$$

where ϵ_{Si} is the silicon dielectric constant, q is the elementary charge, N_d and N_{sub} are the doping concentrations of the n-well and p-substrate, respectively, V_r is the applied bias on the n-well, and V_{bi} is the built-in potential. Using the HR p-type silicon, the depleted depth W can extend up to several tens of micrometers according to (1). However, (1) is defined by the Poisson equation in a 1-D p-n junction, and may not be a good approximation for a real device. For this reason, the best solution to estimate the SCR extension remains the TCAD simulations. The 3-D TCAD simulation (with Synopsis Sentaurus) using analytical doping profiles is shown in Fig. 2.

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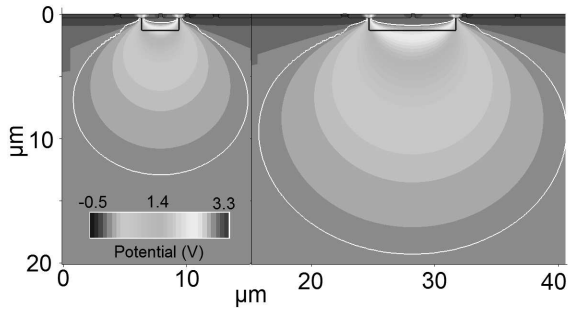

Fig. 2. TCAD simulations of the SCR 3-D effect for two different cathode sizes. The substrate is doped at $N_a = 10^{12}$ cm^{-3}, and the wells are defined by analytical doping profiles. Photodiodes are reverse biased at 3 V. White lines: SCR edge.[1]

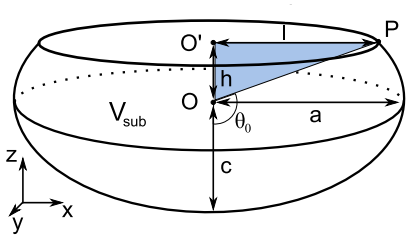

Fig. 3. Schematic of a space-charge volume extension underneath an n-well in a low-doped p-type silicon, as calculated in the Appendix.

A 3-D effect on the SCR geometry is observed due to the use of a relatively small photodiode size (≈10 μm in image sensor applications) and a low-doped ($N_a = 10^{12}$ cm^{-3}) silicon substrate. In particular, the simulations show that the depleted depth and the lateral extension depend on the photodiode size, which is not accounted for in (1). Hence, (1) overestimates the depleted depths for the typical photodiode sizes in image sensors.

To better understand the cathode size effect on the SCR in the substrate, and to obtain a fast and relatively accurate estimation of the depleted depth for such photodiodes, an analytical model has been developed. The SCR in the low-doped substrate represented in Fig. 3 is approximated by an ellipsoid intersected by a plane defined by the wells–substrate interface. l is the cathode half length, and h allows to estimate the depth location of the ellipsoid in the substrate. The depleted volume in the substrate V_{sub} can be calculated from the total charge neutrality principle

$$V_{\text{sub}} = \frac{N_d V_d}{N_a} \tag{2}$$

and by assuming that the 1-D model (1) is still accurate in the n-well because of its relatively high doping concentration. h and l are sufficient to estimate the depletion depth and the lateral extension. The calculation detailed in the Appendix yields (3), which can be numerically solved to find h as a function of l and of the depleted volume in the substrate V_{sub}

$$V_{\text{sub}}(h) = \frac{2\pi}{3f}(l^2 + h^2 f^2)^{\frac{3}{2}}\left(1 + \frac{fh}{\sqrt{l^2 + h^2 f^2}}\right) + \frac{\pi}{3}hl^2. \tag{3}$$

[1]Sentaurus defines the depletion region as the volume where the majority carrier concentration is <10% of the impurity concentration.

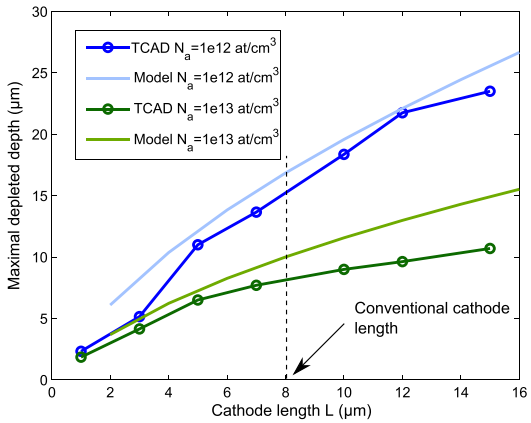

Fig. 4. Maximal depleted depth of a photodiode as a function of its cathode length. A similar trend is observed between the TCAD simulations and the ellipsoid model.

The TCAD simulations show that the ratio of the ellipsoid axes $f = a/c$ remains relatively constant for the doping and cathode sizes of interest here (≈1.2 based on seven different photodiodes). Once h is known, the maximal depth and the lateral extension of the depleted volume are deduced from (12). A comparison of this model with the TCAD simulations shows, as shown in Fig. 4, similar behavior of the SCR maximal extension W_{dep} with the cathode length.

Despite the simple considerations regarding geometries and depleted volume, this model shows a clear dependence between an ellipsoid SCR extension in the bulk and the cathode size. Section III shows the consequences of the SCR extension in a pixel array.

III. Punchthrough Current in a Pixel Array as a Tool for SCR Investigation

A. Punchthrough Current Simulation in a Photodiode Array

Photodiodes with different reverse biases and merged SCRs could generate a punchthrough current similar to the one observed in an NPN transistor.

Such a phenomenon was investigated through TCAD simulations using analytical doping concentrations. The simulated structure displayed in Fig. 5(a) is a line of five 7.5-μm-long p-n photodiodes spaced by 2-μm-long p-wells, in a low-doped ($N_a = 10^{12}$ cm^{-3}) p-type silicon. The photodiode D1 at the left is biased with a fixed potential V_{test}, whereas the four other photodiodes have floating potentials, which have been initially reset at $V_{r0} = 4$ V at $t = 0$ s (as would be the case during the charge integration phase in a 3T image sensor operation). P-wells are grounded. Fig. 5(b)–(d) shows the evolution of the potential of each photodiode in dark conditions and for various values of V_{test}.

The floating photodiode potentials tend to follow the V_{test} potential with a different rate depending on V_{test} and the

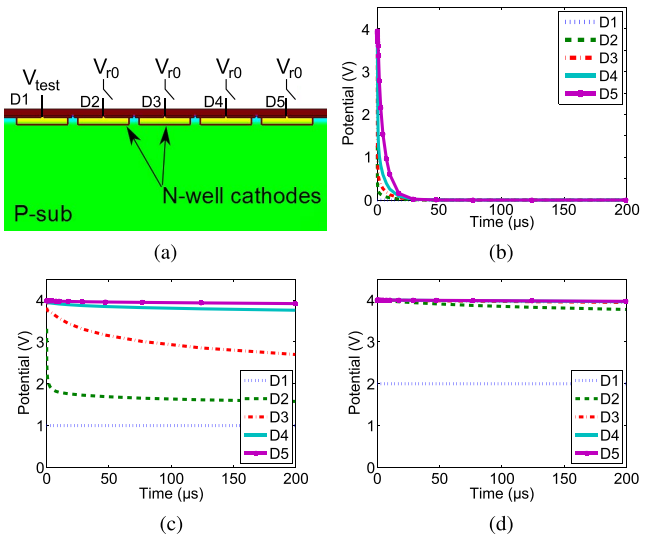

Fig. 5. Transient TCAD simulations of the simulated structure give different potential evolutions depending on the V_{test} value. At $t = 0$ s, the potential on D2–D5 is $V_{r0} = 4$ V, and is floating during the simulation. D1 potential is fixed at V_{test}. (b) Strong punchthrough occurs when $V_{\text{test}} - V_{r0}$ is high. (c) and (d) Reducing the voltage drop between these photodiodes reduces the punchthrough impact. P-wells are grounded in all the simulations. (a) Simulated structure. (b) $V_{\text{test}} = 0$ V. (c) $V_{\text{test}} = 1$ V. (d) $V_{\text{test}} = 2$ V.

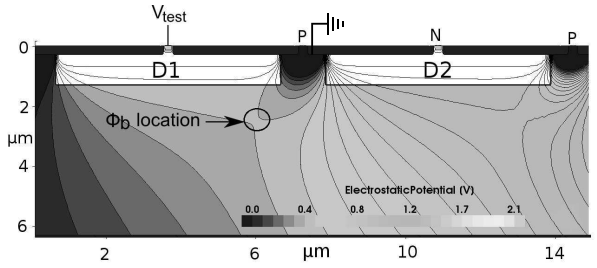

Fig. 6. TCAD simulation of the electrostatic potential of two photodiodes biased with different voltages separated by grounded p-wells. A potential barrier between the two cathodes appears below the p contacts.

distance from D1, indicating different punchthrough current intensities. If these photodiodes were used in a pixel array, the pixels' dark response would depend on the potential difference $\Delta V = V_{\text{ref}} - V_{\text{sig}}$, V_{ref} and V_{sig} being the sampled potentials at the beginning and at the end of the integration time, respectively. A bloominglike effect would appear around the fixed bias pixel.

The conduction mechanism between the photodiodes is driven by the charge injection over a potential barrier [8]. For relatively high voltages between D1 and D2 photodiodes (hence, at $t = 0$ s), punchthrough current is relatively high, but then decreases rapidly with the potential difference reduction as it depends exponentially on the potential barrier ϕ_b [8], shown in Fig. 6

$$I_{\text{th}} \propto A \exp\left(-\frac{q\phi_b}{kT}\right) \tag{4}$$

where A is a constant. Fig. 7 compares the simulated current flowing through D1 as a function of time and the theoretical current given by (4) fitted to the simulated TCAD current.

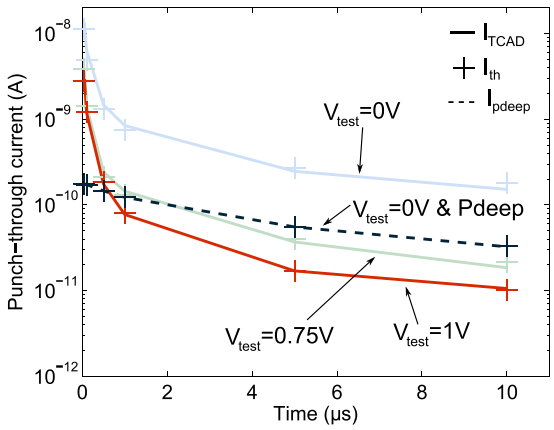

Fig. 7. Punchthrough current as a function of time and V_{test} for the same configuration as in Fig. 5. Solid lines: TCAD-simulated current flowing through D1: I_{TCAD}. Cross markers: current calculated by (4): I_{th}, fitted to the simulated current using the preexponential constant A. Use of a deep p-well (Pdeep) limits the current density by increasing the barrier potential.

TABLE I

TCAD-SIMULATED PUNCHTHROUGH CURRENT FROM A 3 V POTENTIAL DIFFERENCE FOR VARIOUS VALUES OF CATHODE LENGTH L AND CATHODE SPACING

	Spacing between cathodes (μm)		
L (μm)	1.5	3.5	5
1.5	5.1×10^{-9} A	3.3×10^{-12} A	4.5×10^{-13} A
5	4.0×10^{-7} A	9.0×10^{-9} A	6.1×10^{-10} A
7.5	5.5×10^{-7} A	2.8×10^{-8} A	3.7×10^{-9} A
10	6.2×10^{-7} A	4.5×10^{-8} A	8.1×10^{-9} A

As expected, the current density decreases with time due to the ϕ_b variations caused by a potential difference reduction. The barrier height in these simulations ranges from 0.14 to 0.33 V for the highest and lowest currents in Fig. 7, respectively.

As the potential barrier ϕ_b depends on the SCR extension between the photodiodes, it also depends on the cathode length because of the SCR geometrical variation presented in II. For example, Table I presents the simulated punchthrough currents for various cathode sizes and spacings. Increasing the cathode size yields higher current, confirming that the punchthrough current (and the SCR extension) depends on the cathode size for a given spacing.

B. Punchthrough Current Reduction Using deep P wells (Pdeeps)

As it can be seen from Fig. 6, the potential minimum is located at ~ 2 μm below the silicon surface between the cathodes. The Pdeep (located underneath the conventional wells) could be used just below the conventional p-well in order to increase the potential barrier at this location. The simulations using the structure from Fig. 5(a) but with the Pdeeps in-between the cathodes were carried out, and Fig. 7 presents the results for $V_{\text{test}} = 0$ V. Punchthrough current in this case decreases by about one order of magnitude compared with the structure without Pdeep. This confirms the ϕ_b increase and the limited SCR extension caused by the additional Pdeep.

The protocol used in Fig. 5 can be used on a real pixel array to demonstrate the SCR dependence on the pixel geometry.

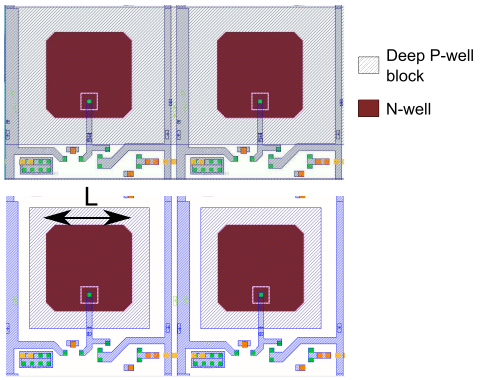

Fig. 8. Layouts of pixels with a given cathode size L. Top: Pdeep is only integrated below the in-pixel circuit. Bottom: Pdeep is also integrated between the cathodes of different columns.

A test vehicle was designed to study these variations, to define safe design rules for CMOS image sensors integration on HR silicon, and to estimate its achievable electrooptical performances using the conventional biases.

IV. Test Device Description

A CMOS image sensor including a 3T pixel array, address decoders, and a readout circuit was designed on a p-type float-zone substrate doped at $N_a = 10^{12}$ cm^{-3} using a CMOS technology with 5 V analog bias. The pixel array contains two pixel pitches (10 and 20 μm), and is divided into different subarrays corresponding to several pixel variations. Various cathode sizes are integrated, and the Pdeep was partially removed from some pixel variations, except below nMOS transistors. Fig. 8 shows the design differences between with and without Pdeep pixels. Each pixel variation is implemented in a 32 × 32 pixels subarray as a compromise between the subarray sizes and statistics, and to limit the impact of neighboring pixel variations. The very low substrate doping was measured by spreading resistance profiling around 10^{12} cm^{-3}, confirming the high resistivity of the processed wafer.

V. Photodiode Design Impact on SCR Extension Studied by Punchthrough Measurements

A. Evidence of Punchthrough Current Dependence on Cathode Size

The same experiments as the one shown in Fig. 5, were conducted on the pixel array using dedicated pixels (called test pixels), for which the cathode potential is controlled by a constant external bias source. The pixel test neighbor responses are monitored as a function of the pixel test cathode bias V_{test} during a normal array operation in dark conditions. P-wells in the pixel array are grounded. The neighbor responses indicate whether or not a current flows between the pixels during the integration time.

Fig. 9 shows the mean current intensity during the integration time t_{int} as a function of V_{test} for four different pixels. The mean current is estimated by $I(V_{\text{test}}) = q \times \Delta V(V_{\text{test}})/(\text{CVF} \times t_{\text{int}})$, using the charge-to-voltage conversion factor (CVF) of each pixel variation. Using two different pixel pitches (10 and 20 μm), we can compare the mean current

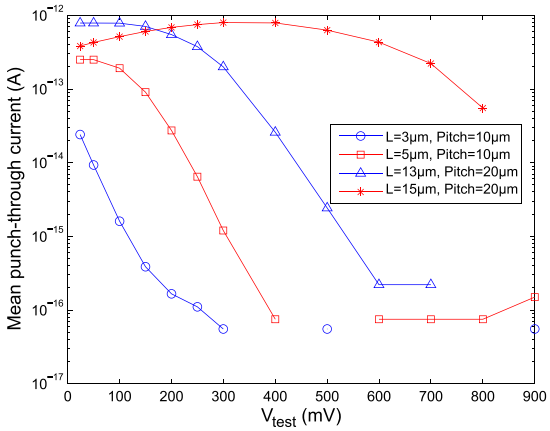

Fig. 9. Measured mean punchthrough current versus test pixel bias V_{test} for four pixel variations. Thanks to different pixel pitches (10 and 20 μm), cathodes with $L = 3$-μm and $L = 13$-μm edge sizes share the same 7-μm spacing. Cathodes with $L = 5$ μm and $L = 15$ μm share a 5-μm spacing.

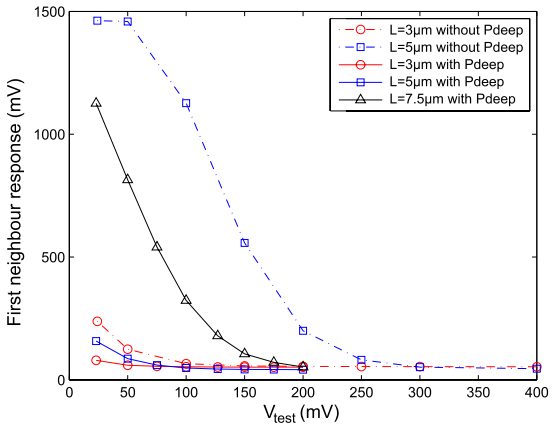

Fig. 10. Measured first neighbor response as a function of V_{test} for various cathode sizes in a 10-μm pixel pitch, with and without Pdeeps around the cathodes.

between the two cathodes with similar spacing (5 or 7 μm) but with different sizes (L =3 and 13 μm for a 7-μm spacing, and L =5 and 15 μm for a 5-μm spacing). The mean current is clearly higher for a larger cathode, and its threshold voltage is also higher (meaning a lower potential differences threshold between the adjacent cathodes), indicating a larger SCR extension for a given spacing and a larger cathode.

For the largest cathode (15 μm), the current decreases for lower value of V_{test}. This is actually an artifact caused by too large punchthrough current. In this case, V_{sig} is saturated at its lowest level, and a very large current decreases the cathode potential during the 1-μs sampling time of V_{ref}. Hence, the measured value of V_{ref} decreases as the punchthrough current increases, which depends on V_{test}.

These results confirm that the SCR extension is caused solely by the cathode size increase.

B. Limitation of the Punchthrough Impact With Pdeep

For the same cathode size, 10-μm pitch pixels have been integrated with and without Pdeep around the cathodes. The punchthrough measurement results in Fig. 10 confirm

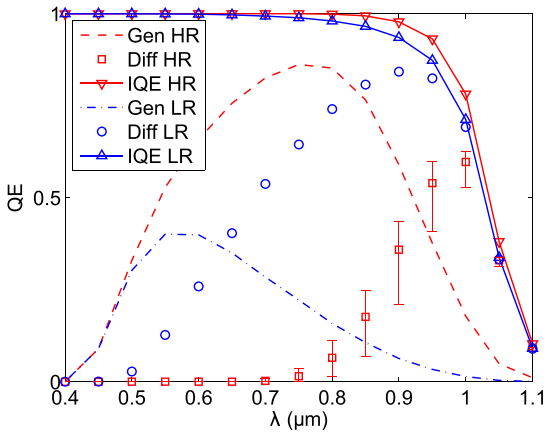

Fig. 11. IQE simulations for HR and LR infinite silicon substrates. Contributions from the depletion (Gen) and quasi-neutral regions (Diff) are displayed for each substrate. Error bars: diffusion variations for $N_a = 5.10^{12}$ cm^{-3} $\pm$ 60%.

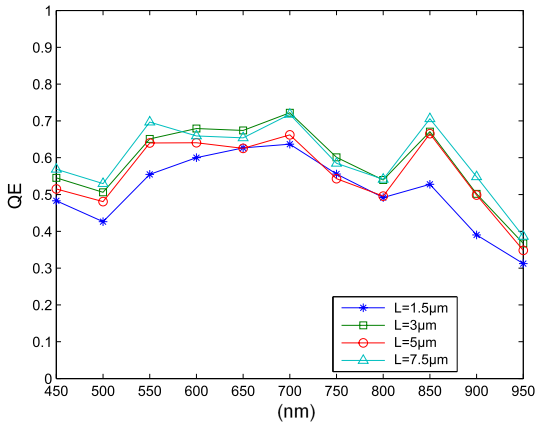

Fig. 12. Measured QE for four different cathode sizes in a 10-μm pixel pitch.

the simulation results as the Pdeep reduces the measured punchthrough impact on the test pixel neighbors.

Electrooptical performances being dependent on SCR, one has to expect higher performances for larger cathode length and without Pdeeps. However, for the same spacing, a larger cathode suffers higher punchthrough current, and a tradeoff must be found. To avoid the punchthrough current in a 10-μm pixel pitch, the cathode length must be 5 μm with a Pdeep and under 5 μm without Pdeeps. In a 20-μm pixel pitch, these sizes are 13 and 10 μm with and without Pdeeps, respectively. Section IV investigates the electrooptical performances as a function of the pixels geometry.

VI. Electrooptical Performances

The electrooptical performances were measured for a front-side illumination using an integrated sphere and 11 interferometric filters ranging from 450 to 950 nm. The CVF was deduced from the Pain–Hancock nonlinear estimation method [9]. The crosstalk was measured with a two-layer-thick metal shield deposited on entire subarrays, and figuring apertures above few pixels. Eventually, the dark current was measured at various temperatures.

A. Quantum Efficiency

Internal QE (IQE) is defined as the ratio of collected charge versus photo-generated charge. An analytical tool developed in [10] and solving the charge diffusion equations is used to compare the performances between the HR and the low-resistivity (LR) bulk silicon. We calculate the IQE for HR silicon ($N_a = 5.10^{12}$ cm^{-3}) and LR bulk silicon ($N_a = 10^{15}$ cm^{-3}), as well as the contributions from the depletion region (Gen) and the quasi-neutral region (Diff). Based on an empirical relation from [11], 600-μm-thick substrates are defined with the electron lifetimes of $\tau = 1$ ms (HR) and $\tau = 0.1$ ms (LR). The results in Fig. 11 show an IQE improvement using HR silicon. The good IQE for the LR bulk substrate is mainly due to the large diffusion current, which is also responsible for the crosstalk in a pixel array.

The measured external QEs (the ratio of collected charge on the incoming photons on the photosensitive surface) are displayed in Fig. 12 for four pixels with a 10-μm pitch and different cathode sizes. This external QE is impacted by light loss in the front-side optical stack. Slight differences can be seen between the variations, which can be related to a CVF measurement uncertainty as the difference is constant with the incident wavelength. A more pronounced decrease is visible for the smallest cathode especially in the near-infrared, which is attributed to a weaker SCR extension in the bulk. Considering a front illumination through a nonoptimized optical stack, the overall response is good, with a limited decrease in the near-infrared spectrum compared with the visible part of the spectrum. Collection of charges generated deep in the substrate is achieved thanks to the large float-zone substrate photosensitive volume and to the long electron diffusion length. However, the charge diffusion is expected to increase the crosstalk, as discussed in Section VI-B.

B. Crosstalk

The crosstalk is the amount of signal in a pixel due to the light incident upon its neighbor pixels. It was measured by using the metal optical shield and by comparing the slope in the electrooptical transfer function linear part of the illuminated pixel with its neighbor's one (which is blind due to the optical shield).

Fig. 13 shows the crosstalk between the pixels with a 20-μm pitch. For the middle wavelengths (between 550 and 700 nm), the crosstalk decreases with the cathode size until it reaches a minimal value for 10 μm and higher cathode lengths. This is mainly due to the SCR extension in the pixel. For a wavelength longer than 750 nm (corresponding to a 8-μm absorption depth), the charges are generated deeper in the substrate, and the crosstalk differences between the 10-μm and higher cathode lengths arise because of the deeper depletion extension of the larger cathodes. For a short wavelength, a higher crosstalk is measured than for a middle wavelength. The TCAD simulation presented in Fig. 13 shows similar trends but with a wavelength shift,[2] and the simulated

[2]Simulations are not calibrated with the selected technology.

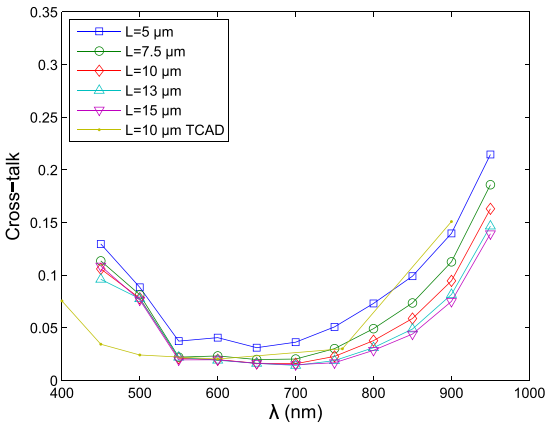

Fig. 13. Measured crosstalk for five different cathode sizes in a 20-μm pixel pitch and the TCAD simulation showing similar trends.

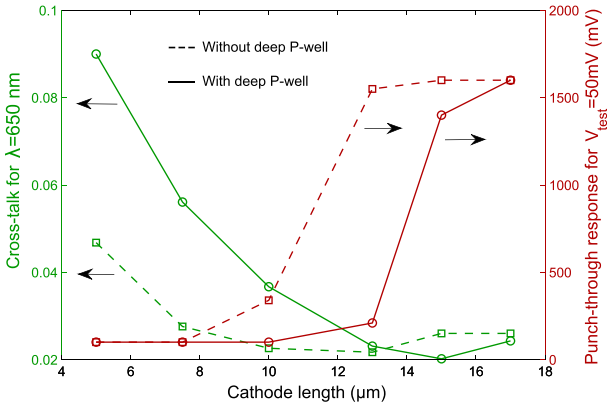

Fig. 14. Punchthrough and crosstalk as a function of the cathode length for a 20-μm pixel pitch, with and without Pdeeps.

short wavelength crosstalk can be explained by an increase in the amount of charges generated in the undepleted p-wells between the cathodes compared with a longer wavelength.

Therefore, increasing the cathode size reduces the crosstalk, but its value seems to saturate to a minimal value for the middle wavelengths. For the longer and shorter wavelengths, the crosstalk increases due to the bulk or surface diffusion process, respectively.

C. Optimum Pixel Design From Punchthrough and Crosstalk Study

If the largest cathodes provide the lowest crosstalk, they are also the most punchthrough sensitive. One could find the optimum cathode size and pixel pitch by studying both the parameters. To this extent, Fig. 14 shows the first neighbor crosstalk for $\lambda = 650$ nm and the punchthrough response for $V_{\text{test}} = 50$ mV as a function of cathode size. As the cathode size increases, the crosstalk decreases until it reaches a minimal value. Just before this point, the punchthrough response starts to increase. Both the phenomena are related to the lateral SCR extension, and this graph indicates the geometrical conditions for which a tradeoff can be found in a given pixel pitch.[3]

[3]The results from a 20-μm pitch are displayed here due to the various cathode sizes available.

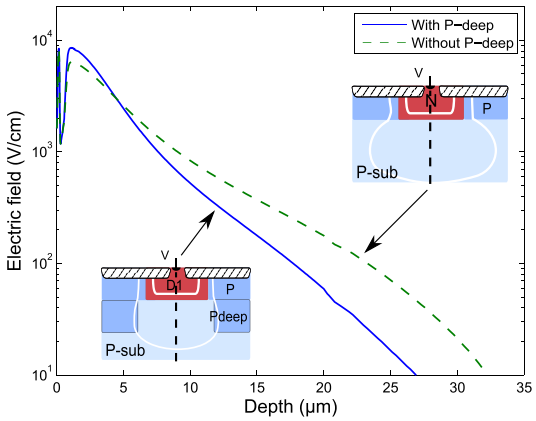

Fig. 15. TCAD simulations of electric fields as a function of depth just below the cathode center, with and without Pdeeps around the cathode.

TABLE II
DARK CURRENT AT 22 °C AND ACTIVATION ENERGY FOR 10-μm PIXEL PITCH

Cath. length (μm)	J_{obs} at 22°C (nA/cm^2)	E_a (eV)
1.5	2.5	1.06
3	2.65	1.02
5	2.66	1.00

The Pdeep impact on the SCR extension is clearly seen in Fig. 14, as it requires a larger cathode size with a Pdeep to achieve similar performances than without Pdeeps. The impact of such feature on the SCR was studied through the TCAD simulations using analytical profiles for the wells and comparing pixels with and without Pdeeps around the cathodes.

Fig. 15 shows the depth profile of the electric field at the cathode middle axis with and without Pdeeps. The electric field gradient is higher with the Pdeep than without, meaning that the SCR extension in the substrate is more limited. Therefore, the SCR extension is not only laterally strained but also limited in depth by the Pdeep. Hence, the Pdeep hinders the achievable electrooptical performances.

D. Dark Signal

Dark current was measured at temperatures ranging from 5 °C to 30 °C in a controlled temperature chamber in order to extract its activation energy. Equation (5) was used to extract the activation energy E_a and to estimate the main dark current source in our device.

The results are displayed in Table II for a 10-μm pixel pitch. The dark current at 22 °C is relatively high compared with other 3T pixel sensors, and could be explained by the larger depleted bulk volume providing a generation current $I_{\text{gen}} \propto \exp(-Eg/2kT)$, Eg being the silicon bandgap energy, and by a large diffusion current $I_{\text{diff}} \propto \exp(-Eg/kT)$ [7, p. 182]. Table II shows that the activation energy is between 1 and 1.06, meaning that the dark current has a nonnegligible diffusion component as it nearly follows a diffusion current dependence with temperature, which would correspond to an activation energy of ∼1.2 eV. This is due to the large amount

of minority carriers available for the diffusion process in the float zone p-substrate

$$I_{\text{dark}} \propto \exp\left(-\frac{E_a}{kT}\right). \tag{5}$$

VII. Discussion and Perspectives

This paper demonstrates very good QE but degraded crosstalk for near-infrared wavelength, and a high diffusion current (dark and photocurrent). All these results are partly attributed to the large quasi-neutral volume underneath the depleted volume. The crosstalk reduction is expected using backside bias or epitaxial wafers. Further considerations must be made in radiative environments, as the larger depleted volume makes the sensor more sensitive to displacement damage dose than the sensors with a more conventional substrate [12].

The SCR defined by the ellipsoid model is calculated for only one photodiode. However, SCRs in a photodiode array partly merge together, and the depletion region becomes deeper to conserve the overall neutrality principle. Hence, the depleted depth is smaller than the 1-D Poisson equation estimation but higher than the one predicted by the ellipsoid model, and depends on the cathode size and the pixel pitch.

For the doping concentration of interest ($\approx 10^{12}$ cm^{-3}), doping level variations are expected between different processed wafers, and the doping concentration measurements remain inaccurate. For a given pixel design, these variations would affect performances. As an example, the error bars in Fig. 11 show the diffusion component variations for $N_a = 5.10^{12}$ cm$^{-3} \pm 60\%$, which can lead to a crosstalk increase.

Increasing the reverse bias of the photodiodes would reduce the crosstalk and increase the bias threshold for punchthrough effects [13]. It would also reduce the performances variability caused by possible doping variations in manufactured wafers. Yet, applying higher voltage than the technology voltages remains difficult in a monolithic APS, as the front-side transistor wells require proper biasing. In this case, multiple well processes could be a solution to isolate the wells from the substrate bias [14].

VIII. Conclusion

We have investigated the performances of a monolithically integrated CMOS image sensor on an HR p-type float-zone silicon wafer, processed in a conventional image sensor CMOS foundry. An analytical model and the simulations show that the SCR extension in the substrate depends on the pixel design (cathode size, implants, and pixel pitch), and is smaller than the theoretical estimation from the 1-D Poisson equation solution.

A method based on punchthrough currents is proposed to study the SCR extension, and confirms the SCR variation with the pixel geometry.

The electrooptical characterizations show a limited QE decrease for a near-infrared wavelength, keeping its value >0.3 up to $\lambda = 950$ nm. However, the crosstalk is degraded by a factor 5 between 700 and 900 nm. Both the results are due to the large neutral volume below the depleted regions, with a long electron diffusion length, allowing a large photosensitive volume (hence, high QE) dominated by a diffusion transport mechanism (hence, higher crosstalk for deeper generated charges). This diffusion volume is also mainly responsible for the relatively large dark current density.

A correlation is demonstrated between the crosstalk and punchthrough measurements, and can be used to estimate the optimal pixel geometry (cathode size and Pdeep implantation) for a given pitch. The Pdeep reduces the SCR extension, and should mainly be used if the cathode spacings and size tailoring are not sufficient to prevent strong punchthrough currents. These currents are of limited concern for a cathode length of 5 μm with a Pdeep and under 5 μm without Pdeeps in a 10-μm pixel pitch, and for 13- and 10-μm cathode lengths with and without Pdeeps, respectively, in a 20-μm pixel pitch.

A backside bias is needed to further increase the electrooptical performances and to reduce the impact of the very low doping concentration variability on the sensor performances.

Appendix
SCR Ellipsoid Model

The depleted volume V_{sub} in the low-doped silicon from Fig. 3 is defined by the ellipsoid equation

$$\frac{x^2+y^2}{a^2} + \frac{z^2}{c^2} \leq 1 \quad -c \leq z \leq h \tag{6}$$

where a and c are the ellipsoid axes, as shown in Fig. 3. Equation (6) can be expressed in spherical coordinates

$$u^2 + v^2 + w^2 \leq 1 \tag{7}$$

$$\text{with} : u = \frac{x}{a}, \quad v = \frac{y}{a}, \quad w = \frac{z}{c} \tag{8}$$

which now define a spherical volume. The volume can be integrated using the substitution method. The Jacobian determinant of the transformation defined in (8) is $|J(u, v, w)| = a^2 c$, and leads to

$$V_{\text{sub}} = a^2 c \iiint du\, dv\, dw = a^2 c \iiint \rho^2 \sin\phi d\rho d\phi d\theta. \tag{9}$$

V_{sub} is the sum of two volumes V_c and V_s; V_c is the volume of a cone defined by the OO'P triangle revolution around the OO' axis, and V_s is the remnant volume of the ellipsoid

$$\begin{aligned} V_{\text{sub}} &= V_s + V_c \\ &= \int_0^{2\pi} d\theta \int_0^1 \rho^2 d\rho \int_{\theta_0}^{\pi} \sin\theta d\theta + \frac{\pi}{3} h l^2. \end{aligned} \tag{10}$$

For $z = h$, $w = h/c$, giving the integration limit θ_0: $\arccos h/c$. The total volume is then

$$V_{\text{sub}} = \frac{2\pi}{3} a^2 c \left(1 + \frac{h}{c}\right) + \frac{\pi}{3} h l^2. \tag{11}$$

A factor f between a and c was then introduced to reduce the number of unknown variables. The following relationships are used:

$$c = \frac{a}{f}, \quad \frac{l}{a} = \sqrt{1 - \frac{h^2}{c^2}}. \tag{12}$$

Using (12) in (10) leads to the complete volume equation (3) depending only on the unknown variable h

$$V_{\text{sub}}(h) = \frac{2\pi}{3f}(l^2 + h^2 f^2)^{\frac{3}{2}}\left(1 + \frac{fh}{\sqrt{l^2 + h^2 f^2}}\right) + \frac{\pi}{3}hl^2. \tag{13}$$

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