A Low-Power FPN Attenuation Method in the Double-Log PMOS APS

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***Abstract*—The active-pixel-sensor (APS) imagers operating in logarithmic mode yield high-dynamic-range images. However, this pixel exhibits a small output signal voltage swing. The double-log PMOS APS improves the signal swing in a factor higher than two compared with the conventional log APS. Fixed-pattern noise across the focal-plane array is particularly critical in the log mode, but can be reduced by double sampling techniques with a voltage reference. This voltage reference is established by means of an internal current and is subject to higher power consumption. In this work an in-pixel voltage reference in voltage mode is proposed, providing a more efficient control and consuming less power than the previous solution, while preserving five transistors per pixel, as before.**

Keywords-CMOS Image Sensor; APS; FPN; Wide Dynamic Range; logarithmic response;

I. INTRODUCTION

Active-Pixel Sensors (APS) have become the ruling choice in CMOS image sensors. In order to achieve a high dynamic range one solution is to modify the behavior of the pixel: the transistor connected to the photodiode is biased in subthreshold mode in order to provide an output voltage that has a logarithmic response with the photocurrent [1], [2] and [3]. The dynamic range is the ratio between the largest non-saturating input signal to the lowest detectable signal. Having a large dynamic range is a desirable feature in image sensors.

The basic logarithmic PMOS APS structure is presented in Fig. 1(a). The low sensitivity of about 50 mV per decade of illumination is one of the main drawbacks of this structure [4]. This limitation is shown by BSIM3v3 simulations in a standard CMOS 0.35 µm technology. The double-log PMOS APS presented in Fig. 1(b) has become an important architecture due to its improved sensitivity when compared to its basic version [4]. M_{load} is the output column amplifier, and in an imager array it is shared among all pixels in a column.

Several kinds of non-idealities limit the performance of CMOS image sensors. Fixed-pattern noise (FPN) is among those non-idealities introduced during fabrication that produce pixel-to-pixel variation under uniform illumination. FPN is caused by devices and interconnection mismatches across the imager array.

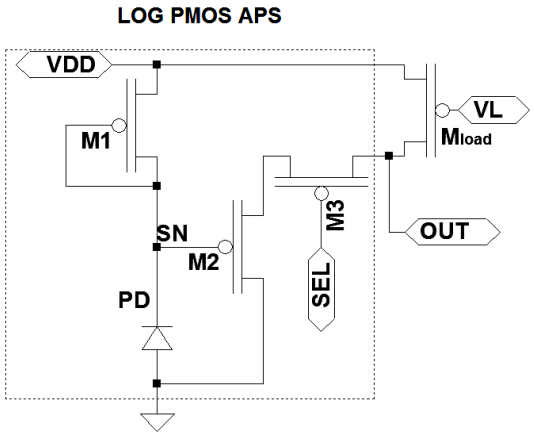
FPN is particularly critical when the APS is operating in logarithmic mode, because in this mode, the output signal swing of a single pixel associated with a one-decade variation in light intensity is of the same order of the mismatch in output signal observed among pixels fabricated on a given wafer batch [5]. Although classical techniques as correlated double sampling can be used to reduce FPN when the APS is operated in linear mode, they cannot be used in logarithmic mode [5], [6] and [7]. Therefore alternative techniques must be used to reduce FPN in logarithmic mode, as the establishment of a voltage reference at the sense node of the pixel, SN in Fig. 1(a) and (b).

To establish the voltage reference at the sense node of the pixel it is necessary to add an extra transistor, M5, to the pixel architecture as shown in Fig. 2 [4], [5] and [7]. This transistor sets a voltage reference during a specific period of time, hereafter indicated as reference time.

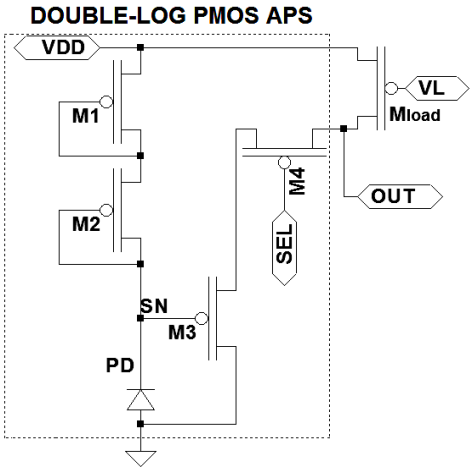
The technique herein proposed to attenuate FPN by voltage reference in the sense node is described in section II, where advantage is taken from the source of M5, which is kept available to the application of a properly chosen voltage level. Simulations results asserting the proposed solution are shown in section III. Finally conclusions drawn from this work are given in section IV.

II. FIXED-PATTERN NOISE ATTENUATION

The pixels presented in Fig. 1(a) and (b) operate in the logarithmic mode on which the light dependent output is produced as follows: the current flowing though M1 in both pixels charges the junction capacitance of the photodiode until the current through M1 reaches the same level of the photocurrent flowing through PD. The charge in the junction capacitance of PD produces a voltage that is also proportional to illumination. The output voltage varies logarithmically with the light irradiance level.



(a)



(b)

Fig. 1. (a) PMOS pixel operating in log mode; and (b) PMOS pixel with double-log configuration.

The light-dependent voltage output for the pixels in Fig. 1(a) and (b) are shown in Fig. 3 by the plots Vout1 and Vout2, respectively. In the BSIM3v3 simulation results presented in Fig. 3, Iph stands for the photocurrent produced at the photodiode PD that is proportional to the illumination condition at which the pixel is subject. The lowest and highest levels of Iph, in this case 10 fA and 1 μA, stand for the darkest and brightest illumination conditions respectively.

The signal swing in a given illumination range is the difference between highest and lowest output voltage levels produced by the pixel. The output of the APS of Fig. 1(a), Vout1 in Fig. 3, presents a signal swing around 300 mV in 120 dB of illumination. Conveniently, the output of the APS of Fig. 1(b), Vout2 in Fig. 3, presents a signal swing around 750 mV in 120 dB of illumination.

Due to device and interconnection mismatches called FPN, the voltage output between two pixels with the same dimensions, in the same array, may present differences, and therefore needs to be corrected. FPN causes image distortions under uniform illumination and thus requires attenuation [8] and [9].

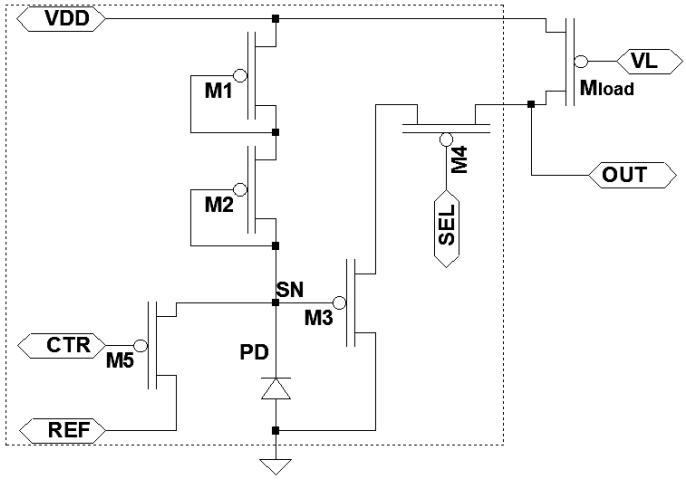


Fig. 2. Double-Log PMOS APS with additional transistor M5.

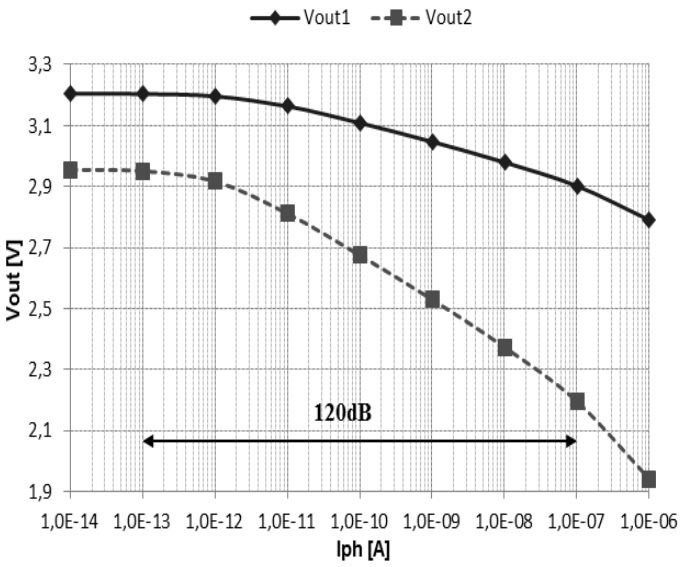


Fig. 3. Output voltages per photocurrent of the APSs in Fig. 1(a) and (b).

The APS presented in Fig. 2, with the REF terminal connected to GND, was first proposed in [4], it embodies an additional transistor M5 that is employed to establish a voltage reference at the sense node of the pixel that is used to implement FPN attenuation. Similar techniques are found in [5], [6], and [7] however these require external circuitry to perform FPN attenuation.

The FPN attenuation technique presented in [4] is performed in two different slots of time, as shown in Fig. 4, and it requires that the REF terminal of the APS in Fig. 2 be permanently connected to GND. In the first slot named logarithmic time the APS is set to produce the regular logarithmic response, with the CTR terminal of the pixel in Fig. 2 connected to VDD. In the second slot, named reference time, the CTR is connected to the GND and the reference voltage is produced at the output of the pixel. During reference time, M5 works in strong inversion and in the saturation region.

To attenuate the FPN, two samples of the output are taken: the first in the end of logarithmic time, S1 in Fig. 4, and the second during the reference time, S2 in Fig. 4. Then the second sample is subtracted from the first sample to generate the output with reduced FPN [4]. As the FPN information is present in both samples, the subtraction operation generates an output with reduced FPN.

The problem with the technique presented in [4] is the lack of control of the voltage reference level at the sense node during reference time. This happens because M5 lacks a good external control of its V_{GS} and therefore does not work properly as a current source as stated in [4] and [7]. The lack of V_{GS} control happens because the source terminal of M5 is connected to the sense node of the pixel that is dependent upon the light intensity. Therefore to set the current source at an appropriate value, it is necessary to first know the level of the sense node voltage, which is not practical.

In order to establish a better control of the voltage reference level at the sense node and to reduce the current flowing through M5, a simple change in the previous technique is proposed in this work. The proposed solution is to connect the REF terminal of the pixel to an external reference voltage instead of connecting it directly to the ground level. In this case M5 still works in strong inversion, however in the triode region.

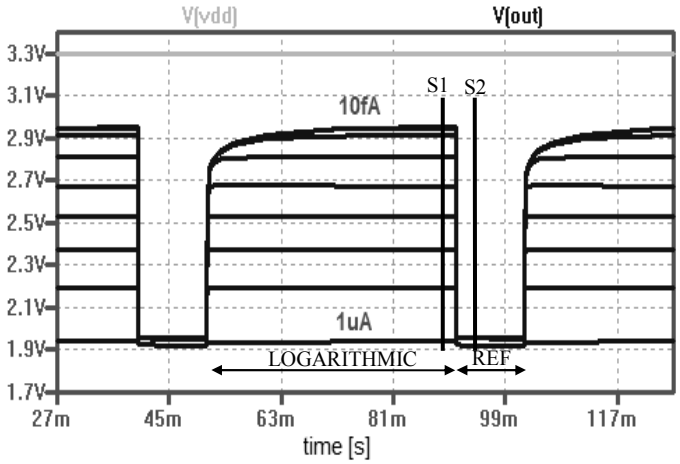


Fig. 4. Output voltage during logarithmic and reference time.

The external voltage reference level might be as close as possible to the voltage of sense node when the pixel is subject to the highest possible illumination level. In Fig. 4 it is assumed that the highest light level produces a photocurrent of 1.00 μA, which corresponds to an irradiance of about 415 KW/m^2 in a photodiode with an area of 137 μm^2. Nevertheless, if in a scene the highest photocurrent in the sensor array is 1nA the external voltage reference can be adjusted to the new level. This adjustment can be done based on the analysis of the previously captured scenes.

The great advantage of the proposed technique is that the current flowing through M5 during reference time can be reduced, thus reducing also the power consumption. The new technique is also able to adjust the level of the reference voltage according to highest level of illumination of a scene. This allows a better control over the current flowing through M5 during the reference time slot, as will be shown in the next section.

III. Simulations and Results

To assert the proposed solution, BSIM3v3 simulations were performed with the pixel of Fig. 3 in a standard 4-metal 2-poly CMOS 0.35 μm technology. Where all transistors have the same dimensions W = 0.70 μm and L = 0.35 μm. The photodiode is a p$^+$-diffusion/n-well diode with an area of 137 μm^2. In the following simulations, the logarithmic time lasts 50 ms, the reference time lasts 1 ms and the external reference voltage is 1.35 V. This value for the reference voltage was chosen based on the lowest voltage level of the sense node, when the pixel is subject to the brightest chosen condition.

The voltage reference V_{REF} at the sense node during reference time for the previous and the proposed solution are shown in Fig. 5 and Fig. 6 respectively. It is easy to note that the reference voltage of the proposed solution is closer to the lowest voltage level at the logarithmic time which is produced by the highest photocurrent of 1 μA.

The drain current through M5 during reference time for the previous and the proposed solutions are shown in Fig. 7, i_{ref_time1} and i_{ref_time2} respectively. As expected, the proposed solution can reduce the level of current through transistor M5 during the reference time. This might not appear significant for a single pixel but in real cameras, with extensive arrays with more than 10 thousand pixels, it represents a reasonable power saving. The reduced power consumption may for example extend the working time of the batteries of the camera.

The effectiveness of the proposed solution in attenuating FPN was verified via Monte Carlo simulations. A total of 256 Monte Carlo runs were performed in the pixel of Fig. 3 when the pixel was subjected to a photocurrent of 1 nA, which lies around the middle of the signal swing. The raw FPN, or standard deviation of the voltage output, before attenuation, is 17.7 mV; and the residual FPN, or standard deviation of the voltage output, after attenuation, is 5.8 mV.

The histogram of the results in number of pixel per grayscale intensity is shown in Fig. 8, where Raw FPN stands for the FPN before attenuation and Res FPN stands for the residual FPN after attenuation. In Fig. 8, the vertical axis stands for the number of pixels and the horizontal axis stands for the grayscale intensity. The 8-bit grayscale presents 256 different intensity levels, being 0 the darkest condition and 255 the brightest condition. The narrower the histogram curve is,

the less is the FPN present in the frame. These results assert the effectiveness of the proposed technique in attenuating FPN.

In the range of 120 dB shown in Fig. 2 the total signal swing of the pixel is around 750 mV. In this range, the pixel of Fig. 2 presents a total FPN of 2.36% of the total signal swing. The remained FPN after correction is 0.77% of the total signal swing. The results show that for the given conditions, the proposed technique can attenuate the total FPN more than three times.

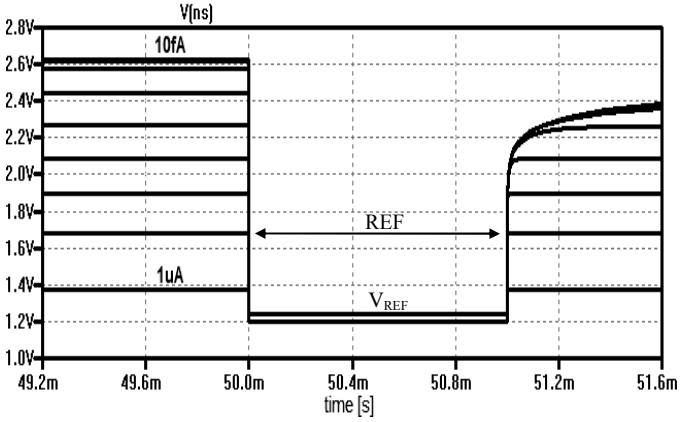


Fig. 5. Sense node plots with the previous solution.

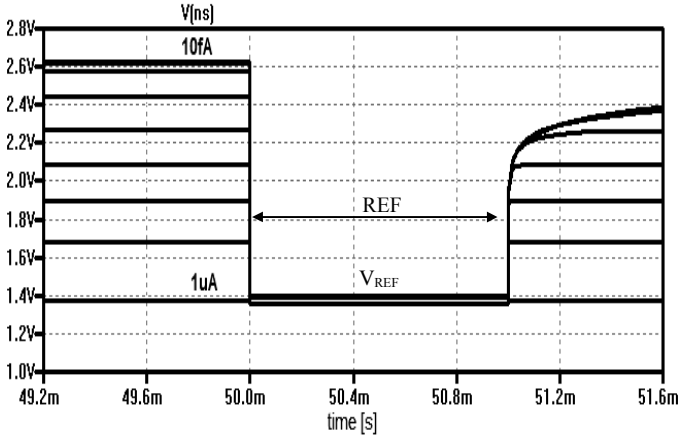


Fig. 6. Sense node plots with the proposed solution.

Now suppose a darker environment where the brightest regions in the image produce much smaller photocurrents per pixel of 1.00 nA, and not more 1.00 µA as in the previous assumption. In this case, if the setup remains the same and the external reference source remains at 1.35 V the proposed solution will still have a reduced current through M5, as can be verified comparing i_{ref_time1} with i_{ref_time2} in Fig. 7. Nevertheless, it can be improved if the external reference voltage level is changed to a value closer the voltage level of the sense node at the new brightest condition.

In the case of the darker environment described above, the previous technique would result in a sense node voltage during reference time as shown in Fig. 9. The plot in Fig. 10 shows the sense node response for a new condition of the proposed technique where an external voltage reference of 2.05 V is employed instead of 1.35 V applied to the previous condition.

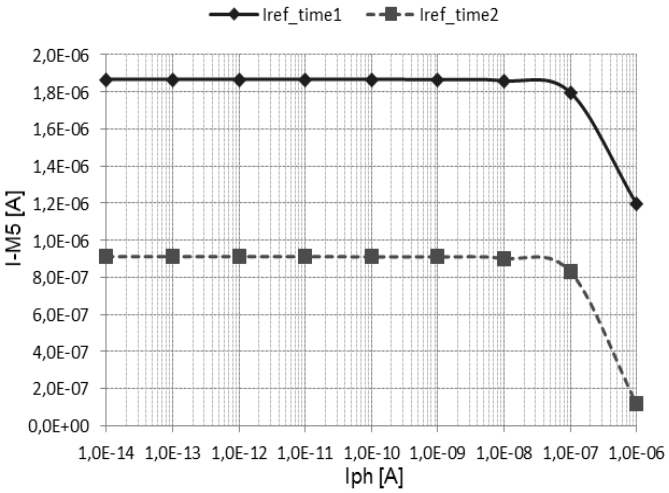


Fig. 7. Current through M5 with the previous solution. Current through M5 with the conventional solution (Iref_time1), and with the proposed solution (Iref_time2).

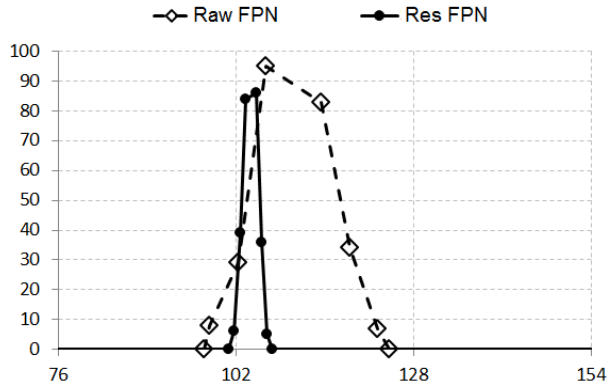


Fig. 8. Histograms of the Monte Carlo simulation results before and after FPN attenuation, Raw FPN and Res FPN respectively.

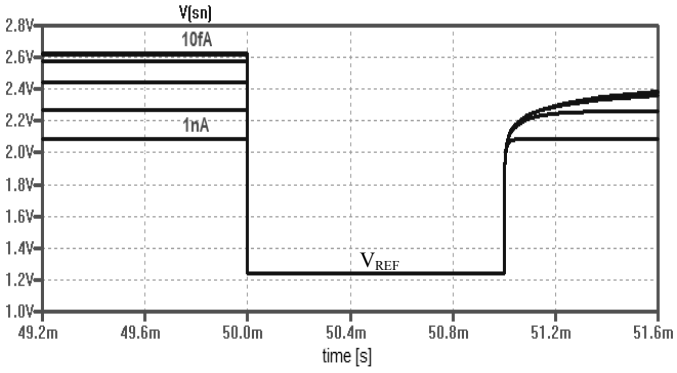


Fig. 9. Sense node waveform for the new condition with the previous solution.

The voltage reference during the reference time with the previous solution remains at the same level shown in Fig. 5. While the adjustment applied to voltage reference of the proposed solution yielded a voltage reference level closer to the sense node voltage level at the new brightest condition.

That produces a considerable reduction in the current through the transistor M5, as shown by the plots in Fig. 11.

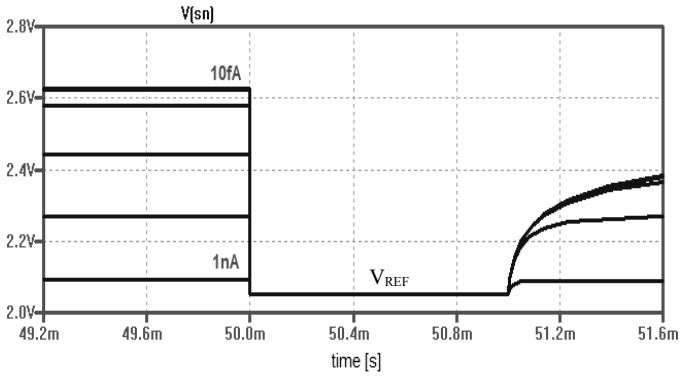


Fig. 10. Sense node waveform for the new condition with the proposed solution.

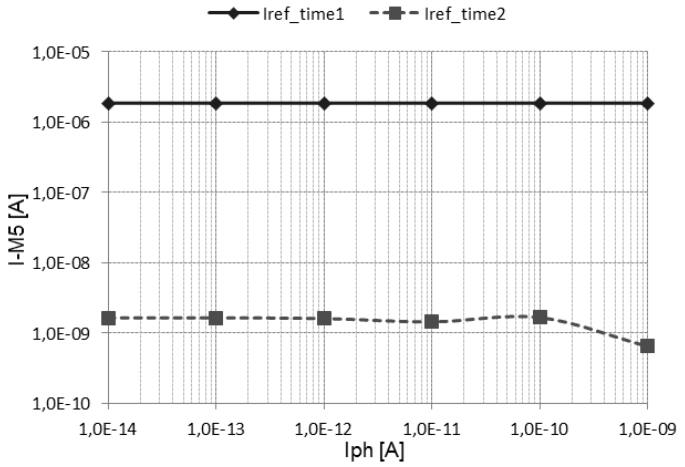


Fig. 11. Current through M5 for the new condition with the conventional solution (Iref_time1), and with the proposed solution (Iref_time2).

I. CONCLUSIONS

The new solution to reduce FPN in the double-log PMOS APS is also able to reduce the total power consumption of the circuit by reducing the current of the additional transistor of the pixel. Besides that, the proposed solution does not increase the pixel complexity by adding more transistors to the circuit structure. The fill factor of the pixel is still high, though the additional connection line, REF, slightly reduces it when comparing with the previous solution. This leads to a CMOS image sensor improvement at no additional fabrication cost. By revisiting and critically evaluating existing solutions, one can come to simple alternatives that can enhance the imager performance quite considerably.

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