Power Consumption Contrasting Model for Different Logarithmic Active Pixel Sensor Topologies

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***Abstract*—The literature presents many different active pixel sensor (APS) topologies operating in the high dynamic range logarithmic mode, as well as, different techniques to improve image quality by attenuating fixed-pattern noise (FPN). Together with the proposed solution, the advantages and disadvantages of each new solution are usually presented in their published reports. However, it is hard to find different solutions developed for the very same CMOS technology, and there is no standard model to effectively contrast their effectiveness according to parameters such as power consumption. This work analyses the power consumption of different logarithmic mode CMOS APSs topologies employing different FPN attenuation techniques. The purpose of such a study is the establishment of a way to contrast different solutions designed in the same CMOS technology, so that one can easily make a decision on what solution to choose based on different parameters, including power consumption.**

Keywords—Active pixel sensor; CMOS image sensor; power consumption; Fixed-Pattern Noise.

I. INTRODUCTION

The power consumption is a very important parameter to be take into account in any CMOS electronic circuit design [1] including image sensors. This is especially important to improve the autonomy of portable and high density microelectronic devices [2]. Reducing power consumption is also of especial interest when concerning the costs related to the power supply for portable or nonportable applications [1]. Applications of CMOS image sensors to the medical field require the integration of multiple image processing functions together with very limited power consumption requirements [3].

Thus, advances towards power consumption reduction bring in their bulge fundamental importance in electronic circuit design. In CMOS devices, the power dissipation may be attributed to factors such as external and internal capacitance charging and discharging. The internal power consumption depends directly on the applied source stimulus to the circuit, and is based in capacitance charging and discharging [4]. In this process, three aspects are especially relevant and must be considered: dynamic or switching power, short-circuit or glitching power and static or leakage power [1] [5].

$$P_{consumption} = P_{dynamic} + P_{short-circuit} + P_{static} \quad (1)$$

The consumed dynamic power is the main source of power dissipation [6], when the circuit has switching activities, charging and discharging a capacitor *C* modeled from the gate of a MOS transistor due to good insulation feature, under a frequency *f*. The $\alpha_{0\to1}$ term represents the node transition activity factor as follow:

$$P_{dynamic} = \alpha_{0\to1} C {V_{DD}}^2 f \quad (2)$$

Thereby the number and size of transistors, and the switching activity directly influence the dynamic power consumption, which is a very important factor for image sensor design with low power consumption [1].

Similarly the gate capacitance, defined as the parallel plate capacitor formed by the gate conductor, the thin oxide insulator and the channel [4], also contributes to dynamic consumption, once there is energy dissipation in each time its output switches, of the same level of the change of energy stored in the gate capacitance [7]. Therefore, in order to reduce the dynamic power consumption, many techniques have been proposed for gate resizing to reduce area and, consequently, getting a smaller capacitance as well a reduction of the chip area [2], [4].

The main disadvantage of this technique is the slowness of smaller gates and in order to face this disadvantage, only transistors out of critical parts of circuit are to suffer gate resizing. Thus, the topologies and operational speed are kept unaltered, but with a substantial power consumption reduction [2].

Others techniques seek to reduce power consumption by reducing switching activity or inhibiting devices structures that can be disabled for a certain period of time [8].

In some cases when the simultaneous activation of both NMOS and PMOS transistors takes place, a short circuit current from the power supply to the ground occurs [1]. Therefore, it generates a short-circuit power consumption:

$$P_{short-circuit} = I_{short-circuit} V_{DD} \quad (3)$$

Even when the transistor gate is not switching, or in its idle state, it presents a current leakage from the power supply to the ground. Such current leakage may arise from substrate current injection and subthreshold effects that were previously

considered in integrated circuit fabrication technologies [1]. This results in static power consumption:

$$P_{static} = I_{static} V_{DD} \quad (4)$$

The total absence of output glitching, also named spurious transitions [1], and reduced parasitic capacitance are some advantages of the CMOS dynamic behavior compared with static form. Nevertheless, CMOS static behavior has no additional power consumption due to pre-charging operations as in the dynamic one [7].

Although considering that the energy consumed by a single transistor CMOS in each switch time is small, the great number of high rate switching transistors has made the energy consumption one of the major design considerations. It is also worthwhile mentioning the accentuated downscaling of the size of transistors over the years, this entails that they ceased to change their states to completely off and the current leakage increases as the manufacturing technology scales down [5]. As any other integrated electronic circuit, CMOS image sensors are very sensitive to technology scaling and needs to compensate the reduced signal-to-noise ratio (SNR) and dynamic range caused by a low operating voltage. Such needs also are subject of study in others works [9].

The small amount of current leakage through each transistor culminate in significant power consumption when multiplied by millions or billions of transistors on a chip [2]. The same power consumption concerns are present in CMOS transistors employed into pixel sensors. It means that as the number of transistors in a pixel sensor increases the power consumption also increases.

In this work, it is presented a contrasting model that allows a fairer comparison, including power consumption, between different pixels topologies designed for the same fabrication technology employing different FPN attenuation techniques. The proposed method is based on the comparison of the results yielded by the different pixels, designed with different circuitry topologies but with same dimensions and in the same technology, where a low power consumption is one of the criterion is employed to define the best possible performance.

The paper is organized as follows: the description of the techniques and their topologies will be given in section II. Simulations results and discussion of the results are given section III. Finally, conclusions drawn from this work are given in section IV.

II. The Four Investigated Topologies

The contrasting methodology is built upon the analyses of the responses of four different pixel topologies, each one designed with different built in FPN attenuation methodologies.

The two first pixel topologies employed for the analyses herein presented are shown in Fig. 1(a) and (b). The first is an all NMOS version of the pixel topology proposed in [10], and the second is a pixel topology proposed in [11]. The output stage of the pixel in Fig. 1(a) is a simple current column amplifier, whereas the output stage of the pixel in Fig. 1(b) employs a differential column amplifier. The dimensions of all the transistors used in the investigated pixels topologies are given in table I.

The two built-in FPN attenuation techniques herein chosen employ current calibration methodologies, where the one employs in-pixel current calibration and the other external current calibration.

In order to investigate both the behavior and the related FPN of the pixel topologies in Fig. 1(a) and (b) when these pixels are designed with different output stages, the topologies presented in Fig. 2(a) and (b) are proposed. The pixel in Fig. 2(a) combines the pixel of Fig. 1 (a) with the output stage of the pixel in Fig. 1(b), and the pixel in Fig. 2(b) combines the pixel of Fig. 1(b) with the output stage of the pixel in Fig. 1(a).

In the four topologies presented in Fig. 1 and Fig. 2, the devices inside the area delimited by the dashed line are internal to the pixel, whereas the other devices are shared by all the pixels in a column of the imager array. The four topologies have been implemented in the 0.35-µm standard CMOS technology. The basic setup of the control signal in Fig. 1 and Fig. 2 for the operation in logarithmic operation is V_{DD} = 3.3 V, V_L = 0.9 V, V_{CAL} = 1.3 V, t_{STTL} = 31 ms and t_{REF} = 1 ms.

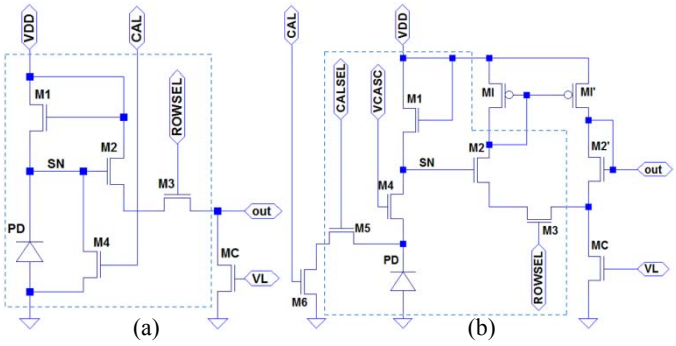

Fig. 1. (a) Logarithmic four FET Active Pixel Sensor (APS) designed for in-pixel current FPN calibration and with simple current column amplifier output stage; and (b) Logarithmic five FET APS designed for out-pixel current FPN calibration and with differential amplifier output stage.

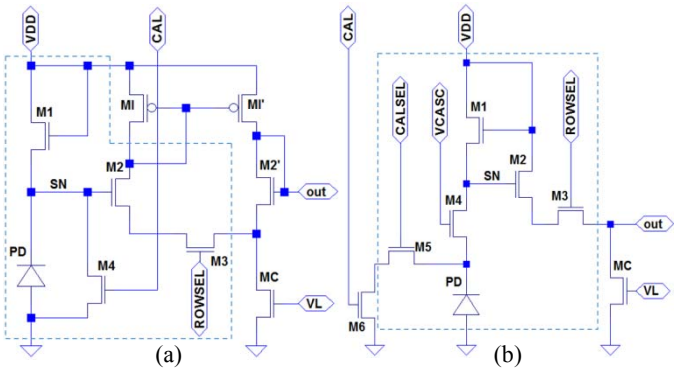

Fig. 2. (a) Logarithmic four FET Active Pixel Sensor (APS) designed for in-pixel current FPN calibration and with differential amplifier output stage; and (b) Logarithmic five FET APS designed for out-pixel current FPN calibration and with simple current column amplifier output stage.

TABLE I. DIMENSIONS OF TRANSISTORS

Transistor	Type	W [µm]	L [µm]
M1, M2, M2', M3, M4, M5, M6, MC	NMOS	0.7	0.35
MI, MI'	PMOS		

All four pixel topologies presented in Fig. 1 and Fig. 2 operate in the Wide-Dynamic Range (WDR) logarithmic mode, with the gate terminal of their reset transistor M1 set at V_{DD} level. The operation cycle of all four topologies are similar to the scheme presented in Fig. 3, where first the pixel is set to produce the light dependent logarithmic output V_{OUT_LOG} then a current source is set to produce the calibration output V_{CAL}. The light dependent output S1 is sampled at the end of the V_{OUT_LOG} period and the calibration output S2 is sampled at the beginning of V_{CAL}. Then the sample S2 is subtracted from S1 producing the output with reduced FPN [10], [12], [13], and [14].

The basic difference between the FPN calibration method employed by the pixel topologies in Fig. 1(a) and Fig. 2(a) from that employed by the pixels in Fig. 1(b) and Fig. 2(b) is that in the first case each pixel has its own current calibration source, whereas in the second case the current calibration source is shared by all the pixels in a column of the imager array. In either methods the terminal CAL of the current calibration sources are set to an adequate level in order establish the desired calibration current during the calibration time.

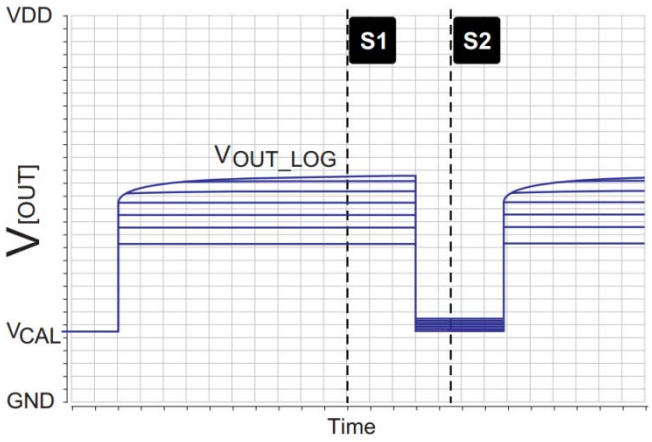

Fig. 3. Scheme of the FPN calibration method employed in this work.

The performance and characteristics of the four pixel topologies concerning their power consumption, complete output signal swing, effectiveness of the applied FPN attenuation methods, signal-to-distortion ratio, and pixel fill factor are contrasted among them in order to establish a decision methodology on what pixel design to choose. Details and discussions on the simulation results will be given in the next section.

III. SIMULATIONS RESULTS AND DISCUSSION

The power consumption of the four topologies presented in Fig. 1 and Fig. 2 were investigated through BSIM3v3 simulation. The current flowing through each pixel for eight different photocurrent levels is presented in Fig. 4. The same results are presented in plots with greater emphasis to photocurrents below to 10 µA in Fig. 5.

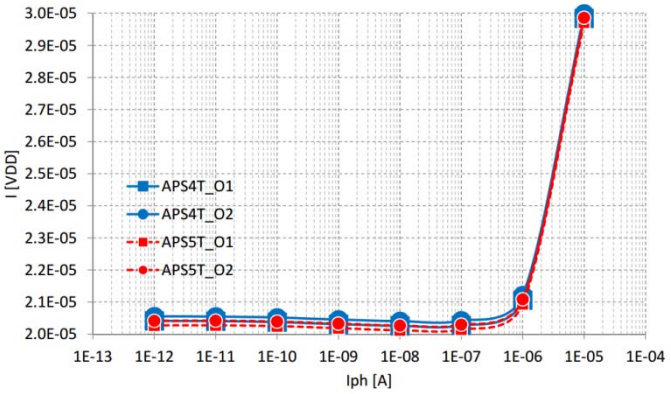

Fig. 4. Current consumption value versus photocurrent of the logarithmic four FET APS in Fig. 1(a) "APS4T_O1" and Fig. 2(a) "APS4T_O2" respectively, and of the logarithmic five FET APS in Fig. 1(b) "APS5T_O2" and Fig. 2(b) "APS5T_O1" respectively.

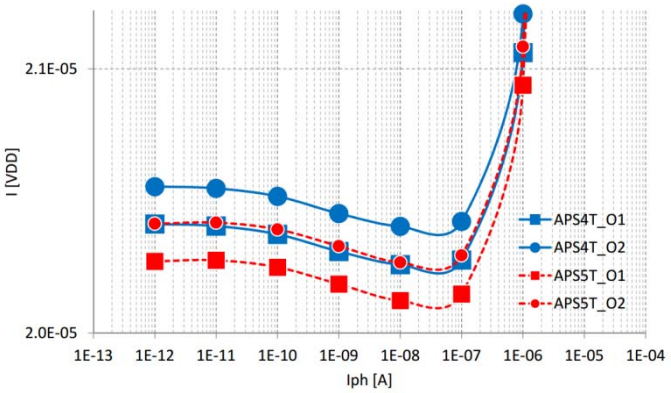

Fig. 5. Current consumption value versus photocurrent of the logarithmic four FET APS in Fig. 1(a) "APS4T_O1" and Fig. 2(a) "APS4T_O2" respectively, and of the logarithmic five FET APS in Fig. 1(b) "APS5T_O2" and Fig. 2(b) "APS5T_O1" respectively. Emphasis to photocurrents below to 10 µA.

Using the product of the voltage applied to V_{DD} and the simulated current consumption, the power consumption plots were generated for the topologies employed in Fig. 1 and Fig. 2. The power consumption results are presented in Fig. 6, and the same results are presented in plots with greater emphasis to photocurrents below to 10 µA in Fig. 7.

The lowering of the supply voltage level represents an effective way to reduce energy consumption since it has a quadratic impact on the power consumption as can be seen in (1). By controlling the threshold voltage and reducing it, the signal swing V_{DD} - V_{th} can be also reduced. Nevertheless the delay can be drastically increased, and special gates will be needed to eliminate short-circuit currents and restore the noise margin to the signal [1]. In this way, each application must judge the operational impact caused by signal swing reduction. This technique is most useful for high-capacitance nodes [1]

present in circuits. Thus, it's worth emphasizing that deliberated lowering of the power supply voltage level in a given fabrication technology may introduce biasing distortions and other limitations. Such a voltage level lowering can be done in an effective way through the choice of a different fabrication technology but depends upon the threshold voltage control and impacts on logic speed.

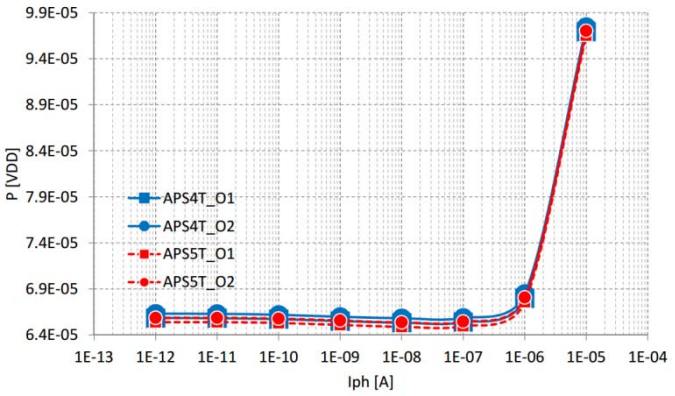

Fig. 6. Power consumption value versus photocurrent of the logarithmic four FET APS in Fig. 1(a) "APS4T_O1" and Fig. 2(a) "APS4T_O2" respectively, and of the logarithmic five FET APS in Fig. 1(b) "APS5T_O2" and Fig. 2(b) "APS5T_O1" respectively.

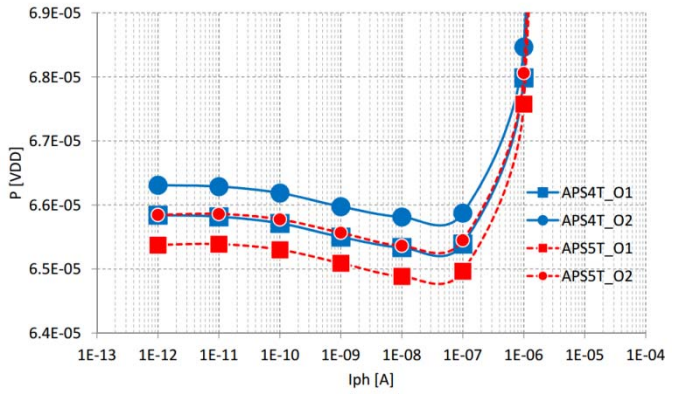

Fig. 7. Power consumption value versus photocurrent of the logarithmic four FET APS in Fig. 1(a) "APS4T_O1" and Fig. 2(a) "APS4T_O2" respectively, and of the logarithmic five FET APS in Fig. 1(b) "APS5T_O2" and Fig. 2(b) "APS5T_O1" respectively. Emphasis to photocurrents below to 10 µA.

From the plots presented in Fig. 6 and Fig. 7 it was found that, the pixel topology with the lowest power consumption is the one presented in Fig. 2 (b). Two factors are responsible for such a power consumption reduction in this pixel: the first is the slight higher resistance provided by cascaded scheme of M1 and M4, and the second is the reduced number of circuit branches of the output stage in this pixel topology.

The silicon area impact is another important point of view to be taken into account, because once a moderate increase in the circuit silicon area can also result in substantial impacts on the power requirements. In this scenario, it is greatly desirable for the image sensor circuit of interest to make use of a minimal silicon area, first because the releasing silicon area enables a higher integrated circuit density, and second because it reduces individual circuit cells power consumption [1]. In this way, the topologies as the APS4T using fewer transistors presents advantages over the others.

Besides the individual pixel power consumption, other important parameters to be taken into account when contrasting the performance and characteristics of a set of pixel topologies include complete output signal swing, effectiveness of the applied FPN attenuation technique, signal-to-distortion ratio, and pixel fill factor as presented in Fig. 8. Concerning the four investigated pixel topologies such characteristics are presented in Table II.

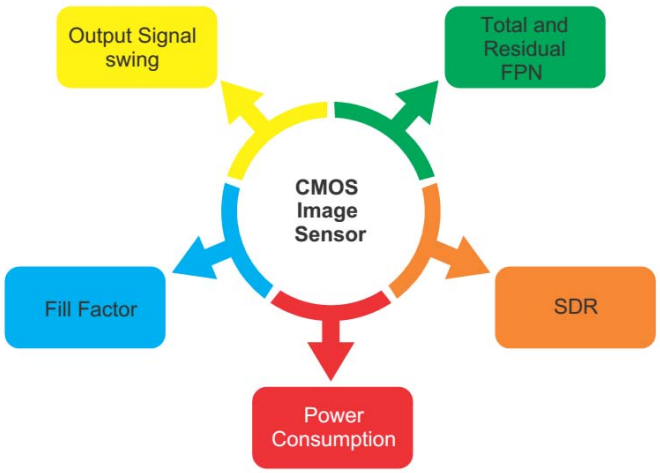

Fig. 8. Criteria for comparing pixels topologies.

In order to establish which of the four investigated pixel topologies can be considered the best to be employed in an imager array design, one of them might be taken as a reference and the other will have their characteristics contrasted with the reference. In this case, the pixel in Fig. 1(b) was chosen as reference and a contrasting percentage table comparing the four pixel topologies to the reference pixel was built, as presented in Table III. In this case all the results for the pixel in Fig. 1(b) are null, because this is the reference one. Concerning the other three pixel topologies, a positive value indicates a result better than the reference pixel, whereas a negative value means the opposite.

Aiming to better quantify the yielded results in the percentage Table III, a score varying from zero to seven was attributed for each given interval as stablished in Table IV. Then, considering each percentage interval in Table III, their sign whether positive and negative, and the scores interval in Table IV, the results in Table III were translated in a score table result as shown in Table V. Finally, the sum of all pixel scores in a column were made, and the results presented in the last row named results in Table V.

TABLE II. CHARACTERISTICS OF THE FOUR PIXEL TOPOLOGIES.

Criterion	APS-Fig1(a)	APS-Fig1(b)	APS-Fig2(a)	APS-Fig2(b)
Calibrated Signal Swing [mV]	374,78	415,10	429,89	361,75
Residual FPN [mV]	6,45	7,79	8,22	6,18
SDR	24,35	22,32	23,40	23,24
Power Consumption [µW]	70,00	70,10	70,50	69,90
Fill Factor [%]	40,46	37,91	40,46	37,91

TABLE III. DIFFERENCE AMONG THE FOUR PIXEL TOPOLOGIES IN PERCENTAGE TAKNING THE PIXEL IN FIG. 1 (B) AS REFERENCE.

Criterion	APS-Fig1(a)	APS-Fig1(b)	APS-Fig2(a)	APS-Fig2(b)
Calibrated Signal Swing [mV]	-9,71%	0,00%	3,56%	-12,85%
Residual FPN [mV]	17,16%	0,00%	-5,56%	20,72%
SDR	9,09%	0,00%	4,83%	4,12%
Power Consumption [mW]	0,07%	0,00%	-0,61%	0,68%
Fill Factor [%]	6,73%	0,00%	6,73%	0,00%

TABLE IV. SCORE BY PERCENTAGE INTERVALS

Interval [%]	Score
$0 < \|Val[\%]\| \leq 0,1$	0
$0,1 < \|Val[\%]\| \leq 1$	1
$1 < \|Val[\%]\| \leq 7$	3
$7 < \|Val[\%]\| \leq 14$	5
$14 < \|Val[\%]\| \leq 21$	7

TABLE V. PIXEL SCORES AND THE TOTAL RESULTS.

Criterion	APS-Fig1(a)	APS-Fig1(b)	APS-Fig2(a)	APS-Fig2(b)
Calibrated Signal Swing [mV]	-5	0	3	-5
Residual FPN [mV]	7	0	-3	7
SDR	5	0	3	3
Power Consumption [mW]	0	0	-1	1
Fill Factor [%]	3	0	3	0
Total	10	0	5	6

The results presented in Table V show that following the proposed contrasting methodology, the pixel in Fig. 1(a) is the one that presents the best set of characteristics, as indicated by the highest achieved score. Yet concerning the results in Table V it would have happened the occurrence of negative score results in the case where a different pixel topology was chosen as reference. However, it would not change the final result because the highest score in this method would yet define the most appropriate pixel topology concerning a chosen set of parameters.

Hence, CMOS image sensors designers can employ the proposed methodology to compare different APS pixel topologies operating in the logarithmic mode aiming the choice of most appropriated design option regarding a set of chosen parameter, including power consumption.

IV. CONCLUSIONS

Power dissipation consists in a highly relevant factor in CMOS devices projects. In this way a contrasting method regarding a chosen set of parameters including power consumption for different pixel topologies was proposed in this work. Estimating the power consumption in CMOS devices is not an easy job due to the influence of other power dissipation sources such as internal crowbar current when both n-type and p-type transistors are simultaneously turned ON, external sourcing and sinking of DC current, and junction leakage. Furthermore, the nonlinear behavior of the gate and junction capacitances makes this a more complex estimation [4]. Therefore, the proposed method to compare the performance and characteristics of different APS pixel topologies operating in logarithmic mode is a powerful and practical tool for image sensor design, since it is able to provide very important information based in a defined set of desirable characteristics, including power consumption.

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