Voltage Mode FPN Calibration in the Logarithmic CMOS Imager

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***Abstract*— The CMOS active pixel sensor (APS) operating in the logarithmic mode is the most common and useful CMOS wide-dynamic-range imager. Notwithstanding, fixed-pattern noise (FPN) between pixels compromises the quality of the image generated by the focal-plane array. Classical techniques as correlated double sampling do not work properly in this mode, and alternative techniques must be applied in order to calibrate FPN. The alternative techniques require either complex pixel circuitry, or external memory and software level calibration. Purposefully to improve image quality at reduced circuitry complexity, a new calibration technique is proposed that can be applied directly to the basic three-FET APS circuit. The efficacy of the proposed technique was experimentally verified with a small pixel array fabricated in a standard 0.35-μm CMOS technology. The experimental results show a steady FPN attenuation within the whole tested illumination range and the improvement of the signal-to-noise and distortion ratio of the array.**

***Index Terms*— Active pixel sensor (APS), CMOS image sensor, correlated double sampling (CDS), double sampling readout subtraction, fixed-pattern noise (FPN), wide dynamic range.**

I. Introduction

THE adequate functionality and circuitry simplicity are some of the characteristics that made the basic three-FET active pixel sensor (APS) architecture one of the preferred choices for CMOS image sensors design. APS circuits have a broad range of applications including those requiring operation with a wide dynamic range [1], [2], such as assistive onboard vision, monitoring of reflecting surfaces, laser welding inspection, and so on [3].

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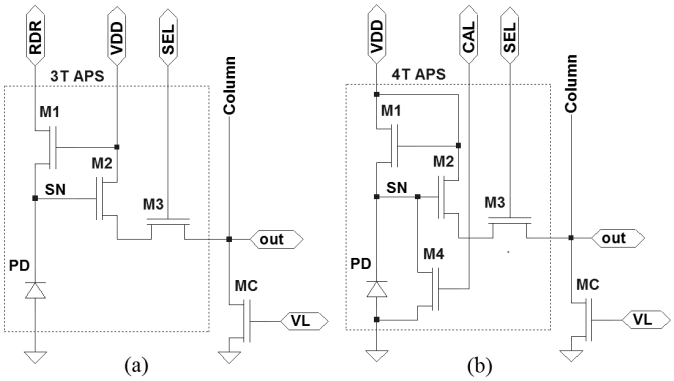

Fig. 1. (a) Three-FET APS with free RDR terminal on which the proposed calibration technique is applied. (b) Four FET APS with in-pixel current reference.

The most common way to operate the APS is in the linear mode in which the circuit presents narrow dynamic range, commonly between 40 and 60 dB. The basic way to achieve a wide dynamic range with the three-FET APS is operating it in the logarithmic mode, in which the circuit presents dynamic range higher than 100 dB [3]–[7]. This is done using the pixel in Fig. 1(a) with the reset-drain (RDR) terminal connected to V_{DD}. The same result is achieved with the pixel in Fig. 1(b) with the CAL terminal connected to GND, where M4 is usually employed as a current source for calibration purposes. The pixel in Fig. 1(b) is an all nMOS version of the pixel architecture proposed in [6]. Similar logarithmic behavior can also be achieved using a pinned photodiode [8], [9]. The most significant limitations of the APS operating in the logarithmic mode include image distortions caused by fixed-pattern noise (FPN), image lag, and low sensitivity toward low illumination [1].

FPNs are the nonidealities introduced during the fabrication process that cause pixel-to-pixel output variation under uniform illumination. It is composed of two components: 1) offset FPN that is independent of the light signal on the pixel and 2) gain FPN that is dependent on the light signal [2].

In the linear mode, offset FPN can be compensated by the well-established correlated double sampling (CDS) technique [2]. In the CDS operation, the calibration point is sampled from the light-dependent output produced at the beginning of the integration time [2]. Nevertheless, in the logarithmic mode or in any linear-logarithmic combination, the classical CDS does not work properly. This happens

because direct subtraction of two samples of the pixel output under the same light condition, without a current (or voltage) reference, as in the linear mode CDS operation, produces a null result. Therefore, alternative techniques must be employed to compensate the offset FPN [10].

Several techniques have been proposed to reduce FPN in the logarithmic mode, including storing the pixel offsets [4], [10], hot-electron injection calibration [11], single-point current calibration [3], [5], [6], double-point current calibration [7], [12], and triple-point software calibration [13].

The storage of the pixel offsets [10] can be implemented with the three-FET APS, at the cost of additional memory and liability to temperature variations. The other techniques, except software calibration, require more complex pixel circuitry, which therefore reduces the fill factor of the APS cell. The software calibration approach introduces additional costs in comparison with self-calibration approaches.

The double-point current calibration presented in [7] compensates for both offset and gain FPN. Such calibration can be performed either by reference images or by current reference. Current (or voltage) references are preferable, because they enable self-calibration. However, this approach introduces more sources of column FPN that might be compensated separately [7].

Further complexity of the double-point calibration is that the algorithm to execute such calibration is not a simple signal subtraction as in the CDS operation [7]. Therefore, it is not simple to perform such calibration at circuit level, and digital domain calibration may be a more convenient choice [12]. Moreover, the five-FET APS needed to apply such a technique [7] presents reduced fill factor in relation to the basic three-FET APS. Employing more complex pixel structure, such as digital pixel sensor [13] with in-pixel ADC, it is possible to mitigate the column FPN introduced by such a technique. However, at the penalty of a very low fill factor of $\sim$2.3% [13].

The single-point current calibration does not achieve the same attenuation level of the double-point current calibration [12]. However, it can be performed at the rate of a regular CDS operation with the same column CDS circuit employed in the linear mode [3].

Either single- or double-point calibration requires a current source coupled to the pixel in order to perform calibration, and such an approach increases pixel complexity [3], [5]–[7], [12]. Using the column current source adds column FPN, which produces vertical streaks on the image [7], [12]. Using an in-pixel current reference as in [3] and [6] adds only a single transistor to the pixel and produces random additional FPN rather than additional column FPN. An example of the in-pixel current reference for FPN calibration is the transistor M4 in Fig. 1(b).

In this paper, we propose a new single-point calibration method that can be applied directly to the basic three-FET APS. The proposed technique requires only the drain terminal of the reset transistor, RDR in Fig. 1(a), to be available to be set at any voltage level. Details of this new approach will be discussed in Section II.

This paper is organized as follows. The description of the proposed technique will be given in Section II. Experimental results asserting the solution and discussion of the results are given in Section III. Finally, the conclusion is drawn in Section IV.

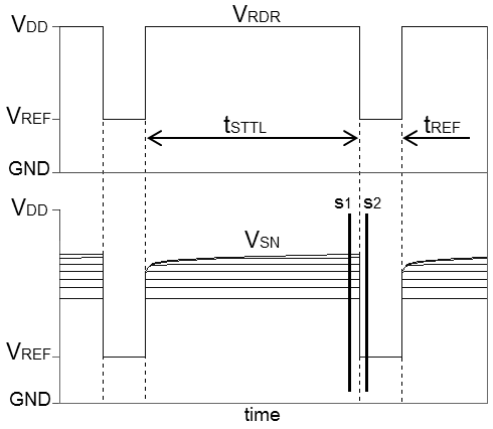

Fig. 2. RDR control signal necessary to execute the proposed FPN calibration and the logarithmic SN waveform with the indication of the two sampling times s1 and s2.

II. Proposed FPN Calibration Technique

Differently from the regular logarithmic three-FET APS where the RDR terminal in Fig. 1(a) is permanently connected to V_{DD}, in this case, this terminal is used to perform the proposed FPN calibration. Instead of using an in-pixel current reference, the proposed technique applies an external voltage reference to the sense node (SN) through the RDR terminal.

The control signal scheme presented in Fig. 2 is applied to achieve the logarithmic response with reduced FPN. In this scheme, the logarithmic response at the SN V_{SN} is produced when the RDR terminal is set to V_{DD} during the setting time t_{STTL}. The logarithmic output is then sampled at the end of t_{STTL} at s1, as shown in Fig. 2. The voltage reference V_{REF} for the FPN calibration is applied to the RDR terminal during the reference time t_{REF} and sampled at the beginning of t_{REF}, at s2. The reference time t_{REF} can be as short as the time necessary for V_{SN} to reach the V_{REF} level and the second sample s2 to be performed.

The calibrated output is produced by subtracting the second sample s2 from the first sample s1. The first sample registers the signal with the light intensity information and the offset FPN of the pixel. The second sample registers the voltage reference V_{REF} and also great part of the offset FPN of the pixel. The subtraction of second sample from the first suppresses the portion of the offset FPN present in both the samples. This technique requires only that the low level of V_{RDR} to be lower than the lowest possible level of V_{SN} and no higher than $V_{DD}-V_{TH}$. This condition is necessary, because M1 must be in the strong inversion linear region during t_{REF}. The lowest level of V_{SN} is reached when the pixel is under the highest illumination condition.

Monte Carlo simulations for both the pixels in Fig. 1(a) and (b), designed in the AMS CMOS 0.35-μm technology, were performed both to evaluate the proposed technique and also to compare it with previous approaches. For each pixel, 256 runs were performed with mismatches of

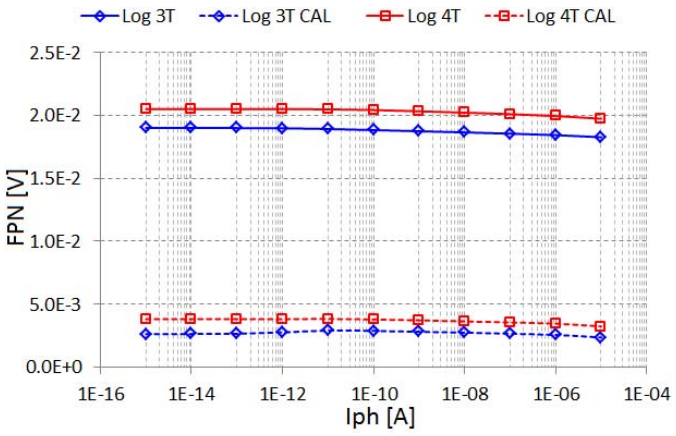

Fig. 3. Simulation results of the raw and the residual FPNs of the logarithmic three-FET APS Log 3T and Log 3T CAL, respectively, and the raw and the residual FPNs of the logarithmic four-FET APS Log 4T and Log 4T CAL, respectively.

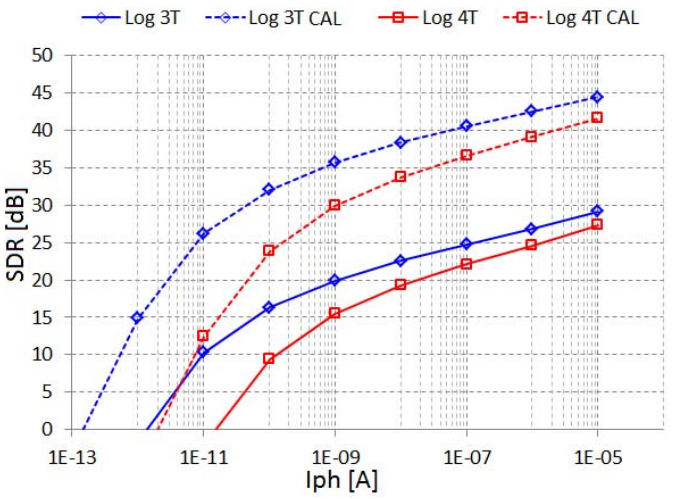

Fig. 4. SDR plots from the simulated results of the three- and four-FET APSs before and after FPN calibration, respectively.

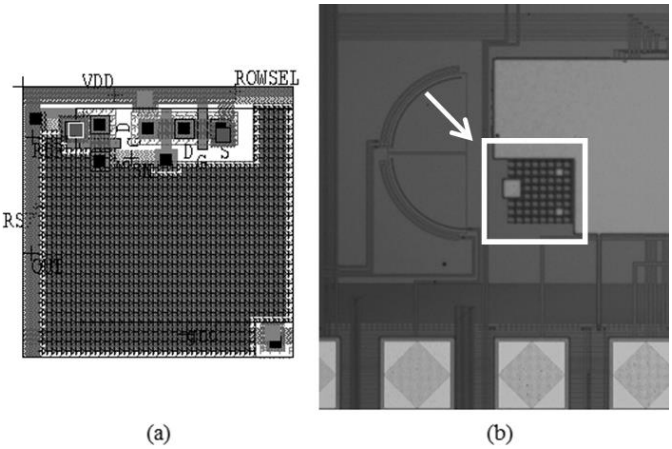

Fig. 5. (a) Layout of a single pixel of the array. (b) Micrograph of the fabricated pixel array.

all the transistors of each pixel and also with the transistor MC for each pixel. Due to the lack of an appropriate model, mismatches of the photodiodes were not performed for this analysis.

The setup of the control signal in Fig. 2 for the logarithmic operation is $V_{DD} = 3.3$ V, $V_{REF} = 2$ V, $t_{STTL} = 30$ ms, and $t_{REF} = 1$ ms. For the pixel in Fig. 1(b), the current source was biased, so that during t_{REF}, the current source would also produce a voltage of 2 V at the SN of the pixel as in the first case. The illumination level from the darkest to the brightest level is emulated by the photocurrents varying from 1 fA to 10 μA.

The raw FPN, before calibration, and the residual FPN, after calibration, for both the pixels are shown in Fig. 3. The plots Log 3T and Log 3T CAL stands for the raw and the residual FPNs of the three-FET APS, whereas the plots Log 4T and Log 4T CAL stand for the raw and the residual FPNs of the four-FET APS.

These results show that the additional transistor M4 in the pixel in Fig. 1(b) contributes with the additional FPN in relation to that of the pixel in Fig. 1(a). In addition, though both the calibration techniques are effective in reducing the offset FPN, the results show that the proposed technique produces even better results.

The signal-to-noise ratio (SNR) is the standard way to evaluate the dynamic range of the image sensors [1], [2], [14]. However, when both noise and distortions are considered, it is more convenient to call it signal-to-noise and distortion ratio (SNDR), as discussed in [14]. For the case where only distortion results are considered as with the presented simulation results, it is more convenient to call it signal-to-distortion ratio (SDR). To evaluate the improvement in the dynamic range, the SDR plots before and after FPN calibration for both the pixels were plotted, as shown in Fig. 4.

In Fig. 4, the plots Log 3T and Log 3T CAL stand for the SDR plots of the three-FET APS before and after FPN calibration, respectively, whereas the plots Log 4T and Log 4T CAL stand for the SDR plots of the four-FET APS before and after FPN calibration, respectively. These results show that while the previous approach produces a dynamic range improvement of 17.50 dB toward low light, the proposed calibration produces a dynamic range improvement of 18.76 dB toward low light. It is also shown that even without calibration, the simple use of the three-FET APS presents a wider dynamic range toward low light than that presented by the four-FET APS version either before or after calibration.

The SDR curves in Fig. 4 also show that the FPN attenuation reduces the effects of the low sensitivity toward the low illumination of the logarithmic mode.

The experimental results for the proposed FPN calibration method will be presented and discussed in Section III.

III. Experimental Results and Discussion

Experimental results carried out on a small pixel array assert the efficacy of the proposed technique. The layout of a single pixel of the array is shown in Fig. 5(a). The array contains only eight rows per eight columns of the pixel shown in Fig. 1(a), and it was designed and fabricated in the AMS standard 4-metal 2-poly 0.35-μm CMOS technology.

TABLE I
MEASURED CHARACTERISTICS OF THE ARRAY

Experimental Control Signal Setup		
Supply Voltage "V_{DD}"	3.3 V	
Load Voltage "VL"	1.0 V	
Settling Time "t_{STTL}"	6 ms	
RDR low level "V_{REF}"	1.8 V	
Reference Time "t_{REF}"	160 µs	
Array Characteristics	**Before FPN Calibration**	**After FPN Calibration**
Signal Swing REG	240 mV	237 mV
Signal Swing R2C	238 mV	234 mV
Sensitivity (or Gain) REG	-47 mV/dec	-46 mV/dec
Sensitivity (or Gain) R2C	-47 mV/dec	-46 mV/dec
FPN in relation to the measured signal swing		
σ_{REG_MAX}	12.95 %	7.22 %
σ_{R2C_MAX}	25.00 %	9.31%
Dynamic Range		
REG	83.52 dB	90.46 dB
R2C	73.06 dB	87.04 dB
Temporal Noise	< 2.5mVrms	

The small pixel array, the micrograph of which is shown in Fig. 5(b), at the position pointed by the white arrow, was designed especially for FPN investigation purposes. The limited silicon area for this project restricted the dimension of the array.

Each pixel of the array is a three-FET APS similar to that of Fig. 1(a), with individual connection to the gate of M1. The pixel size is 10 μm × 10 μm with a fill factor of 56%. The photodiode is an n^+-diffusion/p-subdiode with a total area of 61 μm^2 and a perimeter of 38.5 μm. The pixel full-well capacity and conversion gain are 61.6 fF and 2.6 $\mu V/e^-$, respectively. The transistors M1, M2, and M3, as well as the column amplifier MC, have the same dimensions: 1) $W = 0.70$ μm and 2) $L = 0.35$ μm. The array has two columns with different column amplifier MC transistors, one with $W = 1$ μm and other with $W = 1.20$ μm, and this was done in order to investigate column FPN. In addition, the array has eight pixels with metal shielding for the investigation of the other behavior of the pixel to different light conditions.

The pixel array was tested under eight different uniform illumination conditions, including the dark condition. The light source was a 532-nm solid-state laser. The experiment was carried out at room temperature. The experimental control signal setup is presented in Table I, and it differs from the simulation setup mainly in the length of t_{STTL} and t_{REF}. Owing to the speed constraints of the ADC used in our data acquisition system, t_{REF} was limited to a minimum of ~160 μs. However, with the use of a faster ADC, t_{REF} can be much shorter. The captured frames presented and treated in this paper are all from static uniform illumination fields, and thus the array operating rate was not evaluated.

Some samples of the captured frames before and after FPN calibration are shown in Fig. 6. The irradiance at which each frame was captured is shown above each pair. The effect of the two different column amplifiers MC is noticeable in the frames before FPN calibration. The images are presented in 8-b grayscale with 256 different possible intensities, where 0 is full black and 255 is full white.

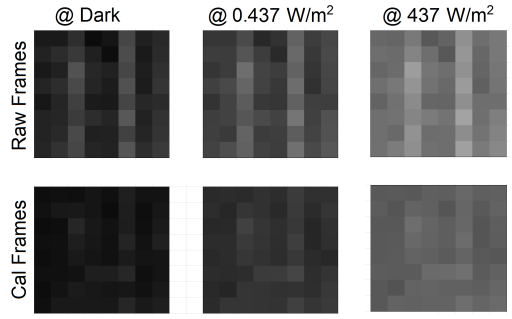

Fig. 6. Three captured frames before and after FPN calibration Raw Frames and Cal Frames, respectively.

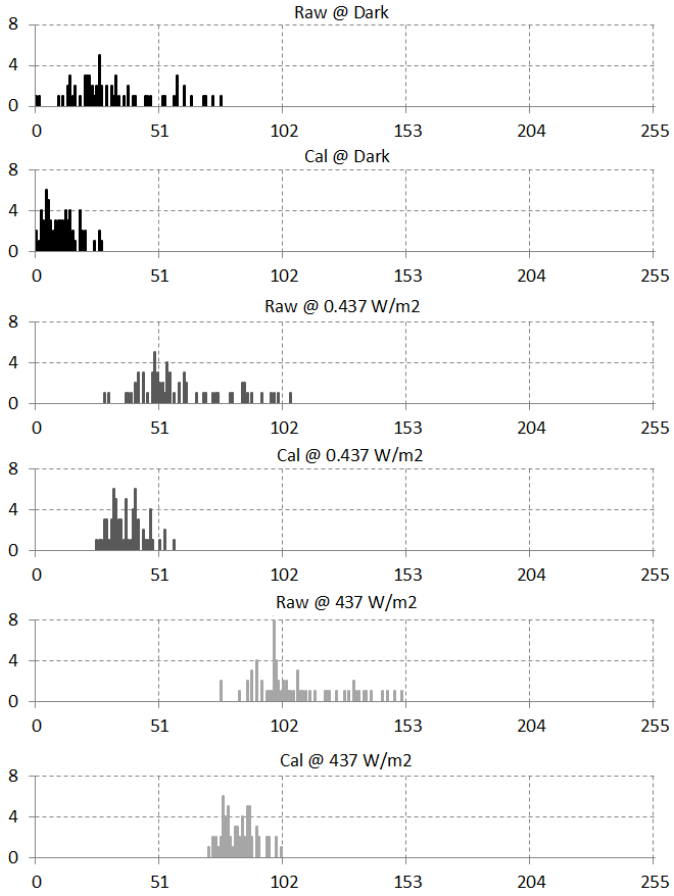

Fig. 7. Histograms, in number of pixels per grayscale intensity, of the three captured frames presented in Fig. 6, before and after FPN calibration labeled Raw and Cal, respectively.

The darkest and the brightest levels of the grayscale intensities in Fig. 6 stand for the measured voltage output limits before and after FPN calibration. Before FPN calibration, the darkest and the brightest levels stand for 1.864 V (0 in grayscale) and 1.391 V (151 in grayscale), respectively, whereas after FPN calibration, these levels stand for 0.865 V (0 in grayscale) and 0.549 V (101 in grayscale), respectively. At dark condition, the FPN was 56.65 mV_{rms} (237 mV_{p-p}) before calibration, and 21.16 mV_{rms} (86 mV_{p-p}) after calibration.

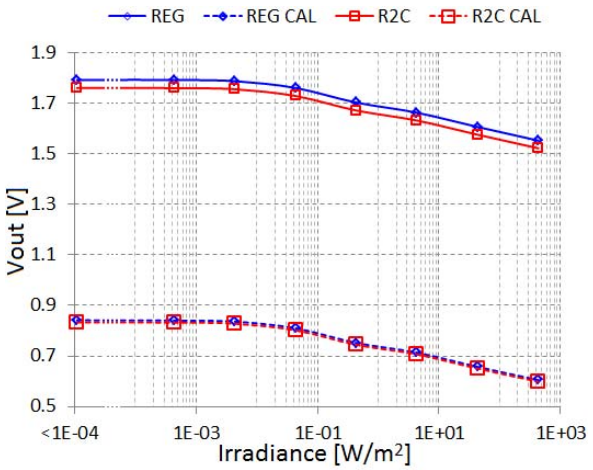

Fig. 8. Voltage output mean value versus irradiance for the regular pixels of the array before and after FPN calibration REG and REG CAL, respectively, and for the regular pixels plus the two different columns of the array before and after FPN calibration R2C and R2C CAL, respectively.

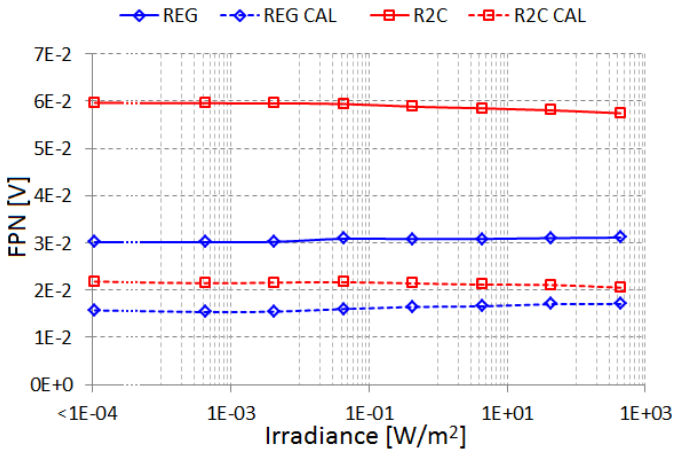

Fig. 9. FPN versus irradiance for the regular pixels of the array before and after calibration REG and REG CAL, respectively, and for the regular pixels plus the two different columns of the array before and after calibration R2C and R2C CAL, respectively.

The histograms showing the spatial variation of the array pixels around the mean value of the frames before and after FPN calibration are shown in Fig. 7. In this case, the mean value represents the illumination level in grayscale intensity, and the spatial variation represents the FPN of the array either before or after FPN calibration. The histograms of the images after FPN calibration show the attenuation of the spatial variation around the mean, thus asserting the effectiveness of the proposed technique.

In order to discuss the important details of the proposed technique, henceforth the measured results will be presented in two different groups. The first considers only the 40 regular pixels of the array that is those without metal shielding and with the same column amplifier dimensions. And the second group considers both the 40 regular pixels and also the two columns with different column amplifiers, the dimensions of which were described in Section II. The second group highlights the additional FPN introduced by the two different column amplifiers of the array and also the efficacy of the proposed technique in attenuating column FPN.

The plots of the mean output value versus irradiance before and after FPN calibration for the eight tested irradiance levels are shown in Fig. 8. The plots REG and REG CAL stand for the mean values of the regular pixels before and after calibration, respectively. And the plots R2C and R2C CAL stand for the mean values of the regular pixels plus the two different columns before and after calibration, respectively.

In Fig. 8, the basic difference between the plots before and after FPN calibration is an offset due to the reference voltage necessary to apply the proposed technique. The measured output signal swing, for both the cases, before and after FPN compensation is shown in Table I.

The plots of FPN versus irradiance, for both the cases, before and after compensation are shown in Fig. 9. The raw and the residual FPNs for the regular pixels of the array are presented by the plots REG and REG CAL, respectively. The plots R2C and R2C CAL stand for the raw and the residual FPNs for the regular pixels of the array plus the two different columns.

These results show that the proposed technique is able to reduce the raw FPN in the logarithmic mode within the whole tested illumination range. They also show that it is very effective in reducing column FPN, and this feature is more evident when the additional column FPN is considered.

The simulated FPN happened to be much lower than the experimental FPN, because in the simulations, only mismatches of the pixel transistors and the column amplifiers were considered. Owing to the lack of an appropriate simulation model, mismatches of the photodiodes were not performed in the Monte Carlo simulations; also, sources of temporal noise were not considered in the simulations, whereas in the experimental results, all the sources of spatial distortions and temporal noise are intrinsically present.

The SNR was plotted using the model for logarithmic compressed response photodetectors, presented and discussed in [1]. As FPN is rather a fixed spatial distortion associated to the pixel array than a dynamic quantity fluctuating over time, when both temporal noise and FPN are considered to calculate this ratio, it is more adequate to call it SNDR [14]. The measured temporal noise of the experimental setup is <2.5 mV_{rms}.

In Fig. 10, the SNDR plots before and after FPN calibration, for both cases, are presented. For the regular pixels of the array, the SNDRs before and after FPN calibration are presented by the plots REG and REG CAL, respectively. The plots R2C and R2C CAL stand for the SNDR of the regular pixels of the array plus the two different columns before and after FPN calibration. For both the cases, these plots show that the proposed technique causes an improvement in the SNDR of the array within the whole illumination range.

The SNDR plots in Fig. 10 show that the measured dynamic range for the imager is 83.52 and 90.46 dB for REG and REG CAL, respectively, whereas for R2C and R2C CAL, it is 73.06 and 87.04 dB, respectively. These results show that toward low light illumination, the dynamic range is limited by spatial distortions and temporal noise, and also that the FPN attenuation produced by the proposed technique

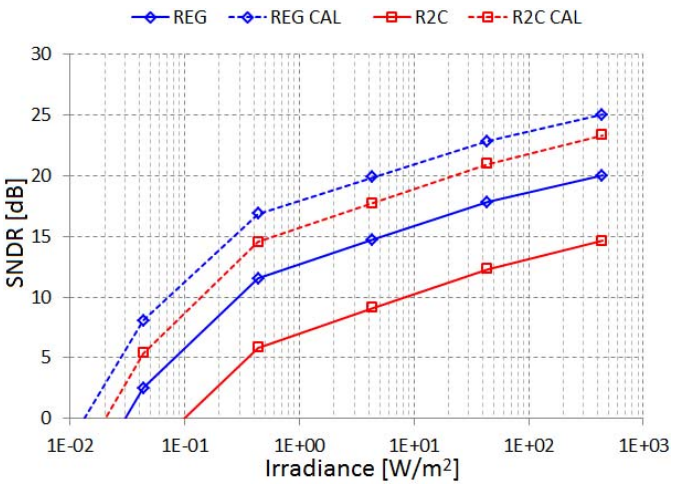

Fig. 10. SNDR plots for the regular pixels of the array before and after calibration REG and REG CAL, respectively, and for the regular pixels plus the two different columns of the array before and after calibration R2C and R2C CAL, respectively.

reduces spatial distortions, and thus the array dynamic range is improved toward low illumination. On the other hand, in the logarithmic mode, it is very hard to determine the highest possible illumination level at which the array can operate, which is limited by the increase of noise level at high illumination that does not allow a distinction of signals related to close illumination levels. However, this limit was not determined in this paper, and therefore, the measured dynamic range is not the highest possible dynamic range the array can yield.

A summary of the main measured characteristics of the array for both the cases considered in this section is presented in Table I, where the label REG stands for the regular pixels of the array and the label R2C stands for the regular pixels plus the two columns with the additional column FPN of the array.

The dynamic ranges before and after FPN calibration when only the regular pixels of the array are considered are 83.52 and 90.46 dB, respectively. In this case, the improvement caused by the proposed technique is of 6.94 dB toward low light illumination. When the additional column FPN is considered, the dynamic ranges before and after FPN calibration are 73.06 and 87.04 dB, respectively. The improvement caused by the proposed technique in this case is of 13.98 dB toward low light illumination. The low pixel density of the array prevented us from showing the produced improvement by means of a high resolution image.

IV. Conclusion

In this paper, it was presented a simple way to attenuate FPN in the three-FET APS operating in the wide-dynamic-range logarithmic mode. The employment of the proposed signal control scheme herein presented only requires the drain terminal of the reset transistor to be available. This is just a minor modification in relation to the conventional three-FET APS architecture. Thus, further complexities to the pixel circuitry are avoided, and its fill factor can be kept as high as that of the basic three-FET APS, except for the slight reduction required to add the separate interconnection line for the aforementioned drain terminal. Monte Carlo simulations confirmed the capability of the proposed technique to attenuate FPN better than an alternative technique presented in the literature. Experimental results confirmed the ability of the proposed technique in reducing FPN also when an additional column FPN is deliberately imposed to the array. The experimental results also showed that the proposed technique causes an improvement in the SNDR of the array. The results presented in this paper show that simple modifications applied to well-established wide-dynamic-range pixel topologies can lead to improved CMOS image sensors at no additional fabrication cost.

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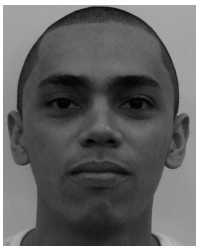

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