FPN Attenuation by Reset-Drain Actuation in the Linear-Logarithmic Active Pixel Sensor

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***Abstract*—The three FET CMOS active pixel sensors (APS) operating in the linear-logarithmic mode is one of the most efficient wide-dynamic-range imagers. However, the quality of the image generated at the focal-plane array is often compromised by fixed-pattern noise (FPN) between pixels. The classical correlated double sampling (CDS) technique is used to reduce FPN in imagers operating in the linear mode. But in the complementary linear-logarithmic mode CDS does not work properly and alternative techniques must be applied to reduce FPN. The ordinary alternative techniques increase either the complexity of the pixel or its external circuitry. In order to avoid these problems a new technique was devised to reduce FPN that can be applied to the basic three FET APS architecture. With the purpose to assert the efficacy of the proposed technique a small array was fabricated in a standard 0.35 μm CMOS technology. Experimental results show that the proposed technique is able to reduce FPN quite steadily within the whole illumination range used to test the array. And therefore, the signal-to-noise-and-distortion ratio (SNDR) of the array is also improved within the whole range of operation.**

***Index Terms*—Active pixel sensor, CMOS image sensor, correlated double sampling, double sampling readout subtraction, fixed-pattern noise, wide-dynamic range.**

I. Introduction

OWING TO functionality and simplicity, active pixel sensor (APS) architectures have become the preferred choice in the design of CMOS image sensors. Nowadays APS circuits are most known by their application in mega-pixel imagers [1]–[3]. However, they have a broader range of applications that may not require arrays that dense, such as in industrial monitoring, line scanners, medical endoscopy, lab-on-chip, etc. [2]–[5]. The APS can be basically operated in two different modes: linear and logarithmic.

In the linear mode the pixel presents good sensitivity towards low illumination [1], [2], but a rather short dynamic range towards high illumination [2]. On the other hand in the logarithmic mode it presents high dynamic range toward high illumination and low sensitivity towards low illumination [1].

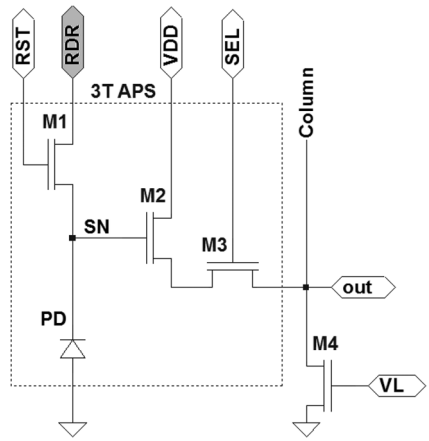

Fig. 1. Three FET CMOS APS with free reset-drain terminal (RDR) on which the proposed DSRS technique is applied.

Alternatively, the pixel can be operated in different linear-logarithmic combinations [1], [6]–[9]. In these combinations the APS makes use of the high sensitivity of the linear mode, at low illumination, and the high-dynamic range of the logarithmic mode, towards high illumination.

Among all the alternative linear-logarithmic combinations, the one with the simplest implementation and fastest operation is that proposed in [7]. This technique can be applied either to the basic three FET APS or to the four FET APS presented in [7]. The use of the three FET APS is preferable because the fill factor of the pixel can be kept higher.

In a three FET APS, as the circuit presented in Fig. 1, the technique works by connecting RDR permanently to the supply voltage $\mathrm{V_{DD}}$, and using a hard-reset approach switches the RST terminal between a maximum and a minimum value. In the hard-reset scheme, applied to suppress reset-induced image lag [10], the maximum value of RST must be higher than $\mathrm{V_{DD}}$ plus the threshold voltage V_{TH} of M1, $(\mathrm{V_{DD}} + \mathrm{V_{TH}})$. This is done so that the sense node (SN) voltage reaches the reset level, $\mathrm{V_{res}}$ in [7], which is the supply voltage level. The key to achieve the complementary linear-logarithmic operation is the low level of RST, which can be set to a predetermined value in the range between $(\mathrm{GND} + \mathrm{V_{TH}})$ and the reset level $\mathrm{V_{DD}}$.

On the other hand, the hard-reset operation can be harmful to the circuit because it overstresses the gate-oxide of MOS transistor M1, reducing its life time as discussed in [11], [12]. This effect reduces, therefore, the lifetime of the APS circuit and of the imager array as a whole.

The four FET APS, reported in [7], was proposed in order to avoid the hard-reset operation to suppress reset-induced image

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lag. However, due to the need of a fourth transistor, it presents a lower fill factor than the basic three FET APS architecture. Nevertheless, it is possible to implement such linear-logarithmic operation in the three FET APS circuit, without the need of hard-reset operation to suppress image lag, by the slight adaptation proposed by the authors in [13], [14].

However, no matter in which mode the APS circuit is operated, Fixed-Pattern Noise (FPN) is a relevant problem to be dealt with [1], [2], [8]–[10], [13]–[21]. FPN are non-idealities introduced during the fabrication process that cause pixel-to-pixel output variation under uniform illumination.

In the linear mode, the FPN can be calibrated using the well-established CDS technique [1], [2]. However, it is only truly correlated when applied to the four FET APS with either a pinned diode or photogate as discussed in [2]. The FPN calibration in the logarithmic mode can be done with a single reference point to compensate for offset FPN [9], [13], and [14]. Whereas to compensate for offset and gain FPN it requires a minimum of two calibration points, besides the sampled signal [9], [15] and [16].

The linear-logarithmic operation presented in [9] produces independently the linear and the logarithmic responses in two different slots of time. Therefore it can also compensate for FPN independently in both operation regions. In this architecture when using single parameter calibration, it requires a sequence of four readout operations, besides waiting for the logarithmic settling time between the second and the third readout operation [9]. This calibration technique is consequently slower than the basic CDS technique, which requires only two readout operations.

The solution presented in [17] uses a linear-logarithmic combination similar to that presented in [7]. This technique also uses CDS to calibrate FPN for the linear region, and the two-parameter calibration proposed in [16] for the logarithmic region. Besides, it still requires an additional method to compensate for FPN in the transition region between linear and logarithmic regions.

With the technique proposed in [17], before choosing which method to apply to compensate for FPN, it is necessary to identify in which region each pixel of the array is operating in each frame, whether in the linear, or in the logarithmic, or in the transition region. This process demands some kind of verification, i.e., computational, that requires extra time besides the time necessary to sample the signal and the reference points. Thus, this technique is also slower than the basic CDS technique.

The calibration technique presented in [8] uses charge injection into the photodiode to perform the FPN compensation. This technique reduces FPN in the logarithmic region, but increases it in the linear region. Besides, it also requires four readout operations to execute such calibration.

In this work the authors present a simple technique to reduce FPN in the three FET APS of Fig. 1, operating in the linear-logarithmic mode, as initially proposed by them in [13] and [14]. This technique uses a double-sampling readout subtraction (DSRS) approach. It can be implemented with a column readout circuits similar to that used by the classical CDS technique, as shown in [13].

One of the advantages of the technique presented in [13] and [14] is that it uses only one reference point to calibrate FPN in either region of operation, however, not fully achieving the optimized FPN calibration level for each particular region, as [9] and [17]. Notwithstanding, the technique proposed herein is able to reduce FPN in both regions of operation, as well as in the transition region, at the rate of a regular CDS operation in the linear APS.

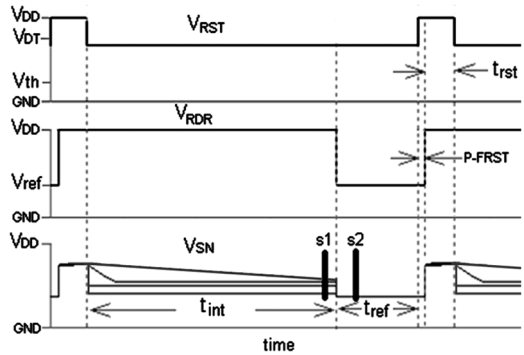

Fig. 2. The RST and RDR control signals necessary to execute the proposed DSRS technique, and the sense-node waveform under four different light intensities with the indication of the two sampling times s1 and s2.

In this work we present characterization results of the array designed to evaluate the technique introduced in [13] and [14], proving its effectiveness. As the proposed technique can be applied directly to the three FET APS, the fill factor of the pixel can be kept as large as possible.

The paper is organized as follows: the implementation of the proposed technique will be described in Section II. The design and implementation of the array will be presented in Section III. Experimental results asserting the solution are shown in Section IV. Discussions of the results are given in Section V. Finally, conclusions drawn from this work are given in Section VI.

II. Fixed-Pattern Noise Compensation

The usual design of the three FET APS is implemented with the drain terminal of the reset transistor, RDR in Fig. 1, fixed at the voltage supply, $\mathrm{V_{DD}}$, level. In order to apply the proposed technique and compensate for FPN in the linear-logarithmic mode, the RDR terminal of the pixel must be free to be connected to any voltage level. This particular connection is used to establish a voltage reference at the sense-node of the pixel, SN in Fig. 1, which will be used for further calibration.

In an imager array all the pixels in a column share the same output column bus. Therefore, the selection of a specific pixel in a column is done by switching its SEL terminal, in Fig. 1, from GND to $\mathrm{V_{DD}}$ level, while the SEL terminal of all the other pixels are kept at GND level.

The complementary linear-logarithmic operation experimentally demonstrated in this work is the one conceptually proposed and simulated in [13], [14]. It differs from the method presented in [7] because the reset-induced image lag is suppressed through the pseudo-flash reset, as described in [13], and therefore the hard-reset scheme is not necessary anymore. This approach is more interesting because the maximum voltage level at the RST terminal is $\mathrm{V_{DD}}$, as shown by the curve $\mathrm{V_{RST}}$ in Fig. 2, and therefore gate-oxide voltage overstress is eliminated.

The linear-logarithmic regimen is produced by choosing a convenient low level for the reset signal of the pixel between $\mathrm{V_{DT}} = (\mathrm{V_{DD}} - \mathrm{V_{TH}})$ and $(\mathrm{GND} + \mathrm{V_{TH}})$ levels, as shown by $\mathrm{V_{RST}}$ in Fig. 2. Note that if the low level of RST is GND, then the circuit operates in pure linear mode. The voltage reference

to perform FPN compensation is produced by choosing a convenient low level for the V_{RDR} control signal as shown by V_{ref} in Fig. 2. The light intensity information is translated as a voltage level, present at the sense-node V_{SN} during the integration time, t_{int}. And the reference voltage, V_{ref}, for FPN compensation will be present at the sense-node during reference time, t_{ref}.

The output of the pixel with reduced FPN is produced by double sampling the output at s1 and s2 in Fig. 2, and then subtracting the second sample from the first sample. The first sample is taken at the end of t_{int} and registers the signal with light intensity information and the offset FPN of the pixel. The second sample is taken at the beginning of t_{ref} and registers the voltage reference, V_{ref}, and also great part of the offset FPN of the pixel. The subtraction of second sample from the first suppresses the portion of offset FPN present in both samples.

The reference time t_{ref} can be as short as the time necessary for V_{SN} to reach V_{REF} level and the second sample s2 to be performed.

The waveform V_{SN} shown in Fig. 2 represents the sense-node signal under four different levels of illumination. When exposed to the three higher levels of illumination V_{SN} reaches the logarithmic region in the beginning of the integration time, t_{int}, and for the lower level, the respective signal remains fairly linear until the end of the integration time.

It is worth noting that this technique requires that the low level of V_{RDR} be lower than the lowest possible level of V_{SN} [13], [14]. The lowest level of V_{SN} is reached when the pixel is under the highest illumination condition, for a chosen integration time.

The period of time in Fig. 2 called P-FRST stands for pseudo-flash reset, meant to reduce reset induced image lag in the imager [13]. This is achieved by resetting the low level of the sense node SN to a predefined low level right before the pixel reset, during the reference time t_{rst}, as explained in [13].

Though the pixel has been designed to evaluate the proposed technique working in the complementary linear-logarithmic mode, it can also be used as a regular linear pixel, where the conventional CDS technique can be applied to reduce FPN. The operation in both modes with their respective technique to compensate for FPN will be shown and discussed by means of experimental results.

III. Array Design and Implementation

To verify the performance of the proposed technique, a small array with eight rows and eight columns of the pixel shown in Fig. 1 was designed and fabricated in the AMS standard 4-metal 2-poly 0.35 μm CMOS technology. Due to silicon area limitation for this project, a larger array could not be implemented.

The size of each pixel of the array is 10 μm × 10 μm. The fill factor of each pixel is 56%. The photodiode is an n^+-diffusion/p-sub diode with total area of 61 μm^2 and perimeter of 38.5 μm. The transistors M1, M2 and M3, as well as the column amplifier M4, have the same dimensions: $W = 0.70$ μm and $L = 0.35$ μm. All pixels in a column share the same column amplifier transistor M4, and the same RST and RDR connections. And in a row, all pixels share the same SEL connection.

As the introduction of non-idealities during fabrication is a random process it is not possible to predict either where it will take place in the array or its magnitude. Therefore, to guarantee that some specific kind of non-idealities would be present in such small array, as column FPN, they were intentionally implemented in the design. This was done to enable the evaluation of the proposed technique, even if process related FPN happened to be absent.

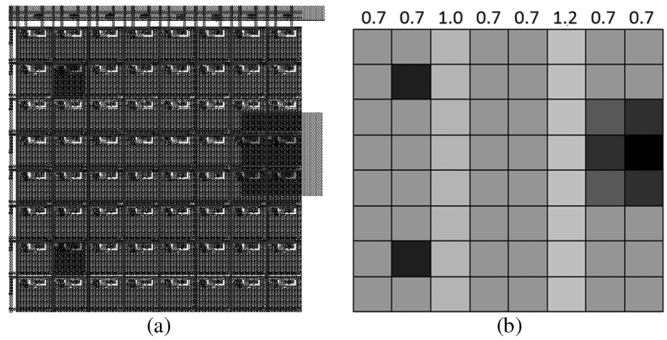

Fig. 3. (a) Designed layout of the pixel array; and (b) the expected image captured under a uniform illumination field with the indication of the width of the column amplifier, in micrometer, of each pixel column.

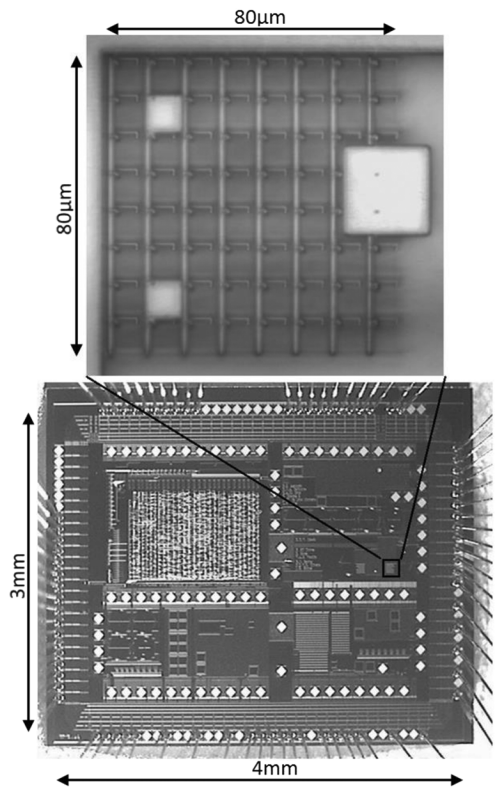

Fig. 4. Fabricated chip with the designed 8 × 8 imager array with their respective dimensions.

The introduced non-idealities were: 1) two column amplifiers, M4, with altered widths and 2) eight pixels with varying ratios of metal shielding.

The designed layout of the pixel array is presented in Fig. 3(a). An example of the expected ideal image resulting from a uniform illumination field is shown in Fig. 3(b). The width of each column amplifier, in micrometer, is shown above each column of the hypothetical image.

A microphotography of the fabricated chip with the designed array, described above, is presented in Fig. 4. The zoomed area of the chip shows the specific array which characterization results will be presented in the next section.

TABLE I
ARRAY DESIGN CHARACTERISTICS AND SIGNAL CONTROL SETUP

Technology	0.35µm 2P4M CMOS	
Pixel Size	10µm x 10µm	
Fill Factor	56%	
Fill Factor of the shielded pixels in their respective (m, n) position	(2, 2) = (7, 2) = 2.3%; (3, 7) = 22.6%; (3, 8) = 14.4%; (4, 7) = 17.3%; (4, 8) = 00.0%; (5, 7) = 27.0%; (5, 8) = 20.7%	
Array Size	8 x 8	
Signal Control Setup	**Linear**	**Linear-Logarithmic**
Supply Voltage "V_{DD}"	3.3V	3.3V
Load Voltage "VL"	1.0V	1.0V
Integration Time "t_{int}"	6ms	6ms
RST low level	GND	2.2V
RDR low level "V_{ref}"	GND	1.4V
Reset Time "t_{rst}"	2ms	1ms
Reference Time "t_{ref}"	0µs	160µs
Pseudo-Flash Reset "P-FRST"	0µs	1ms

The ideal fill factor of the other eight different pixels, designed with metal shielding, varies according the percentage of the shielded area, and their values are indicated in Table I. Each pixel in the array is identified by its (m, n) position, being the position (1, 1) that of the pixel in the upper left corner.

IV. EXPERIMENTAL RESULTS

A. Experimental Setup

The pixel array was tested for the flat-field condition with different intensities, according to the dynamic range of detection in each mode of operation: linear or linear-logarithmic. All the uniform illuminated fields had the same 5.4 mm diameter circular profile. The light source was a 532 nm solid-state laser. An optical setup scheme with a divergent lens and diaphragms was used to produce the flat-field profile from the laser Gaussian profile. The experiment was carried out at 25 °C.

The area of the illuminated circle is more than 12 000 times bigger than that of the imager array. To verify the smoothness of the flat-field, a small area was mapped in the center of the circle, around the region where the array was positioned. The mapped area is just four times bigger than the imager array.

The mapping of the flat field was obtained by registering the voltage output of a single unaltered pixel of the array, pixel (1, 1), scanning the light field in 10-μm steps, as shown in Fig. 5(a). The irradiance for the mapping was 4.37 $\mathrm{W/m^2}$.

When the pixel array is positioned at the center of the flat field, the array response takes the form shown in Fig. 5(b), revealing the FPN of the array for this light intensity. The region where the array was placed is shown at the bottom of Fig. 5(b).

To evaluate the proposed technique and also to compare it with the well-established CDS technique to reduce FPN, the implemented APS array was tested both in linear and in linear-logarithmic modes. In the linear mode the CDS was applied to reduce FPN along the whole range of illumination. And in the linear-logarithmic mode the proposed DSRS technique was applied along the whole range of illumination.

In the linear mode the array was tested under eight different flat-field irradiances along 60 dB. For the complementary linear-logarithmic mode the array was tested under twelve different irradiances along 129.5 dB.

For this specific experiment, the results of which are shown and discussed next, all the images captured by the array are from

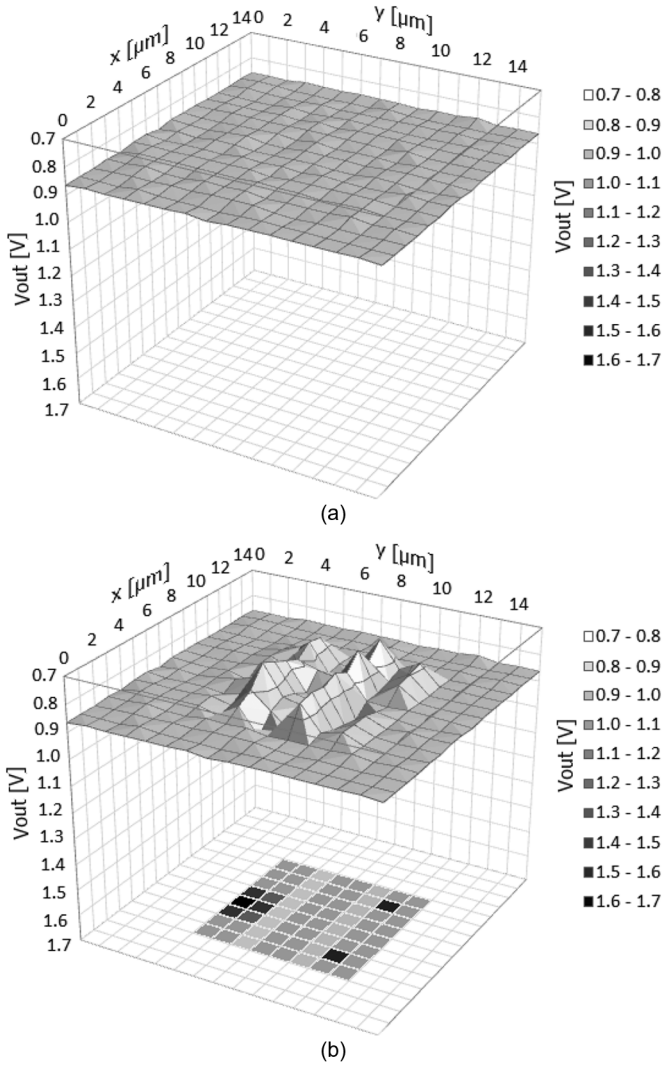

Fig. 5. (a) Profile of the uniform light field; and (b) the pixel-array response to that field with the indication of the position of each pixel of the array.

static uniform illumination fields. Therefore, the frame rate of the array will not be evaluated in this work.

The setup of the signal control, presented in Fig. 2, for the pixel array operating in both linear and linear-logarithmic modes are presented in Table I.

For the array operating in the linear mode the first sample, s1, is taken 10 μs after the beginning of $\mathrm{t_{int}}$ and the second sample, s2, 5 ms after the beginning of $\mathrm{t_{int}}$. This process is repeated for the 64 pixels of the array for each complete frame. It is important to point out that the reset time, $\mathrm{t_{rst}}$, can be much shorter for real-time imaging.

In the linear-logarithmic mode the first sample, s1, is taken 5 ms after the beginning of $\mathrm{t_{int}}$ and the second sample, s2, 20 μs after the beginning of $\mathrm{t_{ref}}$. Speed constraints of the ADC, used in our data acquisition system, limits the reference time $\mathrm{t_{ref}}$ for this experiment to a minimum of about 160 μs. However, with the use of a faster ADC, the reference time $\mathrm{t_{ref}}$ can be much shorter. The pseudo-flash reset, P-FRST, and reset time, $\mathrm{t_{rst}}$, can also be much shorter for real-time imaging.

As we are interested in evaluating the reduction of spatial fixed-pattern noise, spurious fluctuations of other sorts needed to be minimized. Thus, in order to reduce the effect of temporal fluctuations from either the light source or from the control and

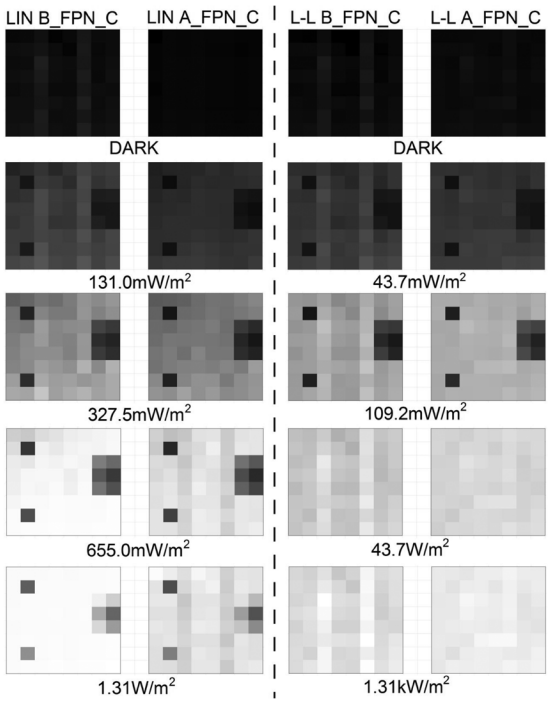

Fig. 6. Captured frames before and after FPN compensation for the linear mode (pairs of left images) and linear-logarithmic mode (pairs of right images).

supply signals, 20 frames were captured for each light condition and the average of the 20 frames was taken to produce the base image for FPN analysis.

B. *Samples of Averaged Frames*

Some of the averaged frames for FPN analysis, for both linear and linear-logarithmic modes, are shown in Fig. 6. The column identified by "LIN B_FPN_C" represents the averaged frame captures in the linear mode before FPN compensation by CDS. The averaged frame captures in the linear mode after FPN compensation by CDS are shown in the column identified as "LIN A_FPN_C." Whereas the averaged frame captures, before and after FPN compensation by DSRS, in the linear-logarithmic mode are shown in the columns identified as "L-L B_FPN_C" and "L-L A_FPN_C" respectively.

The darker and brighter levels of the grayscale in Fig. 6 stand for the measured voltage output limits in each mode of operation before and after FPN compensation, as shown by the output curves presented in Fig. 7. In the linear mode before CDS compensation the darker and brighter levels stand for 1.684 V and 0.239 V respectively, whereas after CDS compensation these levels stand for 0.093 V and 1.446 V respectively. In the linear-logarithmic mode before DSRS compensation the darker and brighter levels stand for 1.655 V and 0.718 V respectively, whereas after DSRS compensation these levels stand for 1.042 V and 0.112 V respectively. All other intermediate levels are grayscale variations between the limits of each mode, before and after FPN compensation.

The light intensity level shown for each pair, before and after FPN compensation, represents the irradiance condition under which the image was captured. The first row represents the darker condition of this experiment for both modes of operation.

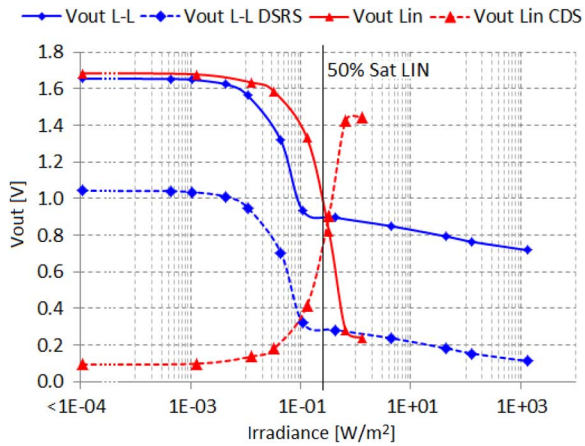

Fig. 7. Voltage output mean value versus irradiance for the linear-logarithmic and pure linear modes before and after FPN compensation "Vout L-L," "Vout L-L DSRS," "Vout Lin," and "Vout Lin CDS" respectively.

The second, third and fourth pairs of frames for linear mode, before and after FPN compensation, are in the range of the light intensity for which the pixel array has the highest light sensitivity, as will be discussed next. The last pair of frames for the linear mode is that for which the regular pixels in the array reach the saturation level. It is important noticing that as the linear mode approaches the saturation level, the CDS technique adds FPN instead of reducing it.

For the linear-logarithmic mode, the second and third pairs of frames lie in the range of highest sensitivity of this mode, which is inside the linear region. The fourth and fifth pairs of frames lie within the logarithmic region. The fifth pair of frames was taken under the highest irradiance on which the array was tested. Even for the highest tested irradiance the linear-logarithmic mode did not reach saturation level, differently from the pure linear mode.

It was observed that from the irradiance of 437 $\mathrm{mW/m^2}$ and beyond, the designed partial optical shielding for those seven pixels with metal shield, in the positions (2, 2), (7, 2), (3, 7), (3, 8), (4, 7), (5, 7), and (5, 8), is rather ineffective. This happens especially due to the large number of photons reaching the photodiode through the small but finite exposed area, and or due to the large number of charge carries diffused through the bulk, coming from the surrounding pixels or through the edge of the array, and reaching these pixels and also the pixel (4, 8). More on this effect is under investigation. Hence for these levels of irradiance the induced FPN, introduced via metal shielding, is not efficient.

The low efficacy of inducing FPN through metal shielding, for high irradiances, can be observed in the two last pairs of frames, before and after FPN compensation, of the linear-logarithm mode in Fig. 6. Nevertheless, other sources of FPN as well as the induced column FPN are still visible, and the proposed technique is shown to be efficient in reducing them.

Comparing the results after FPN compensation, by CDS, in the pure linear mode, with those by DSRS, in the complementary linear-logarithmic mode, it is possible to verify that as the light intensity increases the proposed technique produces better results. Aspects of this effect will be discussed in the next section.

TABLE II
MEASURED CHARACTERISTICS OF THE ARRAY

Array Characteristics	Before FPN Compensation	After FPN Compensation
Signal Swing $_{\text{LIN TOTAL}}$	1.445V	1.353V
Signal Swing $_{\text{LL MEASURED}}$	938mV	930mV
Log Sensitivity	-54.8mV/dec	-53.1mV/dec
FPN LIN in relation to the total signal swing		
σ_{offset}	2.13%	0.76%
$\sigma_{gain,PEAK}$	7.46%	6.80%
FPN LL in the linear region in relation to the measured signal swing		
σ_{offset}	3.28%	2.00%
$\sigma_{gain,PEAK}$	4.00%	3.56%
FPN LL in the log region in relation to the measured signal swing		
$\sigma_{TOTAL,\max} = \sqrt{\sigma_{offset}^2 + \sigma_{gain}^2}$	2.81%	1.59%
$\sigma_{TOTAL,\min} = \sqrt{\sigma_{offset}^2 + \sigma_{gain}^2}$	2.65%	1.34%
Dynamic Range		
Linear-Logarithmic	111.40dB	115.43dB
Linear	46.72dB	55.04dB
Temporal Noise	< 2.5mVrms	

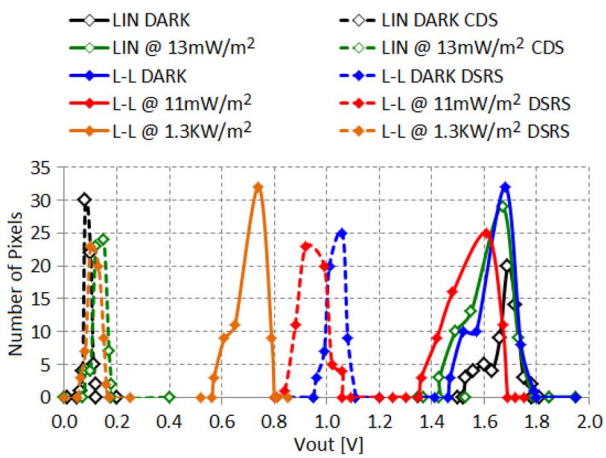

Fig. 8. Histogram showing the total spatial variation of the array, before and after FPN compensation, at dark condition and at some light conditions for the pure linear mode and for the linear-logarithmic mode, labels LIN and L-L, respectively.

C. Array Output Mean Value

The mean output value, for each irradiance, is usually the average of the output of all the pixels in the array. However, in this case only the pixels without induced FPN were taken into account. That is, all the pixels except those of the two different columns and those with metal shield.

The process is the same for both uncompensated and compensated frames. For each irradiance level x, the mean output value, μ_x, is calculated as shown in (1), where n_p is the number of pixels taken in account, which in this case is 40, since the other 24 pixels had a certain degree of distortion deliberately introduced.

When the array is operated in the linear-logarithmic mode, for the uncompensated frames, $V_{o,x}(m,n)$ in (1) stands for the samples of each pixel (m, n) of the array taken at s1 in Fig. 2. Whereas for the compensated frames $V_{o,x}(m,n)$ stands for the difference between the samples s1 and s2, (s1-s2), in Fig. 2.

In the linear mode, for the uncompensated frames, $V_{o,x}(m,n)$ stands for the samples of each pixel taken at the end of the integration time, t_{int}, and for the compensated frames $V_{o,x}(m,n)$ stands for the difference between the samples taken at the beginning of t_{int} from those taken at the end of t_{int}.

The sum of the voltage values of the 16 pixels on the two deviating columns and those additional 8 pixels with metal shield are indicated in (1) as Σ_{col} and Σ_{shld}, respectively, and defined in (2) and (3).

The curves of the mean output value versus irradiance, for both modes of operation, before and after FPN compensation are shown in Fig. 7. The mean values for twelve different irradiances in the linear-logarithmic mode, before and after FPN compensation, are shown by the curves identified as "Vout L-L" and "Vout L-L DSRS" respectively. The curves identified as "Vout Lin" and "Vout Lin CDS" in the same graph are the mean values for eight different irradiances for the linear mode, before and after FPN compensation respectively. The line labeled as "50% Sat LIN" indicates the irradiance for which the array operating in linear mode reaches 50% of the saturation level.

$$\mu_x = \frac{1}{n_p}\left[\left(\sum_{m=1}^{M}\sum_{n=1}^{N} V_{o,x}(m,n)\right) - \Sigma_{col} - \Sigma_{shld}\right] \quad (1)$$

$$\Sigma_{col} = \sum_{m=1}^{M} V_{o,x}(m,3) + \sum_{m=1}^{M} V_{o,x}(m,6) \quad (2)$$

$$\Sigma_{shld} = V_{o,x}(2,2)+V_{o,x}(7,2)+V_{o,x}(3,7)+V_{o,x}(3,8) + V_{o,x}(4,7)+V_{o,x}(4,8)+V_{o,x}(5,7)+V_{o,x}(5,8) \quad (3)$$

The output signal swing, for both modes of operation, before and after FPN compensation is shown in Table II. The sub-label "$_{\text{MEASURED}}$" was used for the signal swing of the linear-logarithmic mode because the maximum irradiance in the setup does not cause saturation, whereas the sub-label "$_{\text{TOTAL}}$" was used for the linear mode.

A histogram showing the total spatial variation of the 64 pixels of the array, before and after FPN compensation, for the dark condition and three other illumination conditions is shown in Fig. 8. The histogram curves labeled as LIN stand for those of the linear mode, whereas those labeled as L-L stand for the ones of the linear-logarithmic mode. The histogram is a graphical evaluation of how significant the FPN reduction is for a given technique. The thinner the curve, the more significant the FPN reduction is. It can be observed that in all cases the compensated curves present a reduction in the deviation in relation to the average signal.

The FPN results for each irradiance and mode of operation, before and after compensation, are given and discussed next.

V. DISCUSSION

A. FPN Attenuation for the Regular Pixels

The standard spatial deviation of the array determines its FPN. In this case, considering only the regular pixels of the array, its FPN is estimated as in (4). Where $(\sigma_x)^2$ is the spatial variance and σ_x is the standard spatial deviation. The variance is estimated using the number of pixels n_p minus one $(n_p - 1)$, in this case n_p is 40. The meaning of $V_{o,x}(m,n)$ for both operation modes are the same as those in (1). The components expressed by $\Sigma_{\Delta col}$ and $\Sigma_{\Delta shld}$, defined in (5) and (6), represent the effect of the two different columns and eight shielded pixels, respectively. In the general case, where no induced FPN is added, the variance is estimated without considering the

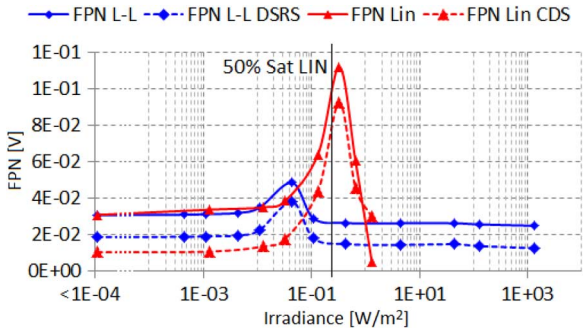

Fig. 9. FPN versus irradiance of the regular pixels of the array for the linear-logarithmic and pure linear modes before and after FPN compensation "FPN L-L," "FPN L-L DSRS," "FPN Lin," and "FPN Lin CDS" respectively.

components $\Sigma_{\Delta\mathrm{col}}$ and $\Sigma_{\Delta\mathrm{shld}}$ in (4). The array FPN must be recalculated for each different light condition.

The curves of FPN versus irradiance, for both modes of operation, before and after compensation are shown in Fig. 9. In the linear-logarithmic mode the FPN values for twelve different irradiances, before and after the proposed DSRS compensation, are shown by the curves identified as "FPN L-L" and "FPN L-L DSRS" respectively. The curves identified as "FPN Lin" and "FPN Lin CDS" are the FPN values for eight different irradiances for the linear mode before and after CDS compensation, respectively.

$$\sigma_x^2 = \frac{1}{n_{p-1}}\left[\left(\sum_{m=1}^{M}\sum_{n=1}^{N}\left(V_{o,x}(m,n)-\mu_x\right)^2\right) - \Sigma_{\Delta col} - \Sigma_{\Delta shld}\right] \quad (4)$$

$$\Sigma_{\Delta col} = \sum_{m=1}^{M}\left(V_{o,x}(m,3)-\mu_x\right)^2 + \sum_{m=1}^{M}\left(V_{o,x}(m,6)-\mu_x\right)^2 \quad (5)$$

$$\Sigma_{\Delta shld} = \left(V_{o,x}(2,2)-\mu_x\right)^2 + \left(V_{o,x}(7,2)-\mu_x\right)^2 + \left(V_{o,x}(3,7)-\mu_x\right)^2 + \left(V_{o,x}(3,8)-\mu_x\right)^2 + \left(V_{o,x}(4,7)-\mu_x\right)^2 + \left(V_{o,x}(4,8)-\mu_x\right)^2 + \left(V_{o,x}(5,7)-\mu_x\right)^2 + \left(V_{o,x}(5,8)-\mu_x\right)^2 \quad (6)$$

Due to PRNU, both modes of operation feature a peak of FPN in the range of high sensitivity of the pixel array. And though both techniques present some degree of FPN attenuation in this range, the peak remains after compensation. The compensation for PRNU demands more accurate calibration techniques as the one presented in [20] for the linear mode, and those proposed in [15] and [16] for the logarithmic mode.

These results show that, although in a non-optimized way, the proposed technique is able to reduce the raw FPN within the whole range of operation of this linear-logarithmic combination. They show also that CDS is more effective for the linear mode than the proposed DSRS technique for the linear region of the linear-logarithmic mode.

The signal-to-noise ratio (SNR) was plotted using the model for multimode sensors, presented and discussed in [22]. When both temporal noise and residual FPN are considered to calculate this ratio, it is more adequate to call it signal-to-noise-and-distortion ratio (SNDR), as is done in [23]. This is due to the fact

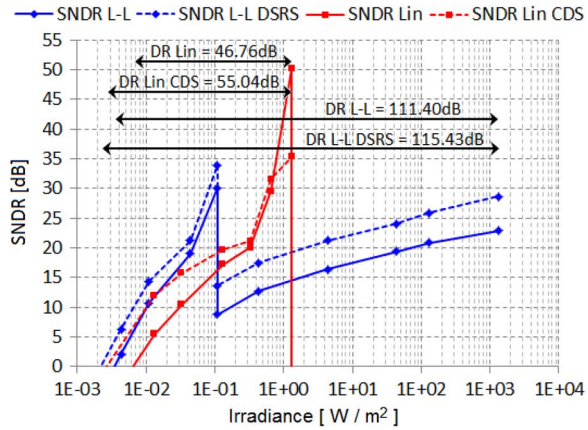

Fig. 10. SNDR curves for the linear-logarithmic and pure linear modes before and after FPN compensation "SNDR L-L," "SNDR L-L DSRS," "SNDR Lin," and "SNDR Lin CDS" respectively, with their respective Dynamic Ranges.

that residual FPN is rather a fixed spatial distortion associated to the pixel array than a dynamic quantity fluctuating over time.

The SNDR curves with their respective dynamic range, before and after FPN compensation, for both operation modes, are presented in Fig. 10. Only the 40 regular pixels of the array were considered to determine the presented SNDR curves.

The proposed technique improves the SNDR of this linear-logarithmic combination along the whole range of illumination, as shown in Fig. 10. The dynamic range towards low light is improved in 8.28 dB in the linear mode with CDS, and in 4.03 dB in the linear-logarithmic mode with the proposed DSRS technique.

Using this combined linear-logarithmic approach, the linear region is not allowed to reach the saturation level as it does in [9]. Therefore, in the present case, the complete useful dynamic range of the linear region is not achieved, as it can be observed in Fig. 10.

A summary of the main measured characteristics of the sensor considering only the 40 regular pixels of the array is presented in Table II.

B. FPN Attenuation With Additional Column-FPN

When considering the two columns with induced FPN the mean value, μ_x, for each irradiance must be recalculated using (1) without considering the component containing the sum of the values of the pixels of these columns, Σ_{col} defined in (2). As well the spatial variance will be calculated using (4) without considering the component $\Sigma_{\Delta\mathrm{col}}$ defined in (5).

The curves of FPN versus irradiance, for both modes of operation, before and after compensation, when the effect of the two columns with induced FPN is taken in account, are shown in Fig. 11.

Comparing the curves in Fig. 11 with those in Fig. 9, the results show that besides the PRNU peak, the additional distortion of the two different columns almost doubles the raw FPN in both modes of operation. The residual FPN, in both modes, after their respective compensation, remains almost at the same level as when the addition distortion was not considered. However, in the linear-logarithmic mode, the residual FPN presents a slight increase in relation to that of the previous case.

The capability of the proposed technique in reducing FPN can also be verified when comparing the resulting images, before and after FPN compensation, of the five pairs of frames

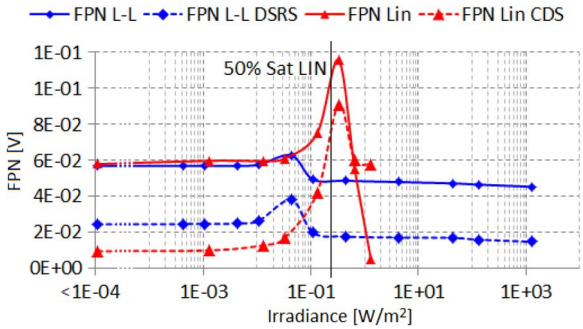

Fig. 11. FPN versus irradiance of the regular pixels plus the two columns with additional distortion of the array for the linear-logarithmic and pure linear modes before and after FPN compensation "FPN L-L," "FPN L-L DSRS," "FPN Lin," and "FPN Lin CDS" respectively.

on the right in Fig. 6. And though it is not optimized as those techniques, applied selectively per mode or region of operation, presented in [9] and [17], the proposed calibration can be executed at least at the same rate of a regular CDS operation in the linear mode.

The effect of those pixels with metal shield is not treated in this work. Concerning these pixels, it was observed that their contributions present far more deviation from the regular situation, where no induced FPN is added, than those of additional column FPN. The analyses of the effect of these pixels are to be discussed in further work.

VI. Conclusion

A simple technique to attenuate spatial fixed-pattern noise (FPN) in the complementary linear-logarithmic APS was presented. The implementation of the proposed technique requires only a minor modification to the conventional three-FET pixel design and control-signal scheme. Therefore, the pixel complexity is kept low and its size small, rendering its fill factor as high as that of the basic three FET APS, except for a slight reduction due to the additional connection line for the reset-transistor drain terminal RDR. Experimental results confirm that the proposed technique is able to attenuate FPN in a quite steady ratio within the whole tested illumination range. This ability is demonstrated even when additional column distortion is deliberately introduced in the pixel array. The lack of a high quality image showing the results before and after FPN compensation, and more detailed comparisons with previous techniques are some of the limitations due to the reduced size of the array used in this work. The presented results show that the proposed solution, based on a simple modification revisiting a well-established pixel topology, leads to an improved CMOS image sensor at no additional fabrication cost.

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