The CHESS-2 Prototype in AMS 0.35 μm Process: a High Voltage CMOS Monolithic Sensor for ATLAS Upgrade.

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***Abstract*–CHESS-2 (CMOS HV Evaluation for Strip Sensors) is a novel ASIC strip architecture designed to investigate the feasibility of using HV-CMOS MAPS (Monolithic Active Pixel Sensors) as alternative sensors for the ATLAS Phase-II Strip Tracker Upgrade. The ASIC is optimized for signal processing, hit pixel position encoding and readout. CHESS-2 includes three independent groups of 128 strips composed of 32 pixels each. The pixel includes a charge sensitive amplifier and the first stage of a comparator inside the collecting well. The second stage, the configuration, the encoding and the readout sections are placed at the periphery of the strips. A novel "fast skip" hit encoding logic identifies the first 8 hit pixel positions with a single-bunch time resolution (25 ns) and sends the data to a fast readout circuitry for serialization and transmission on 14 LVDS channels at 320 MHz. Several substrate resistivity variants have been fabricated for a full characterization of the performance aspects.**

I. Introduction

The LHC luminosity upgrade, known as the High Luminosity LHC (HL-LHC), will require the replacement of the existing silicon strip tracker and the transition radiation tracker. The ATLAS collaboration along with other partners, is exploring the feasibility of using CMOS MAPS (Monolithic Active Pixel Sensors) as alternative sensors to the baseline design [1]. The integration of amplification and data processing functions on the silicon sensor itself offers several attractive benefits like improvement of granularity for pattern recognition, better resolution and costs and material reduction. The last two decades have seen several improvements in the development of MAPS for particle physics. The introduction of deep implants allowed to use sensor substrates through either the use of HR (high resistivity) or HV (high voltage) CMOS processes with higher signal level and faster collection time while retaining full CMOS functionality. These processes, potentially very rad-hard, make them suitable to be used in the ATLAS Phase-II Strip Tracker Upgrade. Two foundries were chosen for this evaluation: HV AMS 350 nm and HR TowerJazz 180 nm [2]. This paper will focus on the AMS-H35 design.

Following the successful results of CHESS-1 AMS, a full reticle ASIC with a segmented strip architecture called CHESS-2 (CMOS HV Evaluation for Strip Sensors) shown in Fig. 1 has been designed to further characterize several crucial performance aspects of HV-CMOS monolithic sensors in a standard process in terms of analog signal sensing and data readout.

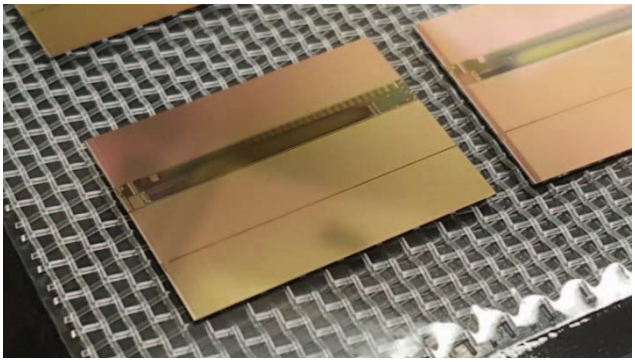

Fig. 1: CHESS-2 die.

The ASIC has been optimized for signal processing and hit position encoding and readout. It is made of three independent groups of 128 strips composed of 32 pixels each, as well as multiple test structures. CHESS-2 has a full reticle size of 20 mm x 24 mm and it has been fabricated in AMS-H35 technology with different substrate resistivity variants: 20, 50-100, 200-300, 600-2000 Ω-cm.

The fabrication of a full size sensor allows the investigation of large scale effects like common mode noise, cross-talk and power drops, the evaluation of the radiation hardness and the

Manuscript received December 5, 2016. SLAC-PUB-16888.

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978-1-5090-1642-6/16/$31.00 ©2016 IEEE

characterization of the pixels in terms of hit efficiency, charge collection speed and signal-to-noise ratio using different methods like source and beam tests.

The pixel size is 40 µm x 630 µm and includes a charge sensitive amplifier and the first stage of a comparator inside the collecting well. The second stage, the configuration, the hit encoding and the readout blocks are located at the periphery of the strips.

The AMS-H35 technology could be used with higher resistivity substrates and design rules for either 60 V or 120 V bias voltages. Fig. 2 shows an example of cross section when a typical small bias voltage is applied for conventional use. Instead in the current application, use of a higher bias voltage will thicken the depletion region across the full width of the pixel.

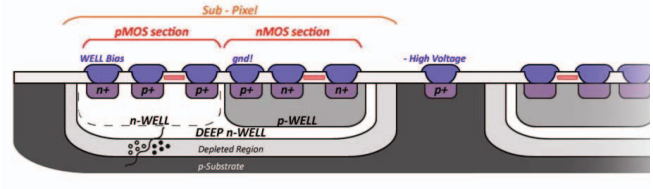

Fig. 2: Example of cross section with a typical small bias voltage for conventional use.

CHESS-2 specifications are summarized in Table I. In this paper the ASIC structure, layout and preliminary performances are presented. In section II ASIC architecture and functionality are discussed. In section III CHESS-2 layout is described. In section IV preliminary results are reported.

TABLE I. CHESS-2 SPECIFICATIONS

Parameter	Value
Substrate Resistivity	20-2000 Ω-cm
Substrate bias voltage	120 V
Number of strips	128
Number of pixels per strip	32
Pixel size	40 µm x 630 µm
Max hit number per 128 strips	8
Max hit number per strip	1 + double hit flag
Timing resolution	25 ns
Readout speed	320 MHz
N. of wirebonds per 128 strips	28 for readout
Additional constraint	Rad-Hard design

II. ASIC ARCHITECTURE

Fig. 3 shows a simplified block diagram of the CHESS-2 single array. The floorplan can be divided in four main parts: the signal charge acquisition, the encoding, the readout and the configuration and calibration sections.

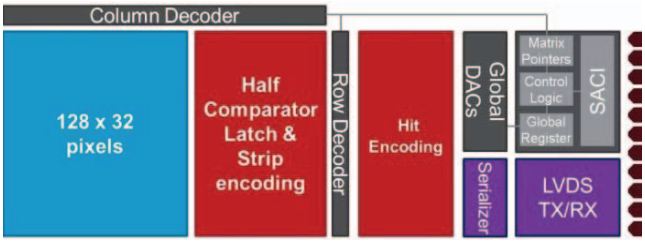

Fig. 3: Simplified block diagram of the CHESS-2 ASIC array.

Fig. 4 shows a simplified schematic of the pixel. The input charge coming from the sensor is amplified, filtered and compared to a programmable threshold value.

Several parameters like the feedback and the first stage comparator currents can be programmed globally. The thresholds can be fine tuned for individual pixels. The baseline and threshold comparator values are set outside the chip. External signal injection is also available in each pixel.

In order to minimize the back injection no digital programming signal is active during operation. Pixels have been shielded from any potential dynamic signals. Custom comparator design reduces its output swing.

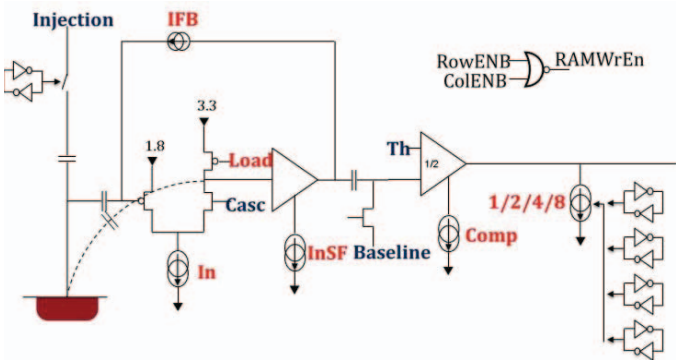

Fig. 4: Simplified CHESS-2 pixel schematic.

Principle of operation of the encoding section at the periphery of the matrix is shown in Fig. 5. It is composed of strip and hit encoding subsections.

The strip logic encodes the column address of the first hit pixel in each strip and raises a flag if a double hit has occurred on the same row. This operation is completed in 25 ns.

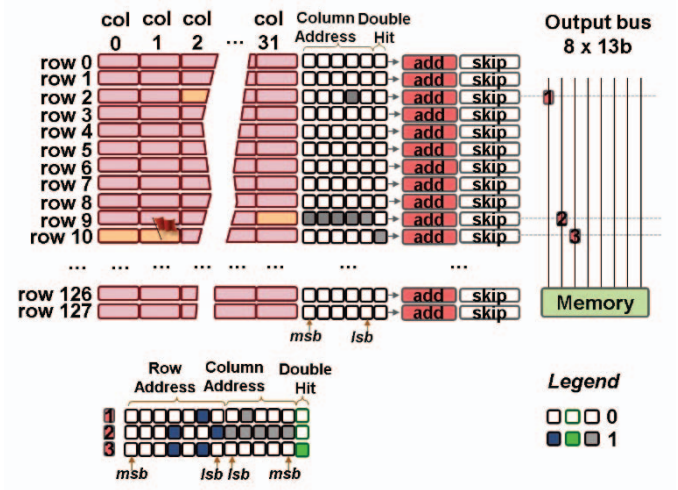

Fig. 5: Principle of encoding operation.

The hit encoding logic identifies the first 8 hit pixel positions with a single-bunch timing resolution (25 ns) and adds the row address to the payload. This performance cannot be achieved with a 3-bit adder for each row and using its value to multiplex the row and column address data payload on 8 memories. This is due to the adder speed (> 1 ns) and the very long capacitive lines. A novel "fast-skip" architecture has been introduced. Scanning all the rows, the sum operation

necessary for the count is performed only if a hit has occurred, otherwise a skip logic will override the operation.

A two stage pipeline-like approach has been implemented to retain effective 40 MHz operation. Fig. 6 shows the basic concept: the operation of finding the first 8 hits over 128 rows in one step can performed in two steps finding the first 8 hits every 32 rows. The first pipeline stage is composed of four parallel "fast-skip" units. Each unit detects the first 8 hits over 32 strips and stores the encoded positions in 11 x 8 bit memories: after the first step, the first 32 hit pixel positions have been detected. The second pipeline stage is composed of one identical "fast-skip" unit which scans the previous 32 stored payloads and defines the first 8 hit pixel positions.

The "fast skip" logic combined with the pipeline-like structure is able to detect the first 8 hits in only 7.6 ns with a latency of one clock cycle.

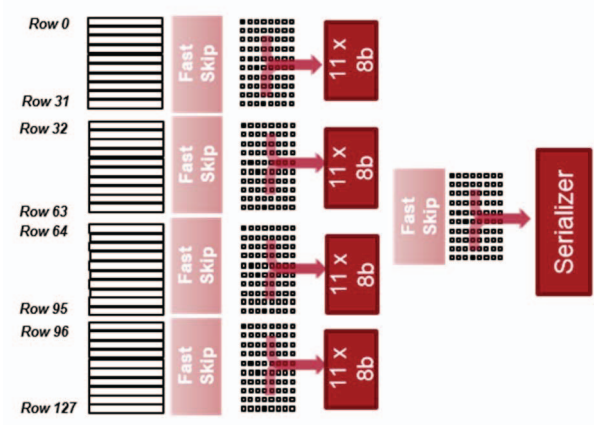

Fig. 6: Hit encoding pipeline-like approach.

The hit encoder generates also a sync/valid signal. Its rising edge provides a synchronization point for the ASIC readout circuit and its signal level indicates if the data payload contains the address of a hit. Fig. 7 shows an example. A hit occurred in the pixel of position row 34, column 0 of the matrix and the valid signal is high.

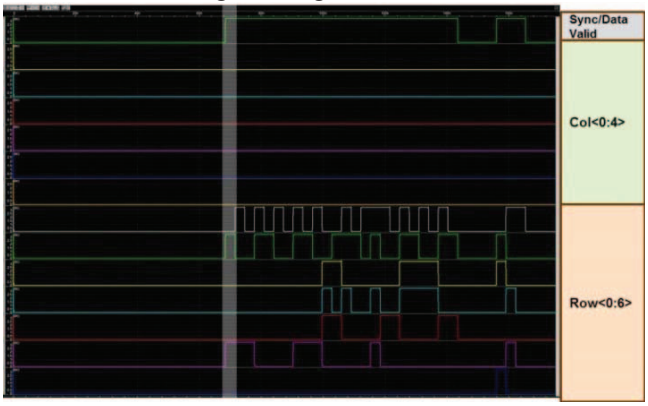

Fig. 7: CHESS-2 hit encoding simulation: hit on row 34, column 0.

In order to avoid crosstalk between different cycles a programmable reset phase is embedded in the hit encoding.

The clock synchronization between the hit encoder and the matrix has been verified in all corners and can additionally be finely tuned with 400 ps steps to compensate for up to 6 ns of delay. As additional debug feature the hit encoding logic can enter in a test mode to evaluate its functionality independently of the analog matrix.

The payload is sent to a fast readout circuit shown in Fig. 8 synchronized to the external 320 MHz clock. A serializer converts the parallel data in a 14-bit serial buffered output to minimize possible delays and to improve driving strength.

LVDS channels allow the transmission of the encoded hit pixel positions and the sync/valid flag outside the chip. LVDS transmitter can be programmed in two possible current modes: the standard LVDS (3 mA) or a current saving mode (200 μA).

The external 320 MHz clock is provided to the chip through a LVDS receiver which can be configured selecting the AC/DC mode and the 100/300 Ω input impedance.

A control unit allows the configuration and calibration of single pixels, rows, columns or the entire matrix and the settings for the hit encoder, the monitoring system and the LVDS receiver and transmitters.

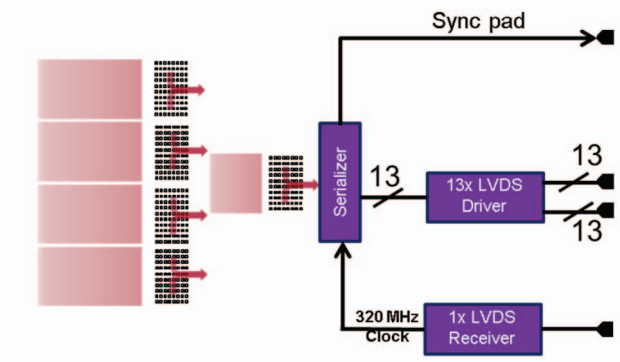

Fig. 8: Readout section.

III. LAYOUT

Fig. 9 shows the layout of the entire ASIC. One array of 128 strips is present at the bottom, the other two are on the top. Test structures are visible in the middle. The total size of the chip has been planned to take advantage of the maximum available reticle size, which is in the order of 20 mm x 24 mm.

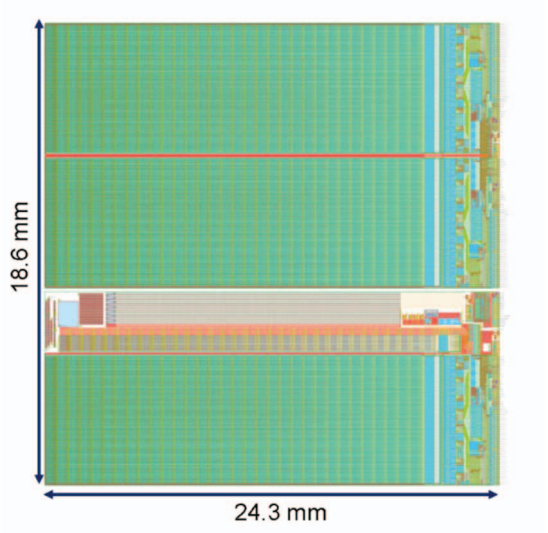

Fig. 9: CHESS-2 ASIC layout.

Every group of 128 strips occupies an area of 5 mm x 24 mm as visible in Fig. 10. Configuration, encoding and readout sections are at the periphery.

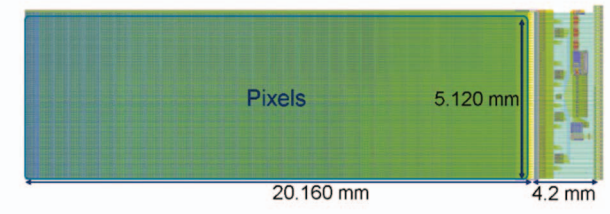

Fig. 10: Layout of a group of 128 strips.

Each strip is divided into 32 pixels composed of 6 connected n-wells surrounded by the substrate as shown in Fig. 11.

The diode fraction is around 50%. This configuration has been chosen after extensive tests on the previous prototype offering better performances compared to the other implemented fraction areas: measurements showed no evidence of breakdown after a radiation dose of 2 x 10^{15} neq/cm^2 with not much leakage current at the foundry guaranteed 120 V operating point [2].

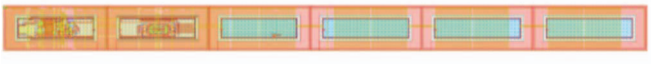

Fig. 11: Pixel layout.

IV. Experimental Results

Among the others, one of the CHESS-2 goals is to investigate bulk and surface properties of the HV-CMOS sensors at high radiation dose. Many types of irradiations have been carried out but only preliminary test results from neutron irradiation are presented in this section.

Several substrate resistivity variants have been fabricated for a further characterization at different doping concentration levels. Preliminary results refer just to a sample with substrate resistivity 200-300 Ω-cm.

Edge-TCT setup is shown in Fig. 12. The edge of a passive pixel array has been illuminated with a pulsed narrow laser beam. In the measurements "X" axis refers to the chip width, "Y" axis refers to the chip depth.

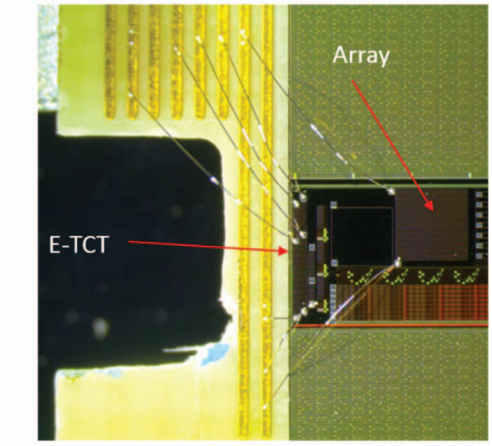

Fig. 12: Edge-TCT setup. "X" axis points across the chip surface, "Y" axis points into the chip depth.

Charge collection profile along a pixel as a function of the silicon y-depth is shown in Fig. 13. Substrate is biased at 100 V.

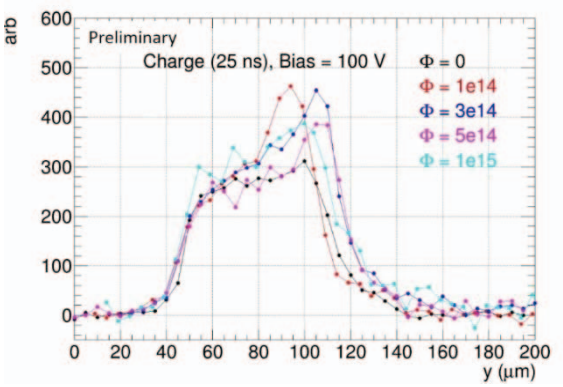

Fig. 13: Charge collection profile as a function of silicon y-depth for different neutron fluence values. Substrate voltage 100 V.

Fig. 14 shows the 2D collected charge profile scanning three adjacent pixels in the x-y plane at 100 V and Φ = 3 x 10^{14} neq/cm^2. The relative depletion regions merged into a large sensitive area and no gaps are visible.

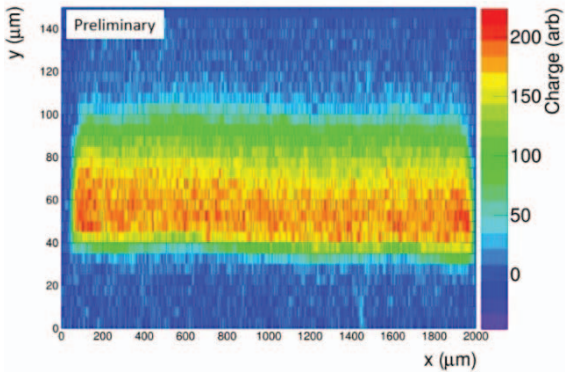

Fig. 14: Collected charge at different x-widths and y-depths. Substrate voltage 100 V, neutron fluence Φ = 3 x 10^{14} neq/cm^2.

Dependence of the charge collection full width at half maximum (FWHM) on substrate voltage for different fluence values has been measured for the sample 200-300 Ω-cm as shown in Fig. 15. The extracted space charge N_{eff} [3] is roughly consistent with the nominal resistivity value for the considered sample.

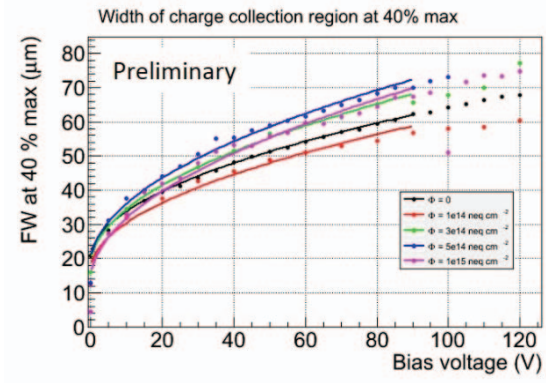

Fig. 15: Dependence of charge profile width on substrate voltage for different neutron fluence values.

V. Conclusion

CHESS-2 is a HV-CMOS monolithic sensor designed for the ATLAS Phase-II Strip Tracker Upgrade. Use of MAPS could allow the following benefits: improvement of the granularity and spatial resolution, reduction of the number of wirebonds, sensor cost and construction time.

The ASIC has been designed to take advantage of the maximum reticle size and contains three groups of 128 strips divided in 32 pixels each.

A novel fast architecture encodes the first 8 hit pixel positions over 128 strips with a bunch crossing time resolution and generates a sync/valid signal. The encoded pixel positions are converted in 14-bit serial outputs and sent out at the frequency of 320 MHz through LVDS channels.

Several resistivity variants have been fabricated to investigate large scale effects, radiation hardness and to characterize different performance aspects like charge collection efficiency.

Preliminary Edge-TCT measurements have been shown for a sample with substrate resistivity 200-300 Ω-cm after neutron irradiation.

Acknowledgements

The research was supported and financed in part by UK Science and Technology Facilities Council (STFC), the Slovenian Research Agency, the United States Department of Energy, grant DE-FG02-13ER41983, and the SLAC LDRD program. The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

The irradiations with protons were performed at the University of Birmingham MC40 cyclotron, supported by the H2020 project AIDA-2020, GA number 654168. The irradiations with neutrons were performed at TRIGA reactor in Ljubljana. The authors would like to thank the crew at the TRIGA reactor in Ljubljana for their help with the irradiation of the detectors, as well as staff at the Gamma Irradiation Facility of Sandia National Laboratory, especially Dr. M. Wasiolek and Dr. D. Hanson.

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