CMOS Active-Pixel Sensor in Low Temperature

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***Abstract*— This paper presents experimental and simulated results of an Active-Pixel Sensor (*APS*) circuit operating at different temperatures (300K, 77K, 60K and 40K). The optical sensor used was a silicon photodiode integrated with its electronics in a standard *CMOS* 0.35µm technology. Interestingly, the pixel worked well at all temperatures tested. These first experimental results are very promising for future hybridization between *APS* circuits and infrared quantum sensors, mostly on III-V semiconductor substrates, or other applications demanding low temperatures.**

Keywords— Active Pixel Sensor, cryogenic circuits, low temperature, CMOS analog integrated circuits; photodiode; optical sensor; integrated optoelectronics.

I. INTRODUCTION

The *APS* is a very useful signal conditioner on image sensor technologies, and it is mainly operated at room temperature.

This kind of circuit consists of a simple transistor configuration, with a source follower amplifier, and a reset switch attached to a photosensor.

The use of *CMOS* microelectronic circuitry in cryogenic temperatures (<77K) is of great importance in some fields, such as infrared imaging [1]. Also, there are situations where conventional image sensors are used at extreme low temperatures, as in outer space missions, where it can reach temperatures of 30K [2].

Although CMOS imagers have been widely used and reported [3] [4], research and development at cryogenic temperatures [5] [6] [7] are often considered sensitive due to the potential applications in warfare technology. Therefore, its results are very often not published.

At cryogenic temperatures, i.e. ~150K, besides material overstress, especially at interfaces, both charge-carrier mobility and availability for conduction are reduced in silicon [8]. Those affect directly a transistor operation, reducing, for example, the threshold voltage and the channel length. In extreme cases, it is expected that the transistor will not function properly.

The *APS* was the chosen structure for the low temperature tests and to be part of a future hybridization with a nanostructured infrared sensor because it is a simple circuit with few transistors; it is less prone to be affected by the reduction of the electron-density; and it is capable of working with photoresistive sensors [9], like the *QWIP* structure – which needs to operate below 80K.

In this work, the initial results on experiments carried out for this circuit with a light sensor in low temperatures, i.e. 77K, 60K and 40K, will be presented, and, the possibility of integrating a cooled sensor to the system will be analyzed.

II. DESIGN AND OPERATION OF THE ACTIVE PIXEL SENSOR

In this paper we use a topology that is usually referred to as a four-transistor *APS* (*4T APS*), consisting of *Reset*, Buffer, Select (*Ts*) and Transfer gate (*Tx*). As a matter of fact, for *Tx* we chose a complementary transistor (*Tx*), combining an *NMOS* and a *PMOS* in parallel to yield maximum analog signal swing [10]. The sense element, which can be a p-n junction, is connected to the transducer node (*Tn*), as shown in Fig. 1. The supply voltage (*Vdd*) is connected to the sense-node (*Sn*) through the *Reset* transistor, and for this a *PMOS* was used to guarantee a higher reset voltage than that of an NMOS switch. The *Ts* transistor is used to select a pixel in a pixel array. The source of the complementary *PMOS/NMOS* *Tx* is connected to the photodiode.

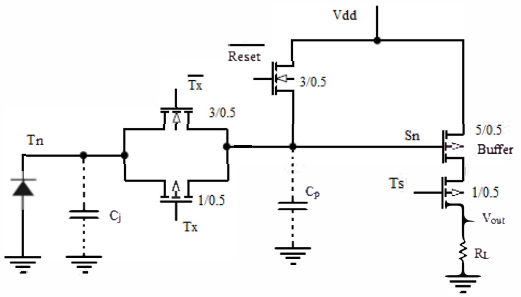

Fig. 1. Circuit schematic of the designed *APS, where channel dimensions are given in microns.*

The pixel circuitry was designed in the OptMA[lab] (Fig. 2a), and was implemented by *AMS* in a standard 0.35µm *CMOS* technology in a 4mm x 3mm die (Fig. 2b). The pixel features an integrated square silicon photodiode (Fig. 3a). There is a top metal layer that shields the circuitry against radiation, leaving only the photosensors exposed.

The photodiode is a p-n junction (Fig. 3a), and its profile is shown in (Fig. 3b). It's concentration values were estimated from the available processes data, in which the epitaxial acceptor concentration is $3.3\text{x}10^{16}$ cm^{-3}, and the n-well donor concentration is $1.6\text{x}10^{16}$ cm^{-3}. The photodiode active area is

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0.0088mm², and its junction capacitance is 1.08μF. The chosen dimensions for this photodiode can be considered large, since it was designed to attend to applications other than imaging in the visible range, such as position sensors or large-pixel infrared imaging or gas detection [3] [4] [11]. The operation of this pixel consists of a period of *Reset* and *Tx* turned on, that charges the photodiode intrinsic capacitance. The voltage over this capacitance is copied to V_{out} through the Buffer transistor. When the transistor *Reset* is turned off, the integration period starts (*Tx* still turned on), which consists of a photogenerated current discharging the intrinsic capacitance through the photodiode.

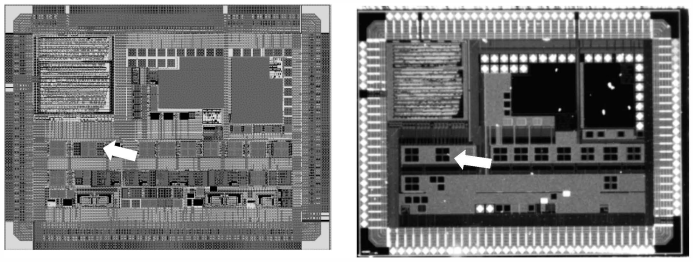

Fig. 2. (a) Design of the CHIP,(b) Picture of the CHIP – The arrow indicates the location of the pixel.

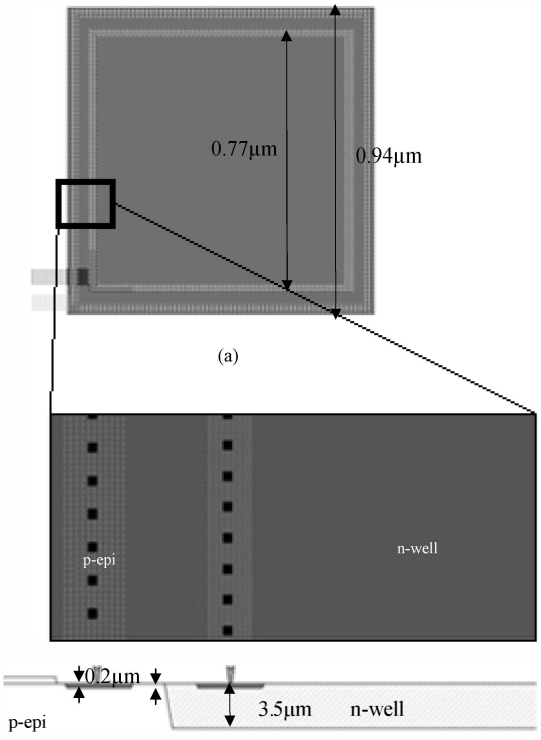

Fig. 3. Photodiode: (a) superficial view (b) Photodiode with layers design thickness.

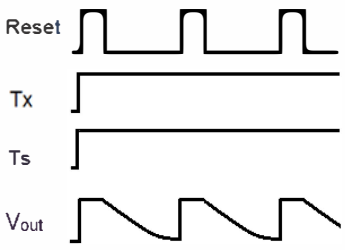

Fig. 4. Reset, Tx, Ts and Vout timing.

If *Tx* is turned off, after *Reset* is also off, the Buffer gate will be isolated from the photodiode. The charge stored on the parasitic capacitance formed by the junction of drain and source of the transistors is then expected to be kept constant, except for the effect of a small drain–bulk leakage current. V_{out} is expected to be constant as well.

III. EXPERIMENTAL SETUP

The optical test setup in Fig. 5 consists of a 532 nm laser beam (Fig. 5- {1}) passing through a variable neutral-density filter (Fig. 5- {2}) and then by a ground matte glass plate (Fig. 5- {3}) to homogenize it, focusing on the chip inside a cryostat (Fig. 5- {4}) (CCS Janis) with a germanium optical window. The optical spot irradiance, ranged from 0.3 W/m² to 4.25 W/m², was measured from a calibrated laser power meter (Thorlabs PM320E) in front of the cryostat optical window.

The AMS 0.35μm chip, with *APS* and integrated sensor, was supplied with 3V. The chip case was fixed to the cryostat support, leaving the chip exposed to light (Fig. 6a). The support was then placed inside the cryostat case in vacuum. In the cryostat the temperature was measured both in the top and in the bottom of the chip support, for higher accuracy.

The additional proxy circuit was designed in printed circuit board, PCB, (Fig. 6b), responsible for the supply, the bias and the readout of the APS signal. This PCB was placed inside a metal housing (Fig. 5- {7}) for electromagnetic shielding. The chip inside the cryostat was connected to the printed circuit board outside through coaxial cabling (Fig. 5-{6}). All the experimental parameters are listed on Table. 1.

Table. 1. Experimental parameters

Supply voltage	3V
External temperature	296K
Cryostat temperatures	40.3K 60K 77.6K 300K
Optical spot irradiance	0.3 W/m² to 4.25 W/m²
Laser wavelength	532nm
Frequency of Reset	1kHz

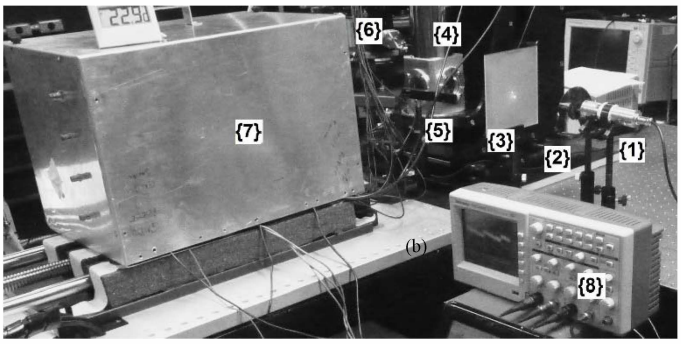

Fig. 5. Setup schematic, the laser beam generated by {1} is filtered in {2} passing through a ground matte glass plate {3} then by a germanium optical window {4} with the chip inside de cryostat and the light intensity is measured on the laser power meter {5}. The signals generated on the chip inside the cryostat are sent by a coaxial cabling{6} to the auxiliary circuit, this being shielded by a metal housing{7}. The response is saved by an oscilloscope{8}.

To generate control signals (*Reset*, *Tx*, *Ts* and MUX inputs) a Texas Instruments MSP430 microcontroller was used. The pixel output was measured by a Tektronix TDS2024B oscilloscope (Fig. 5- {8}).

All measurements were registered after 20 minutes of temperature stabilization. Three intensity measurements were made for four different temperatures.

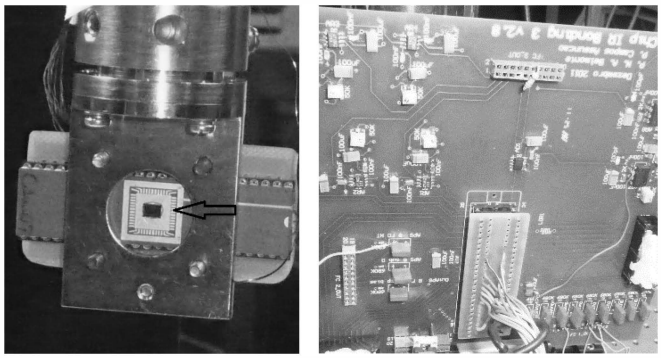

Fig. 6. (a) Picture of the encapsuled chip placed on the cryostat support, the arrow aim to the chip; (b) Additional printed circuit board.

IV. SIMULATION SETUP AND RESULTS

To validate the operation of the designed circuit at room temperature, simulations were made using SPICE and BSIM3v3 device models supplied by the foundry. The photodiode was modeled using a junction capacitance of 1.082pF and current sources whose values were calculated from experimental results. Such simulations were conducted at room temperature due to software restriction in libraries for low temperatures. All the simulated parameters are listed on Table. 2 and the results of the simulation are shown in Fig. 7.

Table. 2. Simulation parameters

Temperature	296K
Supply voltage	3v
Irradiance	0.3 W/m² 1.169 W/m² 4.25 W/m²
Photogenerated currents	0.9nA 3.3nA 5.8nA
Frequency of Reset	1kHz

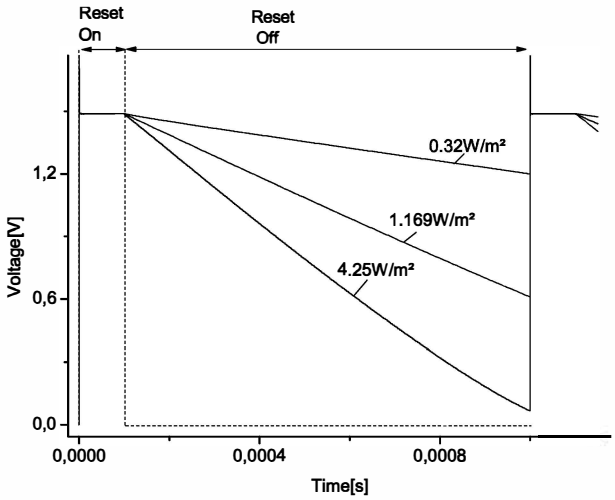

Fig. 7. Simulated output pixel signal of the three irradiances for the temperature of 300K.

V. EXPERIMENTAL RESULTS

The *APS* output voltage measured for each temperature ranging the irradiance is plotted in Fig.8, Fig.9 and Fig.10.

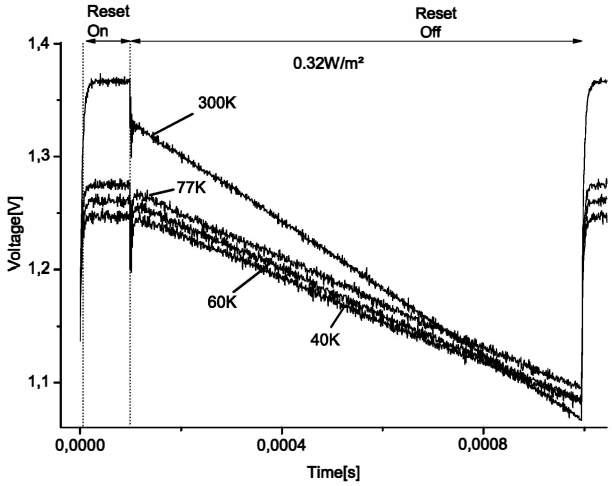

Fig. 8. Measured the output pixel signal of the five temperatures for the irradiance of 0.32W/m².

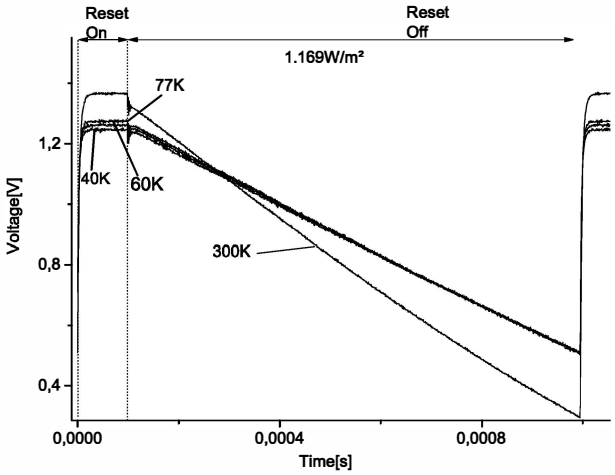

Fig. 9. Measured the output pixel signal of the five temperatures for the irradiance of 1.169W/m².

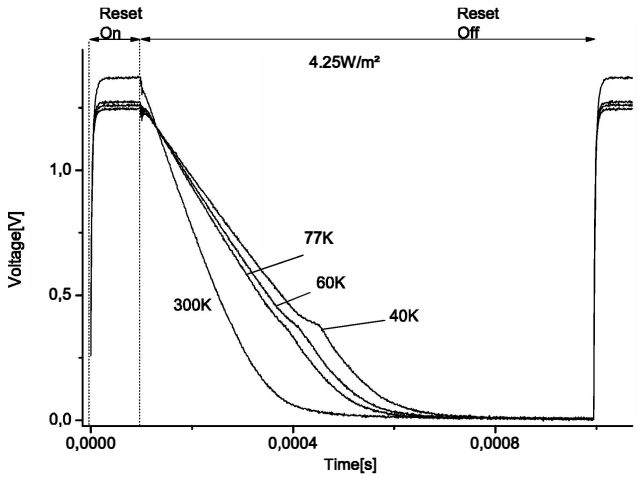

Fig. 10. Measured the output pixel signal of the five temperatures for the irradiance of 4.25W/m².

As we can see on the simulation, the experimental results follow the same pattern at room temperature (300K): the higher the irradiance, the higher the voltage decay during the integration time. The only difference is in the decay slope that can be explained by parasitic impedances present in the

circuit and the bus that were not modeled by the simulator. This shows that the results and events to be analyzed in this section are due to temperature decrease.

The voltage decay that is exponentially related to the photogenerated current, decreases as the temperature goes down. That is caused by the number of carriers available for conduction in the transistor channel. At low temperatures, the thermal energy in the crystal is not sufficient to ionize all the donor impurities present, and the electron density available for conduction is less than the donor concentration in the NMOS, and the hole density available is less than the acceptor concentration in the PMOS.

During the *Reset* period, an increase of V_{out} is seen, being such related to an increase in temperature. These effects are due to the fact that the lower the temperature, the lower the number of carriers in the channel and the greater the channel ON resistance. It causes a larger voltage drop on the *Reset* and the *Tx* transistor channels, leading to a lower V_{out} value.

Another factor that may influence the response of the circuit is the effect of lowering the temperature on the metal bus, the pads and the metal layer that shields the circuit, since the resistivity of these materials may vary with temperature.

It is possible to note that, for the highest intensity (Fig. 10), an event (Fig. 11{3}) occurs, as it is shown on the output plot. This effect can be explained by an analysis of Fig. 11: in {1}, the voltage on the *Tx* transistor drain (*Vd* and source (*Vs*) are equal, since *Tx* is conducting, therefore connecting the *Vdd* voltage to the photodiode. There is a capacitance (*Cj*) intrinsic to the p-n junction which will be analyzed along with the junction capacitance of the *Tx* drain/bulk transistor (*Cp*). When the *Reset* transistor is off, these capacitors begin to be discharged with the photogenerated current. (Time {2} of Fig. 11).

Since the *Cp* capacitance is much smaller than the *Cj* capacitance, the stored charge on the former is totally exhausted. There still are, however, carriers moving through the channel. The time that takes for all these carries to go through the channel is shown on period {3} of Fig. 11. This effect is easily noticed at low temperatures, when the carriers' mobilities drop, and at high currents, when there is a higher chance of capacitance discharge. This effect is imperceptible for higher temperatures, such as room temperature.

The period {4} of Fig. 11 starts when every charge moves through the channel and the voltages *Vd* and *Vs* get to be equal again. When this happens, no more current passes through the channel and the transistor voltage *Vds* is 0V. At this point, the photogenerated current has the same value as the *Cj* capacitance-discharge current.

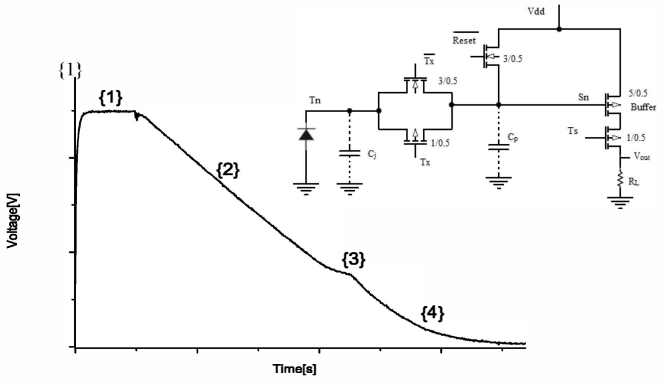

Fig. 11. Pixel output representation, focusing on the event {3} effect.

VI. CONCLUSION

The results presented in this paper are very promising when the development of active pixel sensor hybridization with an infrared sensor in cold operations is concerned. At very low temperatures the APS pixel presented an adequate response, despite the partial freeze-out of charge carriers and mobility reduction, and their consequent effects on transistor operation. It is important to notice the appearance of a kink effect of the response curve, observed at low temperatures, so that precautions can be taken to avoid reading errors in pixel arrays.

These results are still preliminary, which means that there is a need for further experiments that will prove reproducibility and whether the packaging resists long periods of exposure to low temperatures. For now, the results show that the APS work properly at a temperature range that goes from 40K up to 300K. This work is very important for the development of pixels deploying infrared quantum sensors mostly on III-V semiconductor substrates, which feature better working characteristics at low temperatures.

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