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SIMPLIFIED WIDE DYNAMIC RANGE CMOS IMAGE SENSOR WITH 3T APS RESET-DRAIN ACTUATION

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Tese de Doutorado submetida à Banca Examinadora designada pelo Colegiado do Programa de Pós-Graduação em Engenharia Elétrica da Escola de Engenharia da Universidade Federal de Minas Gerais, como requisito para obtenção do Título de Doutor em Engenharia Elétrica.

Orientador: Prof. Davies William de Lima Monteiro

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Aprovada em 31 de julho de 2014.

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Life is just wonderful, it is the greatest gift given to men. Life is the basic fuel of all we do in this world, and despite the several existent worldviews, nobody can ultimately tell whence it really come. Concerning this matter the only choice one has is to believe one worldview, or another, or yet creating one new. I chose to believe the worldview preached by the Christian Bible where it says that life is a gift of the Lord God Almighty that created the heavens, and the earth, and all that in them is.

Both for the gift of life and also for allowing me to perform the very work herein presented, my first thank is to the God that I worship, YHWH. Together with him, I thank my lord Yeshua Hamashia for the hope of preserving life beyond the days of my pilgrimage in this world, and I thank also my precious friend Ruach Kadosh for helping me in my weaknesses, and for teaching me how to direct my steps in this world.

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I thank my wife Keitia, and my two boys Judá Alberto, and David Ben Gurion for being the main reason for which I work in this life. The greatest challenge of my life is being the best minister of God to you ward. More than any title I can receive in this life, being the father of our family is the greatest title for me because it is a title given by our God.

I thank my parents Carlos Alberto and Maria Amelia for all the love and support they gave and give during all the years of my life so far. The good counsels of my father made great difference in my life, among the many the one that says: “be always prepared for the opportunities the life will bring”, I just try to follow them. The support and prayers of my mother also made and make great difference in my life. I thank also my brothers and their families for their presence and support in many important moments of my life. I thank also my apostles, pastors, and brethren from my home church “Ministério Internacional da Restauração” in Manaus, for helping in prayer during these years.

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Abstract

An image sensor is an array of small light-sensitive cells called pixel sensors. A pixel, or picture “pix” element “el”, is the smallest unit of an image. Therefore a pixel sensor is the smallest cell of an image sensor, which is able to detect a single image dot. Such image dot is then used to reconstruct a complete image frame.

Image sensors built in CMOS technology are nowadays largely employed either in professional cameras or in personal mobile devices with embedded cameras. One of the most important features of a good image sensor is the ability to accommodate in the same image regions of high and low luminosity, a feature known as the sensor dynamic range.

Many techniques, found in the literature, are able to extend the sensor dynamic range, each with their advantages and disadvantages, either by extending the saturation level or by reducing the noise floor. Non-idealities introduced during fabrication produce unwanted image artifacts known as fixed-pattern noise – FPN and are among the main contributors to the noise floor in CMOS image sensors.

Techniques applied to reduce FPN in image sensors with large dynamic range are still a challenge, because in applying these techniques other essential features of the sensor are jeopardized, as its processing speed, the reduction of photosensitive area, or the increase in fabrication costs.

The main goal of this work is the improvement of CMOS image sensors, operating with wide dynamic range for general practical purposes, through the application of simple circuit control techniques, without interfering in the fabrication process of the imager. In order to achieve this goal, the present work proposes a simple and innovative approach to increase the dynamic range of the basic and most popular pixel sensor architecture currently employed in CMOS image sensors.

The proposed idea differs from the current state-of-art in two essential points. First, because it is able to increase the sensor dynamic range without the need of boosting the level of any control signal above that of the supply voltage. Second, because, other than any different techniques found in literature, it is able to reduce FNP in this sort of image sensor by means of a simple control strategy.

Boosting the level of some control signals is necessary, in previous techniques found in the literature, in order to avoid the use of more complex pixel-sensor architectures, which reduces the sensor photosensitive area. On the other hand, internal voltage boosting is harmful because it tends to reduce the life time of the imager.

The simplified way to reduce FPN in the herein proposed technique is able to keep unaltered important features of the sensor, as those cited above, at no additional fabrication cost.

This thesis’ defense presentation can be watched, in Portuguese language, at:
https://www.youtube.com/watch?v=vHUhrzmfed4 (Published on: 08/10/2014)

Resumo

Um sensor de imagem é uma matriz de pequenas células fotossensíveis chamadas sensores de pixeis. Um pixel, elemento “el” fotográfico (*picture*) “pix”, é a menor porção de uma imagem. Assim o sensor de pixel é a menor célula de um sensor de imagem, capaz de detectar um ponto singular da imagem. Este ponto é então usado para reconstruir um quadro completo de imagem.

Sensores de imagem CMOS são atualmente largamente utilizados tanto em câmeras profissionais como em aparelhos moveis em geral como celulares. Uma importante característica de um bom sensor de imagem é a capacidade de acomodar na mesma imagem regiões de alta e baixa luminosidade, chamada de alcance dinâmico do sensor.

Muitas técnicas, encontradas na literatura, são capazes de aumentar o alcance dinâmico do sensor, cada uma com vantagens e desvantagens, tanto retardando o nível de saturação quanto reduzindo o ruído base. Não idealidades introduzidas durante o processo de fabricação produzem artefatos indesejáveis na imagem conhecidos com ruído de padrão fixo (*fixed-pattern noise*) – FPN e está entre os principais contribuintes para a determinação do ruído base em sensores de imagem CMOS.

Redução de FPN em sensores de imagem com largo alcance dinâmico ainda é um desafio, pois ao aplicar qualquer das técnicas existentes, outras características essenciais do sensor são comprometidas, como velocidade de processamento, redução de área fotossensível, ou aumento de custo de fabricação.

Este trabalho tem por objetivo aprimorar a operação de sensores de imagem CMOS, que operam com largo alcance dinâmico para aplicações praticas em geral, através da aplicação de técnicas simples de circuito, sem interferir no processo de fabricação. Para isso é proposto uma maneira simples e inovadora de aumentar o alcance dinâmico da mais básica e popular arquitetura de sensor de pixel atualmente usada em tecnologias CMOS.

A ideia proposta tem duas diferenças básicas do corrente estado-da-arte. A primeira é a capacidade de aumentar o alcance dinâmico sem elevar o nível de tensão de qualquer sinal de controle acima do nível da alimentação. A segunda é a simplicidade da técnica de redução de FPN neste tipo de sensor em relação às demais encontradas na literatura.

Nas técnicas, atualmente encontradas na literatura, a elevação do nível de tensão em alguns sinais de controle é necessária para evitar arquiteturas mais complexas, que reduzem a área fotossensível do sensor. Por outro lado a elevação da tensão acima do nível da alimentação é prejudicial, pois reduz o tempo de vida útil do sensor de imagem.

A simplicidade da técnica de redução de FPN proposta neste trabalho é capaz de manter inalterada características importantes do sensor, como aquelas citadas acima, sem custo de fabricação adicional.

A apresentação da defesa desta tese (em português) pode ser visualizada no seguinte link: https://www.youtube.com/watch?v=vHUhrzmfed4 (Publicado em: 10/08/2014)

Table of Contents

Acronyms

ADC (A/D) – analog-to-digital converter
AMS – austriamicrosystems
APS – active-pixel sensor
3T APS – three FETs active-pixel sensor
CCD – charge-coupled device
CDS – correlated double sampling
CMS – complementary-mode sensor
CMOS – complementary metal-oxide-semiconductor
dB – decibels
DM – dummy
DPS – diagram pixel sensor
DR – dynamic range
DRS – delta reset sampling
DSNU – dark-signal non-uniformity
DSRS – double-sampling readout subtraction
FD – floating diffusion
FET – field effect transistor
FPN – fixed-pattern noise
GND – ground
HDR – high dynamic range
I_{PH} – photocurrent
I_{DARK} – dark current in the photodiode
L – length
LAD – local adaptation
LIN – linear
LCR – logarithmic-compressed response
MMS – multi-mode sensor
MOS – metal-oxide-semiconductor
MSC – multiple-scene capture
NMOS – N-type MOS transistor
P-FRST – pseudo-flash reset
PD – photodiode
PPD – pinned photodiode
PIXEL – picture “pix” element “el”
PMOS – P-type MOS transistor
PN – the P type N type semiconductor junction
PPS – passive-pixel sensor
PRNU – photo-response non-uniformity
PTAT – proportional to absolute temperature
Q_{sat} – charge storage capacity
RDR – reset drain
REF – reference
RST – reset
SN – sense node
SNDR – signal-to-noise-and-distortion ratio
SNR – signal-to-noise ratio
SVE – spatial varying exposure
T – total

TH – threshold
T_{INT} – integration time
TTS – time to saturation
V_{DD} – source voltage level
W – width
WCA – well-capacity adjusting

Related Publications

C. A. de Moraes Cruz, D. W. de Lima Monteiro, and I. L. Marinho, "Extended use of Pseudo-Flash Reset Technique for an Active Pixel with Logarithmic Compressed Response," In Proceedings of 25th Symposium on Integrated Circuit and System Design, SBCCI, Brasilia-BR, Aug.-Sep. 2012.

C. A. de Moraes Cruz, D. W. de Lima Monteiro, G. Sicard, and A. K. Pinto Souza, "Simple Technique to Reduce FPN in Linear-Logarithmic APS," In Proceedings of 2013 International Image Sensor Workshop, ISSW 2013, Snowbird-Utah-USA, pp. 141-144, June 12-16, 2013.

C. A. de Moraes Cruz, D. W. de Lima Monteiro, E. A. Cotta, V. F. de Lucena Jr, and A. K. Pinto Souza, "FPN Attenuation by Reset-Drain Actuation in the Linear-Logarithmic Active Pixel Sensor," IEEE Trans. Circuits Syst. I, Reg. Papers, Online Early Access version July 11th, 2014.

Chapter I: Introduction to CMOS Image Sensors

An image sensor is a device used to detect image frames. The sampling of an image frame is performed by translating the illumination intensity of each small portion of the frame into an electrical signal, either a current or a voltage. A single frame can be divided into any number of small portions. Each single portion of the frame is regarded as an element that can assume a voltage or current level, within a range, according to the illumination intensity reaching a specific element. The voltage or current level of each element is then translated into a grayscale level that is displayed to compose the image frame.

The image sensor, or simply an imager, is an array composed of many small light-sensitive cells. The sampled frame is a collection of many small image portions, the exact quantity of which is defined by the number of light sensitive cells composing the imager. Each single small sampled portion of the image frame is called a pixel, or picture "pix" element "el". And therefore, each light sensitive cell of the imager array is called a pixel sensor.

Investigations on solid state image-sensor technology can be traced back to the end of 1960s [1]-[3]. Noble [1] and Chamberlain [2] created the first image-sensor arrays in a metal-oxide-semiconductor (MOS) technology, where each pixel had their own readout amplifiers. But due to many problems with MOS technology, as process variations, this technology was eclipsed by CCDs technology [4]. On October 17, 1969, George Smith and Willard Boyle, at Bell Labs, invented the charge-coupled device (CCD) [4] and [5] that one decade later would become the mainstream image-sensor technology. Smith and Boyle received the Nobel Prize for the invention of CCD Imager in 2009, and though their invention was intended for memory circuit, they perceived that such device would work as a solid-state imager [5]. However the one who made CCD work as an imager and first demonstrated it was Michael Francis Tompsett, who is also the sole owner of patent "Charge Transfer Imaging Devices" [6] (US Patent No. 4,085,456). The lack of credit to Tompsett for his contribution is one of the controversies of this field as explained during the 2013 International Image Sensor Workshop, in Snowbird-Utah-USA.

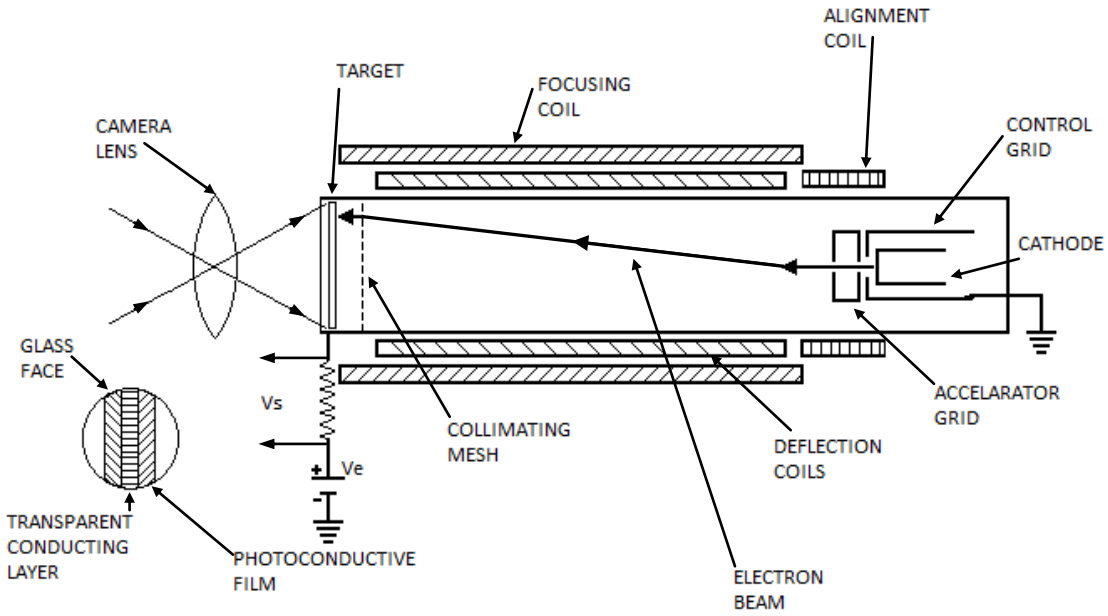
Previously to the solid-state imaging era, image capture was performed by video camera tubes or pickup tubes. Several types of pickup tubes were in use from the 1930s to the 1980s, different versions of such devices include orthicon, vidicon, plumbicon, saticon, trinicon [7]. The vidicon tube, presented in Fig. 1.1(a), was developed during the 1950s at RCA by P. K. Weimer, S. V. Forgue and R. R. Goodrich [7].

The vidicon camera tube works as follows: the target material that is a photoconductive layer is first exposed to radiation coming through the lens from the scene being captured. The various regions of the photoconductive surface have their resistivity changed from a very high resistance to a lower resistance, through charge accumulation, that is proportional to the light intensity reaching a specific region of this surface. After being

exposed to the scene the photoconductive surface is scanned by a beam of low-velocity electrons, which when reaching each specific region of this surface produces a voltage output, Vs on the schematic Fig. 1.1(b), that is proportional to the light intensity to which that region was exposed. The voltage output of each region is then read out and stored to form the image. The charge accumulated on the conductive surface remains until it is scanned by the beam of electrons or until enough time is elapsed for the charge to be completely dissipated from the surface, then the surface is ready for the next capture [8]. It is worth commenting that it is possible to produce a vidicon sensitive over a broad range of the infrared spectrum by using pyroelectric photocathodes [8].

CCD technology matured during the 1970s and from the earlier 1980s to the beginning of the 2000s it was the dominant image-sensor technology [4]. The way for a new generation of silicon image sensors was paved when complementary metal-oxide-semiconductor (CMOS) fabrication process became well established by the early 1990s. This marked a rebirth for MOS image sensors [4].

(a)



(b)

Figure 1.1- (a) Vidicon tube, presented in [8], (b) schematic of Vidicon tube, based on the schematic presented in [8].

Innovations in design and improvements in fabrication technology have led, over the past 15 years, to the increasing adoption of CMOS image sensing technology in several high-volume products, such as optical mice, PC cameras, mobile phones, PDAs, smartphones, tablets, and high-end digital cameras, making them a viable alternative to CCDs [9, 10].

Moreover, the ability to integrate sensing with analog and digital processing circuitry, down to the pixel level, paves the way for new types of CMOS imaging devices for several applications, such as: man-machine interface, surveillance and monitoring, machine vision, and biological testing, among others [9].

1.1 General Overview of CMOS Image Sensor Operation

A CMOS image sensor is an imaging device where the sensing element is an array of pixels, the structure of which is conceptually similar to that shown in Fig. 1.2. In this array, each cell, or pixel sensor, is composed by a photosensor component, such as a photodiode, an in-pixel control circuit, and interconnection lines.

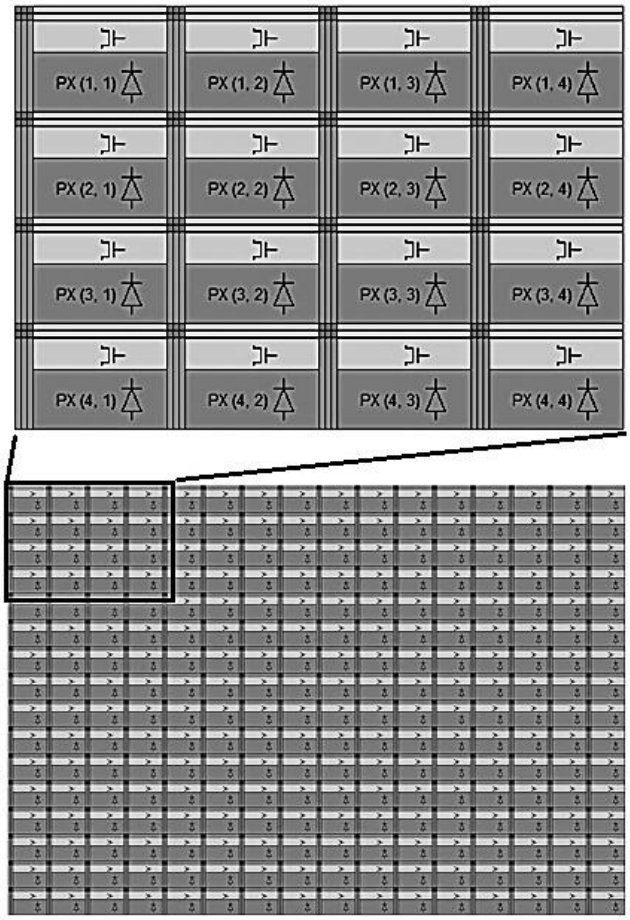


Figure 1.2- Example of an array of pixels [art prepared by the author].

The photosensor, indicated by the symbol of a diode, is the portion of the cell responsible for detecting the light intensity level reaching that particular position in the imaging array. The control circuit, indicated by the symbol of an NMOS transistor, is the

portion of the pixel containing all the electronic components, which execute all the control functions over the pixel sensor, such as enabling the readout of its photosensor response to the light intensity level. The interconnection lines, indicated by horizontal and vertical stripes, are buses through which the electronic control signals and the response of the photosensor are transported into and out of the pixel.

The general electrical schematic of a CMOS pixel sensor is shown in Fig. 1.3(a) and (b). The pixel can be divided into two basic parts, the photosensor element and the control circuit, besides the interconnection lines. The photosensor element, usually a photodiode, can be electrically regarded basically as a dark current source "Idk", a photocurrent source "Iph", and a junction capacitance "Cj". The dark current "Idk" is but the reverse current bias of the PN junction. The photocurrent "Iph" is the current generated by the photons reaching the depletion region of the PN junction. In the absence of a light source, when the pixel is under dark condition, only the dark current will be present, as illustrated in Fig. 1.3(a), otherwise the photocurrent is also present as in Fig. 1.3(b). The junction capacitance "Cj" is the capacitance of the depletion region of the PN junction. The junction capacitance plays a very important role that is storing charge that will be consumed, or recombined, by the charge carriers generated by the photons that reach the depletion region of the PN junction. The dashed diode symbol PD present in the circuit model indicates the position of the photodiode there, however, it is not part of the circuit.

The photons reaching the depletion region of the PN junction generate pairs of charge carriers, electrons and holes. After generation, each pair is separated by the built-in electrical field of the PN junction. Finally the generated carriers are recombined, or consumed, by the charges stored in the capacitance "Cj". The photocurrent "Iph" is dependent on the number of photons reaching the PN depletion region and therefore of the light intensity level.

The illuminated photodiode area shown in Fig. 1.3(c) illustrates the light flux Φ_L, given in lumen, coming from the light source through the cone into the base of which the photodiode lies. The light flux through the surface S is the same reaching the outer surface of the photodiode. The amount of light incident on the surface of the photodiode can be given either in irradiance or in illuminance units. Irradiance is power of light incident on a surface, also called radiant flux density, measured in watt per square meter (W/m^2). Illuminance is the luminous flux incident on a surface, measured in lux. The lux is one lumen per square meter (lm/m^2). The wavelength of 555 nm, green, is the peak of the photopic luminous efficiency function and was chosen by the Commission International d'Eclerage – CIE as the reference for the lumen. By definition, at 555 nm there is 683 lm/W and therefore 1 lux is 0.00146413 W/m^2.

The control circuit performs basic electronic functions of the pixel sensor. There is a great number of electronic functions that can be implemented by the control circuit, but usually only a few basic functions are implemented. Resetting the pixel sensor to an initial state, and reading out its photo-response are among the most commonly implemented functions. The reset and readout functions are indicated by the switch RS and the buffer symbol, respectively, in Fig. 1.3(a) and (b).

A complete image frame is composed by the output response of all the pixels of the array. The output response of each single pixel of the array, according to the illumination level, is determined at the end of its operation cycle. The operation cycle of a CMOS pixel sensor can be didactically divided into six different phases as shown in Fig. 1.4.

The six phases of the operation cycle are performed under the same light intensity level, as illustrated in Fig. 1.4. The first phase is the last state of the pixel before the beginning of the present operation cycle. The second phase is the beginning of the reset period, in which the pixel is set to an initial state, this phase takes place at the very beginning of every operation cycle. During the second phase the junction capacitance "Cj" begins to be refilled with charge carriers.

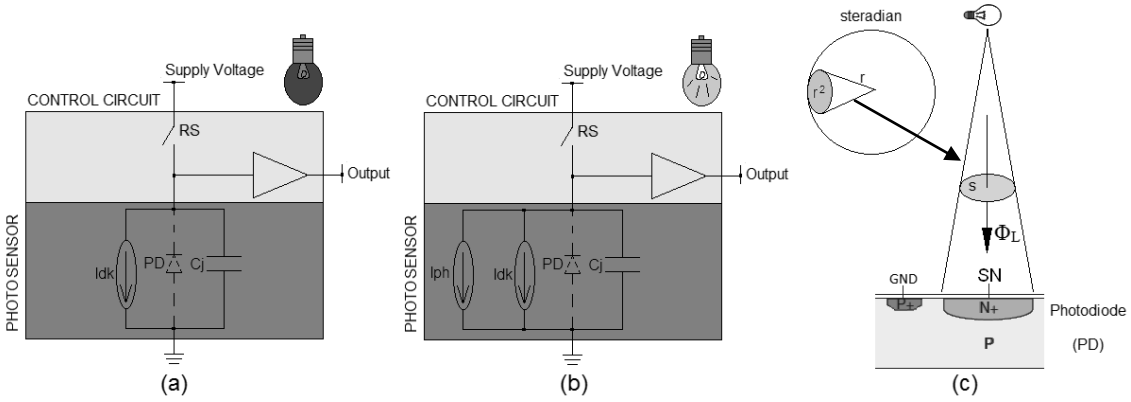


Figure 1.3- General pixel sensor electrical schematic, the dashed diode symbol PD is not part of the model [art prepared by the author].

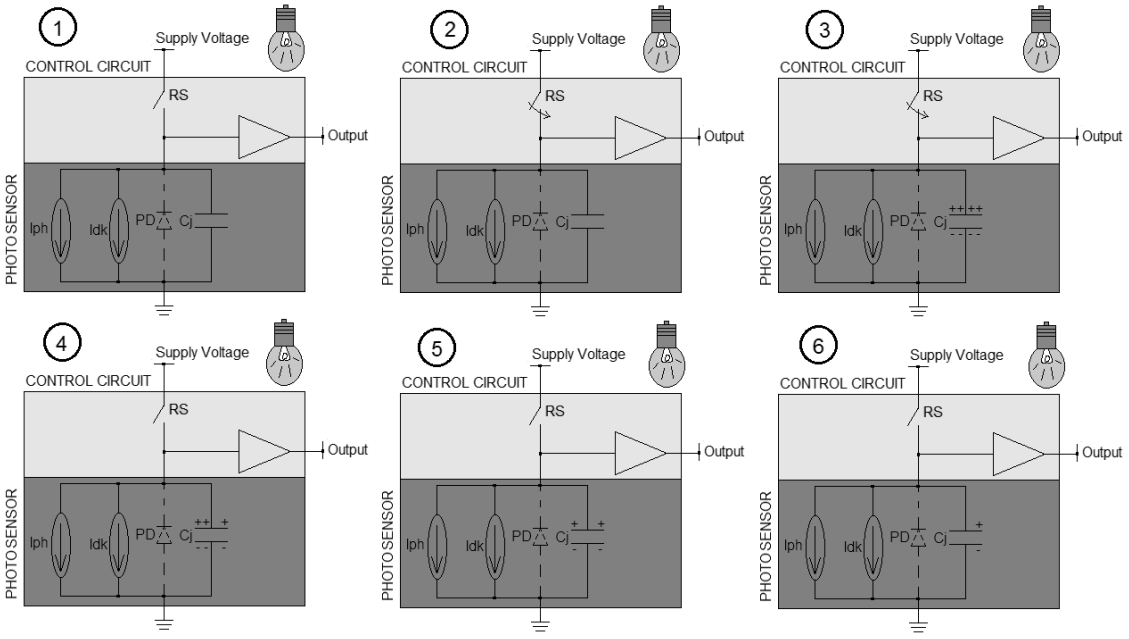


Figure 1.4- CMOS pixel sensor operating phases, the dashed diode symbol PD is not part of the model [art prepared by the author].

The third phase is the end of the reset of the pixel, when the capacitance "Cj" reaches the highest stored charge level. The fourth phase is the beginning the of the exposure time,

when the pixel is exposed to the light reaching its specific position in the array. During the exposure time, the pair of charge carriers generated by the photons reaching the depletion region are consumed by the charge stored in "Cj". The fifth phase is the readout phase, during which the light intensity information is retrieved from the photosensor as electrical signal information and then converted to a digital word representing the light intensity level. The sixth and last phase is but the end of the exposure time, which coincides with the end of the current operation cycle.

The light output information is translated and treated either as voltage or current signal. Along this work the output signal will be treated as voltage output signal, similar to that shown in Fig. 1.5. The output signal in Fig. 1.5 presents all the phases of the operation cycle of the CMOS pixel sensor. For the sake of simplicity it is convenient to divide the operation cycle into three different periods: the reset time, the exposure time, and the sampling time.

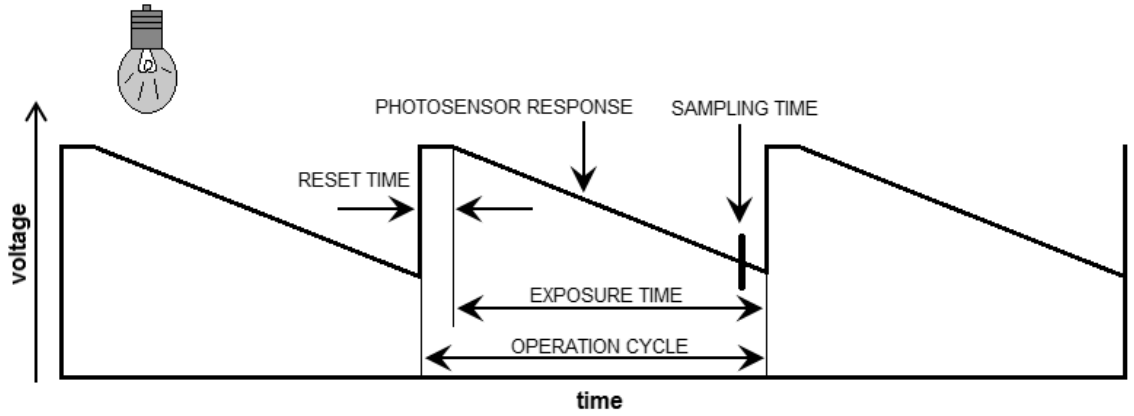


Figure 1.5- Pixel sensor operation cycle [art prepared by the author].

The reset time is the period of time in which the photosensor has its initial state reestablished. This is done at the beginning of each operation cycle. The exposure time is the period of time during which the photosensor is exposed to the light reaching the pixel. The exposure time is commonly known as the integration time, due to the integration like behavior of charges inside the capacitor "Cj" during this period of time. The sampling time, preformed just before the end of the exposure time, is the period of time during which the photosensor response is sampled and registered.

The number of photons reaching the depletion region of the PN junction is dependent on the light intensity. Therefore, the pixel output response is also dependent on the light intensity, as illustrated in Fig. 1.6. In the case where no light is reaching the pixel, the capacitance "Cj" discharges very slowly by the effect of the PN junction dark current, producing the output response as that indicated by the label "1" in Fig. 1.6. If the pixel is exposed to low light intensity, the capacitance "Cj" discharges slowly, yet in a higher rate than that in the previous situation, producing the output response as that indicated by the label "2" in Fig. 1.6. If the light intensity increases, the capacitance "Cj" discharges faster, producing output responses as those indicated by the labels "3" and "4" in Fig. 1.6.

The amount of photocurrent generated inside the photodiode depends mainly upon the properties of the material which the sensor is made of, such as bandgap, quantum

efficiency, concentration of dopants, junction depth, temperature, etc, and also upon the incident radiation wavelength. The ability of a photodetector in converting radiation into electrical signal as photocurrent is also known as responsivity that is given as R = η(λ/1.23985) A/W. Where η is the quantum efficiency of the material and λ is the wavelength of the incident radiation. For example for the wavelength of 555 nm the typical responsivity of a silicon photodiode is about 0.37 A/W. Using these data and cross-multiplication for a photodiode of 12 μm², the irradiance can be determined as a function of the photocurrent (I_{PH}): irradiance = (I_{PH}/(0.37x12))x10¹² W/m². As mentioned above, irradiance can be converted to illuminance given in lux by the following relationship: at 555 nm, 1 lux is 0.00146413 W/m². Therefore for a pixel with this area a small photocurrent of 1 fA is produced when the pixel is subject to an illuminace of 154 mlux, while a large photocurrent of 10 μA is produced when the pixel is subject to an illuminace 1.538 Glux. Concerning the higher limit of 1.538 Glux, an example of such high equivalent illuminance condition can be produced by a 555nm laser with 2mm diameter spot using 7.1W. Some examples of environmental illuminance levels are given below:

- Sun light (outdoors): 100 klux
- Clear sky: 10 klux
- Cloudy sky: 1 klux
- Surgery environments: 10 klux - 20 klux
- Well illuminated rooms: 300 - 500 lux
- Good visibility: 100 lux
- Moon light in a clear sky: 500 mlux
- Cloudy night: 100 μlux

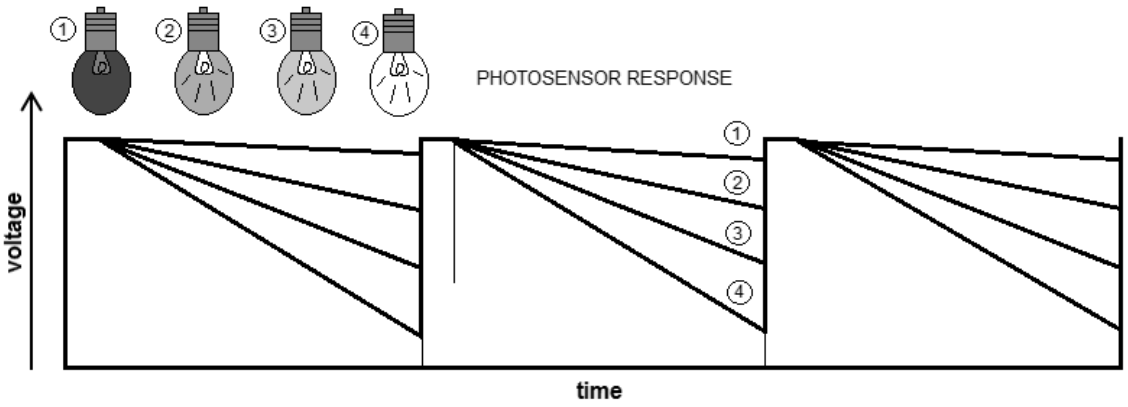


Figure 1.6- Photo-response light dependence [art prepared by the author].

The area of the photodiode designed for experimental verification in this work is 61 μm², therefore, using the rule above, the photocurrent of 1 fA is produced when the pixel is subject to an illuminace of 30 mlux and the photocurrent of 20 μA is produced when the pixel is subject to an illuminace 605 Mlux.

For comparison, the ABNT rule (NBR5413) establishes that for environments for meticulous work, as surgeries, the illuminance must be between 10 klux and 20 klux. The luminous flux of an incandescent light bulb is of 864 lm while that of sodium-vapor lamp is of 90,000 lm. If these fluxes were irradiated through a spherical cap with the same area of the designed pixel, that is 61 μm², the illuminance would be of 14.2 Tlux and 1,474.3 Tlux

respectively. In the literature the experimental range of illuminance for the pixel with the widest dynamic range found, that is of 207 dB [12], is from 9 mlux to about 0.5 Glux.

1.2 General CMOS Pixel Sensor Architectures

The simplest CMOS image sensor cell is the passive pixel sensor (PPS). This pixel sensor is composed of a photodiode and an NMOS transistor, which is employed as a switch for row selection. This pixel architecture is shown in Fig. 1.7. In the imager array built with this pixel architecture, all the pixels in a same column share the same column bus and readout circuitry.

The operation cycle of this pixel begins with the reset time, when both the pixel row selection transistor and the column reset transistor, in Fig. 1.7, are turned on. This happens when both RS and Reset signals, in Fig. 1.7, are at high level. The voltage level of Vref determines the reset charge of the capacitor "Cj". During the exposure or integration time, the pixel row selection transistor must be turned off. The readout operation is performed at the end of integration time by turning on the pixel row selection transistor, while keeping the column reset transistor off. The readout operation of the array is performed one row at a time and before starting the next row readout the column amplifiers and the present row photodiodes are reset [9].

As the PPS cell circuitry requires a single NMOS transistor, the pixel size can be kept as small as possible with a reasonable fill factor. The fill factor of a pixel sensor is its percentage of light-sensitive area [9]. In Fig. 1.7 the fill factor of the conceptual planar pixel structure is the ratio of the gray area indicated by the diode symbol per the pixel total area. The high fill factor is the main advantage of this CMOS pixel architecture. Nonetheless, the column readout is slow and prone to noise disturbances, which jeopardizes its performance and represents its main weakness.

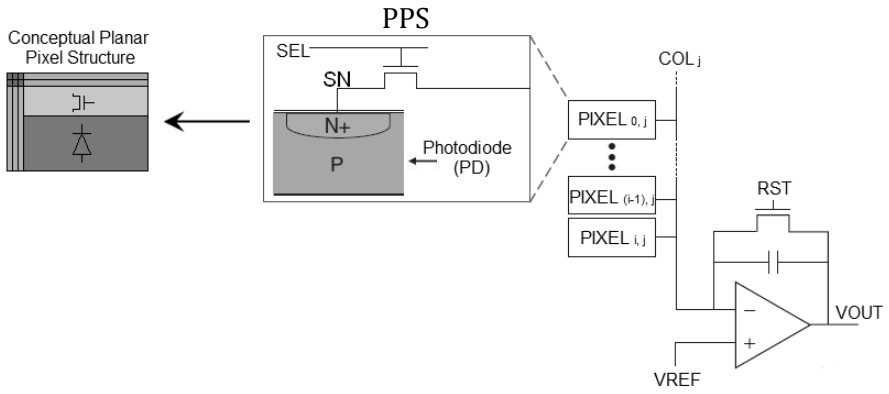


Figure 1.7- Passive pixel sensor (PPS), based on Fig. 10 of [9].

In the early 1990s it was realized that a pixel architecture conceived in 1968 [1] could greatly reduce the main problems of the PPS architecture. This architecture became well known as active pixel sensor (APS) [10].

Since then, APS became the ruling choice in CMOS image sensors. The most common APS circuits feature either three FETs with conventional photodiode (3T APS) or four FETs

with pinned photodiode (4T APS-PPD), as shown in Fig. 1.8. The suffix PPD will be employed to make reference to the 4T APS with pinned photodiode, along the text when the suffix PPD is not present that means a 4T APS with conventional photodiode. In the 3T APS the reset transistor is used to reset the capacitance "Cj" of the pixel photodiode during the reset period. The source follower transistor is employed to decouple the sense node from the large column-bus capacitance. Finally a row-select transistor that connects the source follower output to the column current load. The readout operation of the array is performed at the end of the integration time of each pixel, one row at a time, and then each row of pixel is reset [9].

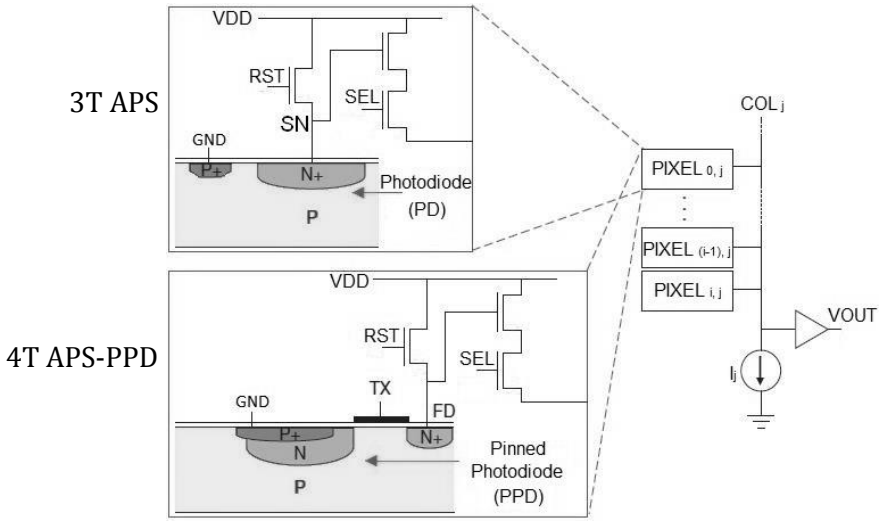


Figure 1.8- schematic of a 3T APS and 4T APS-PPD, based on Fig. 5 of [9].

The 4T APS-PPD employs a pinned photodiode and adds a transfer gate and a floating diffusion (FD) node to the basic 3T APS architecture [9]. Others 4T APS architectures employ a photogate [10] or even a conventional photodiode as will be seen along this text. The charge in the pinned photodiode is transferred via the TX transistor to the FD node at the end of the integration time. Then the charge in the FD node is read out as voltage in the same manner as in the 3T APS architecture.

Moreover, the pixel readout in CMOS APS circuits is a non-destructive process, that is the photodetector charge is not completely drained by the readout circuitry as in as in CCD and PPS imagers [9].

More complex CMOS pixel sensor architectures, usually called diagram pixel sensor (DPS) Fig. 1.9, can be developed by using the ability of CMOS technology to integrate sensing, analog-to-digital (A/D) conversion, and memory altogether locally in the pixel. Better scaling with CMOS technology, and local implementation of techniques to enhance image are some interesting features of DPS. However these additional features are implemented at the cost of a reduced fill-factor [9]. The reduction of the pixel fill factor introduces severe drawbacks in the imager, as will be discussed latter.

There are basically two ways to operate APSs, namely linear mode and logarithmic-compressed response (LCR) mode. The LCR mode is better known as logarithmic mode. The first is the most common way to use the APS circuit and has the main advantage of high sensitivity but a limited dynamic range (DR). The sensitivity of the image sensor

quantifies its ability to react to small changes in light intensity. The DR of an image sensor is defined as the ratio between the largest non-saturating input signal to the lowest detectable signal. The pixel DR quantifies its ability to accommodate an image to both irradiance extremes, i.e. high and low illuminated pixels [11].

CMOS active pixel sensors operating in linear mode have a DR around 40-60 dB while that of CCDs is around 60-70 dB. The DR of the human eye is greater than 90 dB, close to a natural scene that exhibits a DR often greater than 100 dB [9]. There are many ways to extend the DR in CMOS image sensors including the logarithmic mode of operation and different types of linear-logarithmic combinations that usually operates between 100-140 dB [12]. Some techniques are reported even to achieve DR above 200 dB [12].

It is very important to keep in mind that though it is possible for an image sensor to achieve such high DR. There are several other parameters that must be taken into account when evaluating the image sensor performance and comparing it with the human eye system. The main parameters to evaluate the performance of an imaging sensor system include sensitivity, dynamic range, signal-to-noise-and-distortion ratio, dark limit, power consumption, visual field, spatial resolution, and temporal resolution [13]. In this work only the three first parameters mentioned above are considered.

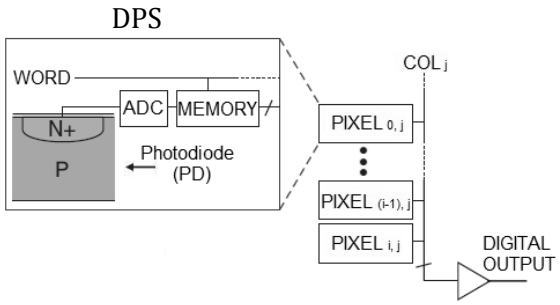


Figure 1.9- Schematic of a diagram pixel sensor (DPS), based on Fig. 11 of [9].

CMOS image sensors, however, suffer from several problems that may heavily limit their performance. In designing CMOS image sensors some trade-offs are fundamental and physical, while others are related to non-idealities in the silicon itself or introduced in the fabrication. A primary focus in CMOS technology is to overcome image artifacts that arise in extreme situations, or are related to certain operation and illumination conditions [14].

Fixed-pattern noise (FPN) is among those non-idealities that produce pixel-to-pixel output variation under uniform illumination. These non-idealities are caused by device and interconnection mismatches across the image-sensor array introduced during the fabrication process. The magnitude of such non-idealities is related to the process tolerance variation specified by each foundry. FPN is composed of two components: offset and gain, which are visible especially at low illumination. Offset FPN is usually more critical than gain FPN [9], [11] and [14]. The offset FPN is the portion of the total FPN that is independent of the light signal. It is caused by the devices and interconnection mismatches and by the variations of the dark current. The offset component of the FPN is commonly referred to as dark signal non-uniformity (DSNU). The gain FPN is the portion of the total FPN that depends on the light signal on the pixel, commonly known as photo-response non-uniformity (PRNU).

Due to active readout circuitry, CMOS image sensors present more sources of FPN than CCDs. The column FPN produced by the column amplifier is the most serious additional source of FPN in CMOS compared to CCD image sensors [11], [12] and [15]. This kind of FPN appears as vertical stripes in the image [15] as shown in Fig. 1.10.

Treatment of image artifacts must be performed in both light extreme situations. Circuit techniques are employed to treat image artifacts in the APS operating in linear mode. Among these circuit techniques are the correlated double sampling (CDS) and the delta reset sampling (DRS) [9]. Other techniques to treat image artifacts can be implemented in diagram pixel sensor (DPS) architectures. However, the use of DPS architectures increases the number of transistors in the pixel, thus reducing its fill factor.

As mentioned before, a great number of relevant features that enhance image quality can be locally implemented by DPS architectures, such as global shutter and CDS [14]. But reducing the pixel fill factor brings other drawbacks up, including lowering pixel extrinsic quantum efficiency and signal-to-noise ratio (SNR). The pixel extrinsic quantum efficiency is the amount of light captured by the pixel converted into electrical signal.

The reduction of fill factor in diagram pixel sensor architectures also reduces the pixel charge storage capacity (Q_{sat}), which increases susceptibility to photon shot noise. In the shot noise limit the SNR scales with the square root of the captured photon signal [14]. This affects applications such as discrimination between shades of gray in a bright image, which is limited by the photon shot noise and not by the absolute noise floor [14]. Low fill factor also increases susceptibility to image blooming and parasitic image artifacts such as dots, lines, and other shapes [14]. Moreover, increasing the number of transistors in a pixel can negatively increase the noise floor of the sensor that is important in light starved applications [14].

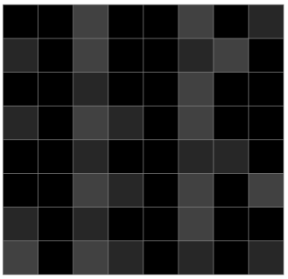


Figure 1.10- Artifacts introduced by FPN [art prepared by the author].

Classical strategies as correlated-double-sampling (CDS) or delta-reset-sampling (DRS) cannot be applied to attenuate FPN in the APS operating in logarithmic mode, because their application in this mode basically annuls the contribution light signal. Therefore other techniques may be applied, including storing the pixel offsets [11], multi-mode readout APS [12], multi-mode logarithmic APS [15], current reference for on-pixel compensation [17], double-logarithmic compression plus discharge transistor for on-pixel compensation [18], and charge injection into the photodiode [19]. Storing pixel offset can be applied to the basic 3T APS, nevertheless it requires additional external hardware to store the FPN information of each pixel of the array. All other techniques require more complex pixel structures than that of the 3T APS, yielding therefore lower fill factor.

1.3 Active Pixel Sensor – Linear Mode

The classical way to operate an active pixel sensor (APS), shown in Fig. 1.11, is the linear mode. In this mode of operation when the RST signal is switched from the ground level to the V_{DD} level, during reset time (t_{rst}), the reset transistor M_1 is turned on, and the junction capacitance of the photodiode is reset to its highest charge level. When the RST signal is switched from V_{DD} to the ground level, the integration time (t_{int}) begins. During the integration time, the junction capacitance of the photodiode will be discharged at a rate that depends on the light intensity level at which the pixel is subject. The voltage at the sense node, SN in Fig. 1.11, and at the output node will be modeled next.

At the end of the reset time and at the beginning of integration time, the voltage between the terminals of the reset transistor M_1, in Fig. 1.11, and on the sense node is shown in Eq. (1.1). In Eq. (1.1) $V_{GS,1}$ is the voltage between the gate and source terminal of M_1, $V_{DS,1}$ is the voltage between the drain and source terminal of M_1, V_{TH} is the threshold voltage of M_1, and V_{SN} is the voltage at the sense node of the pixel. The index "0" means the beginning of integration time, or the value at the end of reset time.

During the integration time the same net voltage, described by Eq. (1.1), can be rewritten as shown in Eq. (1.2), where Q is the charge flowing through the photodiode that can be written as in Eq. (1.3). In this equation I_{PH} stands for the photocurrent, I_{DARK} stands for the dark current, t_{int} is the integration time, $C_{ol,1}$ is the reset-transistor, M_1, overlap capacitance between its gate and source terminals. The overlap capacitance of M_1 is the capacitance in the region where the gate oxide overlaps the source diffusion of this NMOS transistor. In the same equation the "feed-through" charge term when M_1 is turned off is indicated by $C_{ol,1}V_{DD}$, and C_D is the capacitance at the sense node SN [15]. The SN voltage at the end of integration time t_{int} can be written as shown in Eq. (1.4).

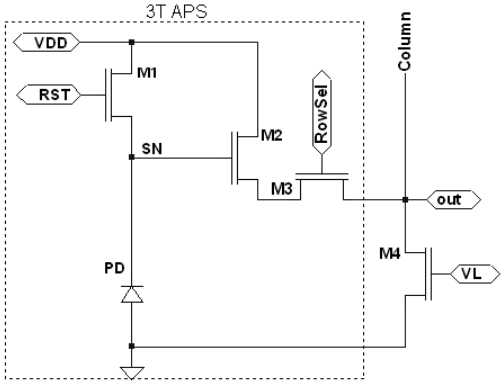


Figure 1.11- Schematic of the basic 3T APS, based on Fig. 6.1 of [15].

$$V_{GS,1}(0)=V_{DS,1}(0)=V_{DD}-V_{SN}(0)=V_{TH,1} \tag{1.1}$$

$$V_{DS,1}(t)=V_{DD}-V_{SN}(t)=V_{DS,1}(0)+\frac{Q}{C_D} \tag{1.2}$$

$$Q=\left(I_{PH}+I_{DARK}\right)t_{\text{int}}+C_{ol,1}V_{DD} \tag{1.3}$$

$$V_{SN} = V_{DD} - V_{TH,1} - \frac{\left(I_{PH} + I_{DARK}\right) t_{\text{int}} + C_{ol,1} V_{DD}}{C_D} \tag{1.4}$$

The output voltage at the end of integration time t_{int} can be written as shown in Eq. (1.5). When the reset transistor is in the saturation, that is $V_{DS,2} \geq V_{DS\_SAT,2}$, $V_{DS,2}$ can be written as in Eq. (1.6). In this equation α is the adjusting parameter of the MOS channel current model SPICE LEVEL 3 [50], if $\alpha = 1$ then it becomes SPICE LEVEL 1. The channel current model for the reset transistor is shown in Eq. (1.7), λ is the inverse of the Early-effect voltage, also known as the channel modulation parameter. The β_2 parameter is shown in Eq. (1.8), where μ_n is the electron mobility in the channel of M_2 and C_{OX} is the oxide capacitance.

$$V_{OUT} = V_{DD} - V_{DS,2} - V_{DS,3} \tag{1.5}$$

$$V_{DS\_SAT,2} = \frac{V_{GS,2} - V_{TH,2}}{\alpha} \tag{1.6}$$

$$I_{DS,4} = I_{DS,2} = \beta_2 \frac{\left(V_{GS,2} - V_{TH,2}\right)^2}{2\alpha}\left(1 + \lambda.\left(V_{DS,2} - V_{DS\_SAT,2}\right)\right) \tag{1.7}$$

$$\beta_2 = \mu_n C_{OX} \frac{W_2}{L_2} \tag{1.8}$$

Now assuming that $\lambda\left(V_{DS,2} - V_{DS,2}^{'}\right) << 1$, then the current in the reset transistor can be rewritten as shown in Eq. (1.9), therefore $V_{GS,2}$ becomes as written in Eq. (1.10). With the voltage net shown in Eq. (1.11), the output voltage can be written as in Eq. (1.12). If the row select transistor M_3 is treated as an ideal switch then $r_{ON\_DS,3} \approx 0$ and the output voltage can be estimated by Eq. (1.13).

$$I_{DS,4} = I_{DS,2} = \beta_2 \frac{\left(V_{GS,2} - V_{TH,2}\right)^2}{2\alpha} \tag{1.9}$$

$$V_{GS,2} = \sqrt{\frac{2 I_{DS,4} \alpha}{\beta_2}} + V_{TH,2} \tag{1.10}$$

$$V_{SN} = V_{GS,2} + V_{DS,3} + V_{OUT} \Leftrightarrow V_{OUT} = V_{SN} - V_{GS,2} - V_{DS,3} \tag{1.11}$$

$$V_{OUT} = V_{SN} - \left(\sqrt{\frac{2 I_{DS,4} \alpha}{\beta_2}} + V_{TH,2}\right) - r_{ON\_DS,3} I_{DS,4} \tag{1.12}$$

$$V_{OUT} = V_{SN} - \left(\sqrt{\frac{2 I_{DS,4} \alpha}{\beta_2}} + V_{TH,2}\right) \tag{1.13}$$

Example of Linear Mode Simulation:

The linear mode operation presented next is the result of BSIM3v3 simulations in a standard 4-metal 2-poly CMOS 0.35 μm technology by Austria Microsystems. In the pixel, such as that in Fig. 1.11, all the transistors M_1, M_2 and M_3, as well as the column current source M_4, have the same dimensions W = 0.70 μm and L = 0.35 μm. The photodiode is an

n^+-diffusion/p-sub diode with total area of 61 μm^2 and perimeter of 38.5 µm. For these dimensions the process parameters yields a junction capacitance of about 61.6 fF and dark current of about 0.055 fA. These values are compliant to those in image sensors designed for CMOS processes with about this feature size [20] and [21].

The control signal setup for the simulation performed with the pixel shown in Fig. 1.11 is the following: the V_{DD} voltage level is set to 3.3 V; the VL voltage level is set to 0.8 V; the RST signal is a pulse with low level set to 0 V, high level set to 3.3 V, time period of 31 ms, pulse width of 1 ms and rise and fall time of 0.1 ns; the RowSel signal may be active only during the output sampling, though in the present simulation this signal was always at V_{DD} level. The photocurrent representing light intensity varies from 0.1 fA in dark condition to 20 µA in a very bright condition. The reset, integration and sampling times as well as the voltage level of the RST and output signals at each instant of time are presented in Fig. 1.12.

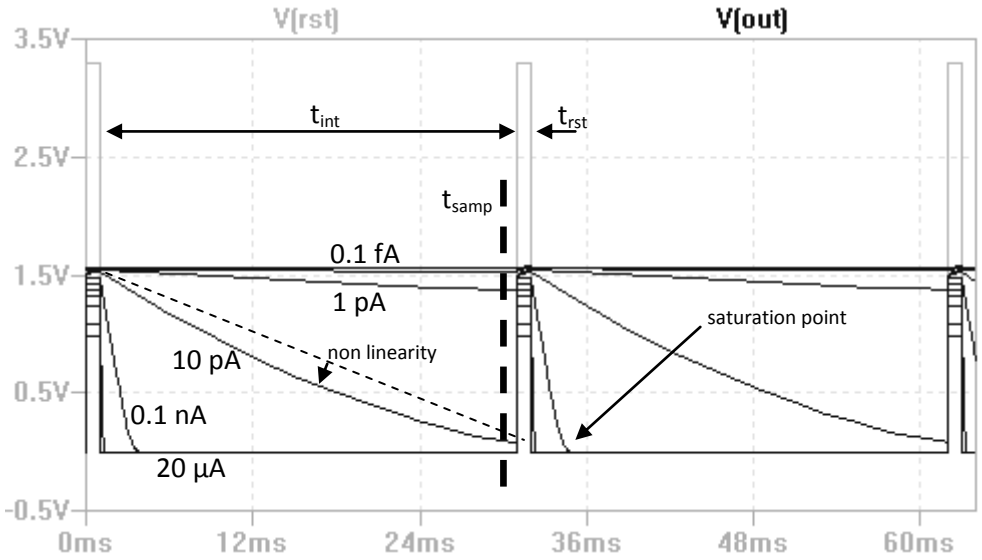


Figure 1.12- Linear mode output voltage [art prepared by the author].

The results presented Fig. 1.12 show that the linearity of each curve depends upon the light intensity and the integration time. It is also shown that the non-linearity increases for those curves produced under high light condition, while under the low light condition the curves are more linear.

The piece of information to be finally collected and processed is the voltage level sampled at the end of the integration time. This information varies according to the light intensity. The light intensity is henceforth treated in terms of its equivalent photocurrent. The higher output voltage level stands for a very low light or dark condition, while the lower voltage level stands for either moderate or high light condition as shown in Fig. 1.13.

The pixel sensitivity, as observed in Fig. 1.13, varies a lot throughout the whole light range intensity. It is very low for low light condition, and then it highly increases in a light level range between the low and moderate light conditions, and finally just after this interval the pixel saturates.

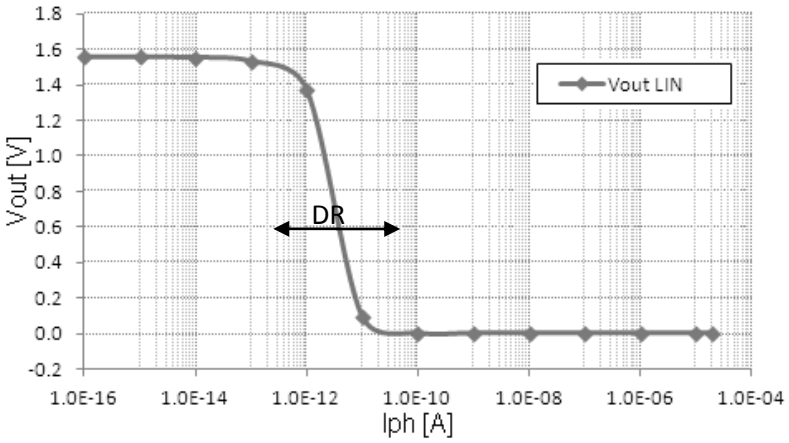


Figure 1.13- Output voltage versus light intensity [art prepared by the author].

The APS high sensitivity operating in linear mode is one of its great advantages. However, toward high light intensity, it saturates for a relatively narrow range of light illumination. Therefore it does not lend itself to applications that deal with irradiances beyond the saturation level, i.e. wide dynamic range applications. Nevertheless, there is a prompt alternative for this weakness, the logarithmic mode, which will be presented next. The DR of the pixel operating in linear mode, shown by the double arrow labeled DR in Fig. 1.13, is around 44 dB.

1.4 Active Pixel Sensor – Logarithmic Mode

For a long time extending the DR of image sensors has been a design concern. The first works reporting techniques to reach high DR with silicon image sensors were those of Chamberlain [22, 23], in the early 1980s. Since then, many derivations of this technique have been applied to CMOS image sensors to extend its DR.

The original idea of Chamberlain to achieve wide dynamic range was connecting the gate of the reset transistor permanently to its source terminal [23], so that it would always operate in the subthreshold region and therefore always yield a logarithmic response. Nowadays, the most common and popular way to achieve a large DR, is by connecting the gate terminal of the reset transistor M_1 permanently to its drain terminal, as shown in Fig. 1.14. This configuration of the 3T APS architecture produces a logarithmic output response with light intensity. It is important pointing that in this configuration M_1 can reach moderate or high inversion region yielding therefore a non-logarithmic response, but still useful. As variations of this configuration may be used in combination with the linear mode, as will be shown later, this is called henceforth the full logarithmic response configuration.

In the full logarithmic mode of operation there is neither reset nor integration time. The reset transistor is always active and when the photodiode is subject to a certain level of light, this transistor supplies the current necessary to compensate for the photocurrent. The pixel photocurrent varies logarithmically with light intensity, as will be shown next.

When the gate terminal of the reset transistor M_1 is connected to V_{DD} for a very long time, or permanently as in Fig. 1.14, it will charge the capacitor of the photodiode up to a

constant voltage. The current flowing through M_1, $I_{DS,1}$, is the same current flowing through the photodiode, I_{PD}, that is composed of two components as shown in Eq. (1.14). The first component is the photocurrent I_{ph} and the second component is the dark current I_{dark} [15]. When the pixel is under dark condition only the dark current is present, otherwise the photocurrent is also present. The current flowing through M_1 can be modeled as in Eq. (1.15), where n is the slope factor (typically between 1 and 2) and v_T is the thermal voltage (kT/q) which is nearly 25 mV at room temperature (300K). The current I_0 is given by Eq. (1.16), where N_{ch} is the channel doping concentration, μ_n is the channel-carrier mobility, ε_{si} is the silicon permittivity and ψ_s is the surface potential, related to the gate voltage, relative to the source, V_{GS} [15].

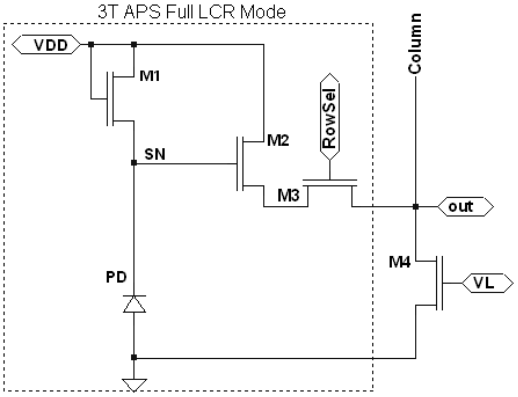


Figure 1.14- 3T APS in full logarithmic mode, based on Fig. 6.3 of [15].

$$I_{DS,1} = I_{PD} = I_{ph} + I_{dark} \tag{1.14}$$

$$I_{DS,1} = I_{PD} = \frac{W_1}{L_1} I_0 e^{\frac{(V_{GS,1} - V_{TH,1})}{n v_T}} e^{\frac{V_{SB,1}}{v_T}\left(\frac{1}{n} - 1\right)} \left(1 - e^{\frac{-V_{DS,1}}{v_T}}\right) \tag{1.15}$$

$$I_0 = \mu_n v_T^2 \sqrt{\frac{q \varepsilon_{Si} N_{CH}}{2 \psi_S}} \tag{1.16}$$

If the condition shown in Eq. (1.17) is satisfied, Eq. (1.15) can be rewritten as in Eq. (1.18), then $V_{GS,1}$ can be defined as in Eq. (1.19). Replacing $V_{GS,1}$ and $V_{SB,1}$ in Eq. (1.19) according to Eqs.(1.20) and (1.21) leads to the V_{SN} expression in Eq. (1.22). The result in Eq. (1.22) shows that V_{SN} varies logarithmically with the photocurrent. If Eq. (1.22) is used to complete V_{OUT} in Eq. (1.13), then it is also shown that the output voltage also varies logarithmically with the photocurrent [16].

$$3\frac{kT}{q} < V_{DS,1} < V_{DD} \Leftrightarrow \left(1 - e^{\frac{-V_{DS,1}}{v_T}}\right) \approx 1 \tag{1.17}$$

$$I_{PD} = \frac{W_1}{L_1} I_0 e^{\frac{(V_{GS,1} - V_{TH,1})}{n v_T}} e^{\frac{V_{SB,1}}{v_T}\left(\frac{1}{n} - 1\right)} \tag{1.18}$$

$$V_{GS,1} = V_{TH,1} + n v_T \ln \frac{I_{PD}}{I_0 (W_1 / L_1)} + V_{SB,1}(n-1) \tag{1.19}$$

$$V_{GS,1} = V_{DD} - V_{SN} \tag{1.20}$$

$$V_{SB,1} = V_{SN} \tag{1.21}$$

$$V_{SN} = \frac{V_{DD} - V_{TH,1}}{n} - v_T \ln \frac{\left(I_{ph} + I_{dark}\right)}{I_0 \left(W_1 / L_1\right)} \tag{1.22}$$

Example of Logarithmic Mode Simulation:

The same pixel circuit employed for the simulations in linear mode is employed here to present the operation in full logarithmic mode. Except for the fact that the reset signal is not necessary, the set of control signals and photocurrent variation are also the same employed for the simulations for the linear mode. The APS output signal, the sampling time, and the time instant when V_{DD} is turned on are shown in Fig. 1.15.

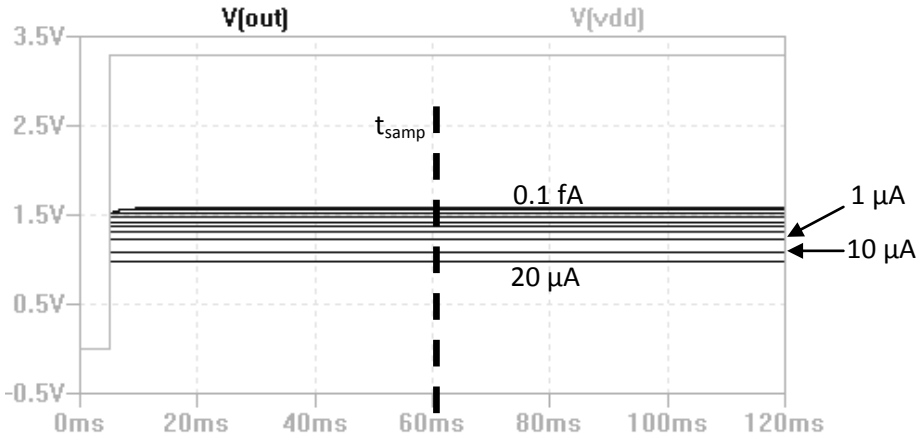


Figure 1.15- Full logarithmic mode output voltage [art prepared by the author].

As in the linear mode the piece of information to be collected and processed is the voltage level, sampled at a specific sampling time as shown in Fig. 1.15. This information varies logarithmically with light, i.e. with its equivalent photocurrent intensity. The higher output voltage level stands for a very low light or dark condition, while the lower voltage level stands for a very high light condition as shown in Fig. 1.16.

The pixel sensitivity, as observed in Fig. 1.16, also varies throughout the whole light range intensity. As in the linear mode the sensitivity is also very low for low light condition, then it smoothly changes to logarithmic response between moderate and high light condition. The simulation results show that at very high light condition the sensitivity increases yet more, but the output does not saturate as in the linear mode. At very high light condition the photocurrent, that is, the reset transistor drain current, increases beyond the logarithmic region where higher order effects begin to take place and the curve slopes steeper. The DR of the pixel operating in logarithmic mode, shown by the double arrow labeled DR in Fig. 1.16, is around 160 dB.

The wide dynamic range toward high light condition is one of the great advantages of the APS operating in logarithmic mode. Nevertheless, it has poor sensitivity at low light condition and it is also a very slow sensor, especially at moderate and low light condition. In the range of moderate and low light condition the sensor yields a low frame rate, because in this range the sense node voltage V_{SN} takes a quite long time to become steady.

This effect will be discussed later. The slow response of this sensor, operating in logarithmic mode, results in image lag, especially in applications where high frame rates are required. Image lag is the result of sampling the signal between consecutive frames before it is given enough time to reach steady state in each frame.

The linear and full logarithmic mode responses for the 3T APS are shown together in Fig. 1.17. Comparing the two voltage curves, it is evident that the sensitivity of the pixel operation in linear mode is much larger than that of the logarithmic mode, especially in the region of moderate light intensity. On the other hand, the DR of the sensor operating in linear mode is much narrower than that of the logarithmic mode, which is especially extended toward high light condition. It is important to highlight that for photocurrents of about 1 μA the logarithmic model for the reset transistor is no longer valid anymore, however the output response is still useful. Despite this fact, for such high photocurrents, this mode will still be called logarithmic mode.

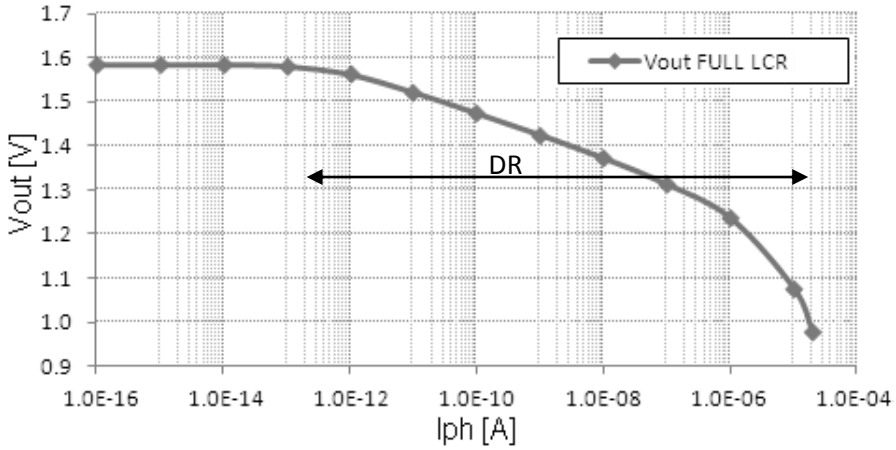


Figure 1.16- Output voltage versus light intensity [art prepared by the author].

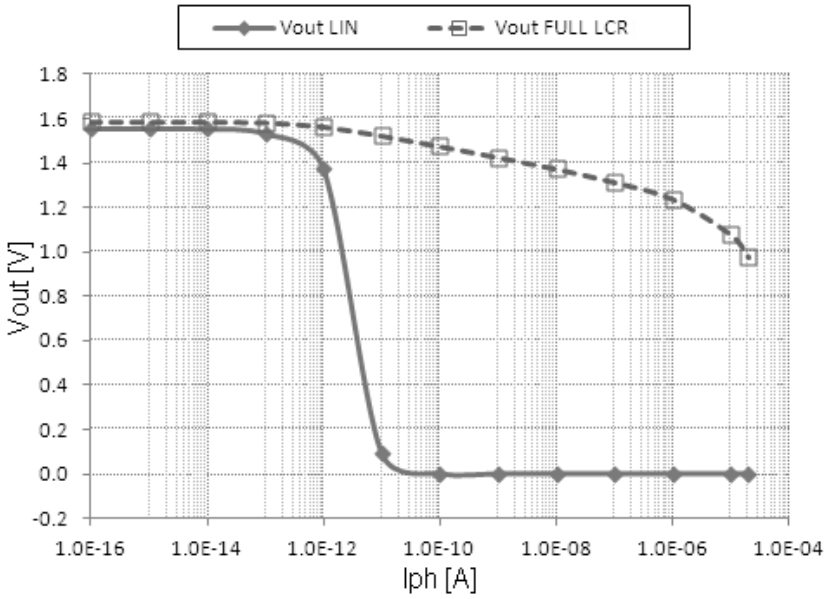


Figure 1.17- Output voltage versus light intensity, linear and logarithmic modes [art prepared by the author].

1.5 General Overview of This Text

In this work it is presented an improved way to combine the linear and logarithmic modes in the 3T APS. The presented solution makes use of the large DR of the logarithmic mode, while keeping the good sensitivity of the linear mode. The proposed solution enables the application of a new way to reduce FPN in the basic 3T APS operating either in proposed combined linear-logarithmic mode or in the pure logarithmic mode. Besides providing a 3T APS with enhanced image quality, the proposed solution also suppresses image lag and do not reduce the pixel fill factor.

As in the CDS and DRS strategies, the presented methods to attenuate FPN are also based on double sampling readout subtraction (DSRS). Such method consists in sampling the output twice and subtracting one sample from the other to suppress FPN components present in both samples. The same circuits employed to perform CDS or DRS can be employed with the proposed methods, therefore external circuitry complexities are avoided. Moreover the proposed techniques are performed at circuit level and not at software level, as in the case of flat field compensation, allowing thus higher frame rates.

In Chap. II the most important methods to produce wide DR in CMOS image sensors are presented and their advantages and disadvantages are discussed. The fundaments of the linear-logarithmic combination adopted by this work are also explored in this chapter.

The image lag problem is discussed in Chap. III where three methods to suppress such problem are presented. The pseudo-flash reset is a technique primarily devised to suppress image lag in the APS operating in linear mode. In this chapter it is shown that pseudo-flash reset can have its use extended to both linear-logarithmic and pure logarithmic modes of operation.

Fixed-pattern noise analysis through circuit simulations are presented and discussed in Chap. IV. A new way to perform a simple FPN simulation analysis is presented altogether with their results. Standard Monte Carlos simulation analysis is also presented in this chapter, showing the amount of FPN introduced by different transistors of the pixel.

In the literature there are few methods dealing FPN attenuation in combined linear-logarithmic modes. These methods are introduced in Chap. V, section 5.4. The proposed method to attenuate FPN in the chosen linear-logarithmic combination is presented and described in section 5.5. Simulation results showing the effectiveness of the proposed technique, and comparisons with the standard CDS technique applied to the linear mode are presented in the three last sections of Chap. V.

Experimental results asserting the effectiveness of the proposed technique in attenuating FPN in the linear-logarithmic mode are presented in Chap. VI. To this purpose only a small pixel array with eight rows and eight columns was designed. The array was fabricated inside a multi-user integrated circuit in the standard 4-metal 2-poly AMS CMOS 0.35 μm technology.

The main goal of the experiments performed in this work was evaluating the FPN attenuation ability of the proposed technique. For this purpose the fabricated array was tested only under static uniform illuminated fields for different irradiance levels. In this

case as the array is very small and operation speed was not a concern, a basic ARDUINO UNO microcontroller was employed as data acquisition system and to perform the necessary control signal. The FPN attenuation yielded by the proposed technique was verified as expected within the whole irradiance range used to test the array, as shown in section 6.3 of Chap. VI.

The experimental setup was built on a breadboard as presented in section 6.2. As the prototyped imager array and the proposed technique produced the expected results under such non-customized electrical environment, it is expected to work even better on a customized printed circuit board.

Owing to the static nature of the fame captures results presented in Chap. VI and to speed constraints of the ARDUINO UNO microcontroller ADC, the array frame rate was not evaluated in the experimental measurements. And therefore the image lag suppression ability of the proposed technique is not evaluated in the experimental measurements as well.

The main characteristics, together with considerations, and comparisons of the different techniques found in the literature to attenuate FPN in the linear-logarithmic mode are provided in section 6.4. A brief discussion about future works is presented in end of Chap. VI. Finally the main conclusions drawn out of this work are exposed and briefly discussed in the conclusion chapter.

Chapter II: CMOS Active Pixel Sensors with Wide Dynamic Range

The main known strategy to achieve a wide dynamic range is operating the pixel in logarithmic compressed-response mode. The technique was first reported by Chamberlain [22, 23] in the early 1980s, and extensively explored since then. The bases of this technique were presented in the Chap. I.

Besides the full logarithmic mode of operation, many alternative techniques to enlarge the dynamic range of CMOS image sensors are found in the literature. The most important of these techniques include well-capacity adjusting [24]-[26], multiple scene capture [27]-[31], spatial varying exposure [32], time-to-saturation [33]-[35], the local adaptation (artificial retina) [36]-[38], and complementary-mode sensor (multi-mode sensor) [41]-[47].

The complementary-mode sensor (CMS) technique combines the good sensitivity of the pixel operating in linear mode with the wide dynamic range of the logarithmic mode of operation, providing therefore a simple and effective way to extend the dynamic range of APS circuits. Details of this technique will be given later in this chapter.

2.1 Six Important Techniques to Extend Dynamic Range

In this section a short description of six of the most important techniques to extend the dynamic range found in the literature is given. Only the main idea, the features, and problems of these techniques is considered here. The six techniques presented next are the full logarithmic mode, the well-capacity adjusting, the multiple scene capture, the spatial varying exposure, the time-to-saturation, and the local adaptation (artificial retina).

2.1.1 Full Logarithmic Compressed Response

The full logarithmic mode, as described in the previous chapter, works in non-linear mode. The extended dynamic range (DR) is reached with a short signal swing, as shown in Fig. 2.1, which results in quite low signal-to-noise ratio (SNR). The full logarithmic mode has low pixel-level circuitry complexity. However, to make use of the extended dynamic range afforded by the sensor, the external pixel circuitry might be very precise [11]. This mode of operation has also low level of external circuitry complexity.

Compressing the sensor response yields a very low signal swing for low illumination level, but increases logarithmically towards high illumination. Under low illumination, the sensor sensitivity depends upon a good signal-to-noise ratio SNR and a very sensitive ADC conversion. Besides that, in low illumination condition, the settling time to achieve logarithmic steady state may take from hundreds of milliseconds to many seconds [16]. Such slow response results in a very slow frame rate or else a large image lag.

Notwithstanding, this mode is suitable to detect high light intensities in the scene with a reasonable speed.

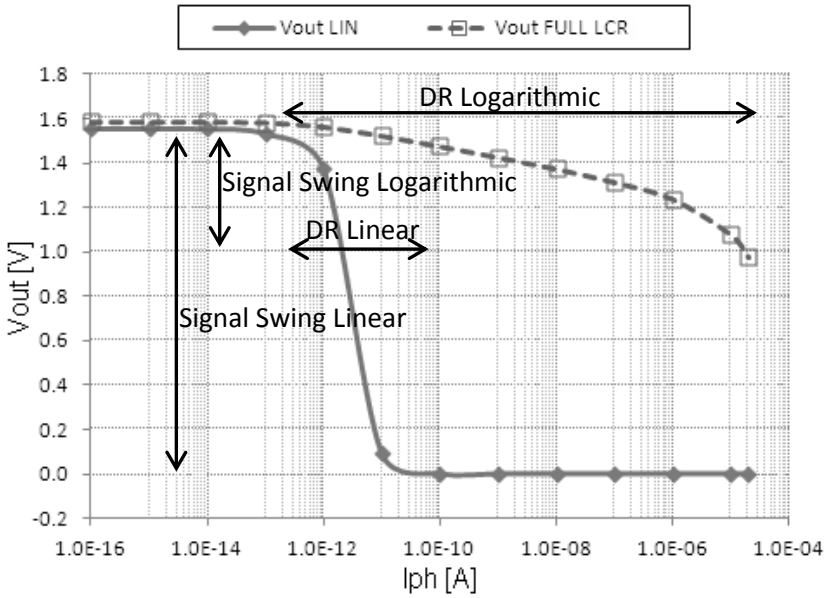


Figure 2.1- Output voltage versus light intensity, linear and logarithmic modes [art prepared by the author].

Due to the non-linear response, classical double-sampling readout subtraction (DSRS) techniques, as correlated double sampling (CDS) or delta reset sampling (DRS), cannot be applied to reduce fixed-pattern noise (FPN). Other techniques can be applied to reduce FPN, but they increase either pixel or external circuitry complexity. The proposed technique to reduce FPN, introduced later in this text, can be employed to solve this problem without increasing either pixel or external circuitry complexity.

This technique has a considerable low response, due to the very long time required to achieve steady state, yielding therefore low frame rates especially at low light conditions.

2.1.2 Well-Capacity Adjusting

The well-capacitance adjusting (WCA) is performed by adjusting the capacitance of the PN junction photodiode. This capacitance varies with the inverse of the square root of the voltage applied on this diode. The adjustment can be done by changing the voltage level of the gate of the reset transistor of the 3T APS, [24]. The technique works by increasing the available well capacitance one or more times during integration time. This technique was first implemented and described by Knight [24] in the early 1980s. In his work Knight pointed that “sensor linearity is not necessarily always desirable” and due to the possibility to extend the dynamic range of the sensor “explicit control over the shape of the output function would be even more desirable”.

The simplest way to implement the technique is applying a reset signal with modulated low level amplitude direct to the reset transistor as did Decker in [26]. In his work Decker used a 4T pixel [26], however his technique can readily be applied to the 3T APS as shown in Fig. 2.2. The technique is implemented by gradually reducing the gate voltage of the reset transistor M_1 during integration time, instead of switching it directly to the ground

level as in the linear mode. The low level of the reset signal can be adjusted one or many times in equal or different steps during the integration time. The trade-off between sensitivity versus DR is directly related to the width, height, and number of steps applied to the reset terminal of M_1.

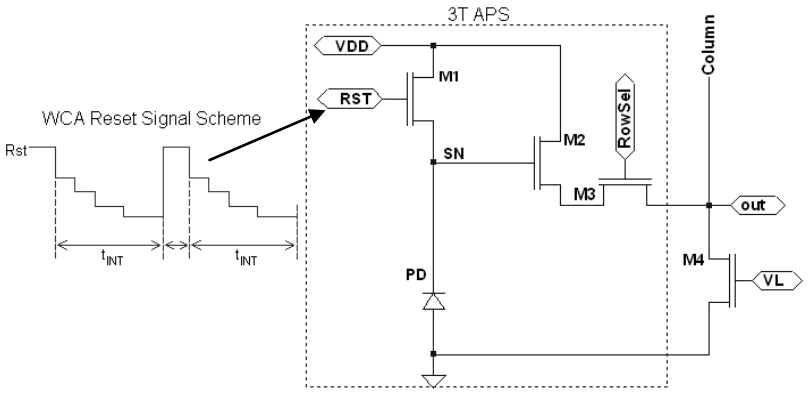


Figure 2.2- Well-capacity adjustment scheme in the 3T APS, based on the illustration of page 29 of [11].

This technique presents low level complexity for either pixel or external circuitry, and the pixel can operate at the rate of the regular linear mode of operation. However, due to the multiple reset switches, additional noise may be introduced.

2.1.3 Multiple Scene Capture

The multiple scene capture (MSC) works exclusively in linear mode and combines images captured with different exposure times, or integration times, to produce the wide DR image. Short integration time is used to capture high light components in the scene, t_{BRIGHT}, while long integration time is used to capture the low light components, t_{DARK}, as shown in Fig. 2.3.

In both cases shown in Fig. 2.3, the end of integration time corresponds to the maximum light intensity that each pixel can process before reaching saturation. Differently from this ideal model, in the simulation results presented in Fig. 1.12, it is noticeable that the non-linearity increases for higher light intensity and that the linearity is higher for low light intensity. This technique usually extends the dynamic range toward high light condition. Nevertheless, some reports claim to extend it also towards low light condition by appropriately averaging the captured images to reduce noise [11, 30].

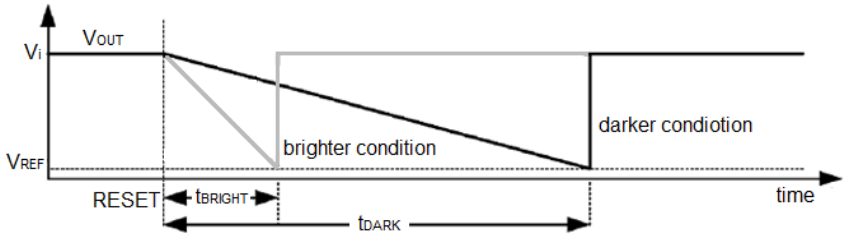


Figure 2.3- Integration time for different light intensity conditions, based on Fig. 1(a) of [29].

As it works exclusively in linear mode, classical DSRS techniques as CDS or DRS can be applied to reduce FPN, and the SNR is kept almost in the same level as that of the regular linear operation mode.

The implementation of this technique can be performed with two or more captures. Dual capture would be the easiest to implement, combining two subsequently registered frames for short and long integration times, respectively. The short exposure captures details of well illuminated regions in a scene, while the long exposure captures details of dark regions, otherwise filtered by the short exposure capture. Nevertheless, although the long exposure highlights poorly illuminated regions of a given scene, it also promotes the blooming of well illuminated regions. The latter often renders well lit objects larger than they actually are. On the other hand the short exposure capture renders normal size of well lit objects. Therefore the composite image will display unwanted discontinuities on the silhouette edge of these objects. This effect can be overcome by reducing the difference between exposure times, however compromising the main purpose of the technique, i.e. to extend the dynamic range. The implementation of multiple captures is quite difficult and requires very high speed and nondestructive readout together with on-chip memory and some logic to perform reconstruction of the wide DR image during capture [11].

The complexity level of the pixel circuitry is from moderate to high, while the external circuitry complexity level is from low to moderate. Moreover, the imager depends on a very high operation speed to yield a reasonable frame rate with good image quality.

2.1.4 Spatial Varying Exposure

The spatially varying exposure (SVE) technique is performed by spatially varying pixel exposure to the image brightness by means of neutral density filters [11]. The pixel sensitivity is defined by its brightness exposure level [32]. This technique uses conventional image sensors. However the imager spatial resolution is reduced.

The image array shown in Fig. 2.4 is an example of how to implement the SVE technique. The brighter pixels have greater exposure to radiance and capture the low light components of the image. The darker pixels have lower exposure to radiance and capture the high light components of the image. The pixels with the moderate level of exposure capture light components between the brighter and darker ones.

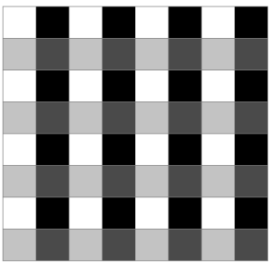


Figure 2.4- Spatial varying exposure example, based on Fig. 1 of [32].

The sensor under SVE technique operates in linear mode. Therefore classical DSRS techniques as CDS or DRS can be applied to reduce FPN as well as in multiple scenes capture technique. However, reducing pixel sensitivity by blocking light reduces also SNR.

The wide dynamic range image is captured in a single frame readout operation resulting in high frame rates. Dynamic range is extended only toward high light levels.

If the light filter array is at hand, the technique is indeed very simple to be implemented. Notwithstanding, as spatial resolution is reduced, very high resolution sensors are demanded. Since no change in the pixels structures is needed, the pixel circuitry complexity is low. Nevertheless, due to difficult implementation, external circuitry has high complexity.

2.1.5 Time-to-Saturation

The time to saturation (TTS) technique is based on the notion that stronger signals elicit responses more quickly than weaker ones [35]. Each pixel in the imager is reset, then exposed to a definite light brightness, and then let to integrate until it reaches either saturation or a predefined voltage level. When such level is reached an event is fired. Each event is captured by a global counter that generates an event index for each pixel in the imager. The event index is an integer. The pixels with smaller indices are those exposed to brighter conditions while those with larger indices are those exposed to darker conditions. Once all pixels in the array have responded, the stored indices are read out and the image is synthesized.

This technique uses exclusively linear operation mode. Nevertheless classical DSRS techniques as CDS or DRS cannot be applied to reduce FPN. Actually the only reported way to reduce FPN in imagers using technique is by very careful circuit design [34].

Since each pixel in the imager reaches saturation, the SNR is maximized for each pixel. Minimum detectable light intensity is limited by the maximum defined integration time. And the maximum detectable light intensity is limited by circuit mismatches, readout speed and FPN [11].

Implementing this technique is very difficult. If event information is stored in external circuit, signals of equal amplitude, therefore generated at the same time, can severely limit performance. If it is performed at pixel level, pixel size can became unacceptably large [11].

2.1.6 Local Adaptation (artificial retina)

The local adaptation technique (LAD) or artificial retina is based on how the earlier biological retina visual processing is believed to occur. The retinal process description presented in the next paragraph has been used as the base of this model, which investigates how the retina distinguishes contrast between two points in a range of many orders of light intensity. The cross section of the biological retina is shown in Fig. 2.5.

The photoreceptors transduce the local light intensity of an image focused on the retina into an electrical potential [36]. This electrical potential is proportional to the logarithm of the light intensity [36]. In this technique the photoreceptors are modeled as usual photodiodes or phototransistors working in logarithmic mode.

The horizontal cells, distributed in the inner nuclear layer, spatially and temporally average the output of the photoreceptors. Each horizontal cell output represents a

spatially weighted average of the photoreceptors output in its vicinity. The further away the photoreceptor is the less weight is given it. The artificial retina technique models the horizontal cells functionality as passive cables in which the weighting function decreases exponentially with the distance [36]. These passive cables form a hexagonal resistive network, as shown in Fig. 2.6. Each pixel of the imager is connected to a point in this resistive network.

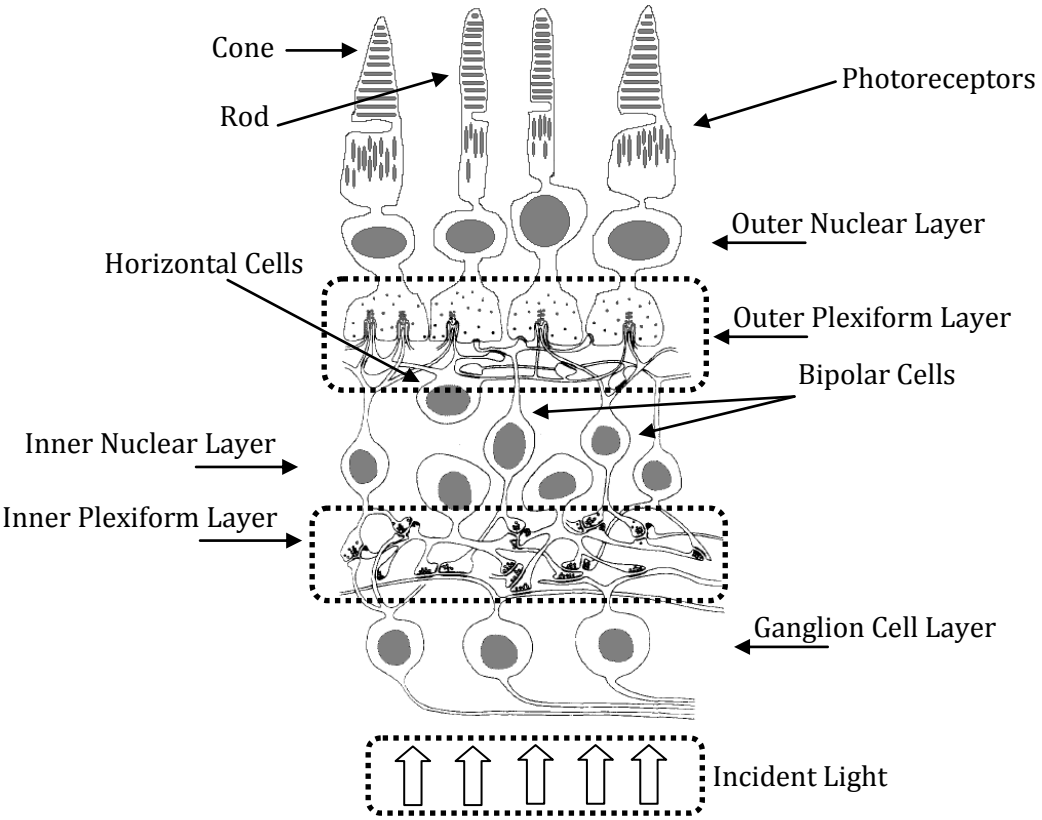


Figure 2.5- Cross section of the biological retina, based on Fig. 1 of [36], and on Fig. 22.14 of [39], and on Fig. 4.3 of [40].

Finally the bipolar cells, also located in the inner nuclear layer of the retina, yield an output that is proportional to the difference between the photoreceptors output and the horizontal cells output [36]. These signals are further processed to form the image. Only these three primary steps are counted in this method.

The interesting point of this technique is the implementation of lateral inhibition that is a ubiquitous feature of peripheral sensory systems. This feature provides a reference value with which to compare the signal. This reference value is the operating point of the system. In the retina system this operating point is locally calculated by the horizontal cells. The use of local rather than global operating point references gives the eye the ability to distinguish details in both the brighter and darker areas of high contrast scenes [38].

This technique can be implemented with any variation of the logarithmic compressed response mode. As in the full logarithmic and WCA modes, classical DSRS techniques as CDS or DRS cannot be applied to reduce FPN, because the response is not exclusively linear. Signal-to-noise ratio is reduced, because of the subtraction of hexagonal resistive

network local point output from the local pixel output. The pixel circuitry complexity of this technique is high, whereas external circuitry complexity is low.

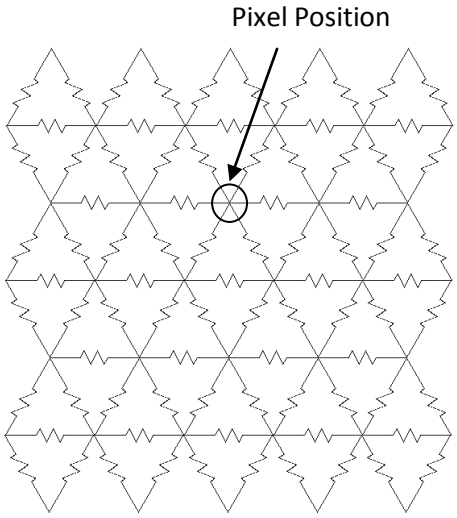


Figure 2.6- Hexagonal resistive network, based on Fig. 3 of [36].

2.2 Complementary-Mode Sensor

The best known way to combine in the same frame the good sensitivity, toward low light, of the linear mode with the wide dynamic range, toward high light, of logarithmic mode is using the technique called complementary-mode sensor (CMS) or multi-mode sensor (MMS).

In the late 1990s two ways to combine the linear and logarithmic modes were proposed. The first method was proposed by Tu [41], in which the linear and logarithmic mode is independently selected. The second method was proposed by Hynecek [45, 46], in which the pixel automatically changes from the linear to the logarithmic mode depending exclusively upon the light intensity. The scheme of Hynecek requires a minimum of four transistors per pixel. In the literature Hyneck is found to be the first to use the term lin-log for a pixel using such technique [45, 46]. Then in the in the early 2000s, Wäny [47] presented a technique similar to that of Hynecek, patenting it as LINLOG^{tm}. The difference is that the technique of Wäny can be applied to the basic 3T APS. The LINLOG^{tm} idea gave birth to the PhotonFocus Company.

2.2.1 Linear-Logarithmic Combination of Tu

In the method proposed by Tu [41], the linear and logarithmic responses of the pixel are independently read, and after specific analysis one of the two responses is chosen to be displayed [44]. The long time required to both sample either responses and perform the analyses of which mode to choose, is the main weakness of such approach, because it drastically reduces frame rate [44]. A simple scheme of how to operate the 3T APS with such scheme is shown in Fig. 2.7 [42, 43]. In this circuit when the LOG terminal is high, the pixel is set to logarithmic mode, and when the LOG terminal is low then the RST control signals the circuits and the pixel is set to the linear mode.

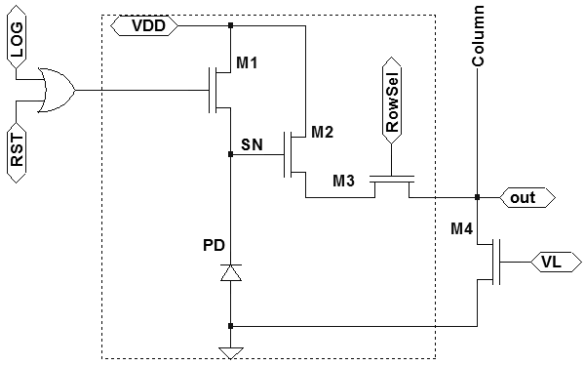


Figure 2.7- Linear-logarithmic pixel scheme, based on Fig. 2 of [43].

2.2.2 Linear-Logarithmic (Lin-Log) Technique of Hynecek

The pixel architecture proposed by Hynecek [45, 46] is shown in Fig. 2.8(a). In his lin-log concept it is necessary for the V_{bias} level to be higher than V_{DD}, being in this case V_{DD} a constant clamping voltage level. The high level of the reset signal in this case must be V_{bias}. In order to avoid the need of in-chip voltage higher than the voltage supply V_{DD}, Choubey and Collins [21] implemented a slight change in the Hynecek lin-log circuit as shown in the pixel of Fig. 2.8(b). In the pixel of Fig. 2.8(b), called here Hynecek-Choubey APS, V_{bias} is lower than V_{DD}.

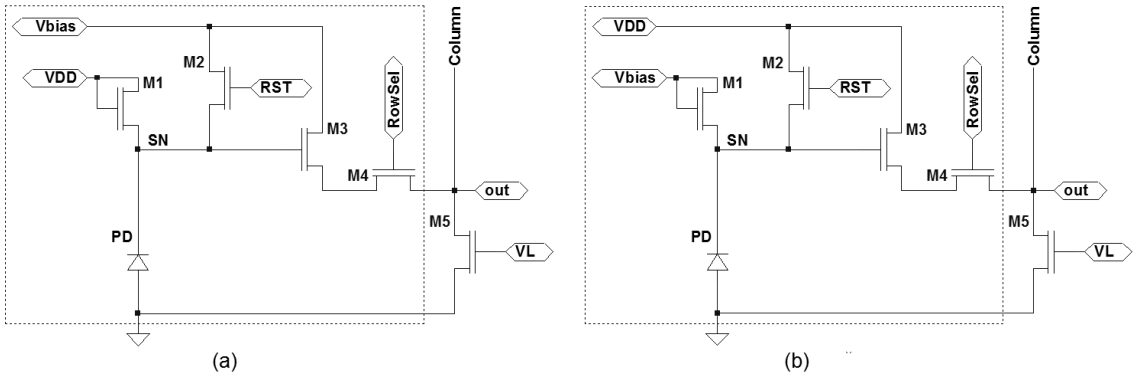


Figure 2.8- Lin-log pixel architecture used by Hynecek, based on Fig. 2 of [46] (a) and Choubey, based on Fig. 2 of [21] (b).

An example of the lin-log output yielded by the pixel of Hynecek-Choubey under twelve different light intensity levels is shown in Fig. 2.9. The dimensions of all the four transistors of the pixel and of the column amplifier, as well as of the photodiode are the same as those of the pixel in Fig. 1.11 used to produce the results shown in Fig. 1.12.

In the results shown in Fig. 2.9, the photocurrent representing light intensity varies from 1 fA in dark condition to 20 μA in a very bright condition. The voltage source V_{DD} level is 3.3 V and that of V_{bias} is 2.0 V and the voltage level at the load node VL is set to 0.8 V. The RowSel signal may be active only during the output sampling, nevertheless in the present simulation this signal was always at V_{DD} level. The integration time t_{int} lasts 30 ms and the reset time t_{rst} lasts 1 μs. The sampling time takes place at the end of the integration time as indicated by dashed vertical line labeled as t_{samp}.

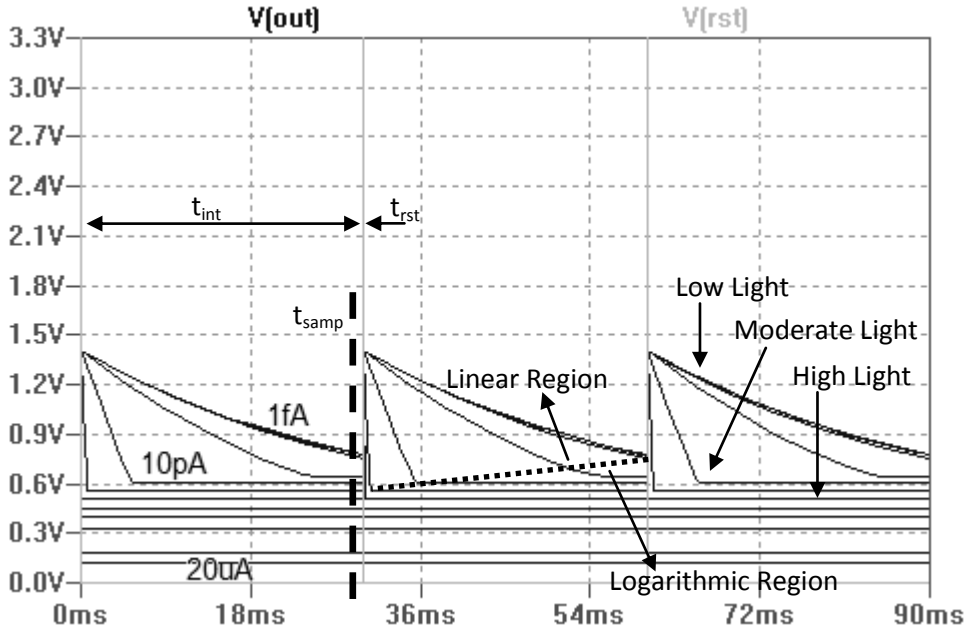


Figure 2.9- Lin-log response of pixel of Hynecek-Choubey [art prepared by the author].

When the pixel is subjected to a low light intensity the photodiode output, SN signal as well as the voltage output, will be in the linear region throughout the whole integration time, unless the integration time is long enough. However a very long integration time is not practical. Under moderate light condition the output signal presents a linear region in the beginning of the integration time and a logarithmic region at the end of the integration time. The diagonal dashed line in Fig. 2.9 shows the interface between the linear and logarithmic regions. When the pixel is subjected to high light conditions the linear region is far too steep to be treated, therefore only the logarithmic region is of interest in this case.

2.2.3 Linear-Logarithmic (LINLOG™) Technique of Wäny with 3T APS

Wäny [47] was the first to apply the complementary-mode operation to the 3T APS, thereby creating the LINLOG trade mark and patented the technique. This idea was so appealing that in 2001 gave birth to the successful PhotonFocus AG Company, which is specialized in wide dynamic range CMOS imagers. In 2004 Wäny left PhotonFocus and founded AWAIBA Lda a design house specialized in the development of customized CMOS image sensors. As the method proposed by Hynecek, the one proposed by Wäny also yields wide dynamic range results at high frame rates.

Though Wäny was not the first to make use of the complementary-mode operation, apparently he was the first to apply it to the basic 3T APS. This is important because the fill factor of the pixel can be kept as high as possible, avoiding therefore the need of the spare clamping transistor, M_1 in Fig. 2.8(a) and (b). Nevertheless, it requires a hard reset approach to eliminate image lag, as shown by the signal scheme of Fig. 2.10, which is the heart of the technique proposed by Wäny in [47]. Image lag problems will be explored in the next chapter.

In the scheme proposed by Wäny, the control signal labeled $V_{log\text{-}res}$ is the signal applied to RST terminal of the pixel shown on Fig. 1.11. The hard reset scheme is applied so that

the reset level of sense node SN reaches V_{DD}. The hard reset approach works by raising the high level of the reset signal above that of the power supply V_{DD} plus the threshold voltage V_{TH} of the reset transistor. In the scheme of Fig. 2.10 the voltage supply V_{DD} is presented as V_{res}. The sense node signal is indicated in this scheme by V_{signal}.

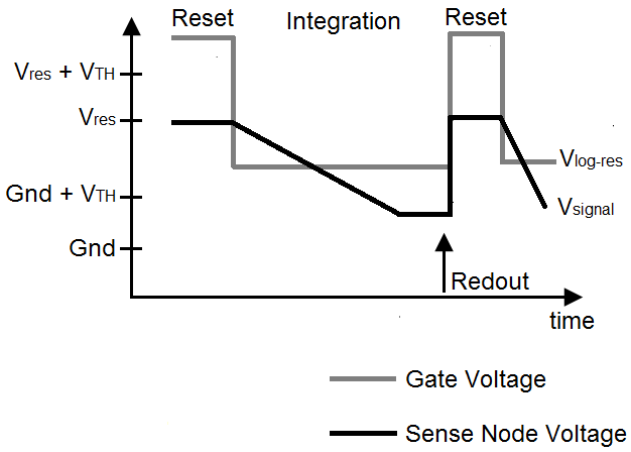


Figure 2.10- LINLOG^{tm} scheme of Marin Wäny, based on Fig. 4 of [47].

The key to achieve the complementary linear-logarithmic operation with the scheme of Fig. 2.10 is the low level of the reset signal $V_{log\text{-}res}$. The low level of $V_{log\text{-}res}$ can be set to any predetermined value in the range between (GND + V_{TH}) and the reset level (V_{res} + V_{TH}), or (V_{DD} + V_{TH}). On the other hand, the hard-reset operation can be harmful to the circuit because it overstresses the gate-oxide of MOS transistor M_1, reducing its life time as discussed in [48]-[51]. This effect reduces, therefore, the lifetime of the APS circuit and of the imager array as a whole.

Simulation results of the sense node and output signals yielded by the 3T APS with the LINLOG^{tm} scheme are shown in Fig. 2.11 and Fig. 2.12 respectively. The dimensions of the three transistors of the pixel, and of the column amplifier, as well as the dimensions of the photodiode are the same as those of the pixel in Fig. 1.11 used to produce the results shown in Fig. 1.12.

As in the case of the simulation of pixel of Hynecek-Choubey the photocurrent representing light intensity varies from 1 fA in dark condition to 20 μA in a very bright condition. The voltage source V_{DD} level is 3.3 V, and the low level of $V_{log\text{-}res}$ is 2.0 V, and VL is set to 0.8 V. The RowSel is always at V_{DD} in the present simulation. The integration time t_{int} lasts 30 ms and the reset time t_{rst} lasts 1 μs. And the high level of the $V_{log\text{-}res}$ is 4.4 V. This voltage level is necessary to guarantee that the sense node voltage reaches V_{DD}, which is V_{res}, during the reset time.

The simulation results show that the shorter the reset time, the higher the $V_{log\text{-}res}$ high level must be. For example, using $V_{log\text{-}res}$ high level of 4.1 V, the reset time must be around 250 μs. Therefore the hard reset approach depends not only upon the high level of $V_{log\text{-}res}$ but also upon the reset time length.

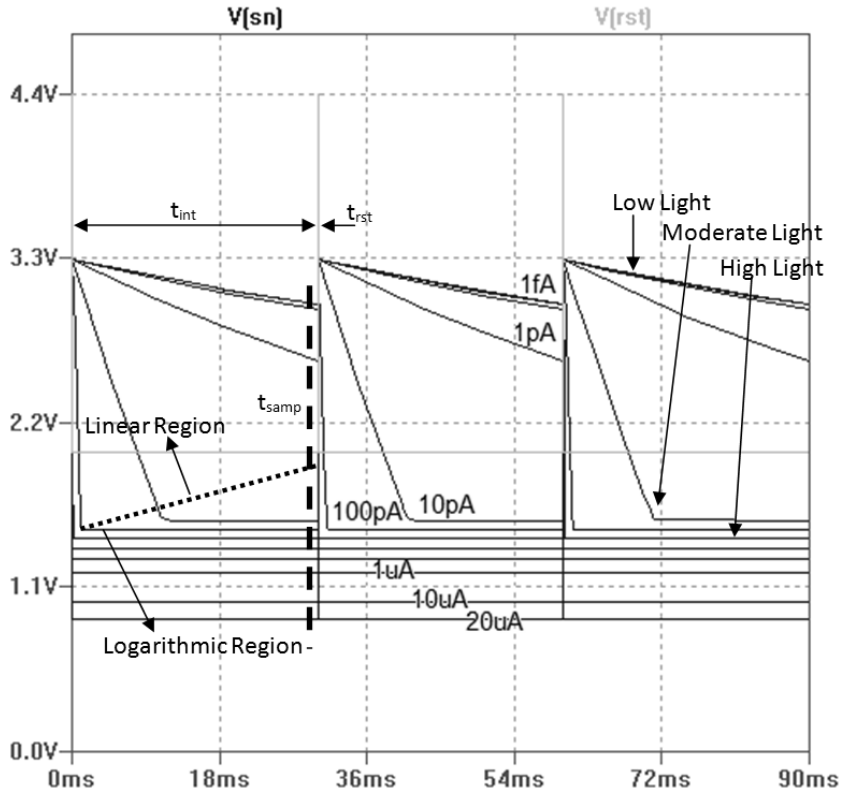


Figure 2.11- Sense node response of the 3T APS with the LINLOG^{tm} scheme [art prepared by the author].

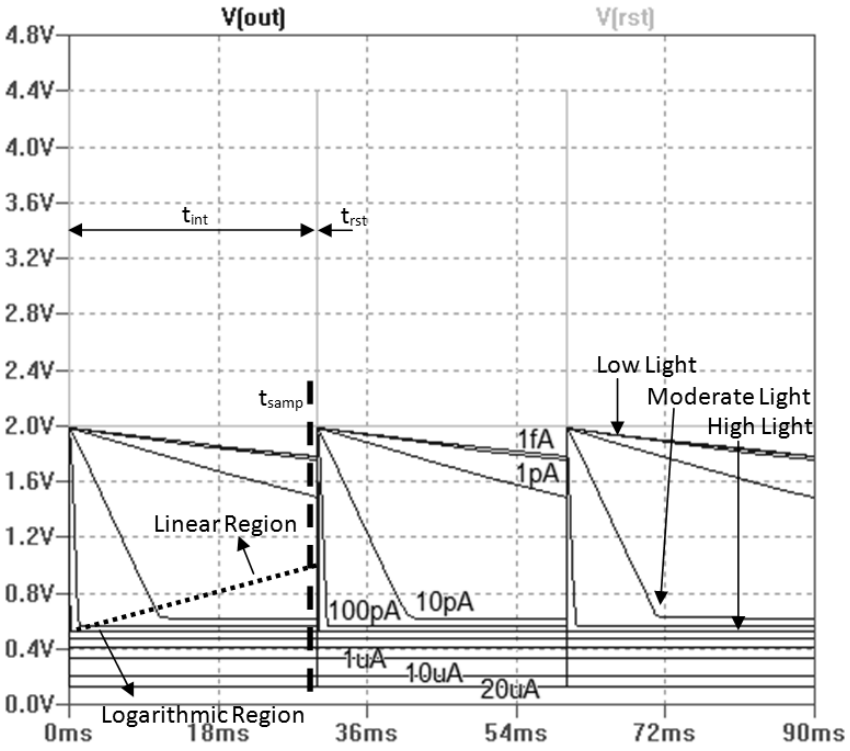


Figure 2.12- Output response of the 3T APS with the LINLOG^{tm} scheme [art prepared by the author].

Basically the hard reset approach is used to suppress image lag, due to incomplete reset, in the transition from a high light illumination condition to a low light condition. Details of this problem will be discussed in the next chapter. Simulations that expose the difference between the complementary-mode scheme without hard reset and the LINLOG^{tm} scheme are shown in Fig. 2.13 and Fig. 2.14 respectively. The pure complementary-mode and the LINLOG^{tm} schemes were both applied to the 3T APS. To exemplify the transition between scenes of different illumination levels, during the first integration time the pixel is under a photocurrent of 10 pA, whereas during the four subsequent integration times the pixel is subject under lower photocurrents. Three different photocurrent levels are used in this example of 1 fA, 10 fA and 100 fA.

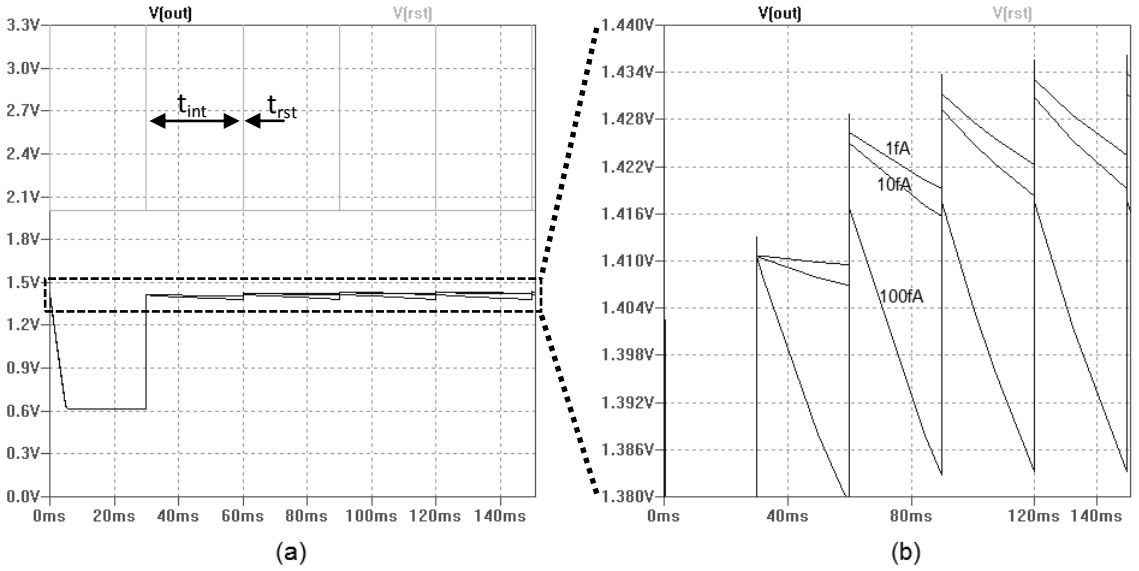


Figure 2.13- Output of the 3T APS with complementary-mode scheme without hard reset (a), and zoomed area (b) [art prepared by the author].

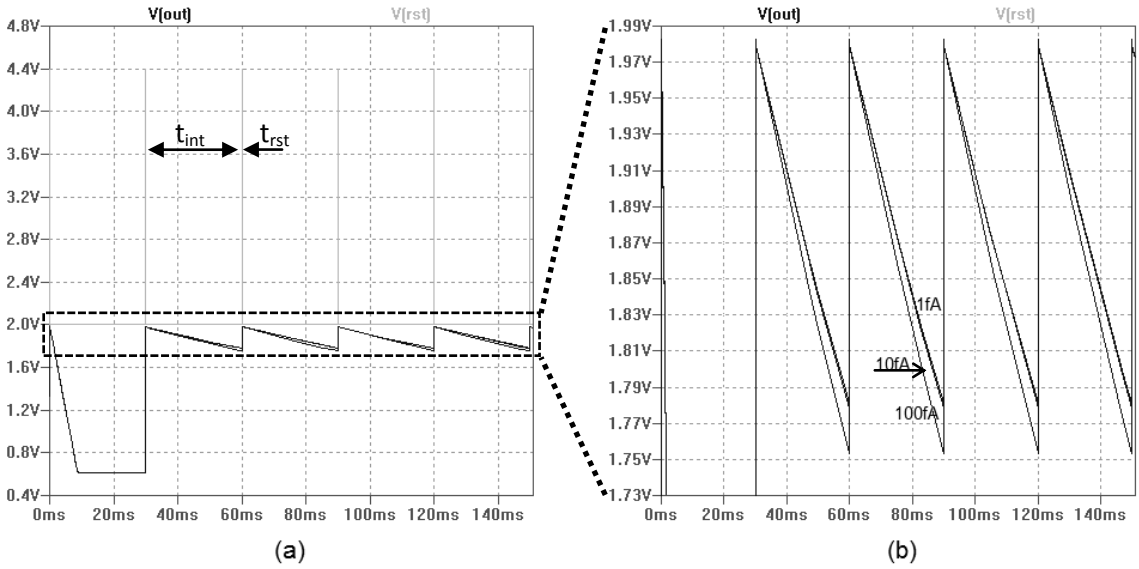


Figure 2.14- Output of the 3T APS with the LINLOG^{tm} scheme (a), and zoomed area (b) [art prepared by the author].

The complementary-mode scheme without hard reset applied to the 3T APS is shown in Fig. 2.13. The zoomed area on the right shows the difference between the four different voltage levels after the reset operation. Though a specific photocurrent mimicking low illumination level does not change between the four integration times, the final reset level is not the same. This is the effect known as incomplete reset, and causes image lag.

As in the results shown in Fig. 2.12, the LINLOG^{tm} results under the same illumination conditions, just mentioned, is presented in Fig. 2.14. The zoomed area on the right shows the absence of incomplete reset image lag.

2.2.4 Linear-Logarithmic (LINLOG^{tm}) Technique of Wäny with 4T APS

The implementation of the LINLOG^{tm} scheme with the 3T APS requires a voltage booster to produce a voltage higher than that of the power supply V_{DD}. The voltage booster circuit must be integrated together with imager sensor in the same chip. Acknowledging this burden, Wäny proposed in the selfsame patent [47] an alternative APS architecture with four transistors, presented in Fig. 2.15. This architecture is very similar to that of Hynecek-Choubey. The fourth transistor has the same function of the clamping transistor M_1 of the pixel architecture of Hynecek-Choubey. However, instead of driving both the drain and the gate terminals with the clamping voltage V_{bias}, in the architecture of Wäny only the gate terminal of the clamping transistor M_1 is driven by V_{bias}. In the 4T APS architecture of Wäny V_{bias}, is labeled $V_{log\text{-}res}$.

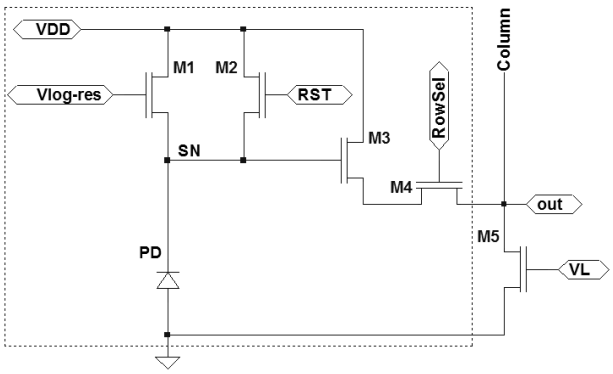


Figure 2.15- 4T APS architecture with the LINLOG^{tm} scheme, based on Fig. 5 of [47].

The 4T APS proposed by Wäny, as that of Hynecek-Choubey, is free from incomplete reset image lag. Simulation results of this pixel, under low light condition, are presented in Fig. 2.16. As in the previous case, during the first integration time the pixel is under a photocurrent of 10 pA, whereas during the four subsequent integration times the pixel is subject to lower photocurrents. Three different photocurrent levels are used in this example of 1 fA, 10 fA and 100 fA. The voltage supply level V_{DD} and the high level of the $V_{log\text{-}res}$ are 3.3 V, the low level of $V_{log\text{-}res}$ is 2.0 V, and VL is set to 0.8 V. The RowSel is always at V_{DD} in the present simulation. The integration time t_{int} lasts 30 ms and the reset time t_{rst} lasts 1 μs.

Different from the LINLOG^{tm} scheme for the 3T APS that uses hard reset, the reset voltage of the sense node does not reach V_{DD}, as shown in Fig. 2.16(a). The zoomed area on the right shows the absence of incomplete reset image lag. The only disadvantage of this pixel architecture is that its fill factor is lower than that of the basic 3T APS.

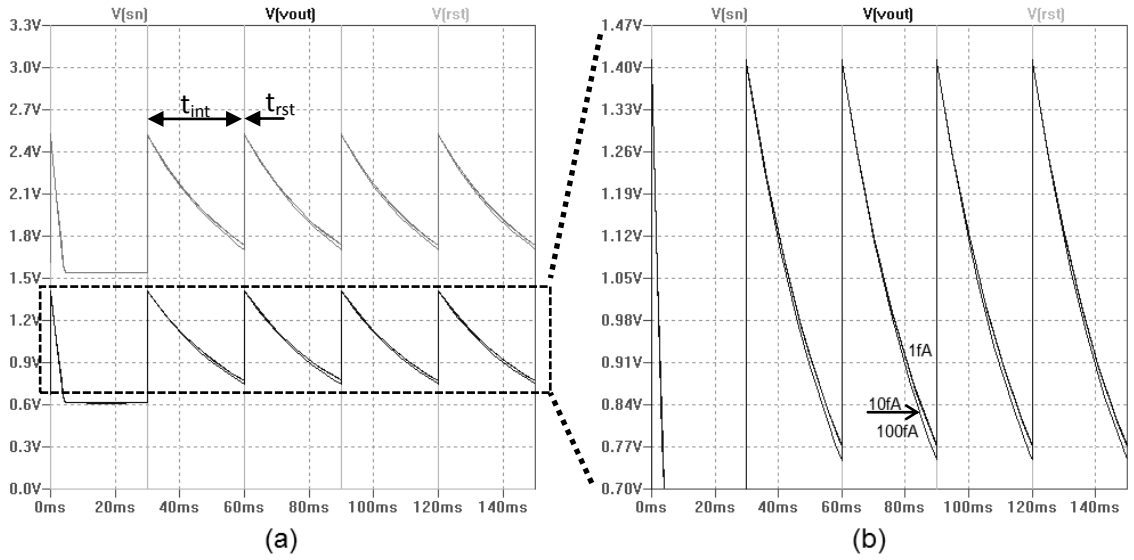


Figure 2.16- Sense node signal and output of the 4T APS with the LINLOG^{tm} scheme (a), and zoomed area (b) [art prepared by the author].

The complementary-mode technique has an interesting feature which is the adjustment of the clamping voltage to any desirable level between V_{DD} and GND. The clamping voltage can be done at the very beginning of every integration time. In the case of the 3T APS with the LINLOG^{tm} scheme, the clamping voltage is the low voltage level of the reset signal $V_{log-res}$. For example, taking the output voltage level of the results shown in Fig. 2.12 at the position indicated by t_{samp}, it is possible to plot the output voltage against the illumination level as shown by the curve Vout($V_{log-res}$ = 2.0 V) in Fig. 2.17. The sampling is taken at 29 ms after the beginning of the integration time. The illumination level is indicated by the photocurrent level I_{ph}. In this case the clamping voltage is 2.0 V. However, if the clamping voltage is changed to 2.5 V the output response follows the curve Vout(Vlog-res = 2.5 V) in Fig. 2.17. The linear and logarithmic region of each curve is indicated by the arrows. These results show that the higher the clamping voltage the shorter is the linear region.

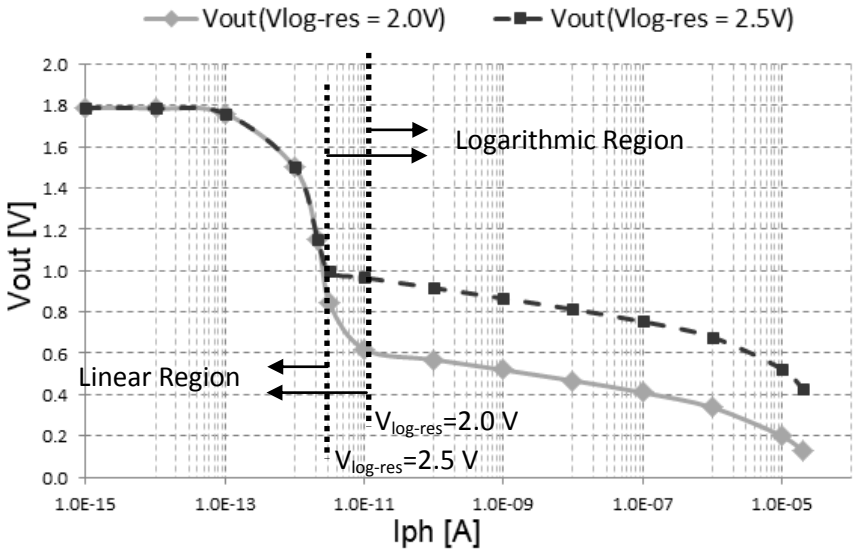


Figure 2.17- Output voltage versus light intensity in complementary-mode sensor for two different clamping levels [art prepared by the author].

2.2.5 Linear-Logarithmic Combination in the 3T APS without Hard-Reset

With the complementary-mode sensor approach it is possible to adjust the clamping voltage from the full logarithmic mode to the complete linear mode. Let us ignore by now the reset induced image lag and apply the complementary-mode scheme, without the hard reset operation. Now using a clamping voltage of 2.5 V and the high level of the reset of 3.3 V, the 3T APS yields an output voltage with the illumination as that shown in Fig. 2.18. These results are produced by photocurrents varying from 1 fA to 20 μA.

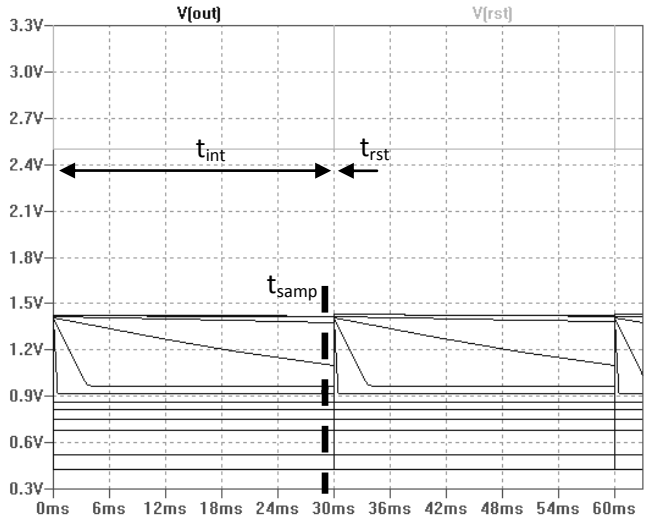


Figure 2.18- Output voltage of the 3T APS with complementary-mode sensor scheme using a clamping voltage of 2.5 V [art prepared by the author].

The voltage against illumination, produced by sampling the results shown in Fig. 2.18, at the position indicated by t_{samp}, is presented by the curve labeled as "CMS" in Fig. 2.19. As in the previous case the sampling is taken at 29 ms after the beginning of the integration time.

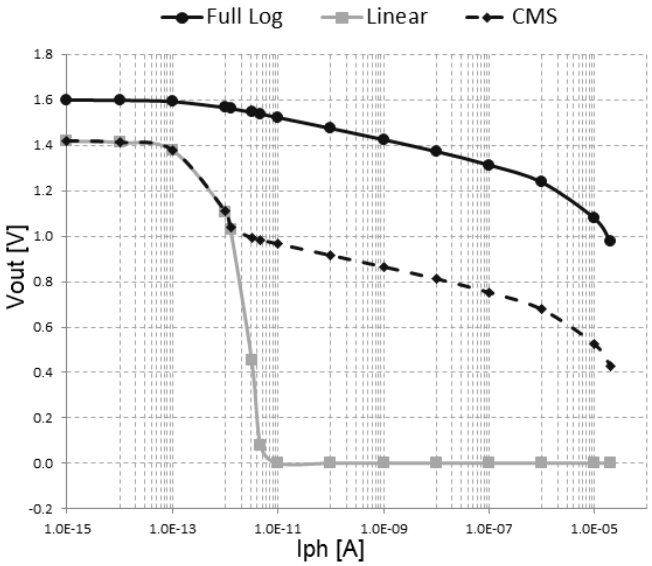


Figure 2.19- Output voltage versus light intensity, logarithmic, CMS and linear modes [art prepared by the author].

Setting the clamping voltage to 3.3 V the 3T APS produces a full logarithmic response and the output voltage against the illumination is shown by the curve labeled “Full Log” in Fig. 2.19. And setting the clamping voltage to GND, it produces a complete linear response as shown by the curve labeled “Linear” in Fig. 2.19. In order to produce a better fitting to the curves three other levels of photocurrent of 1.26 pA, 3.16 pA, and 4.64 pA, where used to produce the results of Fig. 2.19.

The reset induced image lag will be explored with more details in the next chapter, where a new way to reduce this problem in the complementary-mode sensor applied to the 3T APS will be presented. The new alternative technique presented in this work avoids the burdens of the hard reset operation, while keeping the fill factor of the pixel as high as possible. Moreover, besides reducing image lag, the proposed technique enables a way to reduce FPN in the 3T APS operating in either in full logarithmic or complementary-mode sensor via double sampling readout subtraction (DSRS).

2.3 Qualitative Comparisons of the Wide Dynamic Range Techniques

A qualitative comparison between the seven presented techniques to extend CMOS image sensor dynamic range is given in table 2.1.

Table 2.1: Qualitative comparison between the seven HDR schemes.

	Full Logarithmic - Compressed Response	**Well-Capacity Adjusting**	**Multiple-Scene Capture**	**Spatial Varying Exposure**	**Time-To-Saturation**	**Local Adaptation (artificial retina)**	**Complementary-mode Sensor**
DR	+	+	+	+	+	+	+
Linearity	No	No	Yes	Yes	No	No	No
Low Light Sensitivity	-	+	+	±	+	±	+
High Light Sensitivity	±	±	±	±	+	±	±
Classical DSRS	No	No	Yes	Yes	No	No	No
Frame Rate	-	+	±/-	+	-	±/+	+
Pixel Complexity	-	-	±/+	-	+	+	-
External Circuitry Complexity	-/±	-	-/±	+	+	-	-

“+”: High; “±”: Moderate; “-”: Low;
“-/±”: From low to moderate;
“±/+”: From moderate to high.

Chapter III: Image Lag Treatment

Two or more consecutive frames of the same static image, at the same light condition, may be sampled as undesired different images due to delay in the photosensor response. This causes visual response delay when portions of dynamic frames change from brighter to darker conditions, producing artifacts that do not exist in the real image. Such effect is illustrated in Fig. 3.1, where it is shown four different captures of a moving bright circle across a dark background from the left to the right. In the first situation, first row captures, there is image lag whereas in the second case, second row captures, there is no image lag. The image lag in the first row shows that the effect of the previous captures vanishes slowly from the pixels where the bright circle was first registered. This problem is common to APS operating in either linear or logarithmic mode. The delay in the sensor response occurs when the sensor is not given enough time to reach steady state before sampling its voltage output.

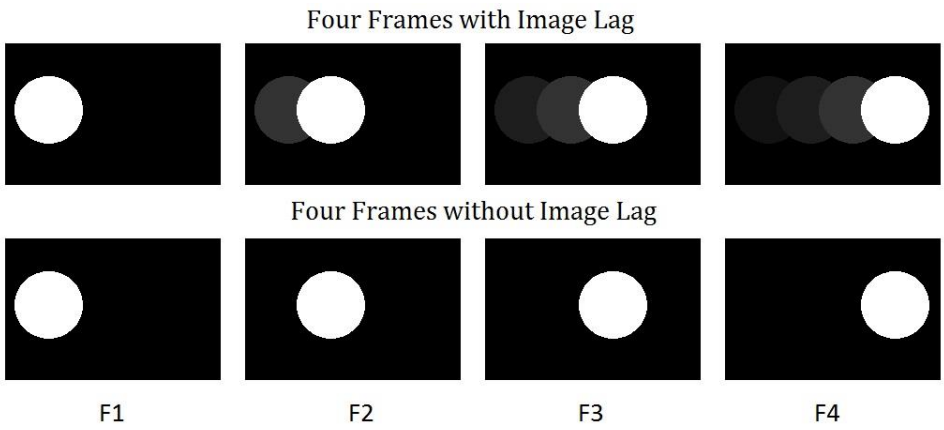


Figure 3.1- Sequence of frames with and without image lag [art prepared by the author].

A sequence of four consecutive frames taken by a single pixel, the APS of Fig. 1.11, operating in linear mode under low light condition is shown in Fig. 3.2. The integration time used for this simulation is of 30 ms and the output voltage is sampled 29 ms after the beginning of the integration time. During the first integration time, the pixel is under a photocurrent of 10 pA, emulating high light condition, and during the four subsequent integration times the pixel is under a photocurrent of 1 fA. This plot shows that each of the four frames F1, F2, F3 and F4 has a different voltage level. This voltage difference between the consecutive frames characterizes the image lag induced by incomplete reset. Basically the shorter the integration time, the large the image lag is.

It is worth pointing out that the incomplete reset refers to a condition where the reset state of the first frame, in a given sequence, is incomplete. That occurs only when the scene or part of it goes from a condition of moderate or high illumination to a condition of low illumination. The other way round produces no image lag.

The image lag for each individual pixel in an imager appears as output voltage difference between consecutive samples. For example, using three different photocurrent values representing low light conditions, i.e. 1 fA, 10 fA, and 100 fA, the sampled results

produced at the end of the integration time is shown in Fig. 3.3. The three bold lines in each frame represent the sampled output level of the pixel under each illumination level.

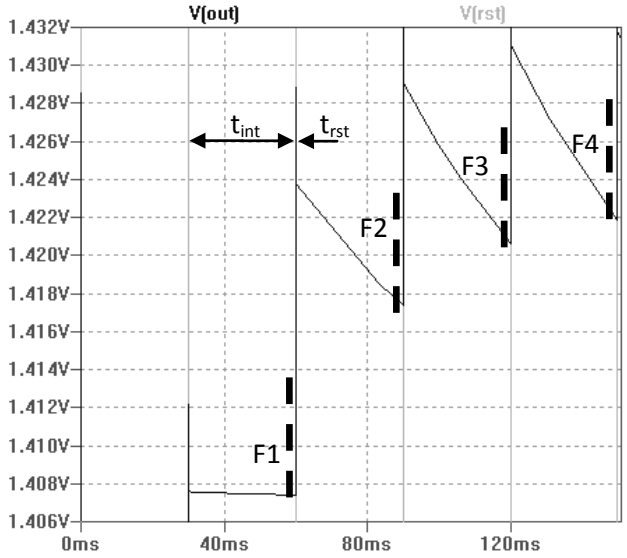


Figure 3.2- Voltage output image lag of four consecutive frames of a 3T APS operating in linear mode under low light condition [art prepared by the author].

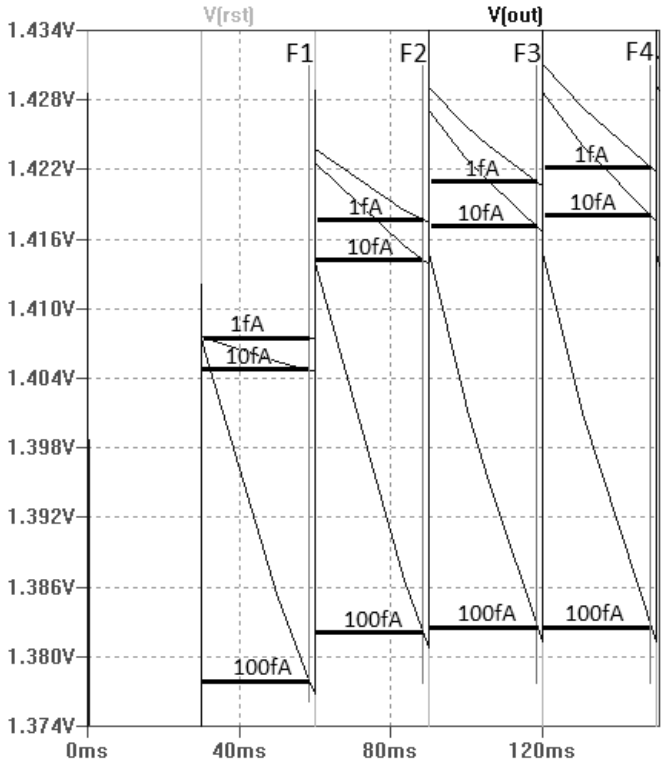


Figure 3.3- Image lag under three different light intensities [art prepared by the author].

The voltage difference between two consecutive samples, especially between the first two F1 and F2, may reach many millivolts. When many samples are taken of the same image under the same light intensity, the lag between consecutive samples is reduced, as it is shown in Fig. 3.3. When comparing the three different sampling groups, it is observed

that the lag reduces as the light intensity increases. The third sampling group is taken under the highest light intensity and has the lowest degree of image lag.

For the APS operating in linear mode the image lag occurs due to incomplete reset of the photodiode and limits the imager frame rate. When it is operating in full logarithmic mode it may take from hundreds of milliseconds to many seconds for the pixel to reach steady state [16], therefore image lag is particularly worse in this mode.

There are basically three methods to reduce image lag induced by incomplete reset. The first method is using a PMOS transistor as the reset transistor. The second method is using the hard reset approach to ensure the complete reset of the photodiode, as introduced in the previous chapter. The third method is the pseudo-flash reset that emulates the same reset level even under very low light conditions. The advantages and disadvantages of these methods will be discussed next.

3.1 PMOS Reset Transistor

The first method to eliminate image lag induced by incomplete reset is to replace the NMOS reset transistor of the basic 3T APS by a PMOS transistor as shown in Fig. 3.4. Doing this the polarity of the reset signal must be inverted. When active, with GND applied to its gate, the PMOS reset transistor allows the photodiode to reach a complete reset, i.e. the SN node reaches V_{DD} level.

The output voltage of the pixel of Fig. 3.4 when subjected to a photocurrent of 1 fA is shown in Fig. 3.5. This is the same light level that produced the results shown in Fig. 3.2 using the pixel of Fig. 1.11. The same voltage level at the end of integration time for each of the four consecutive samples shows that the image lag is completely overcome by means of this method.

The integration time used for this simulation is also 30 ms. As pointed before, incomplete reset induced image lag is worst for shorter integration times. It is possible to verify that the same reset level is achieved for the four frames presented in Fig. 3.5. Therefore, even for shorter integration times, there will be no image lag.

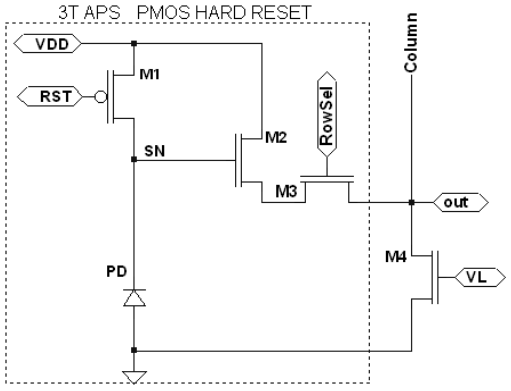


Figure 3.4- 3T APS with PMOS reset transistor, based on Fig. 5(a) of [15].

Image lag is more critical for low light condition than for moderate and high light conditions. Therefore, overcoming the problem for low light condition it is also overcome for moderate and high light conditions.

Simulations show that under three different low light conditions, 1 fA, 10 fA, and 100 fA, the image lag is completely suppressed by the use of this method as shown in Fig. 3.6. No perceptible image lag was observed among the four consecutive frames F1, F2, F3 and F4 in each of the three groups.

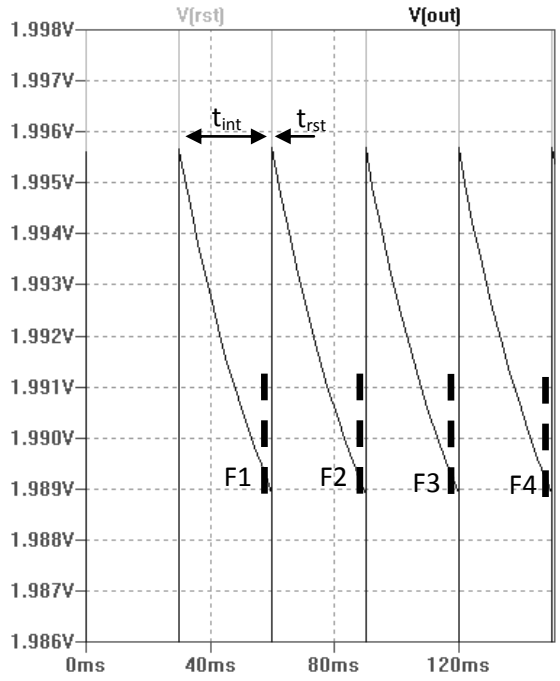


Figure 3.5- Voltage output without image lag using PMOS reset [art prepared by the author].

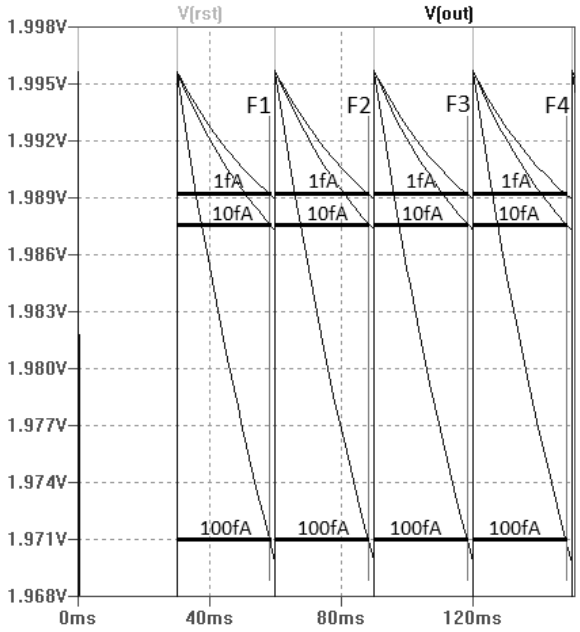


Figure 3.6- No perceptible image lag observed among the four consecutive samples under three different light conditions [art prepared by the author].

The main drawback of this method is the reduction of fill factor due to the use of a PMOS transistor. In the standard CMOS fabrication process, while the NMOS transistor is built on

the very silicon substrate, the PMOS transistor requires an extra n-well region embedded into the same substrate. Therefore, for the same transistor-channel dimension, i.e. W=0.35 μm and L=0.70 μm, the PMOS transistor requires a bigger area than does the NMOS transistor, thus reducing the fill factor of the pixel.

3.2 Hard Reset

The second way to eliminate reset-induced image lag is overdriving the reset transistor, this method is commonly known as hard reset. This method was already introduced for the complementary LINLOG^{tm} mode. Either for the linear or for the complementary mode the method works by setting the high level of the reset signal at a voltage higher than that of the power supply V_{DD} plus the threshold voltage V_{TH} of the reset transistor. This allows the reset transistor to operate in strong inversion along the whole reset time. Using this approach, the reset level of the sense node (SN) of the photodiode is V_{DD} level.

The output voltage of the pixel of Fig. 1.11 under three different low light conditions, 1 fA, 10 fA, and 100 fA, when the hard reset is applied is shown in Fig. 3.7. These results show that image lag is completely suppressed by the use of this method. No perceptible image lag was observed among the four consecutive frames F1, F2, F3 and F4 in each of the three groups.

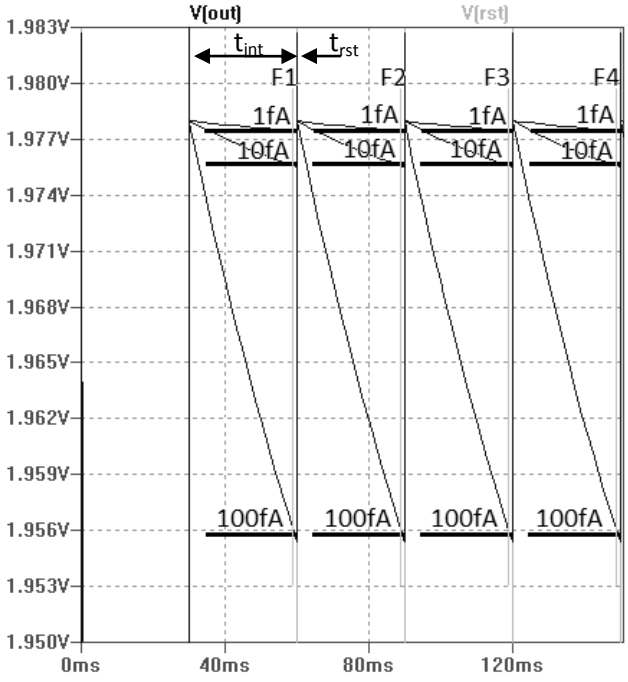


Figure 3.7- No image lag detected among the four consecutive samples under three different light conditions [art prepared by the author].

The following signal setup was used for simulations presented above. The voltage source V_{DD} level is 3.3 V, the low level of the reset signal RST is GND, and VL is set to 0.8 V. The RowSel is always at V_{DD} in the present simulation. The integration time t_{int} lasts 30 ms and the reset time t_{rst} lasts 1 μs, and the high level of the reset signal is 4.4 V. As in the case of the LINLOG^{tm} scheme, this voltage level is necessary to guarantee that the sense node voltage reaches the reset level, V_{DD}, during the reset time.

As previously pointed out, it is important noticing that the shorter the reset time, the higher the high level of the reset signal must be. For example using RST high level of 4.1 V, the reset time must be around 250 μs. Therefore the hard reset approach depends not only upon the high level of the reset signal but also upon the reset time length.

As happens with the use of a PMOS, the hard reset approach has also the advantage of reaching the highest possible sense node reset value that is V_{DD}. The fill factor is not affected by the use of this method as it was with the PMOS reset version.

This method has basically two drawbacks. First it requires a voltage booster to produce a voltage higher than that of the power supply V_{DD}. The voltage booster circuit must be integrated together with imager sensor in the same chip. Second, it provokes gate-oxide voltage overstress to the reset transistor, which is harmful to the device. The gate-oxide overstress reduces the lifetime of the MOS transistor and therefore of the pixel itself [48]-[51].

3.3 Pseudo-Flash Reset

The third method to suppress image lag is called pseudo-flash reset. The pseudo-flash reset was devised to eliminate image lag in the 3T APS operating exclusively in the linear mode [16]. The implementation of this method requires the drain terminal of the reset transistor to be free to be connected to any voltage level between GND and V_{DD}, as shown in Fig. 3.8.

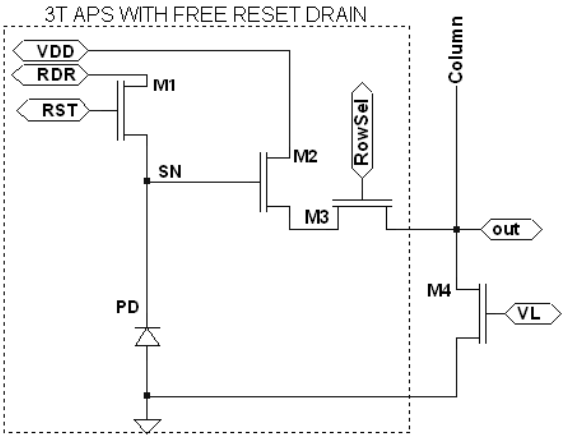


Figure 3.8- 3T APS with free reset drain, based on Fig. 6 of [15].

In the regular linear mode of operation, when the pixel is under high light condition the charge in the photodiode is quickly drained during integration time by its large generated photocurrent. At the beginning of the reset time, the reset transistor will be operating in the saturation region. Shortly after the beginning of the reset time, the reset transistor will reach the subthreshold regimen. At the end of the integration time the charge in the photodiode will be quite independent of the charge value at the beginning of the reset time, this independence prevents image lag to happen under high light condition.

On the other hand if the pixel is under low light condition the charge of the photodiode will be slowly drained during integration time by its small generated photocurrent. If the integration time is not long enough the reset transistor will begin the reset time already in

the subthreshold regimen. In this case, if the reset time is not long enough, the charge in the photodiode at the beginning of reset time will greatly affect its charge at the end of the selfsame integration time. When the charge at the end of reset time is dependent upon the charge at the beginning of reset time, the reset of the photodiode will consequently be incomplete especially for short reset times. Therefore under low light illumination a short reset time results in image lag induced by incomplete reset.

The pseudo-flash reset method consists in applying a low voltage pulse in the drain of the reset transistor of the pixel in Fig. 3.8 while the gate voltage is in high level, as shown in Fig. 3.9. This is done in order to drain the residual charge in the photodiode that remains after the integration time. This allows the reset transistor to begin the reset time in the saturation region independently of the light level at which the pixel is subjected. Image lag induced by incomplete reset is thus avoided.

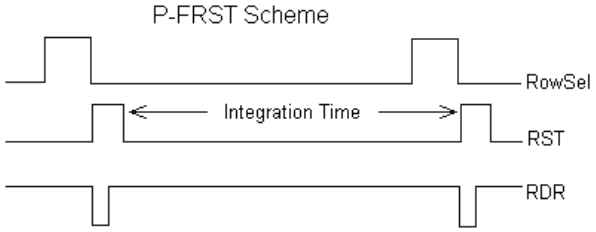


Figure 3.9- Pseudo-flash reset signal scheme, based on Fig. 6 of [16].

The signal scheme shown in Fig. 3.9 applied to the pixel shown in Fig. 3.8 guarantees that the reset transistor will begin the reset time in the saturation regimen, which is necessary to suppress image lag [16]. Besides suppressing image lag the pseudo-flash reset does not increase reset temporal noise [16], which happens to the previous presented methods.

For the simulations performed with the pixel of Fig. 3.8, presented here, the RDR signal has a period of 30 ms, and a pulse width of 0.1 μs. The RDR pulse starts 0.05μs before the beginning of the reset time. The reset time has a period of 30 ms and a pulse width of 1 μs.

The output voltage of the pixel of Fig. 3.8 under three different low light conditions, 1 fA, 10 fA, and 100 fA, when the pseudo-flash reset is applied is shown in Fig. 3.10. The simulation results show that image lag is also completely suppressed by the use of this method. No perceptible image lag was observed among the four consecutive frames F1, F2, F3, and F4 in each of the three groups.

The main difference between the pseudo-flash reset and the two previous presented methods is that the maximum sense-node reset level is not achieved, as in the previous cases. Nevertheless it achieves almost the same maximum value reached by the basic 3T APS operating in pure linear mode.

Due to reasons exposed before, we know that if the method is able to overcome image lag for low light conditions, it does also for higher light conditions. Also if the image lag is overcome with short integration times, the same thing happens for longer integration times.

The main drawback of this method is that as the pixel needs an individual routing for the drain terminal of the reset transistor different from that of the V_{DD}. In this case the fill

factor of the APS using pseudo-flash reset, Fig. 3.8, depends also on the number of metal layers featured in the CMOS technology in which the pixel is to be fabricated. For instance, if the technology has only two metal layers, then the basic 3T APS, Fig. 1.11, will have its fill factor a little larger than that of the APS using pseudo-flash reset. On the other hand, if the CMOS technology features four metal layers, as the AMS 0.35µm CMOS technology used for this project, then the fill factor of the APS using pseudo-flash reset can be maximized to be the same as that of the basic 3T APS. The dependency of the fill factor on the number of metal layers featured in the technology is the main drawback of this method.

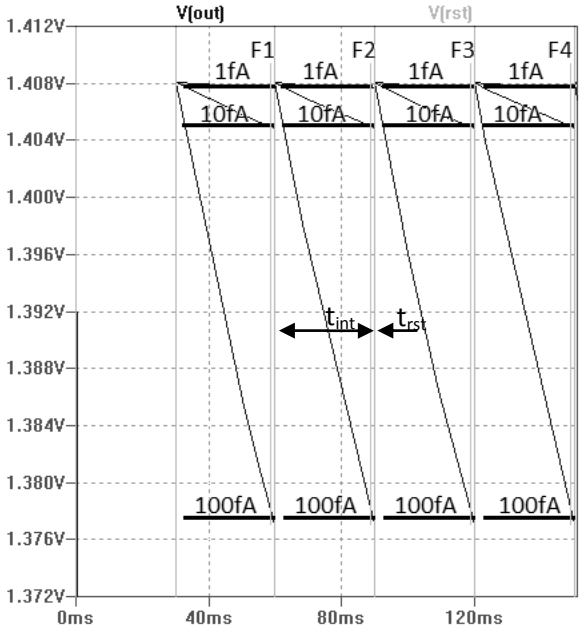


Figure 3.10- Voltage output without image lag using pseudo-flash reset [art prepared by the author].

3.4 Image Lag in the Full-Logarithmic Mode

Besides the low sensitivity toward low illumination, another weakness of the basic 3T APS operating in full logarithmic mode is the very long time required for the pixel to reach the steady state, especially at low light conditions. This slowness results in low frame rates or else in image lag. Classically there is no way to solve this problem because in this mode the pixel operates continuously and there is no reset scheme as in the linear mode. Nevertheless, using the pixel of Fig. 3.8, with the advent of the individual routing for the drain terminal of the reset transistor it is possible to establish an initial reference time for every single readout process as in the case of the linear mode. This initial reference time is called henceforth pseudo reset for the full logarithmic mode.

This is the first additional application discovered during the elaboration of this work for which the independent routing of the reset transistor drain terminal of the 3T APS can be used. The pseudo reset is not meant to set the photodiode to the maximum charge but rather to the minimum. And differently from the regular linear mode of operation there is not an integration time but a logarithmic charge accumulation dependent on the light illumination level.

The continuous operation of the full logarithmic mode APS, with the gate of the reset transistor at V_{DD}, is shown in Fig. 3.11. These plots represent the output of the pixel of Fig. 1.11 operating in full logarithmic mode when it changes from a condition of high illumination to a condition of low illumination. The high illumination condition remains until 30 ms then it changes to low illumination condition represented here by the photocurrents 1 fA, 10 fA, and 100 fA. As in the previous cases the pixel is sampled four times during intervals of 30 ms.

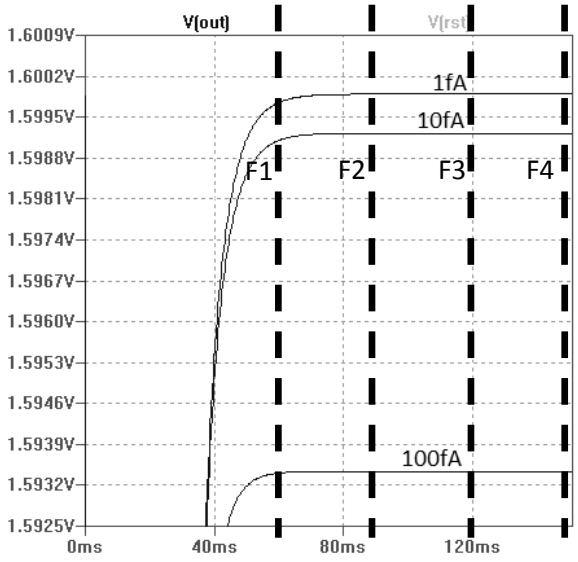


Figure 3.11- Continuous operation of the full logarithmic pixel [art prepared by the author].

It is easy to notice the lag between the two first frames F1 and F2, especially for the two lower light conditions. In this case the pixel is sampled at a rate of 33.3 Hz, if a higher rate is needed the problem become even worse. When the image lag begins to be a problem the only solution is reducing the imager frame rate. However, frame rates lower than 30 Hz will not produce the effect of smooth dynamic frames to the human eyes. To solve this problem a new approach is proposed here by the use of the free drain terminal of the reset transistor of the 3T APS presented in Fig. 3.8.

This is done by applying a low pulse to the RDR terminal in Fig. 3.8 just after the readout operation. An example of such operation is presented in Fig. 3.12, where after each frame readout operation a low RDR pulse of 0.1 μs is applied to establish the pseudo reset for the full logarithmic mode. The output readout operation has a period of 30 ms and the low light conditions are represented by the photocurrents of 1 fA, 10 fA, and 100 fA.

The results presented in Fig. 3.12 show that the image lag is completely suppressed by the use of the proposed method. No perceptible image lag was observed among the four consecutive frames F1, F2, F3, and F4 in each of the three groups.

This method is critical to very low light condition due to the low sensitivity of the full logarithmic mode. Nevertheless, this weakness can be compensated by the use of complementary-mode sensors as will be shown next.

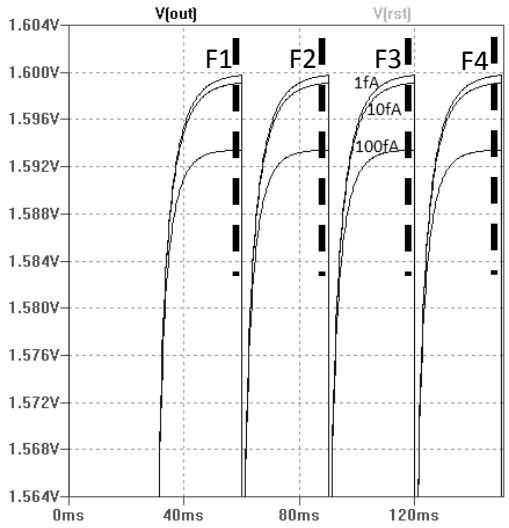


Figure 3.12- Full logarithmic mode with the proposed pseudo reset [art prepared by the author].

3.5 Image Lag in Complementary-Mode Sensors

As pointed in the previous chapter, image lag is one of the main problems in complementary-mode sensors. In section 2.2 it was shown that the hard reset approach proposed by Wäny [47] can be used to suppress image lag in this complementary mode. However it causes other problems as gate-oxide overstress. To solve the image lag problem together while avoiding gate-oxide overstress, in this work we also propose the application of the pseudo-flash reset to the complementary mode sensor. It is shown to be as effective as in the linear mode proposed in [16], and also as in the proposed application for the full logarithmic mode.

The output voltage of four consecutive frames of the pixel of Fig. 3.8 operating in complementary mode is presented in Fig. 3.13. The simulations were performed with reset low voltage level of 2.5 V with a period of 1 μs, and integration time of 30 ms. The low illumination level at which the pixel is subject is 1 fA, 10 fA, and 100 fA. The four samples F1, F2, F3, and F4 are taken at the end of integration and the image lag is clearly seen in the results.

The output voltage of four consecutive frames of the pixel of Fig. 3.8 operating in complementary mode with the inclusion of the pseudo-flash reset is presented in Fig. 3.14. For these simulations the RDR signal has a period of 30 ms, and a pulse width of 0.1 μs, the RDR pulse starts 0.05μs before the beginning of the reset time. The reset time has a period of 30 ms and a pulse width of 1 μs. The low illumination level at which the pixel is subject is 1 fA, 10 fA, and 100 fA, and the four samples F1, F2, F3, and F4 are taken at the end of integration. These results show that the image lag is completely overcome by the use of the pseudo-flash reset.

So far the use of the individual routing of the drain terminal of the reset transistor of the basic 3T APS has shown to be useful to reduce image lag in the pixel operating either in linear, or full logarithmic mode, as well as in the complementary mode.

Basically to reduce image lag using the pseudo-flash reset, it requires only that the low RDR voltage level to be lower than the sense node voltage level at the end of integration time [16]. However, while bringing it directly to GND requires only a basic digital gate cell, as an inverter, bringing it to any intermediary voltage level between V_{DD} and GND requires a dedicated analog circuit control.

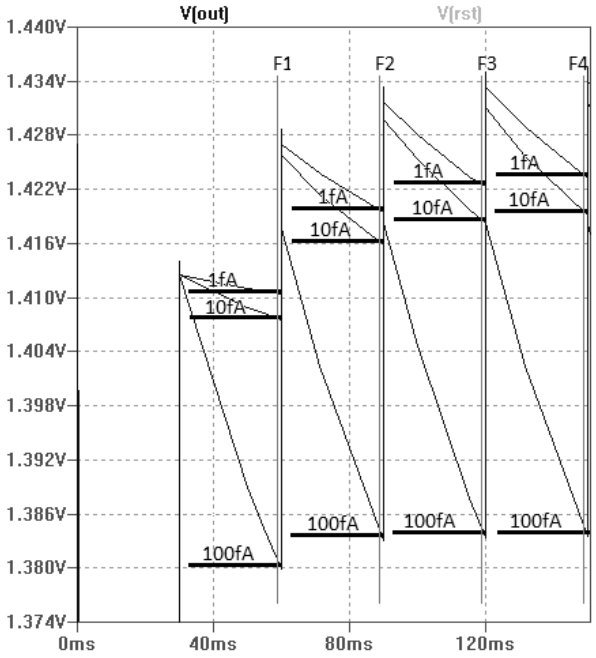


Figure 3.13- Complementary-mode sensor output with image lag [art prepared by the author].

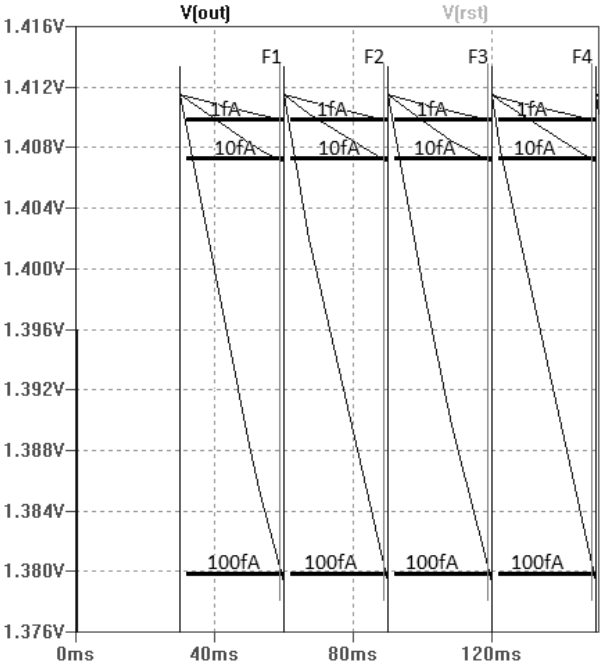


Figure 3.14- Complementary-mode sensor output without image lag [art prepared by the author].

To implement pseudo-flash reset to execute the function for which it was devised in [16], that is suppressing image lag, it is enough just bringing RDR signal to GND during the appropriate time interval. However, as it will be shown in Chap. V, there are other useful functions that can be implemented using the drain reset terminal with analog control. In this work a new function for the use of the RDR terminal is proposed, that is the establishment of voltage reference points which can be used to compensate FPN, improving therefore image quality.

Chapter IV: Fixed-Pattern Noise

When a single pixel array as that shown in Fig. 3.8 is fabricated, mismatches in its devices in relation to the designed version will hardly cause any significant effect. However, in an array of any dimension, as that shown in Fig. 4.1, device and interconnection mismatches cause image distortions called fixed-pattern noise.

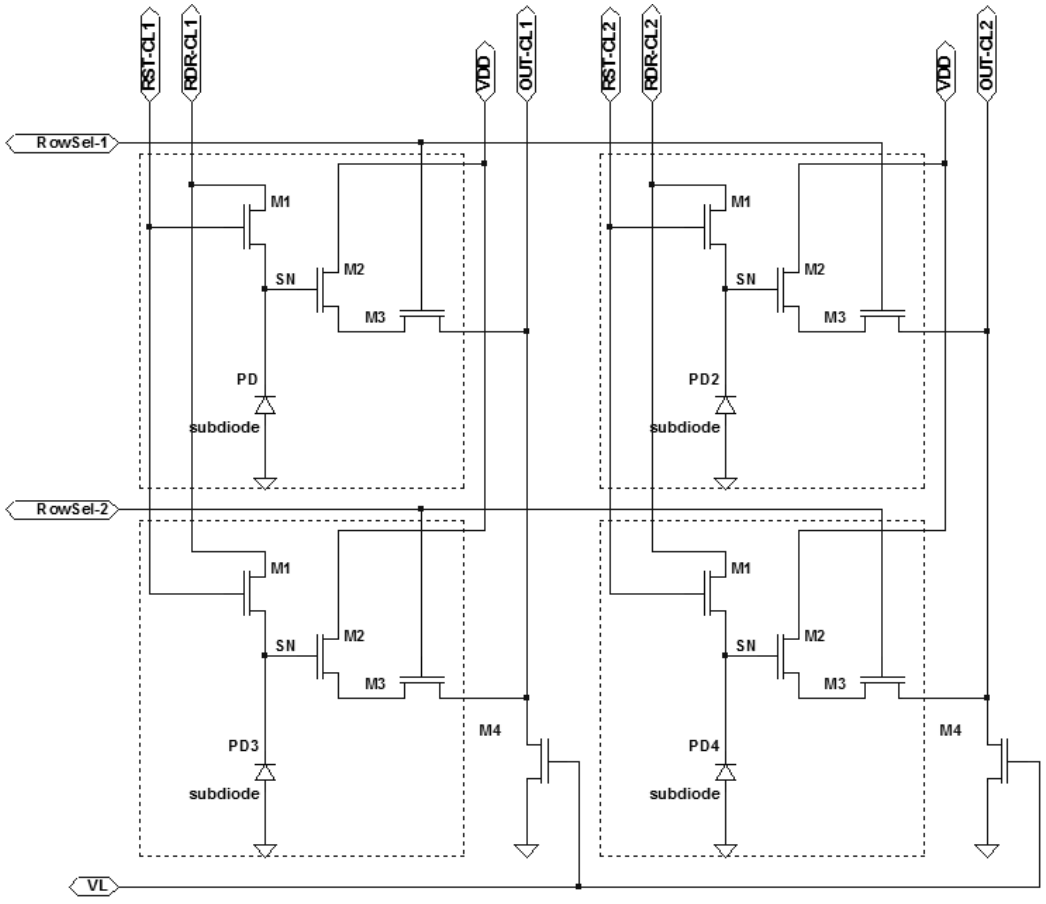


Figure 4.1- Example of a 2x2 pixel array with shared column amplifiers M_4 [art prepared by the author].

Fixed-pattern noise (FPN) is not noise in the strict sense of the word, as temporal noise. FPN are non-idealities that cause image distortions, and are results of device and interconnection mismatches across the pixel array. Basically FPN results in slight voltage output differences among the pixels of the array, i.e. the 2x2 array presented in Fig. 4.1, when they are subject to spatially uniform light illumination.

An example of FPN in a pixel array with eight rows and eight columns is shown in Fig. 4.2. This example presents the ideal expected image result on the top of each pair of images, and the FPN distorted image result on the bottom of each pair of images. As the mismatches are random events that happen during fabrication, it is not possible to predict where in the array they will take place, neither how strong they will be. In all cases,

whether FPN level is relevant or not, the design of CMOS image sensor requires a way to reduce these image distortions.

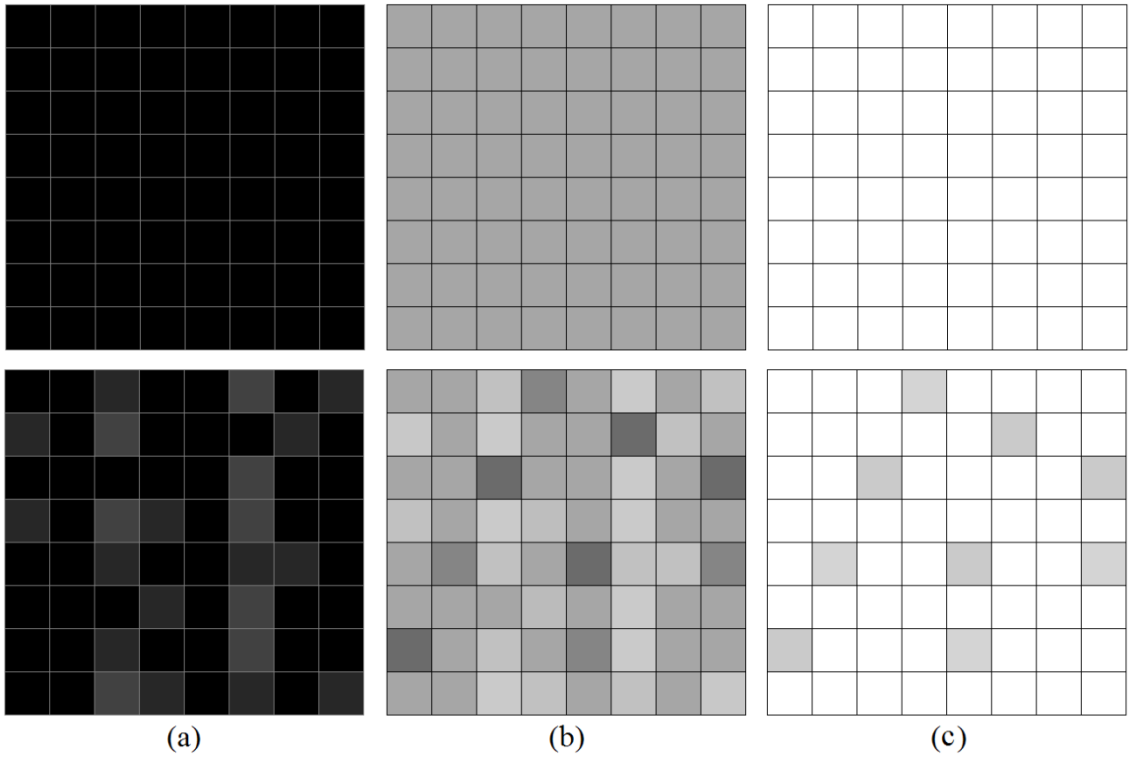


Figure 4.2- Pixel array example with ideal and FPN distorted image results under three different illumination levels (a) under dark condition, (b) under moderate light condition, and (c) under high light condition [art prepared by the author].

To determine the array FPN magnitude, for a given uniform light intensity level, the first step is the calculation of the mean output value of the pixel array. The mean output value would be the value of all the pixels in the array, if it were hypothetically free from fabrication non-idealities, as the images on the top of Fig. 4.2. It is usually the average output of all the pixels in the array. For each irradiance level x, the mean output value, μ_x, is calculated as shown in Eq. (4.1), where n_p is the number of pixels of the array, and $V_{o,x}(m, n)$ stands for the samples of each pixel (m, n) of the array.

The standard spatial deviation of the array, as estimated in Eq. (4.2), determines its FPN magnitude, where $(\sigma_x)^2$ is the spatial variance and σ_x is the standard spatial deviation. The variance is estimated using the number of pixels n_p minus one (n_p - 1). The array FPN must be recalculated for each different light condition.

$$\mu_x = \frac{1}{n_p}\sum_{m=1}^{M}\sum_{n=1}^{N} V_{o,x}(m,n) \tag{4.1}$$

$$\sigma_x^2 = \frac{1}{n_p - 1}\sum_{m=1}^{M}\sum_{n=1}^{N}\left(V_{o,x}(m,n) - \mu_x\right)^2 \tag{4.2}$$

In the simulation stage of the design, devices and interconnection mismatches must be introduced in the circuit schematic in order to investigate and analyze both the raw FPN and the residual FPN after treatment. The standard way to perform this analysis is via

Monte Carlo Simulations. However, a simpler method for faster analysis was devised and is presented next. Afterwards, the results of the proposed method of analysis are compared with the results of Monte Carlo Simulations. It is important pointing out that only the FPN introduced by the transistors of the pixel is investigated with the simulation results. As the foundry does not have models for the photodiodes, the FPN introduced by the photodiode will not be considered in the simulation but will be discussed in the experimental results.

4.1 Simplified FPN Analysis

The proposed analysis method consists in using two 3T APS, similar to that shown in Fig. 3.8, with individual routing for the drain terminal of the reset transistor. The first APS is kept as reference "APS A", with the dimensions of all its transistors as indicated on the left of table 4.1. The second APS, "APS B", is designed following the same patterns of "APS A" except for slight dimension changes in some of its transistors, emulating distortions such as FPN to be quantified and treated. The deviations in the W dimension of the transistors of the "APS B", in relation to the reference one, are applied as shown on the right side of table 4.1. In this table ΔW is the deviation, the first number in the index stands for the transistor number in the pixel, whereas the second number in the index stands for the number of the pixel.

Table 4.1: Induced deviations in the W dimensions of the transistors of the "APS B"

APS A (reference)	**APS B**
W_{1_pixA} = 0.7 µm/ L_{1_pixA} = 0.35 µm	$W_{1\_pixB} = W_{1\_pixA} \pm \Delta W_{1\_pixA}$/ $L_{1\_pixA} = L_{1\_pixB}$
W_{2_pixA} = 0.7 µm/ L_{2_pixA} = 0.35 µm	$W_{2\_pixB} = W_{2\_pixA} \pm \Delta W_{2\_pixA}$/ $L_{2\_pixA} = L_{2\_pixB}$
W_{3_pixA} = 0.7 µm/ L_{3_pixA} = 0.35 µm	$W_{3\_pixB} = W_{3\_pixA} \pm \Delta W_{3\_pixA}$/ $L_{3\_pixA} = L_{3\_pixB}$
W_{4_pixA} = 0.7 µm/ L_{4_pixA} = 0.35 µm	$W_{4\_pixB} = W_{4\_pixA} \pm \Delta W_{4\_pixA}$/ $L_{4\_pixA} = L_{4\_pixB}$

As previously pointed out, the column FPN produced by the column amplifier, transistor M_4 in Figs. 3.8 and 4.1, is the most serious additional source of FPN in CMOS image sensors [11, 15]. This kind of FPN appears as vertical stripes as shown in the image presented in Fig. 1.10. In order to study the FPN produced by mismatches of either the column amplifier or the other transistors in the pixel, the mismatches are deliberately introduced by modifications of some dimensions of the devices used in the pixel.

In the reference APS, each of the four transistors of the reference pixel M_1, M_2, M_3, and M_4 have W and L dimensions of 0.7µm and 0.35µm respectively. To investigate and treat FPN between "APS A" and "APS B", changes of ±1%, ±5%, ±10% and ±20% are arbitrarily applied to the W dimension of each of the four transistors of the second pixel. These are preliminary analyses performed to evaluate the FPN compensation technique proposed in this work, which will be presented in the next chapter. More accurate analyses based on Monte Carlo simulations are also presented later both in this chapter and in the next.

4.2 Distortion Introduction for Simplified FPN Analysis

When two different APS circuits, under the same illumination level, are biased by the same set of control signals, the output voltage differences between them come out of device mismatches introduced by fabrication non-idealities. The same output voltage difference between the "APS A" and "APS B" can be produced in several different ways as mismatches of W/L dimensions, gate-oxide thickness, doping concentration, threshold voltage, etc. The output voltage difference between "APS A" and "APS B" is called hereby voltage FPN.

The resultant voltage FPN between "APS A" and "APS B" when one of the four transistors of the "APS B" has its W dimension 10% different from the reference APS, can also be produced by some other combination of L, and or gate-oxide thickness mismatches. Therefore, a simple way to study FPN effects between two similar APS circuits, as well as techniques to reduce them, is by applying slight differences in the W dimensions of the transistors of one of the APS circuits while the other is kept as reference.

The presented results employ the complementary linear-logarithmic mode for both APSs with the following control-signal setup: The V_{DD} voltage level is 3.3 V; the VL voltage level is set to 0.8 V; the RST signal is a pulse with low level set to 2.5 V, high level set to 3.3 V, time period of 31 ms, pulse width of 1 ms and rise and fall time of 0.1ns; the RowSel signal may be active only during the output sampling, though in the present simulation this signal was always at V_{DD} level. The photocurrent representing light intensity varies from 0.1 fA in dark condition to 20 μA in very bright condition. The RDR signal in the following simulations is set to V_{DD}.

The total output voltage FPN between "APS A" and "APS B" when W_4 of the "APS B" is 10% wider than that of the "APS A" within the whole light illumination range, and along the whole operational cycle, is shown in Fig. 4.3. In Fig. 4.3 Vout1 is the output voltage of the "APS A" and Vout2 is the output voltage of the "APS B". Fig. 4.4 shows the total output voltage FPN when W_4 is 10% narrower than that of the "APS A". The dashed lines in both plots are the instant at the end of integration time where the output is to be sampled.

The output voltage FPN as a function of the light illumination level is produced by sampling each curve shown in Figs. 4.3 and 4.4 at the end of integration time, for the various different light levels. The result of this procedure for the positive difference between the W dimensions of the transistor M_4 of the "APS B" in relation to that of "APS A" is shown in Fig. 4.5. Had both APSs no dimension deviation, the plot of Fig. 4.5 would have been null within the whole light intensity range.

The total output voltage FPN between "APS A" and "APS B" operating in CMS mode and the total output voltage FPN between the same two APSs operating in linear mode are plotted together in Fig. 4.6. Comparing both results it is observed that for low light illumination both CMS and linear mode show the same output voltage FPN level as expected. On the other hand, in moderate and high light illumination the linear mode seems to yield better results. However, it is not as it appears because as the light level increases the linear mode output response quickly saturates as shown in Fig. 1.17.

Therefore, for high light conditions only the FPN result of the APS operating in CMS mode is taken into account.

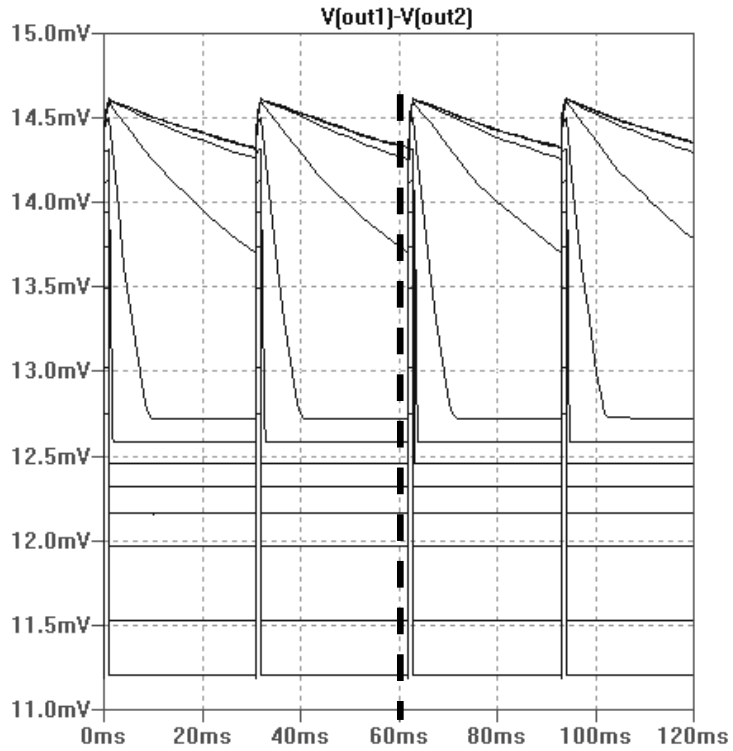


Figure 4.3- Total FPN with W_4 of the "APS B" 10% wider [art prepared by the author].

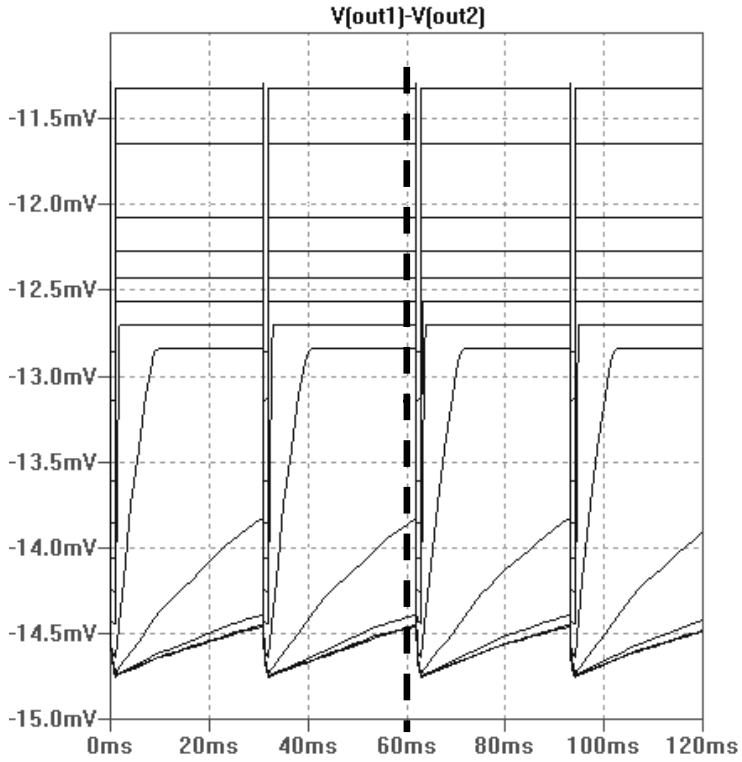


Figure 4.4- Total FPN with W_4 of the "APS B"10% narrower [art prepared by the author].

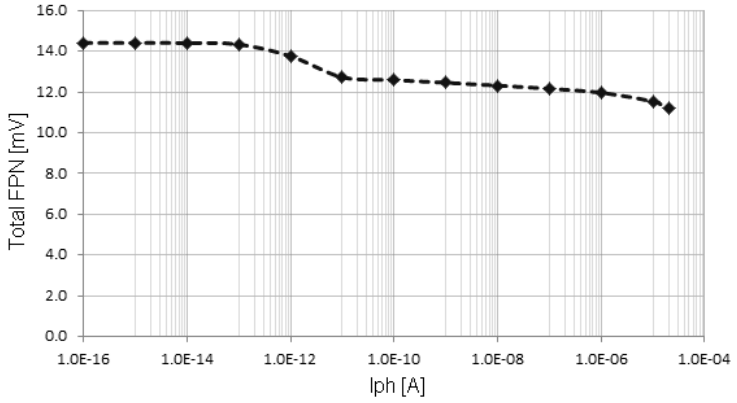


Figure 4.5- Total FPN for W_4 of the "APS B" 10% different from the reference [art prepared by the author].

The different transistors in the pixel produce different results of FPN voltage level against light illumination as will be shown in the next diagrams. The following results are for the transistors M_1, M_2 and M_3 with W dimension 10% wider than that of the reference APS. The plot shown in Fig. 4.7 is the total FPN result when W_1 of the "APS B" is 10% wider than that of the reference pixel.

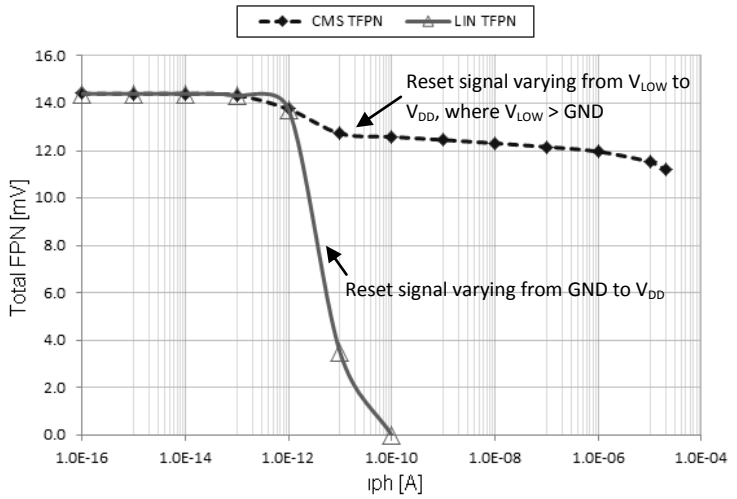


Figure 4.6- Total FPN for W_4 of the "APS B" 10% different from the reference for CMS and linear mode [art prepared by the author].

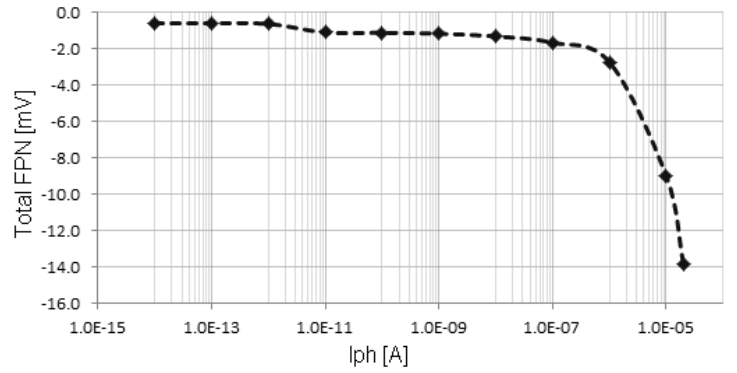


Figure 4.7- Total FPN for W_1 of the "APS B" 10% different from the reference [art prepared by the author].

The plots shown in Figs. 4.8 and 4.9 are the total FPN results when W_2 and W_3 of the "APS B" is 10% wider than the reference pixel respectively. It is worth to point out that in three figures, namely Figs. 4.7, 4.8, and 4.8 the signal of the total FPN result is different from that produced when the same differences are applied to the transistor M_4 as shown in Fig. 4.4. Each transistor in the pixel has a different influence pattern in the total FPN voltage against the light intensity. The same difference applied to the different transistors in the pixel produces results with different signal and amplitude variations with light intensity.

The signal of the response depends upon the direction the current flows through the transistor, toward or backward the output node. In the transistor M_4 the current flows away from the output node, whereas in the transistors M_1, M_2 and M_3 the current flows towards the output node.

The amplitude variation of each plot with the light intensity is quite different from each other. Only that produced by M_1 is deviates a lot from the form produced by the other three. The higher amplitude throughout the whole light intensity is that produced by the transistor M_4. The lowest amplitude variations are those produced by the transistors M_1 and M_3, but that of M_1 increases considerably in the high light region.

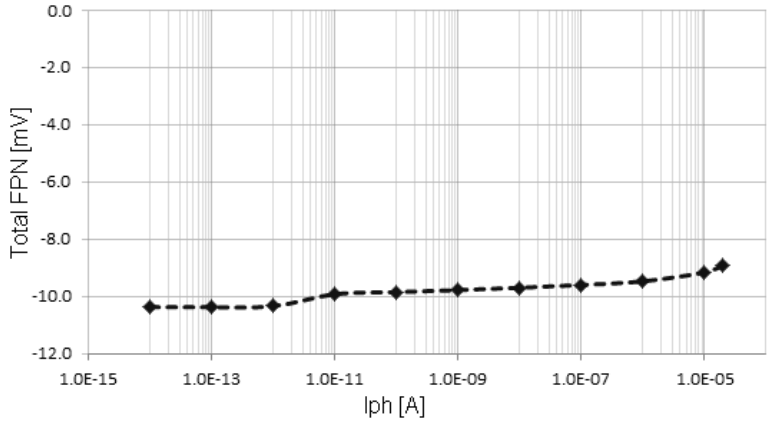


Figure 4.8- Total FPN for W_2 of the "APS B" 10% different from the reference [art prepared by the author].

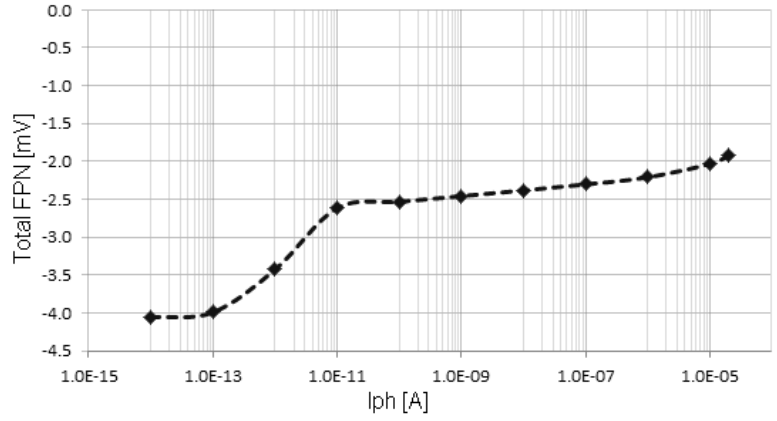


Figure 4.9- Total FPN for W_3 of the "APS B" 10% different from the reference [art prepared by the author].

4.3 Induced FPN with Variations in the W Dimension

The output voltage FPN induced by deviations applied only to the W dimension of the reset transistor M_1 of the "APS B", as shown in table 4.2, are presented in the following set of curves. The curves shown in Fig. 4.10 are the output voltage FPN when the deviations ΔW_{1_pixA} are 1%, 5%, 10% and 20% respectively.

As the deviation of W_1 of the "APS B" increases in relation to that of the reference APS, the output voltage FPN increases almost at the same rate, which can be observed comparing the four sets of curves. Other important detail with relation to deviations in the W dimensions of the reset transistor is that the output voltage FPN increases considerably in the high light region when compared with the same deviation in other transistors of the pixel as shown next.

Table 4.2: Deviations of W1 of the "APS B"

APS A (reference)	**APS B**
W_{1_pixA} = 0.7 µm/ L_{1_pixA} = 0.35 µm	$W_{1\_pixB} = W_{1\_pixA} \pm \Delta W_{1\_pixA}$/ $L_{1\_pixA} = L_{1\_pixB}$
W_{2_pixA} = 0.7 µm/ L_{2_pixA} = 0.35 µm	$W_{2\_pixB} = W_{2\_pixA}$ / $L_{2\_pixA} = L_{2\_pixB}$
W_{3_pixA} = 0.7 µm/ L_{3_pixA} = 0.35 µm	$W_{3\_pixB} = W_{3\_pixA}$ / $L_{3\_pixA} = L_{3\_pixB}$
W_{4_pixA} = 0.7 µm/ L_{4_pixA} = 0.35 µm	$W_{4\_pixB} = W_{4\_pixA}$ / $L_{4\_pixA} = L_{4\_pixB}$

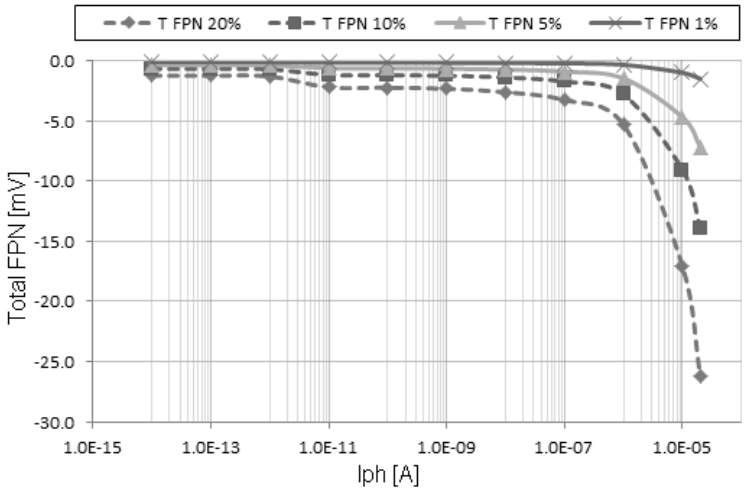


Figure 4.10- Total FPN for W_1 of the "APS B" 1%, 5%, 10% and 20% different from the reference APS [art prepared by the author].

The output voltage FPN induced by deviations applied only to the W dimension of the source follower transistor M_2 of the "APS B", as shown in table 4.3, are presented in the following set of curves. The curves shown in Fig. 4.11 are the output voltage FPN when the deviations ΔW_{2_pixA} are 1%, 5%, 10% and 20% respectively.

Table 4.3: Deviations of W_2 of the "APS B"

APS A (reference)	**APS B**
W_{1_pixA} = 0.7 μm/ L_{1_pixA} = 0.35 μm	$W_{1\_pixB} = W_{1\_pixA}$ / $L_{1\_pixA} = L_{1\_pixB}$
W_{2_pixA} = 0.7 μm/ L_{2_pixA} = 0.35 μm	$W_{2\_pixB} = W_{2\_pixA} \pm \Delta W_{2\_pixA}$/ $L_{2\_pixA} = L_{2\_pixB}$
W_{3_pixA} = 0.7 μm/ L_{3_pixA} = 0.35 μm	$W_{3\_pixB} = W_{3\_pixA}$ / $L_{3\_pixA} = L_{3\_pixB}$
W_{4_pixA} = 0.7 μm/ L_{4_pixA} = 0.35 μm	$W_{4\_pixB} = W_{4\_pixA}$ / $L_{4\_pixA} = L_{4\_pixB}$

When deviations in W_2 of the "APS B" make it wider than that of the reference APS, both shown in table 4.4, it produces an output-voltage FPN that increases almost at the same rate observed in Fig. 4.10, as happens with positive deviations in W_1 of the "APS B".

As light intensity increases the output voltage FPN, related to the source follower transistor M_2, slightly decreases as happens with the two other transistors M_3 and M_4. During the change from the linear region to the logarithmic region the variation of the output FPN voltage has the strongest variation with light intensity.

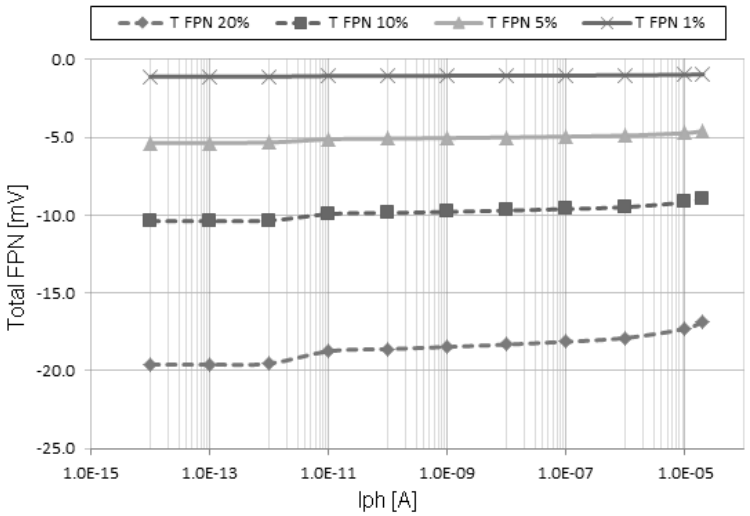


Figure 4.11- Total FPN for W_2 of the "APS B" 1%, 5%, 10% and 20% different from the reference APS [art prepared by the author].

The output voltage FPN induced by deviations applied only to the W dimension of the access transistor M_3 of the "APS B", as shown in table 4.4, are presented in the following set of curves. The curves shown in Fig. 4.12 are the output voltage FPN when the deviations ΔW_{3_pixA} are 1%, 5%, 10% and 20% respectively.

When deviations in the W dimension of the row selector transistor M_3 of the "APS B", the transistor's dimensions of which are shown in table 4.4, make it wider than that of the reference APS, the output voltage FPN also increases almost at the same rate, as observed comparing the four sets of curves shown in Figs. 4.10 and 4.11. As light intensity increases, the output voltage FPN, related to the row select transistor M_3, slightly decreases as with the two other transistors M_2 and M_4.

Table 4.4: Deviations of W_3 of the "APS B"

APS A (reference)	**APS B**
W_{1_pixA} = 0.7 µm/ L_{1_pixA} = 0.35 µm	$W_{1\_pixB} = W_{1\_pixA}$ / $L_{1\_pixA} = L_{1\_pixB}$
W_{2_pixA} = 0.7 µm/ L_{2_pixA} = 0.35 µm	$W_{2\_pixB} = W_{2\_pixA}$ / $L_{2\_pixA} = L_{2\_pixB}$
W_{3_pixA} = 0.7 µm/ L_{3_pixA} = 0.35 µm	$W_{3\_pixB} = W_{3\_pixA} \pm \Delta W_{3\_pixA}$/ $L_{3\_pixA} = L_{3\_pixB}$
W_{4_pixA} = 0.7 µm/ L_{4_pixA} = 0.35 µm	$W_{4\_pixB} = W_{4\_pixA}$ / $L_{4\_pixA} = L_{4\_pixB}$

As it happens with the transistor M_2, during the change from the linear region to the logarithmic region, the variation of the output FPN voltage has the highest variation with light intensity. Among the three transistors M_2, M_3 and M_4, through which the output column current flows, the lowest output voltage FPN variation within the whole light-intensity range is that produced by the M_3 transistor.

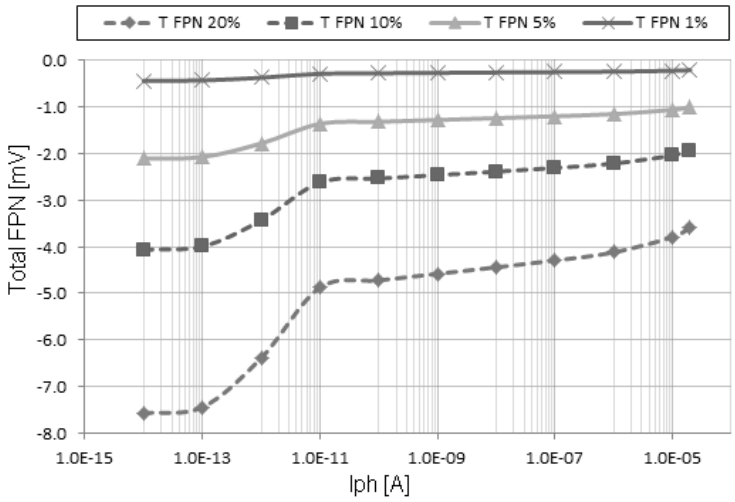


Figure 4.12- Total FPN for W_3 of the "APS B" 1%, 5%, 10% and 20% different from the reference APS [art prepared by the author].

The output voltage FPN induced by deviations applied only to the W dimension of the column amplifier transistor M_4 of the "APS B", as shown in table 4.5, are presented in the following set of curves. The curves shown in Fig. 4.13 are the output voltage FPN when the deviations ΔW_{4_pixA} are 1%, 5%, 10% and 20% respectively.

Table 4.5: Deviations of W_4 of the "APS B"

APS A (reference)	**APS B**
W_{1_pixA} = 0.7 µm/ L_{1_pixA} = 0.35 µm	$W_{1\_pixB} = W_{1\_pixA}$ / $L_{1\_pixA} = L_{1\_pixB}$
W_{2_pixA} = 0.7 µm/ L_{2_pixA} = 0.35 µm	$W_{2\_pixB} = W_{2\_pixA}$ / $L_{2\_pixA} = L_{2\_pixB}$
W_{3_pixA} = 0.7 µm/ L_{3_pixA} = 0.35 µm	$W_{3\_pixB} = W_{3\_pixA}$ / $L_{3\_pixA} = L_{3\_pixB}$
W_{4_pixA} = 0.7 µm/ L_{4_pixA} = 0.35 µm	$W_{4\_pixB} = W_{4\_pixA} \pm \Delta W_{4\_pixA}$/ $L_{4\_pixA} = L_{4\_pixB}$

The largest output voltage FPN is that produced by the column amplifier transistor M_4 of the pixel in Fig. 3.8. When deviations increase in the W dimensions of the transistor M_4 of the "APS B" in relation to the reference APS, the output voltage FPN also increases almost at the same rate as observed comparing the four sets of curves shown in Figs. 4.10, 4.11, and 4.12. As light intensity increases, the output voltage FPN, related to the column amplifier transistor M_4, slightly decreases as happens with the two other transistors M_2 and M_4.

As happens with the transistors M_2 and M_3, during the change from the linear region to the logarithmic region the variation of the output FPN voltage has the highest variation with light intensity. Among the three transistors M_2, M_3 and M_4, through which the output column current flows, the highest output voltage FPN variation within the whole light intensity range is that produced by the transistor M_4.

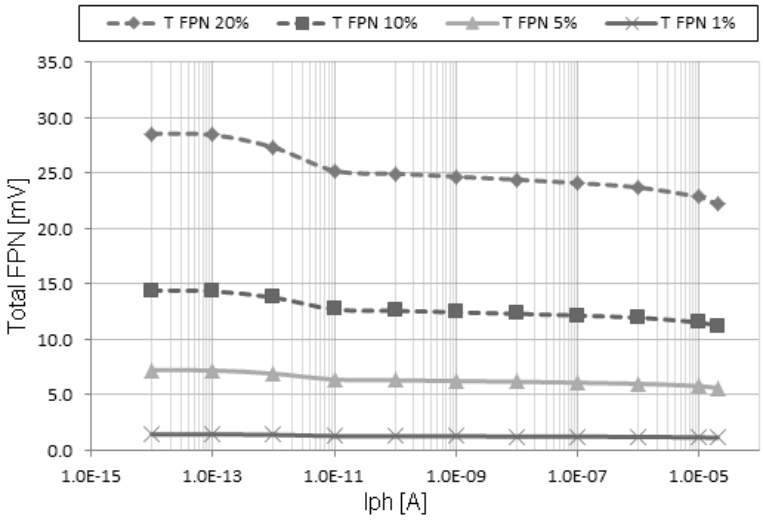


Figure 4.13- Total FPN for W_4 of the "APS B" 1%, 5%, 10% and 20% different from the reference APS [art prepared by the author].

4.3 Pixel FPN with the Monte Carlo Analysis

The results presented above are useful to perform a simple analysis of two different circuits with a single parameter variation in one of their devices. The Monte Carlo analysis suits far better for multi-parameter variation. However, the Monte Carlo analysis requires more powerful simulation tools, and the availability of variation models, to be performed than the previous analysis presented above.

To emulate the FPN distortion across an array of 256 elements, Monte Carlo simulations were performed in the Cadence Virtuoso V. 6.1.5 sub-version IC6.1.5.500.132. These simulations were performed in the pixel of Fig. 3.8, designed in the AMS CMOS 0.35 μm technology. Three types of FPN analyses were performed. The first analysis is the column FPN that is performed with mismatches only of the column amplifier transistor M_4. The second analysis is the FPN along a column that is performed with mismatches of the three transistors of the pixel M_1, M_2 and M_3. And the third analysis is the FPN across the array that is performed with mismatches of M_1, M_2, M_3 and M_4.

The setup of the control signal was adjusted for the linear-logarithmic operation with the V_{DD} voltage of 3.3 V, the reset low level is fixed at 2.5 V. The illumination level is represented by photocurrents varying from 1 fA to 10 μA.

The results presented here are the mean and standard deviation of the voltage output of the pixel of Fig. 3.8 of the 256 Monte Carlo simulations for each photocurrent. These values are determined by Eq. (4.1) and Eq. (4.2) respectively. The mean voltage output curve is presented in Fig. 4.14, which curve is similar for the three types of analysis. The voltage FPN curves for the three different analyses are shown in Fig. 4.15. The column FPN, where only mismatches of M_4 are taken into account, is indicated by the curve "COLUMN FPN", the array FPN, where the mismatches of M_1, M_2, M_3, and M_4 are considered, is indicated by the curve "ARRAY FPN", and the FPN along a column, where the mismatches of M_1, M_2, and M_3 are considered, is indicated by the curve "A-COL FPN".

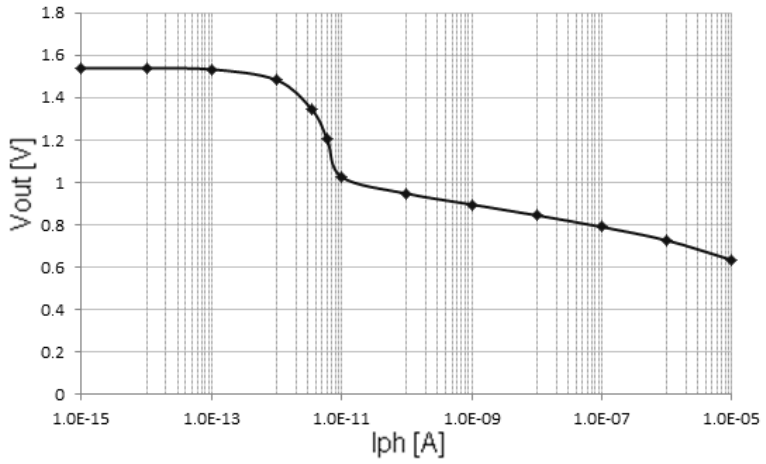


Figure 4.14- Mean voltage output versus illumination level [art prepared by the author].

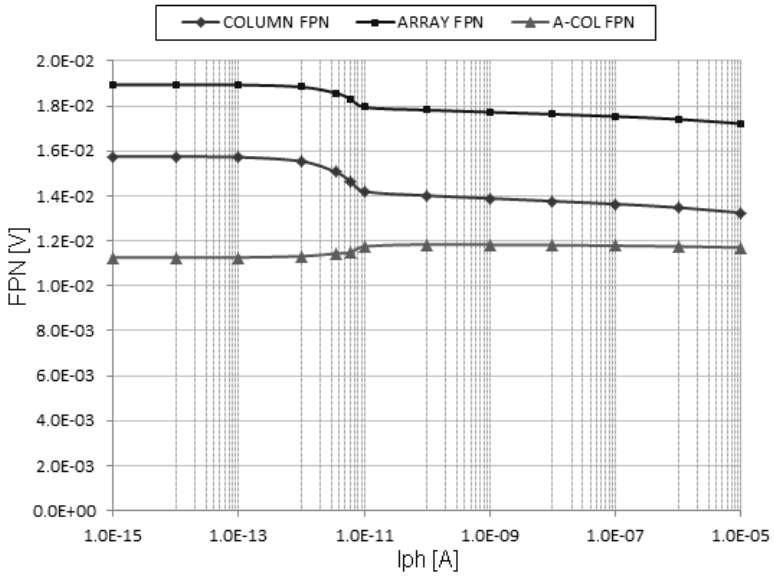


Figure 4.15- Voltage FPN for the three different analyses [art prepared by the author].

It is important noticing that the magnitude of the column FPN yielded by the Monte Carlo simulations is close to that of the curve "T FPN 10%" presented in Fig. 4.13. The Monte Carlo simulation for a single photocurrent is very time consuming, thus the

variation of each individual transistor is not individually analyzed as in the previous case with the simplified analysis. Instead it is more efficient to study the variance of many transistors per simulation, as shown by the curves ARRAY FPN and A-COL FPN presented in Fig. 4.15.

The results presented in Fig. 4.15 show that the column FPN, has a large contribution to total array FPN. As said before, the photodiode also presents a great contribution to the total array FPN. However, there is no simulation model for this device. Actually, the model for diodes is a very simple one that is not as reliable as those for the transistors. Therefore, while a reliable model for photodiodes is not available, it is more efficient to investigate the photodiode FPN directly in the fabricated array. In the next chapter the proposed technique to reduce FPN will be presented.

Chapter V: Simplified Technique to Attenuate Fixed-Pattern Noise

Concerning the complementary-mode sensors (CMS) there are few methods found in the literature dealing with FPN compensation, which will be presented and discussed in this chapter. The FPN compensation technique proposed in this work is also presented in this chapter. The proposed technique makes use of the individual connection of the drain of the reset transistor of the APS in Fig. 3.8. This connection is employed to produce a pixel-level voltage reference that is thus applied to perform FPN compensation in either pure logarithmic or linear-logarithmic mode of operation. The proposed FPN compensation method can be applied to the basic 3T APS so that the pixel size can be kept as small as possible. Moreover, it can be executed at the same rate of a regular CDS operation.

5.1 Source of Fixed-Pattern Noise in CMOS APS

In the previous chapter the raw output voltage FPN due to variations in each of the four transistors of the basic 3T APS were presented. Other source of spatial distortions is the FPN introduced by the photodiode that will be treated only in the experimental results. Besides spatial distortion, sources of temporal noise in CMOS image sensors are also to be considered.

The main sources of noise in CMOS APS image sensors, which are present in the signal after a readout operation, are:

a) shot noise, that occurs during integration time and is inherent to the photon flux and to carrier thermal generation in the detector;

b) reset (kT/C) noise in M_1, due to charging nodes through a resistive channel during reset time. Accurate analysis reported in [16] shows that reset noise power is closer to ($kT/2C$) when the sub-threshold current in M_1 does not reach steady state during reset time, especially in low light condition;

c) readout circuit noise, caused by device thermal and flicker noise;

d) offset FPN due to device and connection mismatches – especially those of the pixel source-follower FET-, and also by dark current variation known as dark-signal non uniformity (DSNU);

e) gain FPN often referred to as photo-response non uniformity (PRNU) [52].

The offset FPN and reset (kT/C) noise are basically the only components, among all the described sources of noise, which can be suppressed by performing DSRS [9].

Referring to the pixel in Fig. 3.8, M_1 is the reset transistor, PD is the photodiode, SN is the sense node where the photodiode light-dependent voltage is developed, M_2 is the source-follower transistor, M_3 is the pixel access transistor and M_4 is the column-current-

load, in the drain terminal of which the output voltage V_o is developed. Offset FPN is mostly found in M_2, M_3 and M_4, as shown in the previous chapter, where M_2 and M_3 produce offset FPN in the pixel region and M_4 produces the offset FPN on the column line.

While M_2 is operating in strong inversion ($V_{GS} > V_{TH}$) and M_4 is operating in the saturation region ($V_{DS} > V_{GS} - V_{TH}$), the offset FPN of M_2, M_3 and M_4 is found to be quite independent of the SN *voltage* [16].

The output voltage as in Eq. (5.1), according to the model given in [15], shows that the offset FPN in M_2 may be due to variations in $V_{TH,2}$, W_2 and L_2; in M_3 the variations are concentrated in its channel resistance $r_{DS,3}$; and the column offset FPN is mainly due to variations in I_{BIAS-0}, the bias current of M_4. The column storage capacitance, that is the total capacitance of the column line and does not appear in this model, is also a source of readout offset FPN. These sources are always present in any readout operation.

$$V_O \approx V_{SN} - \left(V_{TH,2} + \sqrt{\frac{2I_{BIAS-0}}{\mu_N C_{OX}\left(W_2 / L_2\right)}} \right) - r_{DS,3} I_{BIAS-0} \qquad (5.1)$$

The kind of noise present in the sense-node voltage V_{SN} depends on the pixel operation mode, whether in the linear or the logarithmic mode. If it is operating in linear mode, the V_{SN} model is given by Eq. (5.2) else it is given by Eq. (5.3), where $V_{G,1}$ is given by Eq. (5.4).

$$V_{SN} \approx V_{DD} - V_{TH,1} - \frac{\left(A_D J_{PH} + I_{DARK}\right) t_{INT} + C_{OL,1} V_{DD}}{C_D} \qquad (5.2)$$

$$V_{SN} \approx \frac{V_{G,1}}{n} - \frac{V_{TH,1}}{n} - v_T \ln\left[\frac{I_{PH} + I_{DARK}}{I_0 . \left(W_1 / L_1\right)} \right] \qquad (5.3)$$

$$V_{G,1} = \frac{V_{DD}}{x}; \;\; V_{TH,2} < V_{G,1} \le V_{DD} \qquad (5.4)$$

In both operational modes the common sources of offset FPN found in the transistor M_1 are its threshold voltage $V_{TH,1}$, its channel width W_1 and its channel length L_1. And in the photodiode the FPN sources are the dark current I_{DARK} and the photocurrent I_{PH}, where the photocurrent is given by the product of the diode surface area A_D and the photocurrent density J_{PH}.

In linear mode other three additional sources of offset FPN are found, the first is due to "feed-through" charge when M_1 is turned off $C_{OL,1}V_{DD}$, the second due to the capacitance of the sense node C_D, and the third due to the integration time t_{INT}.

Additional sources of offset FPN in the logarithmic mode are due to the sub-threshold slope factor n (typically between 1 and 2), and due to I_0 given in Eq. (5.5). The component I_0 is dependent upon the thermal voltage v_T (kT/q), the channel doping concentration N_{CH}, the channel-carrier mobility μ_N, the silicon permittivity ε_{Si}, and the surface potential ψ_S.

$$I_0 = \mu_N v_T^2 \sqrt{\frac{q \varepsilon_{Si} N_{CH}}{2\psi_S}} \qquad (5.5)$$

5.2 Double Sampling Subtraction Techniques

Although all the sources of offset FPN present in the transistors M_2, M_3 and M_4 can be reduced by CDS or DRS, only two of those sources found in M_1 and PD can be reduced by these methods, namely $V_{TH,1}$ and $C_{OL,1}$ found in Eq. (5.2). This occurs because in CDS the first sample does not include the integration time and the second does, as shown in Fig. 5.1(a). On the other hand in DRS the first sample includes the integration time and the second does not, as shown in Fig. 5.1(b).

In the logarithmic mode it is not possible to apply DSRS because in doing this, the very sensor signal would be cancelled unless it was possible to read the sense node with a reference signal. Such reference is a voltage or current signal applied directly on the sense node that does not change with light intensity. The reference signal would be either one that does not change with light variation or that has a voltage swing different from that of the main signal. Might there be a reference signal, then performing DSRS would yield signal results different from zero and therefore treatable.

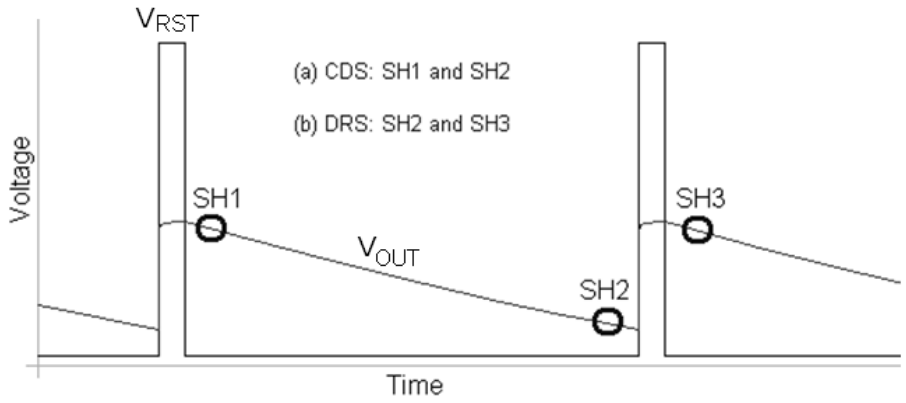


Figure 5.1- (a) Sampling sequence for CDS and (b) sampling sequence for DRS, similar to Fig. 14 from [9].

Figure 5.1 illustrates a case of constant illumination where the output voltage FPN present in the first sample of CDS and in the second sample of DRS are the same, as well as the second sample of CDS and the first sample of DRS as shown in Fig. 5.1. It is possible to apply DSRS by sampling twice the results of the pixel of Fig. 3.8 operating in linear mode, the first time at the beginning of integration time and the second time at the end of integration time, as shown in Fig. 5.2.

The results of the raw output S_{H2LIN} and the output after DSRS, $V_{sh1,\ sh2}$ that is S_{H1} subtracted from S_{H2}, are shown in Fig. 5.3. In comparison with the raw signal, after DSRS the output result suffers great reduction in the low light region. It is important noticing that when the pixel is operating in the linear mode after the raw output reaches the lowest voltage level, at the point indicated by the vertical bold line in Fig. 5.3, neither the raw output nor the output after DSRS have any useful meaning because the output voltage has reached the ground level.

Using the simplified analysis proposed in the previous chapter, for the pixel of Fig. 3.8 operating in linear mode, when the W dimension of the column-current-load transistor M_4

is 10% wider than that of the reference pixel, the output voltage FPN between both pixels is shown in Fig. 5.4 by curve T LIN, where T stands for total.

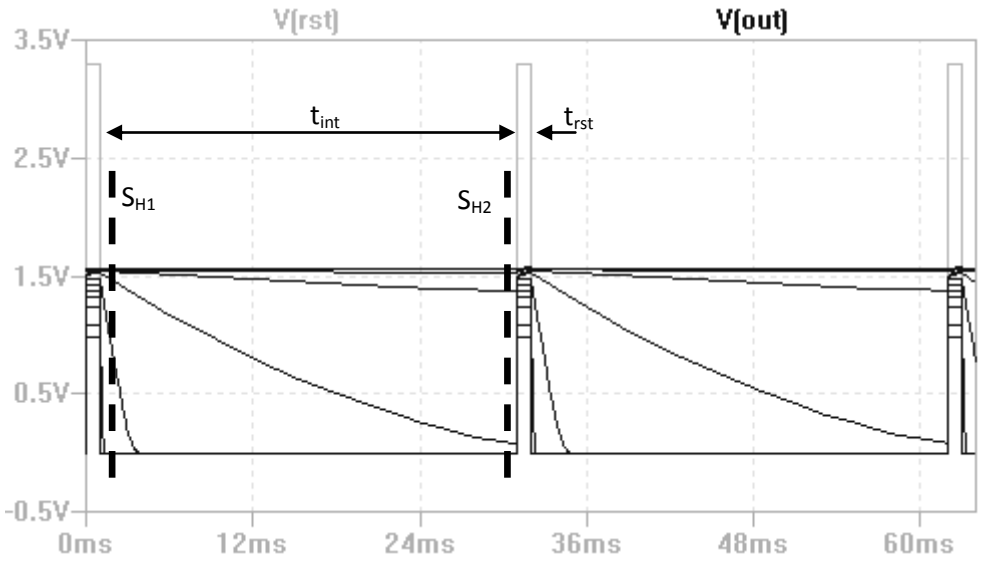


Figure 5.2- DSRS in the linear mode output voltage [art prepared by the author].

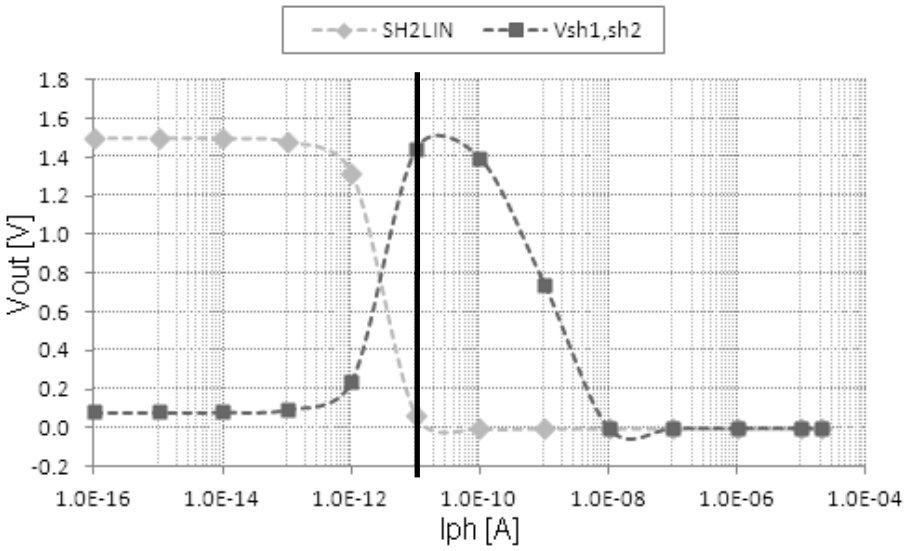


Figure 5.3- Output signal before and after DSRS in Linear mode [art prepared by the author].

The remaining voltage output FPN after the DSRS is shown in Fig. 5.4 by the curve R LIN, where R stands for residual, for the W dimension of M_4 of the altered pixel 10% wider than the reference pixel. In the low light region, where the linear mode of operation is most effective, the output voltage FPN is greatly reduced by applying DSRS correction. Nevertheless, when the pixel goes into high light condition, the DSRS compensation collapses and the FPN grows yet higher than that of the raw signal as shown by the arrows in the cross-section.

To evaluate the improvement conferred by the FPN compensation technique to the signal output the signal-to-noise ratio of the pixel must be used as a guideline. The signal-to-noise ratio (SNR), usually expressed in decibels (dB), is the ratio between the input

signal power to the average noise power [9, 31]. However, when both temporal noise and FPN distortions are considered to calculate this ratio, it is more adequate to call it signal-to-noise-and-distortion ratio (SNDR), as pointed in [13]. This is due to the fact that residual FPN is rather a fixed spatial distortion associated to the pixel array than a dynamic quantity fluctuating over time.

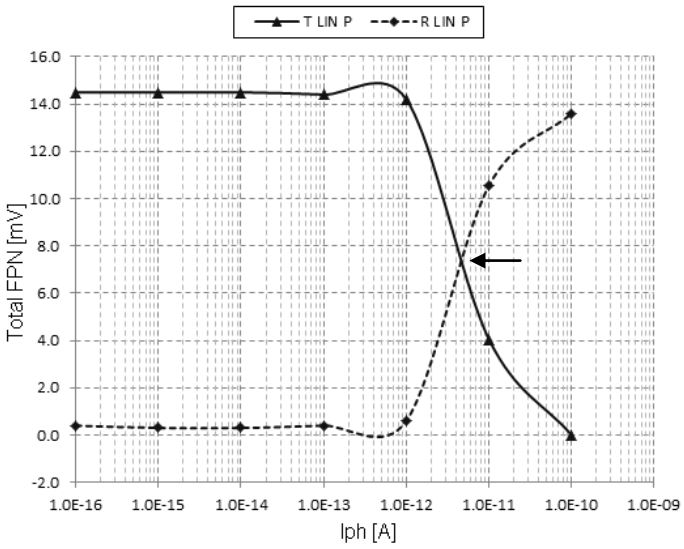


Figure 5.4- Output voltage FPN between "APS A" and "APS B" where W_4 of the "APS B" is 10% wider than the reference pixel, T and R stand for total and residual respectively [art prepared by the author].

The SNDR for the linear mode is determined as shown in Eq. (5.6), where the input signal is the voltage variation at the sense node, and the square root of the denominator is the average input referred noise power. The voltage variation at the sense node ΔV_{SN}, defined in Eq. (5.7), is a function of the photocurrent and integration time, where K is the gain of the source follower amplification. In the square root of the denominator, the component of temporal noise due to the readout and reset noise, σ_r^2, is defined in Eq. (5.8), the component due to the photocurrent and integration time noise, $\sigma_{I_{PH}}^2$, is defined in Eq. (5.9), and the component due to the dark current and integration time, $\sigma_{I_{DARK}}^2$, is defined in Eq. (5.10). The component in the square root of the denominator due to distortions is summed up in σ_{FPN}^2 and is defined in Eq. (5.11).

$$SNDR_{linear} = 20\log_{10}\frac{\Delta V_{SN}(I_{PH}, t_{\text{int}})}{\sqrt{\sigma_r^2 + \sigma_{I_{PH}}^2 + \sigma_{I_{DARK}}^2 + \sigma_{FPN}^2}} \tag{5.6}$$

$$\Delta V_{SN}(I_{PH}, t_{\text{int}}) = \frac{\Delta V_{out}(I_{PH}, t_{\text{int}})}{K} = \frac{V_{out}(I_{PH}, t_{\text{int}}) - V_{out}(I_{DARK}, t_{\text{int}})}{K} \tag{5.7}$$

$$\sigma_r^2 = \sigma_{reset}^2 + \sigma_{readout}^2 \tag{5.8}$$

$$\sigma_{I_{PH}}^2 = \frac{q}{C_{ph}}\frac{\Delta V_{out}(I_{PH}, t_{\text{int}})}{K} \tag{5.9}$$

$$\sigma^2_{I_{DARK}} = \frac{q}{C_{ph}} \frac{V_{out}(I_{DARK}, t_{\text{int}}) - V_{out}(I_{DARK}, 0)}{K} \tag{5.10}$$

$$\sigma^2_{FPN} = \sigma^2_{Gain\_FPN} + \sigma^2_{Offset\_FPN} \tag{5.11}$$

As the analyses performed up to this point consider only the FPN distortions, only the distortion average power is used to calculate the SNDR. In this case the ratio becomes only signal-to-distortion ratio SDR, expressed in decibels (dB) as shown in Eq. (5.12).

$$SDR_{linear} = 20\log_{10} \frac{\Delta V_{SN}(I_{PH}, t_{\text{int}})}{\sqrt{\sigma^2_{FPN}}} \tag{5.12}$$

The SDR curves, before and after DSRS compensation, are shown in Fig. 5.5. The curves "SDR LIN T" and "SDR LIN R" stand for the ratios before and after FPN compensation respectively. The dynamic range of each curve is indicated by the double arrowed lines, where "DRi" and "DRf" stand for the dynamic range before and after FPN compensation respectively. The DSRS compensation improves the SDR towards low light illumination, whereas it has almost no beneficial effect towards high illumination. The abrupt far right limit for both curves happens because at this point the signal falls to zero and the SDR goes to minus infinity. When other sources of FPN are taken in account as those introduced by mismatches of the photodiode and PRNU, not taken into account in the simulations, this ratio is lowered, and the total SNDR is yet lower.

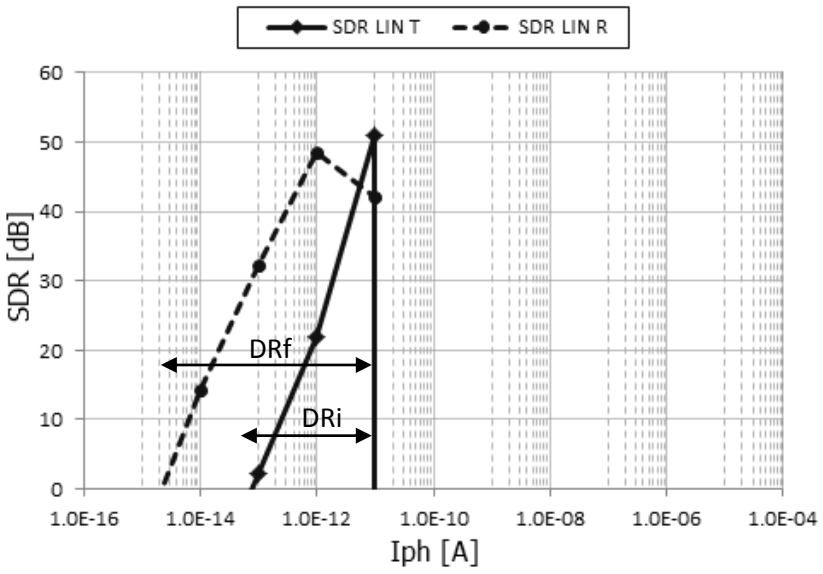


Figure 5.5- SDR linear before and after DSRS compensation [art prepared by the author].

5.3 Techniques to attenuate FPN in Logarithmic Mode

Many techniques to reduce FPN in APS operating in logarithmic mode were developed along the years, however, all of them increase the complexity either of the pixel or of the external pixel circuitry. The details of these techniques are not going to be explored in this work, but only the main idea behind each technique and the pixel schematic used to implement it.

5.3.1 Storing Pixel Offset

The first technique, storing the pixel offsets [11, 53], is the only one found in the literature that can be implemented using the basic 3T APS shown in Fig. 1.11. Notwithstanding it can also be implemented with on-pixel memory [53]. The idea relies in storing the offset of each pixel of the array in either an on-pixel or an external memory. Afterward every time the pixel output is read out it is subtracted of the offset related to that pixel.

The drawback of this technique is that if the pixel has local memory its size becomes too large with low fill factor. When using external memory the drawback is that if for any reason the pixel offset changes over time, it is necessary to refresh the memory periodically with the new offset value. Moreover, the external memory size must be of the same size of the imager array.

5.3.2 The Multimode Readout APS

The multimode readout technique [12], which pixel is shown in Fig. 5.6, is used to achieve a large dynamic range of even 200 dB, as reported in [12]. The drawback is that the pixel uses 10 transistors, being four of them of the PMOS type, which are larger than those of NMOS type and greatly reduces the fill factor of the pixel.

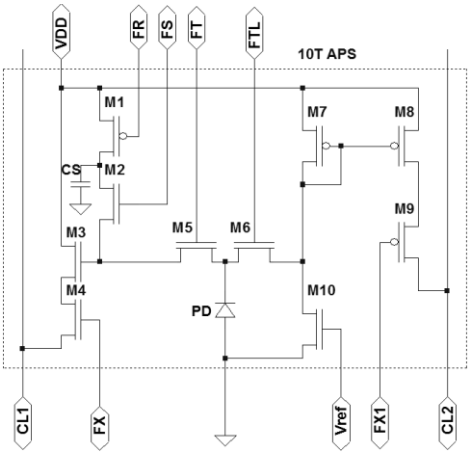


Figure 5.6- Multimode readout APS, similar to Fig. 16.7.1 of [12].

5.3.3 Multimode Linear-Bi-Logarithmic APS

The multimode linear-bi-logarithmic APS [15], shown in Fig. 5.7, is used to achieve a high dynamic range by changing the operation mode of the pixel to the most appropriate according to the light condition. The pixel has basically three modes of operation, linear mode, log mode and double-log mode, as shown in Fig. 5.7. The idea to reduce offset FPN is to perform modal double sampling readout as explained in [15]. As with the previous technique the main drawback is the increased number of transistors in relation to that of the basic 3T APS that reduce the pixel fill factor. Notwithstanding, the complexity of this pixel is much lower than that of the pixel shown in Fig. 5.7.

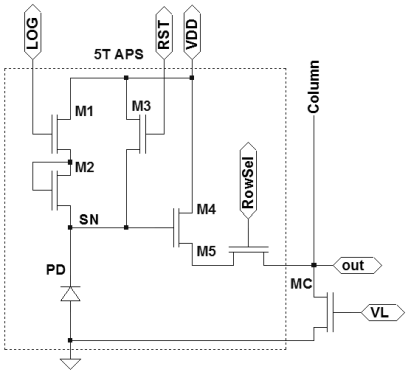


Figure 5.7- Multimode logarithmic APS, similar to Fig. 6.6 of [15].

5.3.4 Current Reference for On-Pixel Compensation

Another technique is the on-pixel compensation by current reference [17], whose pixel is shown in Fig. 5.8. The idea of this technique is quite similar to one of the techniques proposed in this work, but with two fundamental differences. The first difference is that this technique uses a current reference to perform FPN compensation, whereas the proposed technique uses a voltage reference to perform FPN compensation. The second and main difference is that this technique uses a 5T APS pixel to perform FPN compensation, whereas the proposed technique uses the basic 3T APS keeping the fill factor as large as possible.

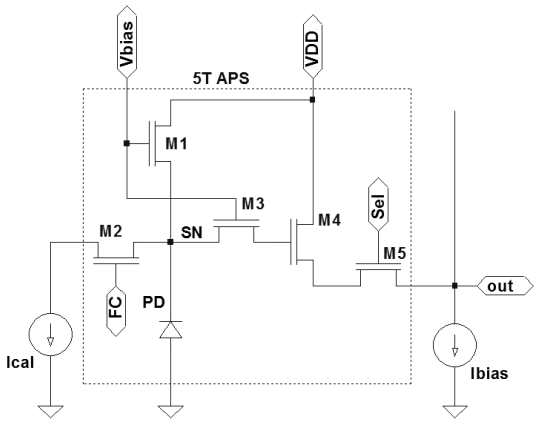


Figure 5.8- On-pixel compensation with current reference, similar to Fig. 2 of [17].

5.3.5 Double-Logarithmic Compression plus Discharge Transistor

Double-logarithmic compression plus discharge transistor for on-pixel compensation [18] is another technique which also resembles the proposed technique to be presented next. This technique is implemented using the pixel shown in Fig. 5.9. This pixel works in logarithmic operation mode only. It uses two PMOS transistor to bias the photodiode with the logarithmic light dependent current.

The compensation is performed by the transistor M5 in the pixel that produces a voltage reference level that is used for DSRS to compensate for FPN. This technique has three main weaknesses. The first is using a 5T APS, and the second is the employment of PMOS transistors in the pixel circuitry. Both approaches reduce the pixel fill factor. The

third problem is that M5 is not biased as a current source, therefore it is not easy to control the level of the compensation current.

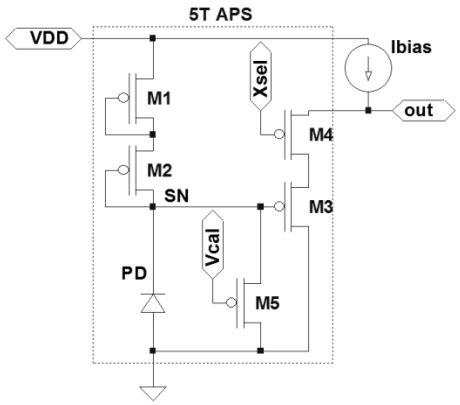


Figure 5.9- On pixel compensation with double-logarithmic compression, similar to Fig. 4 of [18].

5.4 Techniques to Attenuate FPN in Complementary-Mode Sensor

In the linear mode, the offset FPN can be compensated using the well-established CDS technique which requires a single compensation point. The single compensation point requires only two readout operations performed by the CDS circuit. On the other hand, the compensation of gain FPN requires much more complex and slow techniques, such as optical flow analysis [54]. Notwithstanding, gain FPN is more critical in the region of illumination where the sensor presents the higher sensitivity, which is at high illumination near saturation region. In the region of high sensitivity the SNDR of the sensor is high, thus gain FPN is not as critical as offset FPN at low illumination. Therefore the compensation of offset FPN is more necessary than that of gain FPN. More details of this will be discussed in more detail in the next chapter with the experimental results.

The FPN compensation in the pure logarithmic mode can also be done with a single reference point to compensate for offset FPN [44], [55], and [58]. To compensate for offset and gain FPN it requires a minimum of two compensation points, besides the sampled output signal [44], [55] and [58]. As the SNDR in the pure logarithmic mode is lower than that in the linear mode, the gain FPN compensation is more necessary than in the linear mode, especially at low illumination. However the compromise between image quality and speed of operation is far more critical in the logarithmic mode than in the linear mode. That is, the more compensation points are needed to improve the FPN attenuation, the slower the sensor operation becomes, with respect to the regular CDS operation in linear mode.

The compensation for FPN in the complementary linear-logarithm mode is challenging. Excluding the compensation technique proposed in this work, only seven other different compensation techniques are found in the literature that deal with such problem [56], [19], [44], [55], [59], [60], and [61], being the two latter contemporary of the very technique herein proposed. Details of these seven techniques are presented and discussed next.

5.4.1 FPN Compensation by Electronic Dark Reference Frame [56]

The compensation solution presented in [56] is performed on the 4T APS circuit presented in Fig. 5.10. The APS employs a photodiode operating in its photovoltaic region to produce the light dependent output voltage. As PD works in its photovoltaic region the light dependent voltage at SN is negative, therefore the PMOS source follower circuit formed by M_3 and M_2 are employed to read the SN voltage out. The output result at SN was theoretically expected to be logarithmic, however experimental results presented in [56] show that actually the output results is linear to low light illumination and logarithmic to high light illumination. Thus in this work it is also considered a different linear-logarithmic APS. The pixel is operated in two phases the first is the reset phase where $V_Z = V_{DD}$, and the second is the settling during which V_Z = GND. The linear-logarithmic light dependent output is produced during the settling time.

The light dependent output is sampled at the end of the settling time. In order to perform FPN compensation an electronic dark reference is produced by sampling the pixel output during the reset time and then subtracting the second sample from the first. This process is done in a switching capacitor circuit that is shared by all pixels in the same column of an array with such APS [56].

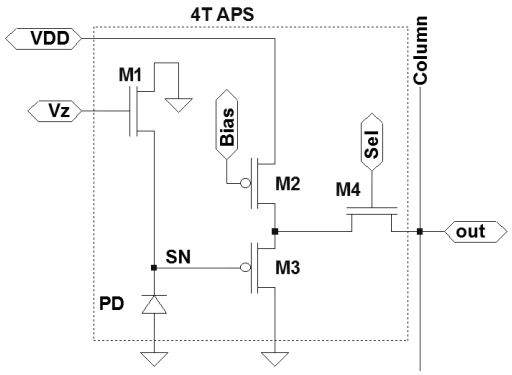


Figure 5.10- 4T APS with 2NMOS and 2PMOS, based on Fig. 5(b) of [56].

The solution presented in [56] can be performed at the rate of a regular CDS technique. However there are some points to be considered concerning this solution. First it is unusual to use the photodiode in its photovoltaic region and the benefits of such approach are not clear when compared with other linear-logarithmic approaches. Second the solution claims to compensate for FPN however it does not provide the raw FPN results in order to assert the effectiveness of the technique, in fact they present only the residual FPN. These results are important to verify the effectiveness of any FPN attenuation method as will be discussed in Chap. VI, but they are yet more important for new approaches as the one presented in [56]. Moreover the use of two PMOS transistors drastically reduces the fill factor of this pixel in relation to the basic 3T APS due to the NWELL necessary to build these transistors.

5.4.2 FPN Compensation by Charge Injection into the Pinned Photodiode [19]

The technique presented in [19] uses the 4T APS-PPD presented in Fig. 5.11 to produce the linear-logarithmic combination. In its external circuitry it uses four sets of analog

memory arrays with some additional hardware to execute FPN compensation operation. The FPN compensation is performed through charge injection into the photodiode.

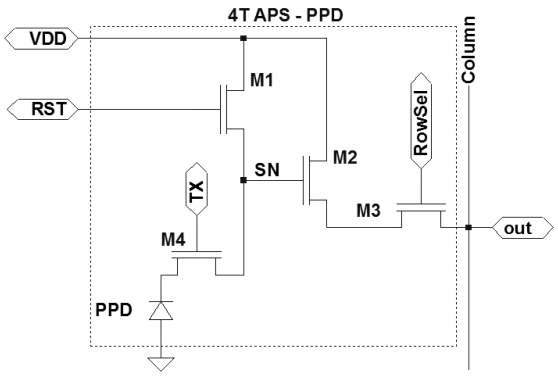


Figure 5.11- 4T APS – PPD, based on Fig. 5 of [9].

This solution requires a sequence of four readout operations per pixel which are stored into the analog memory for further FPN compensation. Compared with the basic CDS technique which requires only two readout operations, this technique is quite slow what reduces the frame rate of the array. This technique indeed reduces FPN in the logarithmic region of operation, however it causes the increasing of the FPN in the linear region [19]. Besides increasing the FPN in linear region, another drawback of this technique is the use of external memory for the compensation that might be at least of the size of the pixel array. Moreover, though the 4T APS-PPD is not complex, the fill factor of this pixel is lower than that of the 3T APS for the same pixel size.

5.4.3 FPN Compensation per Mode of Operation [44]

The independent linear and logarithmic combination presented in [44] is similar to the linear-logarithmic combination of Tu [41], presented in the sub-section 2.2.1. Differently from the solution of Tu that makes use of the basic 3T APS, the solution proposed in [44] uses the 7T APS presented in Fig. 5.12.

This technique combines independently the linear and logarithmic operation in a single pixel. This approach allows independent optimized-FPN-compensation for each mode of operation. For the linear operation it uses DRS technique which is similar to CDS but does not reduced reset noise “kT/2C” noise [9].

With the logarithmic mode of operation the solution can use either one or two reference points to compensate for FPN. When the FPN compensation is performed using a single reference point, it requires a minimum of four sequential readout operations per pixel to execute such compensation. To produce the reference points for the FPN compensation in the logarithmic region, it uses a column-based cascode current mirror to perform on-pixel compensation similar to that presented in sub-section 5.3.4.

The two first readouts sample the linear response and the reference point to compensate the linear output, and the third and fourth readouts sample the logarithmic response and the reference point to compensate the logarithmic output. Between the second and third readout it is necessary to wait for the settling time of the logarithmic response of the pixel. The need of a minimum of four readout operations and the

additional time necessary for the logarithmic settling time make this technique very slow when compared with the basic CDS operation. The use of two compensation points for the FPN compensation in the logarithmic mode further slows this technique down [44]. Moreover the use of seven transistors per pixel reduces its fill factor when compared with that of the basic 3T APS.

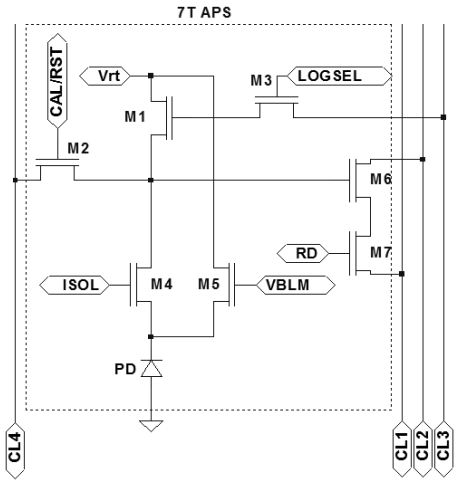


Figure 5.12- 7T APS for independent linear and logarithmic operation, based on Fig. 2 of [44].

5.4.4 FPN Compensation per Region of Operation [57]

The work presented in [57] proposes an optimized method to reduce FPN in a linear-logarithmic imager similar to that proposed by Hynecek [45] presented in the sub-section 2.2.2. This technique requires first a method to identify in which region each pixel of the array is operating in each different frame whether in the linear, or in the logarithmic, or in the transition region. Then it uses DRS [9] to compensate for FPN in the linear region. In the logarithmic region it uses the two parameters FPN compensation procedure proposed in [58] that is offset and gain compensation. To produce the reference points for the FPN compensation in the logarithmic region it also uses a current reference for on-pixel compensation similar to that presented in sub-section 5.3.4. The 5T APS in which such technique is applied is shown in Fig. 5.13.

And for the transition region it proposes two different techniques to compensate for FPN. The first uses a divede-by-2 algorithm to estimate the photocurrent in the transition region and then compensate for FPN. However, experimental results presented in [57] have shown that temporal noise jeopardizes this method, and further complexities make it useless for most commercial applications. The second method uses two readouts of the output signal, where the first is around the middle of integration time, and the second at the end of integration time. Then it estimates the photocurrents that are likely to produce the transition region at the end of integration time, and uses the first readout to compensate FPN for these photocurrents. As the first readout, for these photocurrents, lies inside the linear region, then DRS can be used to compensate for FPN. Simulations have shown that the latter is more effective than the former option [57].

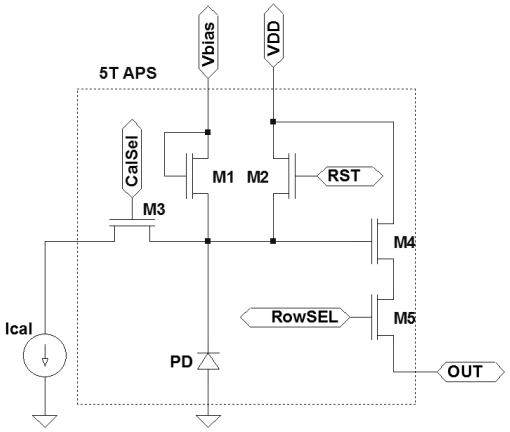


Figure 5.13- 5T APS for complementary linear-logarithmic operation, based on Fig. 1a of [57].

To apply such optimized technique it is necessary to know beforehand in which region each pixel of the array is operating, before choosing which technique to apply. This demands some kind of computational verification, what consumes extra time in addition to that already necessary to sample the signal and reference points. This imposes speed limitations to this technique when compared to the basic CDS technique, reducing therefore the imager frame rate. Moreover, the results presented in [57] do not provide the raw FPN information in order to compare with the residual FPN and to really assert the effectiveness of this technique.

5.4.5 Single Point FPN Compensation per Mode of Operation [59]

The solution presented in [59] makes use of the 7T APS presented in Fig. 5.14. The linear-logarithmic operation employed by this APS is similar to that of [44]. The main difference from the solution of [44] is that the liner-logarithmic transition point performed at circuit level rather than at software level as in [44]. Also this solution makes use of CDS compensation for the linear mode and single-point current reference compensation for the logarithmic mode.

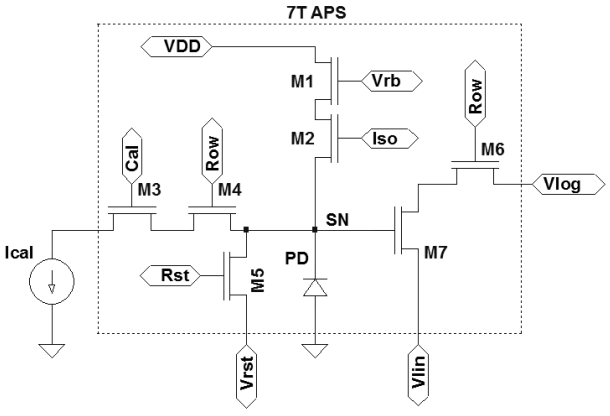


Figure 5.14- 7T APS for single reference point FPN compensation per operation mode, based on Fig. 1 of [59].

Similar to the solution presented in [44] this technique also requires four sequential readout operations per pixel to perform FPN compensation. In addition to the four

readout operations it is also necessary to wait for the settling time of the logarithmic mode, making this technique much slower than a regular CDS operation. For the same pixel size the fill factor of this pixel is also much lower than that of the basic 3T APS.

5.4.6 FPN Compensation by Two-Step Charge Transfer [60]

The work presented in [60] also makes uses the 4T APS-PPD presented in Fig. 5.11 to produce its linear-logarithmic combination. The linear-logarithmic response is also produced by the clamping the low level of the reset terminal of M_1 in Fig. 5.11.

The FPN compensation is performed by sampling the output three times, and performing two different DSRS operations and using an algorithm at software level to choose between the two DSRS results [60]. The first sample is performed at the beginning of the integration time, just after the reset operation as in the case of a regular CDS operation. The second sample is taken at the end of the integration time right after a pulse at TX terminal of M_4 in Fig. 5.11 with high V_{TX} at a chosen intermediate level between GND and V_{DD}. After the second readout pulse at TX is done with high V_{TX} at full high level, VDD, and right after the second TX pulse the third readout is performed [60].

At the special CDS circuit employed in [60] the second readout is subtracted from the first producing the first compensated result V_1 and the third readout is also subtracted from the first producing the second compensated result V_2. Then an algorithm is employed to investigate in which region the APS is operating and choose between the two results to this intend a reference point is chosen. If the APS is in the linear region, below the reference point, the second result V_2 is chosen and displayed. Else the first result is chosen and a offset V_{OFF_SET} is added to the V_1 and the result ($V_1 + V_{OFF\_SET}$) is displayed.

This approach really produces results with attenuated FPN, however the use of three readout operations and the need of software level verification makes it slower than a regular CDS operation.

5.4.7 FPN Compensation with Modified Reset Reference [61]

The linear-logarithmic combination presented in [61] makes use of the 5T APS presented in Fig. 5.15. In the APS of Fig. 5.15 the transistor M_1 works as the reset transistor during the reset time and the transistor M_2 works as the linear-logarithmic control transistor during integration time. M_3 is employed as a switch to decouple the SN from Vs during the reset time and also during the first sampling operation.

In order to perform FPN compensation the output is sampled twice and then the second sample is subtracted from the first sample to produce the output with reduced FPN. The first sample is performed right after the reset phase with V_{res} and V_{ref} at V_{DD}, and V_{SW} at GND. The second readout is performed at the end of the integration time with V_{res} and V_{SW} at GND, and V_{ref} at the clamping voltage level to produce the linear-logarithmic response. Different from the CDS and DRS technique which sample the reference point just after the reset signal is made low, this technique sample the reference point while the reset signal high yet with SN decoupled from the reference point Vs.

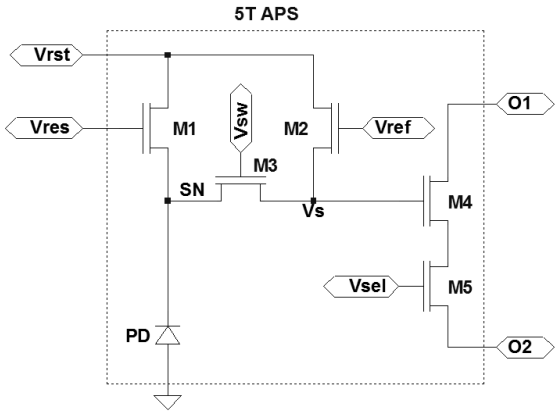


Figure 5.15- 5T APS for modified CDS compensation, based on Fig. 1 of [61].

This technique is interesting and as the solution presented in subsection 5.4.1 it can be performed at the rate of a regular CDS operation. However, the results presented in [61] show only the residual FPN. Without the raw FPN information to compare with the residual FPN it is hard to assert the effectiveness of this technique as in the case of the method presented in sub-section 5.4.1. Moreover the 5T APS yields a fill factor lower than that of the basic 3T APS for the same pixel size.

5.5 Proposed Techniques to Attenuate FPN in CMS Imagers

The previous sections presented the core idea together with the pixel schematic of the main techniques found in the literature to reduce FPN in CMOS APSs operating in pure logarithmic or in linear-logarithmic mode. In this section the proposed idea to reduce FPN in the basic 3T APS operating in complementary linear-logarithmic mode is presented.

The main difference of the proposed technique from those previously presented is that it performs FPN compensation directly in the 3T APS in either linear, or logarithmic, or the transition region, and does not need external memory to perform such compensation. Moreover, the technique uses a single reference point to perform the compensation in either region of operation, allowing FPN compensation at the rate of a regular CDS operation.

Suppose the pixel of Fig. 3.8 operating in CMS mode, and one intends to apply CDS or DRS to reduce readout offset FPN from the sensor response presented in Fig. 5.16 during integration time. It would be necessary, as in [57], to know beforehand whether the sensor was in the linear or in the logarithmic region and apply it only in the linear region, otherwise subtraction would nullify the signal output in the logarithmic region.

Also as in [57], to identify the linear or logarithmic regime, it would be necessary further signal processing with information of previous states of the pixel. The solution proposed in this work avoids both further signal processing and increasing pixel complexity.

The proposed solution consists in using the individual connection of the drain terminal of the reset transistor of the pixel of Fig. 3.8 to establish a voltage reference which would take into account the offset FPN introduced by devices of the pixel. Double sampling the

pixel output, the first sample will register the signal and the offset FPN, and the second will register the voltage reference and also part of the offset FPN. The subtraction of the first sample from the second suppresses the component of offset FPN present in both samples.

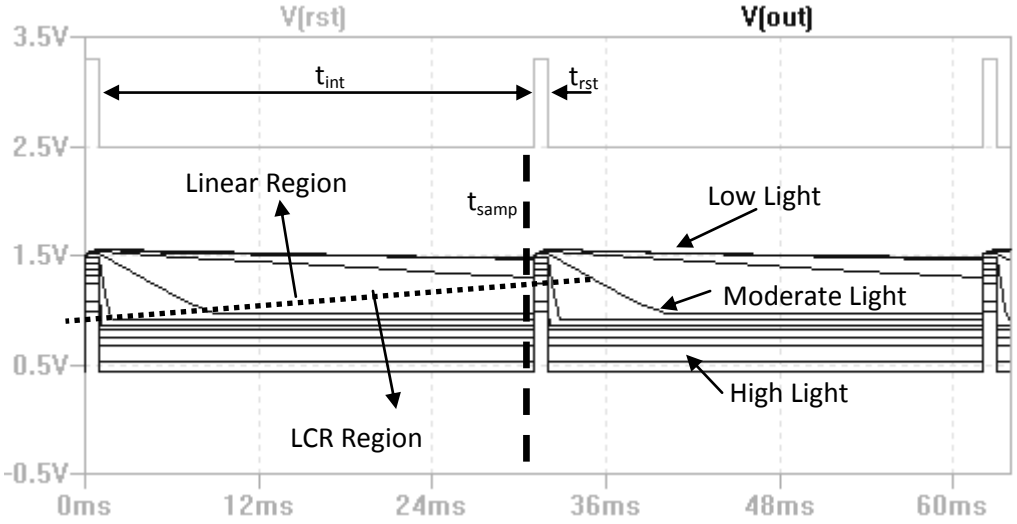


Figure 5.16- Complementary linear-logarithmic mode output voltage [art prepared by the author].

To implement the proposed solution two sets of control signals can be used to establish the voltage reference. These sets are shown in Figs. 5.17 and 5.18, respectively. In both schemes the plot on the top represents the sense node signal under various levels of illumination, the plot in the middle represents the reset signal and the plot on the bottom represents the RDR signal. The sequence in which the proposed solution is performed will be explained next.

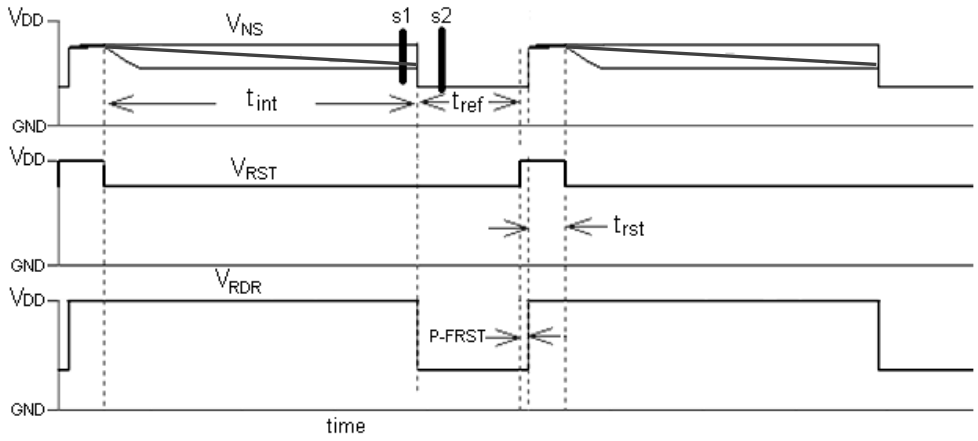


Figure 5.17- Double-sampling voltage reference, first signal scheme [art prepared by the author].

On the first scheme of Fig. 5.17 the RDR low level voltage must be lower than the voltage established on the sense node by the highest light level of interest. For instance, in the simulations performed here the V_{DD} level is 3.3 V, the reset low level voltage is 2.5 V and for a fictitious very high photocurrent of 10 μA the sense node level is higher than 1.4

V, therefore the RDR low level must be lower than 1.4 V. The pseudo-flash reset (P-FRST) takes place between the end of reference time t_{ref} and the beginning of reset time t_{rst}.

The readout sampling is to be performed as shown in Fig. 5.17, at the end of integration time, s1, and during reference time "t_{ref}", at s2. Then, subtracting the output signal at s1 from the voltage reference at s2 will result in the compensated output signal with attenuated offset FPN. The main concern of the application of such scheme is that the voltage reference must feature very low noise, not to disturb the compensated output results under very low light conditions due to resistive coupling to the voltage reference source [62].

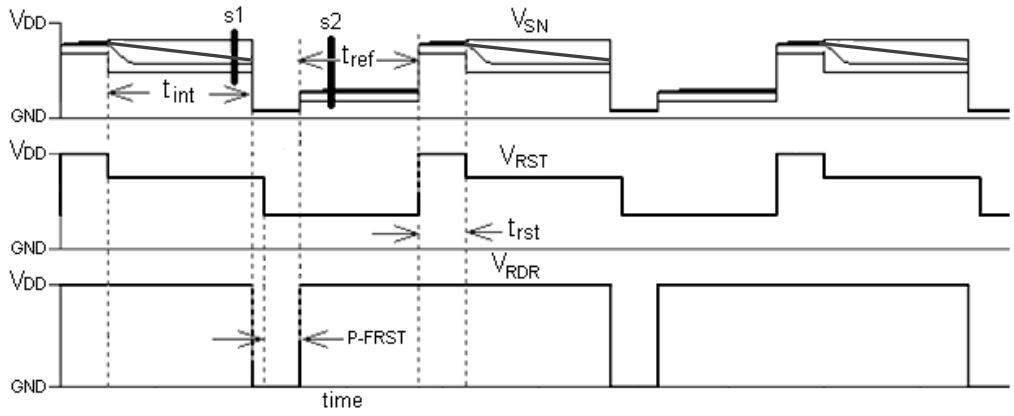


Figure 5.18- Double-sampling voltage reference, second signal scheme [art prepared by the author].

In order to perform the DSRS with reduced concern about the noise level, a second signal scheme is proposed as shown on Fig. 5.18. In this scheme the RDR low voltage level can be the ground level, and during P-FRST the reset signal has one more step. The voltage level of the second step of the reset must assure that the highest voltage level on the sense node after P-FRST is lower than that achieved by the highest light level of interest during the established integration time. In this case the pseudo-flash reset (P-FRST) takes place between the end of integration time t_{int} and the beginning of reference time t_{ref}.

As in the first scheme the output is sampled twice, at s1, in the end of integration time and, at s2, in the beginning of reference time "t_{ref}". The subtraction of the signal at s1 from that at s2 yields a signal with reduced readout and column offset FPN. The cost of this DSRS scheme is a reduced signal swing for high light levels in relation to the original output s1, which means lower sensitivity.

The sensitivity of our APS operating in logarithmic mode under high light intensity is around 55 mV per decade of photocurrent, which is compliant to those reported in the literature [20], [21], and [58]. Using the second DSRS scheme, in the worst case, the output sensitivity after subtraction is reduced to 6 mV/decade. Though it is reduced about ten times the sensitivity of the original signal s1, yet it is higher than that of s1 at low light condition that can be lower than 1 mV/decade, even for operation in linear mode when I_{PH} is close to I_{DARK} [21]. If necessary, further amplification can be performed to improve sensitivity. Nonetheless, as said before, the offset FPN is more critical at low light condition.

5.6 Simplified Simulations Results for the Proposed DSRS Schemes

The simulations were performed to verify the ability of the two proposed DSRS schemes in attenuating FPN, first against each other and next against CDS in the linear mode. The induced FPN technique presented in section 4.2 is used now to evaluate the results of both the proposed technique for the pixel operating in CMS linear-logarithmic mode and CDS technique for the pixel operating in linear mode. Some of the simulation results presented in this section were also presented in [63].

The signal setup to drive the pixel in complementary mode is the same employed in section 4.2. The output voltage FPN between the reference APS and the modified APS is determined by subtracting the first sample, s1 of Fig. 5.17, of modified APS from the first sample of the reference APS, s1 of Fig. 5.17, as shown in Eq. (5.13).

$$V_{FPN\_TOTAL} = V_{OUT\_REF\_S1} - V_{OUT\_MOD\_S1} \tag{5.13}$$

The residual output voltage FPN between the reference APS and the modified APS after DSRS compensation is determined by subtracting the compensated output of modified APS from the compensated output of the reference APS. The compensated output of each pixel is determined by subtracting the second sample from the first sample of each APS. The result is shown in the Eq. (5.14).

$$V_{REDUCD\_FPN} = \left(V_{OUT\_REF\_S1} - V_{OUT\_REF\_S2}\right) - \left(V_{OUT\_MOD\_S1} - V_{OUT\_MOD\_S2}\right) \tag{5.14}$$

The voltage output results for the pixel operating in CMS mode using both proposed DSRS schemes are shown in Fig. 5.19, where the curve labeled “CMS” is the sampling of the output signal V_0 at the end of integration time, which lasts 30 ms. The curve “CMS DSRS 1” is produced by the subtraction of “CMS” from that at s2 using the first scheme shown in Fig. 5.17, in this case the RDR voltage level during reference time “t_{ref}” is 1.4 V. The curve “CMS DSRS 2” is produced by the subtraction of “CMS” from s2 using the second scheme shown in Fig. 5.18, in this case RDR voltage level during reference time “t_{ref}” is 1.5 V.

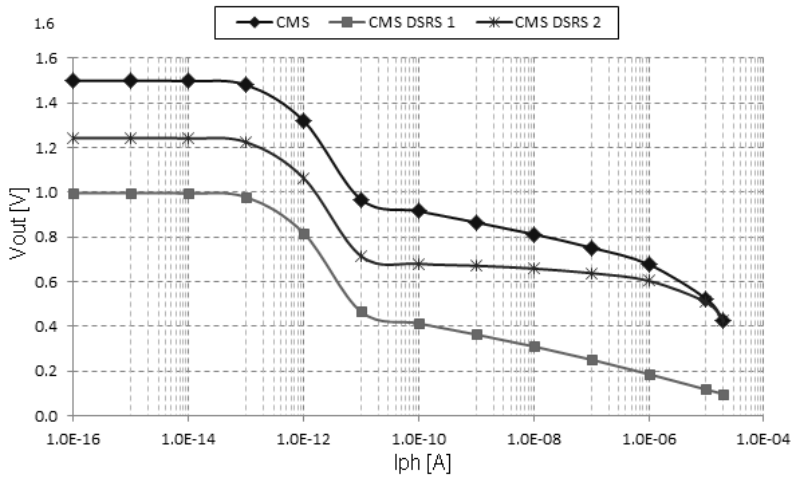


Figure 5.19- Output Signal before and after DSRS in CMS mode [art prepared by the author].

The two plots “CMS DSRS 1” and “CMS DSRS 2” present almost the same slopes of the curve “CMS” in low and moderate light conditions. In high light condition “CMS DSRS 1” yet follows the form of “CMS”, while “CMS DSRS 2” presents reduced signal swing in relation to the curve “CMS”, as previously pointed.

The results of the raw and residual FPN using the both proposed DSRS schemes for W_4 varying 10% are shown in Fig. 5.20. The raw FPN between the “APS A” and “APS B” operating in CMS mode, is shown by the curve “FPN CMS”, when W_4 of the “APS B” is 10% wider than the reference APS. The residual FPN, after DSRS using the first proposed scheme, between the “APS A” and “APS B” operating in CMS mode is shown by the curve “R FPN DSRS 1”. Using the second proposed scheme, the reduced FPN after DSRS between the “APS A” and “APS B” operating in CMS mode is shown by the curve “R FPN DSRS 2”.

Comparing both proposed DSRS schemes, it is clear that the first scheme is more effective than the second along the whole light intensity range. The results presented in Fig. 5.20 shows that as the illumination grows high, while the residual FPN using the first DSRS scheme is steadily reduced, that of the second scheme grows up to the value of the raw FPN before compensation. Although the second DSRS scheme was devised to avoid concern about the reference voltage noise level, it has at least two serious disadvantages in relation to the first scheme that is reduced signal swing and reduced effectiveness in attenuating FPN. The first DSRS scheme thus presents better performance in attenuating FPN, and as will be shown by the experimental results, the noise level at the reference voltage is not a big concern.

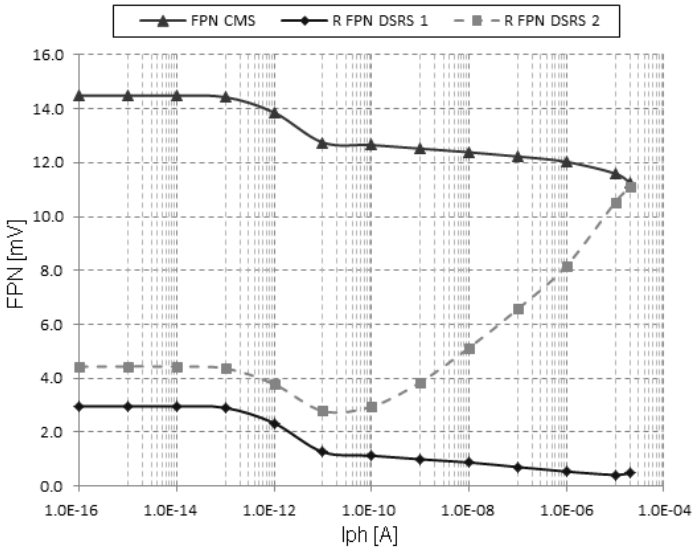


Figure 5.20- Output voltage FPN between “APS A” and “APS B” when W_4 of the “APS B” is 10% different from that of the “APS A” [art prepared by the author].

The SNDR for the complementary linear-logarithmic mode considers both the SNDR for the linear region as presented in Eq. (5.6), and the SNDR for the logarithmic region [31] as presented in Eq. (5.15). In the SNDR of the logarithmic region presented in Eq. (5.15), the input signal is the voltage variation at the sense node, and the square root of the denominator is the average input referred noise power. The voltage variation at the sense node ΔV_{SN} is a function of the photocurrent defined in Eq. (5.16), where K is the gain of the source follower amplification. In the square root of the denominator, the component of

temporal noise due to the readout and reset noise, σ_r^2, is defined in Eq. (5.8), and the component due to the kT/C noise, $\sigma_{kT/C}^2$, is defined in Eq. (5.17), where C_{ph} is the capacitance at the sense node. The component in the square root of the denominator due to distortions is summed up in σ_{FPN}^2 and is defined in Eq. (5.11).

$$SNDR_{\log} = 20\log_{10}\frac{\Delta V_{SN}(I_{PH})}{\sqrt{\sigma_r^2 + \sigma_{kT/C}^2 + \sigma_{FPN}^2}} \tag{5.15}$$

$$\Delta V_{SN}(I_{PH}) = \frac{\Delta V_{out}(I_{PH})}{K} = \frac{V_{out}(I_{PH}) - V_{out}(I_{DARK})}{K} \tag{5.16}$$

$$\sigma_{kT/C}^2 = \frac{q}{C_{ph}}\frac{1}{2}\frac{kT}{q} \tag{5.17}$$

The signal-to-distortion ratio SDR for the logarithmic region expressed in decibels (dB) is shown in Eq. (5.18).

$$SDR_{\log} = 20\log_{10}\frac{\Delta V_{SN}(I_{PH})}{\sqrt{\sigma_{FPN}^2}} \tag{5.18}$$

The SDR curves, before and after DSRS compensation, are shown in Fig. 5.21. The curve "SDR CMS" stands for the ratio before FPN compensation, the curves "SDR CMS DSRS 1" and "SDR CMS DSRS 2" stand for the ratios after FPN compensation through the first and second DSRS schemes respectively. The compensated SDR curves show that the use of the second compensation scheme has beneficial effects in the linear region and also in the beginning of the logarithmic region. However as the light intensity increases the uncompensated SDR curve presents better results than the compensated SDR curve with the second scheme. On the other hand, the first compensation scheme presents improvement along the whole illumination range in either region of operation. Moreover the SDR curve where the first compensation scheme was applied presents better results than the SDR curve with the second scheme, within the whole illumination range.

The dynamic range of each curve in each region of operation is indicated by the double arrowed lines, where "DR Lin 1", "DR Lin 2" and "DR Lin 3" stand for the dynamic range in the linear region and "DR Log" stands for the dynamic range in the logarithmic region. The dynamic range of the uncompensated curve is indicated by "DR Lin 1", and the dynamic range of the compensated curves with the two proposed DSRS techniques are indicated by "DR Lin 2" and "DR Lin 3" the first and second schemes, respectively. In the logarithmic region, as the SDR curve is greater than zero for all three situations, the three curves have the same dynamic range. The total dynamic range of any of the three curves is the sum of the dynamic range of the linear region with that of the logarithmic region.

Using either of the two DSRS compensation techniques improves the dynamic range of the sensor towards low light intensity, while the dynamic range towards high light region remains the same. These results show the first proposed DSRS technique presents the highest dynamic range.

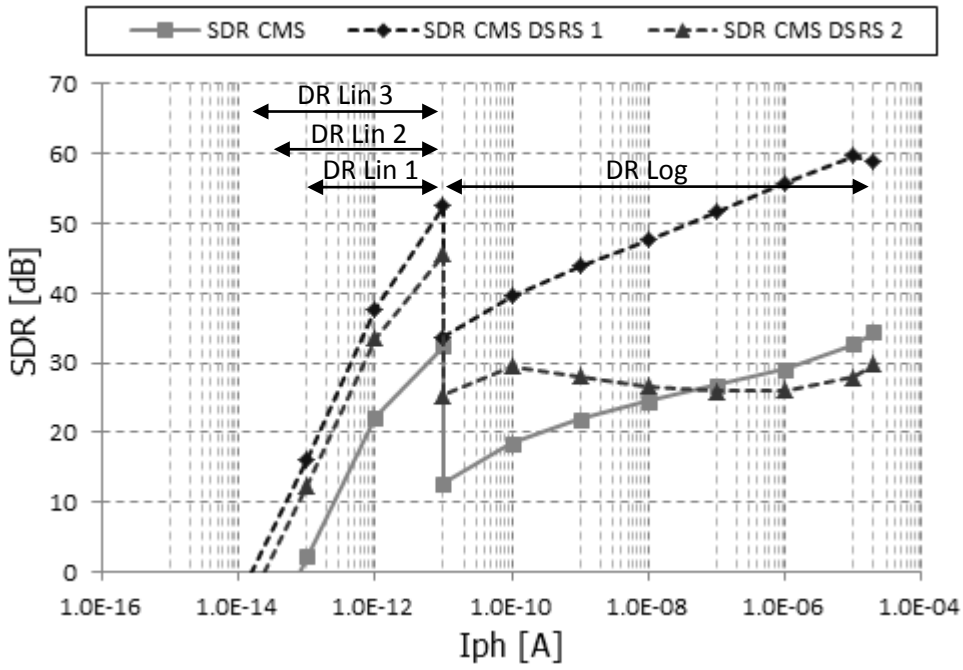


Figure 5.21- SDR before and after FPN compensation with both DSRS schemes [art prepared by the author].

The results presented above show that the first proposed DSRS scheme presents many more advantages to be implemented than the second proposed DSRS scheme. Among the advantages of the first proposed scheme are better FPN attenuation, higher SDR results, and higher dynamic range. Thus, more detailed analysis will be henceforth carried out only for the first proposed scheme.

5.7 Monte Carlo Analysis of the Proposed DSRS Technique

The first proposed DSRS compensation scheme presented in Fig. 5.17 is now further explored through Monte Carlo Analysis, and the results are compared against the classical correlated double sampling (CDS) applied to the linear mode. The Monte Carlo analysis presented here follows the same patterns of the previous raw FPN results presented in the last section of Chap. IV. Each single point of every curve presented next represents the results of 256 Monte Carlo runs performed in the Cadence Virtuoso V. 6.1.5 sub-version IC6.1.5.500.132. The simulations were performed in the Virtuoso Analog Design Environment XL – ADE XL using the Monte Carlo simulation model "cmosmc", with the pixel presented in Fig. 3.8, designed in the AMS CMOS 0.35 μm technology. Part of the simulation results presented in this section was already presented in [64].

Three types of FPN analysis were performed. The first analysis is the column FPN that is performed with mismatches only of the column amplifier transistor M_4. The second analysis is the FPN along a column that is performed with mismatches of the three transistors of the pixel M_1, M_2 and M_3. The third analysis is the FPN across the array that is performed with mismatches of M_1, M_2, M_3 and M_4. The simulations were performed for the complementary linear-logarithmic mode using the DSRS compensation scheme presented in Fig. 5.17.

The setup of the control signals presented in Fig. 5.17 for the linear-logarithmic operation is the following: the supply voltage V_{DD} is 3.3 V, the reset low level is fixed at 2.5 V, and the low level of RDR is 1.4 V. The illumination level is represented here by photocurrents varying from 1 fA to 10 µA.

A time-domain pixel output voltage example for only 10 Monte Carlo runs with the setup described above is given in Fig. 5.22. Each time slot in Fig. 5.22 shows part of the integration and reference times of the pixel in Fig. 3.8, where mismatches of M_1, M_2, M_3 and M_4 were applied. To produce the results for each photocurrent as presented next, the output of pixel was sampled twice in the region indicated by black rectangle, which is zoomed in as shown in Fig. 5.23, according to the scheme in Fig. 5.17.

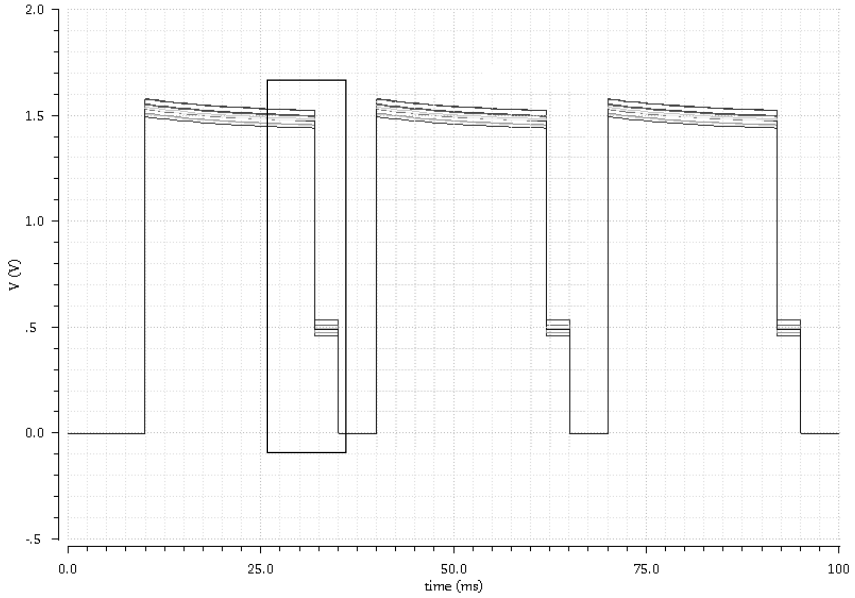


Figure 5.22- Output for 10 Monte Carlo runs with I_{PH} = 1 pA [art prepared by the author].

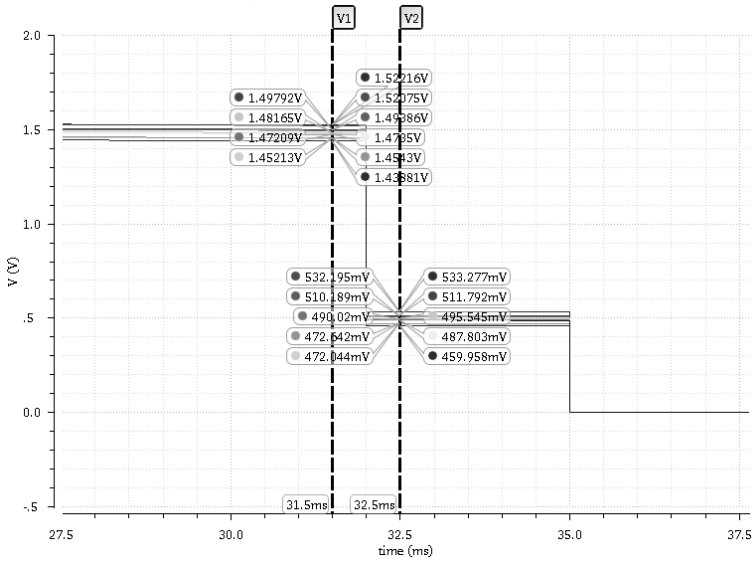


Figure 5.23- Sampling times, where V1 and V2 stand for s1 and s2 respectively [art prepared by the author].

The mean output voltage level and the standard deviation of the output are determined by Eq. (4.1) and Eq. (4.2) respectively. The mean voltage output level for the three types of analysis before DSRS compensation has the same curve as indicated by the curve “CMS” in Fig. 5.24. After DSRS compensation the mean output level also has the same curve for the three types of analysis, as indicated by “CMS DSRS 1” in Fig. 5.24. Both curves “CMS” and “CMS DSRS 1” present the same variations within the whole illumination range, and the main difference between them is the offset around 0.5 V.

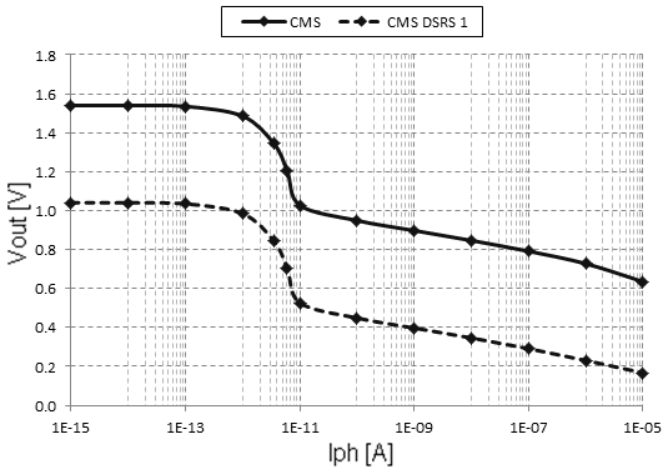


Figure 5.24- Mean voltage output versus illumination level before and after DSRS [art prepared by the author].

The raw and residual FPN for the three different analyses are shown in Fig. 5.25. The column FPN, where only mismatches of M_4 are taken into account, is indicated by the curves “COL FPN” and “R COL FPN” before and after DSRS compensation respectively. The array FPN, where the mismatches of M_1, M_2, M_3, and M_4 are considered, is indicated by the curves “ARR FPN” and “R ARR FPN” before and after DSRS compensation respectively. The FPN along a column, where the mismatches of M_1, M_2, and M_3 are considered, is indicated by the curves “A-COL FPN” and “R A-COL FPN” before and after DSRS compensation respectively.

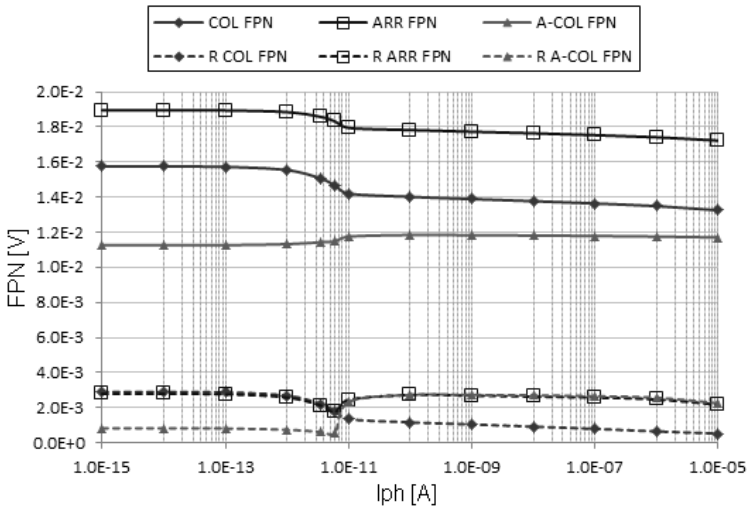


Figure 5.25- Raw and residual FPN for the three different analyses [art prepared by the author].

The array FPN is a composition of the two other types of FPN as can be observed by the result of both sets of curves before and after compensation shown in Fig. 5.25. These results show that before FPN compensation the column FPN has a dominate affect, in both regions of operation, over of the raw array FPN. After DSRS compensation, the column FPN still keeps a dominant effect in the linear region, whereas in the logarithmic region the FPN along a column dictates the behavior of the residual array FPN. As the raw and residual array FPN presents the effects of the two other sources of FPN considered here, only the array FPN is taken into account in the following discussions. Notwithstanding, it is important recalling that the photodiode presents a great contribution to the total array FPN. However there is no simulation model for this device. The effect of the photodiode will be discussed with the experimental results.

5.8 The proposed DSRS Technique versus CDS Technique

In this section the Monte Carlo simulation results of the proposed DSRS technique are compared with the results yielded by the CDS technique. The importance of the comparison of the proposed DSRS technique with the CDS technique is twofold: first, the CDS is a standard and fast compensation technique for the pure linear mode and, second, the proposed technique can be executed at the same rate of the regular CDS operation. Also CDS in applied to compensate for FPN in the linear region of the linear-logarithm combinations presented in [44] and [57]. Moreover, as is shown the attenuation level of the proposed DSRS technique in the linear region of the CMS mode is close to that yielded by the CDS in the linear mode.

The proposed DSRS technique is designed to be applied to the basic 3T APS operating in complementary linear-logarithmic mode, while the CDS technique is to be applied when the pixel is operating in the pure linear mode. The mean voltage output results for the pixel in Fig. 3.8 operating in both linear-logarithmic and pure linear modes are shown in Fig. 5.26. The curves “CMS” and “CMS DSRS 1” are the same presented in Fig. 5.24, whereas the curves “LIN” and “LIN CDS” are the mean value results of the pixel before and after CDS compensation. Although the presented results for the linear mode are shown within the complete illumination range, the results are useful only until the saturation point indicated by the bold black vertical line.

The raw and residual array FPN results using the proposed DSRS compensation technique in complementary linear-logarithmic mode and CDS in the pure linear mode are presented in Fig. 5.27. The raw and residual array FPN curves for the linear-logarithmic mode, labeled “FPN CMS” and “R FPN CMS”, are the same presented in Fig. 5.25. Whereas the raw and residual array FPN for the pure linear mode are identified by the curves labeled “FPN LIN” and “R FPN LIN” respectively.

The results presented in Fig. 5.27 show that raw array FPN in the linear region of the complementary linear-logarithmic mode and that of the linear mode present the same level. As the linear mode approaches the saturation, the raw FPN curve steeply slopes to zero volts. The compensated results show that in the low light range the CDS produces better results for the pure linear mode than the proposed DSRS technique for the linear region of complementary linear-logarithmic. However, in the pure linear mode as the

saturation level is approached, the CDS compensation collapses and does not work anymore. On the other hand the proposed DSRS technique is effective within the whole range of illumination.

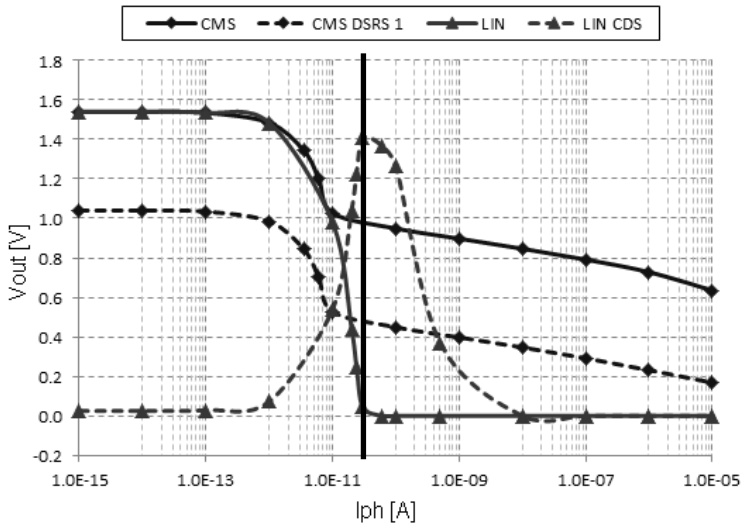


Figure 5.26- CMS and pure linear mode output curves, before and after FPN compensation [art prepared by the author].

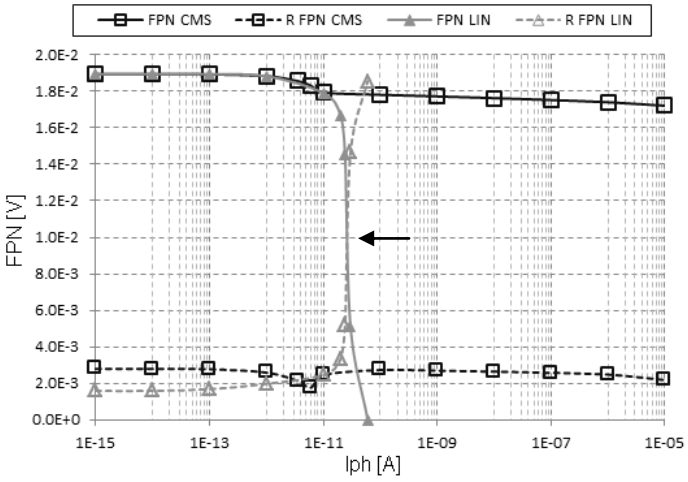


Figure 5.27- Array FPN in CMS and linear modes before and after FPN compensation [art prepared by the author].

The SDR curves of the CMS and linear modes, before and after DSRS and CDS compensation, are shown in Fig. 5.28. The SDR plots before and after DSRS compensation in the linear-logarithmic mode are presented by the curves labeled as “SDR CMS” and “SDR CMS DSRS 1” respectively. The curves labeled “SDR LIN” and “SDR LIN CDS” are the SDR curves before and after CDS compensation in the pure linear mode. The dynamic ranges of the linear mode before and after CDS compensation are 39.17 dB and 57.50 dB, respectively, and those of the linear-logarithmic mode before and after DSRS compensation are 149.63 dB and 166.02 dB, respectively.

The SDR curves for the linear mode show that the CDS compensation improves the dynamic range of the linear mode in around 18.33 dB toward the low light illumination as

shown by the “DR1” in Fig. 5.28. These results also show that the compensated linear SDR curve is improved in almost the whole illumination range until close to the saturation region. The SDR curves for the linear-logarithmic mode show that the proposed DSRS compensation improves the dynamic range of the CMS mode in around 16.39 dB toward the low light illumination as shown by the “DR2” in Fig. 5.28. Different from the linear mode, the compensated SDR curve of the CMS mode is improved within the whole illumination range in either region of operation.

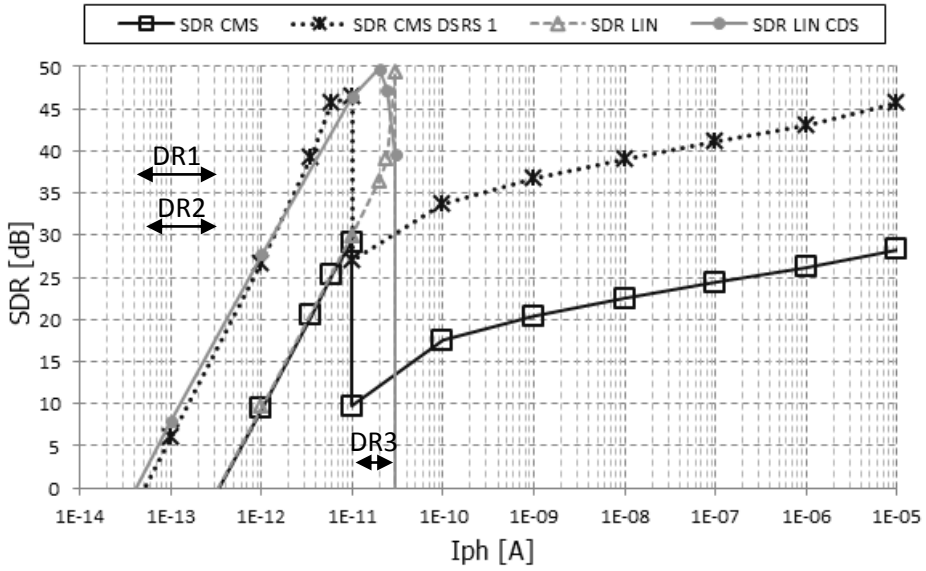


Figure 5.28- SDR before and after FPN compensation for linear-logarithmic and pure linear modes [art prepared by the author].

The linear region of the complementary linear-logarithmic mode used in this work is not allowed to reach the total dynamic range of the pure linear mode as in the case of the combination proposed in [44]. This effect is presented by the results shown in Fig. 5.28, where the difference between the dynamic ranges of the linear region of the CMS mode to that of the linear mode is around 10.37 dB as shown “DR3” in this selfsame plot.

The FPN compensation techniques presented in [44] and [57], for two different linear-logarithmic combinations, use CDS to compensate for FPN in the linear region of these combinations. Therefore CDS results presented here show what results are expected in the linear region of these techniques. In the logarithmic region these solutions apply current reference for on-pixel compensation similar to that presented in sub-section 5.3.4, that requires at least one more transistor per pixel, reducing the pixel fill factor. As these techniques use optimized FPN compensation for each region of operation, they are able to achieve better results than the proposed DSRS technique. However, these techniques require computational methods to identify in which region the pixel is operating, before deciding which compensation technique to apply whether CDS in the linear region or current compensation in the logarithmic region. The additional time required for computational analysis besides the time necessary to sample the signal output and reference points make these techniques much slower than the regular CDS technique.

Though the proposed DSRS technique is not able to achieve the attenuation level reported to be achieved in [44] and [57], it is able to attenuate FPN within the whole

illumination range as shown by the results above. The improvement in the linear region is close to that achieved by the CDS technique in the linear mode, and the SDR improvement in the logarithmic region is basically the same as that achieved in the linear region. Moreover, the proposed technique is able attenuate FPN in both regions of operation at the same rate of a regular CDS operation. In the next chapter, experimental results confirming the ability of the proposed technique in attenuating FPN will be presented.

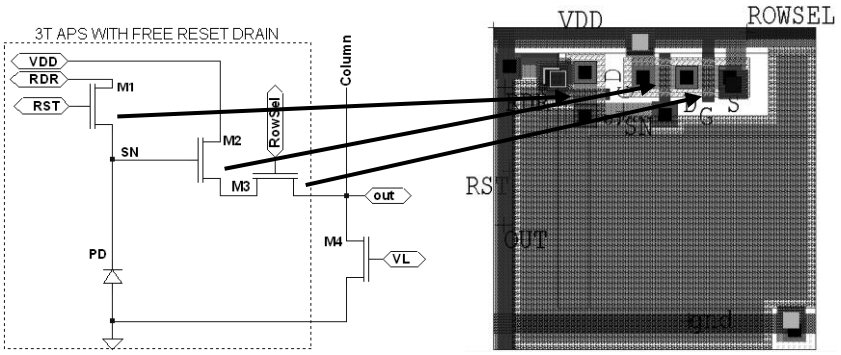
Chapter VI: Experimental Results

The characterization results of the small array designed to evaluate the proposed DSRS technique are presented in this chapter. Part of the characterization results presented here were already presented and discussed in [65]. Discussion on the results and comparisons with different techniques available in the literature are treated in this chapter.

6.1 Array Design Implementation

A small array with eight rows and eight columns of the pixel, for which the schematic is shown in Fig. 6.1(a), was designed and fabricated to evaluate the performance of the proposed technique. The array was fabricated in a standard 4-metal 2-poly n-well 0.35µm CMOS technology. Due to silicon area limitation for this project, a larger array could not be implemented.

The layout of a single pixel of the designed array is presented in Fig. 6.1(b). The size of each pixel of the array is 10µm x 10µm. The fill factor of each pixel is 56%. The photodiode is an n^+-diffusion/p-sub diode with total area of 61µm^2 and perimeter of 38.5µm. The transistors M_1, M_2 and M_3, as well as the column amplifier M_4, have the same dimensions: W = 0.70µm and L = 0.35µm. All the pixels of a single column share the same column amplifier transistor M_4, and the same RST and RDR connections. And in a row, all pixels share the same SEL connection.



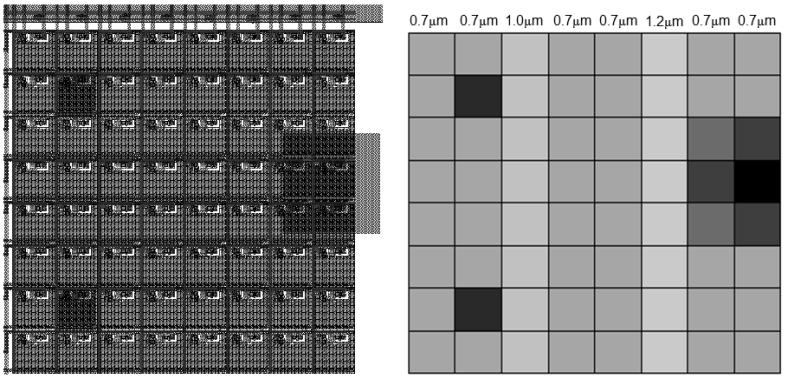
(a) (b)

Figure 6.1- (a) 3T APS schematic diagram and; (b) layout of a 10µm x 10µm pixel with a fill factor of 56% [art prepared by the author].

During the fabrication the introduction of non-idealities is a random process, thus it is not possible to predict either in which position of the array they will occur or their magnitude. Thus, to guarantee that some specific kind of non-idealities would be present in such small array, as column FPN, they were intentionally implemented in the design. This was done to enable the evaluation of the proposed DSRS technique, even if process-related FPN happened to be absent.

The non-idealities intentionally introduced in the array design were: 1) two column amplifiers, M_4, in which the transistor widths were different from the other; and 2) eight

pixels with varying ratios of metal shielding. The layout of the designed array is presented in Fig. 6.2(a). In the case that process related FPN happened to be absent, the only distortion possible to be observed in the array under uniform illumination would be those deliberately designed, an example of such intended image is shown in Fig. 6.2(b).

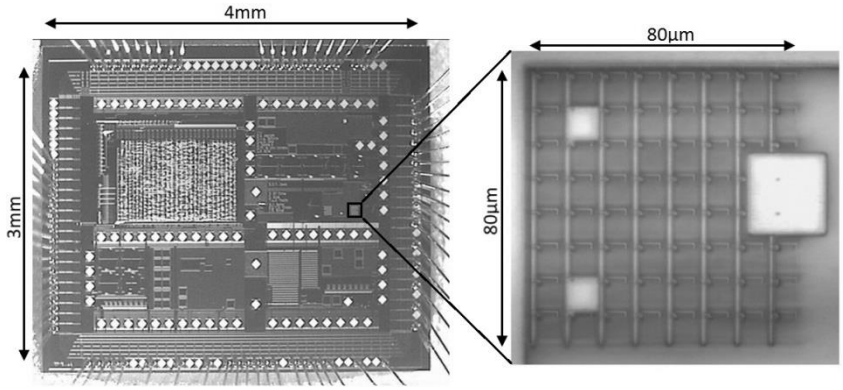


(a) (b)

Figure 6.2- (a) Designed layout of the pixel array; and (b) the expected image captured under a uniform illumination field [art prepared by the author].

Concerning the eight pixels with metal shielding, their ideal fill factor varies according the percentage of the shielded area. Each pixel in the array is identified by its (m, n) position, being the position (1, 1) that of the pixel in the upper left corner. The pixels in the positions (2, 2) and (7, 2) have the same fill factor of 2.3%, those of the pixels in the positions (3, 7), (3, 8), (4, 7), (4, 8), (5, 7) and (5, 8) are 22.6%, 14.4%, 17.3%, 0.0%, 27.0% and 20.7% respectively.

The fabricated chip containing the designed array, described above, is presented in the microphotography shown in Fig. 6.3(a). It is important to emphasize that this is a multi-user integrated circuit with many different circuit structures to be tested and investigated by different groups. The small imager array occupies the area indicated by the black rectangle in Fig. 6.3(a). The zoomed area of the chip presented in Fig. 6.3(b) shows more clearly the specific designed array, which characterization results are presented in the next section.

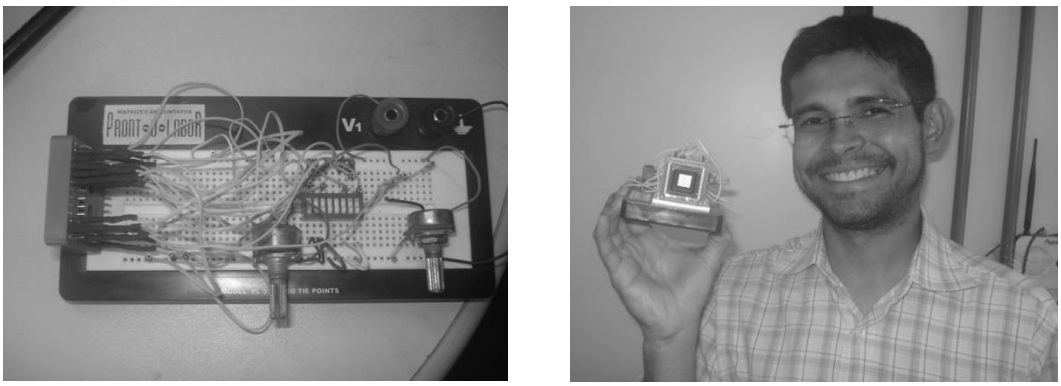


(a) (b)

Figure 6.3- (a) Fabricated chip and (b) the designed 8x8 imager array [art prepared by the author].

6.2 Experimental Setup

The experimental setup to evaluate the performance of the proposed DSRS technique with the fabricated array was prepared at the Laboratório de Óptica de Materiais – UFAM (OPTIMA – UFAM). Previously some basic tests were performed to verify if the array was responding according to what was expected of an imager array that is with the integrating and logarithmic response of the pixels. To this intent, a simple setup, where manual switches are employed to select each pixel of the array, was prepared. This basic setup is shown in Fig. 6.4(a), and the front part of the setup is shown in Fig. 6.4(b). The early manual tests were successful.



(a) (b)

Figure 6.4- @CETELI - UFAM (a) Basic setup prepared for early manual tests; (b) just after the first successful manual test [art prepared by the author].

The evaluation of the effectiveness of the proposed FPN attenuation technique is the main focus of the experiments which results are presented in this chapter. To this intent the array is tested under static uniform illuminated fields for different irradiance levels. To this purpose the employment of an ARDUINO UNO microcontroller was found to fit very well. Therefore the automation of the control and readout operation of the output of each APS of the array was implemented with this microcontroller.

The schematic of the setup of the test system is presented in Fig. 6.5. The ARDUINO UNO is connected to a PC via USB interface. The PC is employed to input the control software into the microcontroller, and also to display and store the data acquired from the array. The microcontroller requires a 5.0 V power supply and it also delivers 5.0 V digital signals. The set of signals produced by the microcontroller are the address to select each element of the array indicated by “5.0 V ADD”, the RST and RDR control signal indicated by “5.0 V RST” and “5.0 V RDR” respectively. The output of the array is read out by the ADC of the microcontroller and sent to the PC. The array must not be driven by signal with voltage amplitude higher than 3.3 V, thus an analog interface “ANL INTF” is employed to limit the signals coming from the microcontroller in 3.3 V. The analog interface is implemented with three units of the dual complementary pair plus inverter CD 4007. In this design the low level of the RST and RDR signals are determined externally by the terminal “ERST” and “ERDR” respectively.

The test setup using the ARDUINO microcontroller is shown in Fig. 6.6. It is interesting noticing that the proposed technique yielded the expected results even under such non-

customized electrical environment, thus it is expected to work even better on a customized printed circuit board. It is also important pointing out that although speed of operation is not a concern for this kind of experiment, it is a limiting factor for dynamic captures. And the use of this microcontroller imposes a slow ADC conversion time of about 120 µs that is very slow to be applied to dynamic imaging purposes. Therefore the ability of the proposed technique to suppress image lag is not evaluated by the experimental results herein presented.

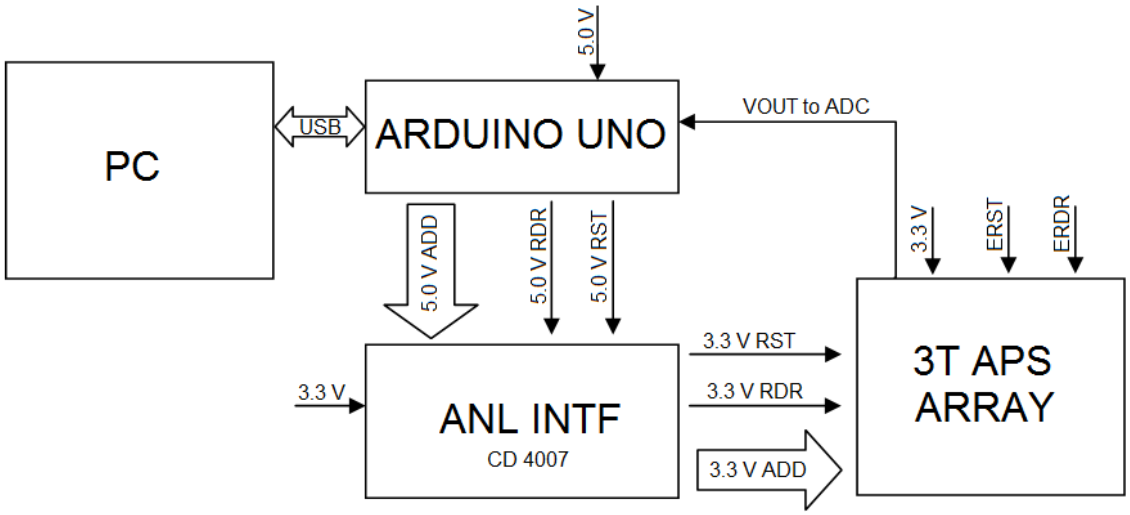


Figure 6.5- Schematic of the experimental setup [art prepared by the author].

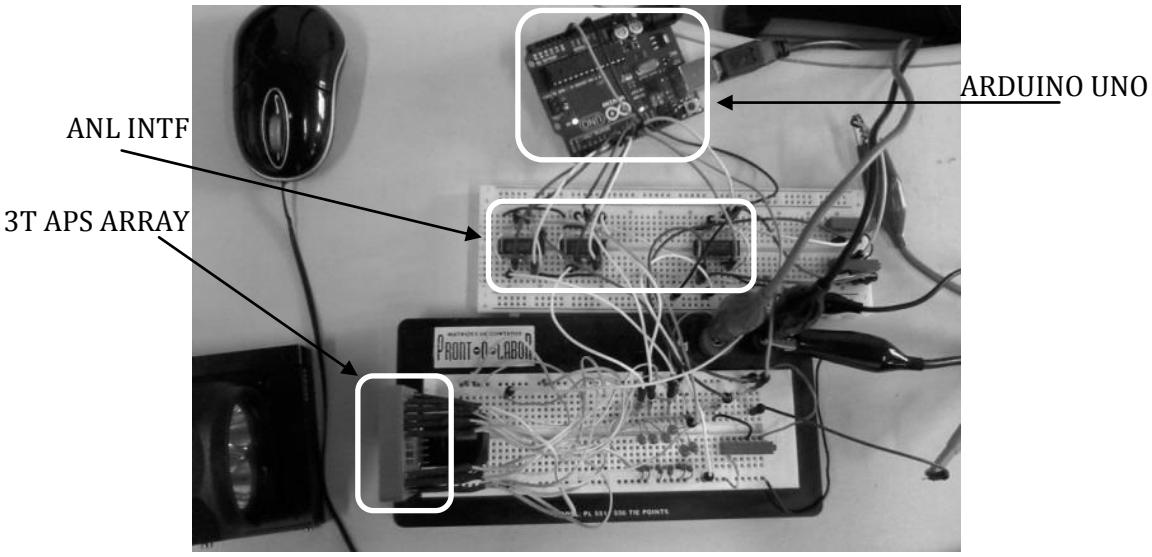


Figure 6.6- @CETELI - UFAM Setup with automated control using ARDUINO UNO microcontroller [art prepared by the author].

Using the setup presented in Fig. 6.6, some tests were carried out to verify the actuation of the devised RDR control signal over the output of the pixels of the array. The voltage output "V_{OUT}" of a pixel of the array at the end of integration time "t_{int}" is presented in Fig. 6.7. The positions around which the light dependent signal and reference point for FPN compensation are sampled are indicated by "S1" and "S2" respectively. The complete reference time of about 160 µs is indicated by "t_{ref}".

The length of the reference time depends mainly upon two variables, which are the speed of the ADC conversion and also the discharge speed of the capacitance "C_{PH}" of the photodiode, "PD" in Fig. 6.1(a), at the beginning of reference time. Some details of the reference time are shown in Fig. 6.8 where it is shown that the discharge of "C_{PH}" lasts around 8 µs. The rate at which the "C_{PH}" discharges depends mainly upon the resistivity in the path between the sense node "SN" of the APS and reference voltage source. Thus the discharge time can be reduced by reducing the resistance in this path, for example by switching RST from the low level to the highest level just before the beginning of the reference time. Nevertheless, for this specific experimental setup, the ADC conversion that lasts around 120 µs is far lengthier than the discharge time of "C_{PH}".

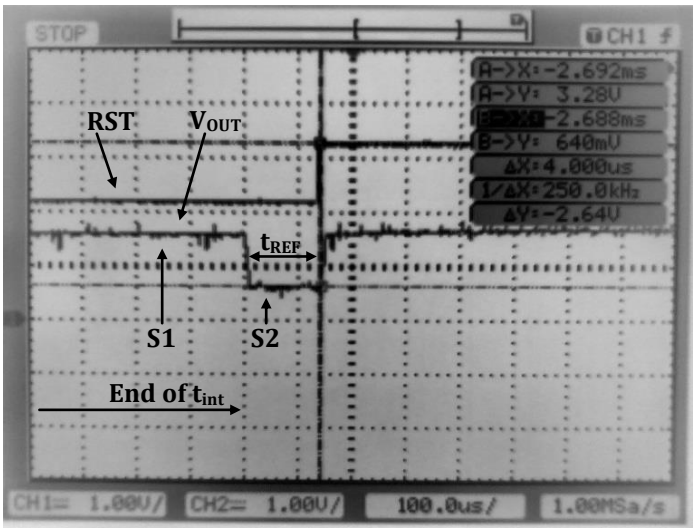


Figure 6.7- Sample of the end of integration time and complete reference time, voltage x time [art prepared by the author].

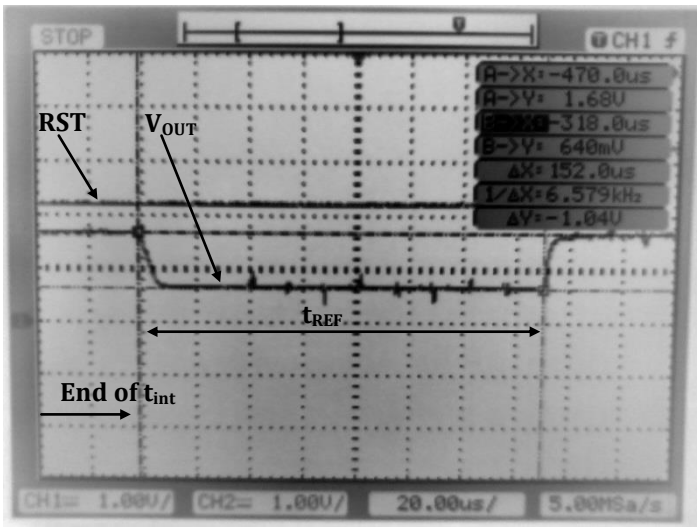


Figure 6.8- Details of the reference time, voltage x time [art prepared by the author].

The pseudo-flash reset "P-FRST", which happens at the end of the reference time, is presented in Fig. 6.9. For this specific experimental setup the "P-FRST" lasts around 6 µs. Though for the experimental results presented here the RST signal was kept at low level

during the whole reference time, it was observed later that switching it to the highest level during the reference time helps, for example, reducing the discharge time of "C_{PH}".

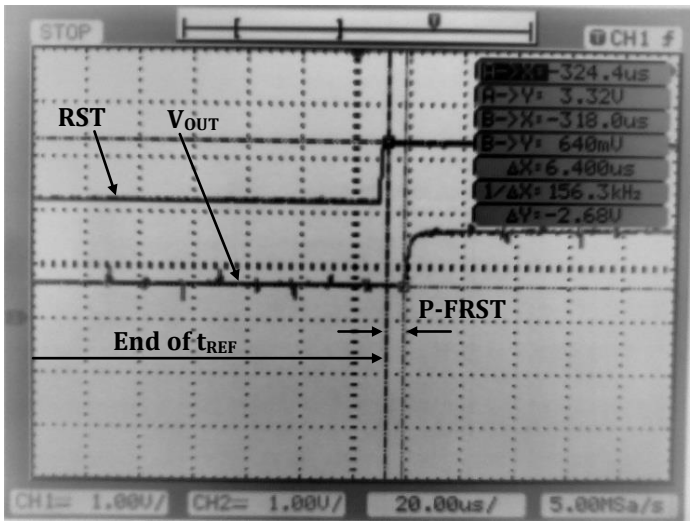


Figure 6.9- End of the reference time and complete pseudo-flash reset, voltage x time [art prepared by the author].

The standard experimental way to produce flat illuminated fields to measure and investigate FPN is by using an integrating sphere [44]. However, such apparatus was not readily available in our laboratories. Therefore, an alternative way to produce the needed flat field was to be devised.

In order to produce the flat-field condition for different light intensities to test the fabricated array, an optical setup scheme such that presented in Fig. 6.10 was prepared. In this scheme the laser beam passes through a divergent lens and two diaphragms "DPHR1" and "DPHR2" produce the flat-field profile at the imager surface from the laser Gaussian profile. All the uniform illuminated fields produced for each level of light intensity had the same 5.4mm diameter circular profile as shown in the imager surface in Fig. 6.10. The light source was a 532nm solid-state laser. The experiment was carried out at 25^{0}C.

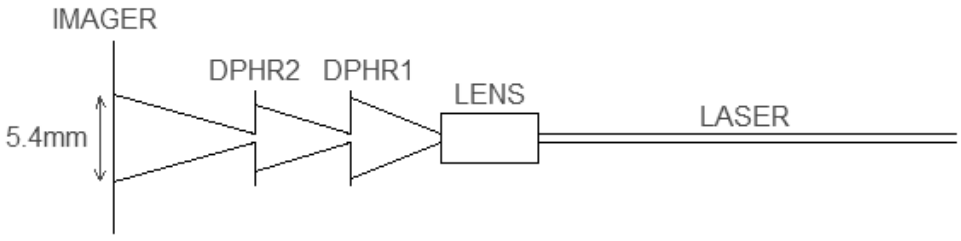
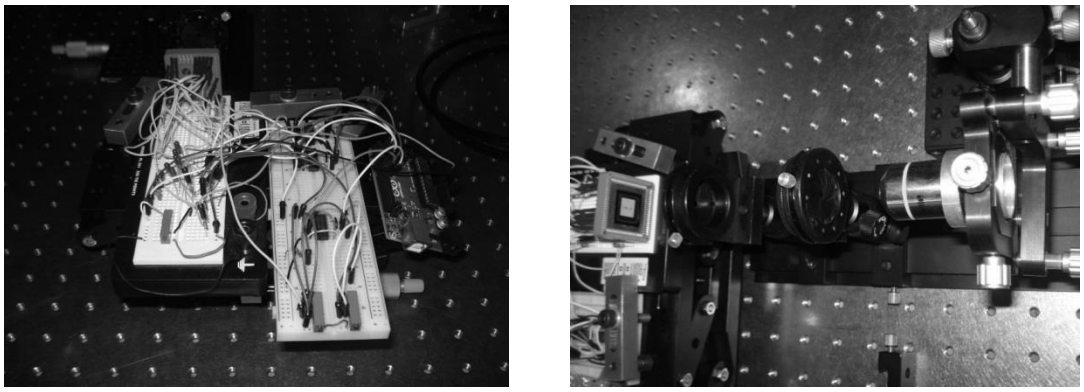


Figure 6.10- Optical setup scheme to produce a local uniform light illuminated field [art prepared by the author].

The optical setup scheme prepared over an optical table at the OPTIMA – UFAM is presented in Fig. 6.11(a) and (b). The rear part of setup control of the imager is shown in Fig. 6.11(a). The front part of the setup where the lens, the two diaphragms, and imager array appear is shown in Fig. 6.11(b).

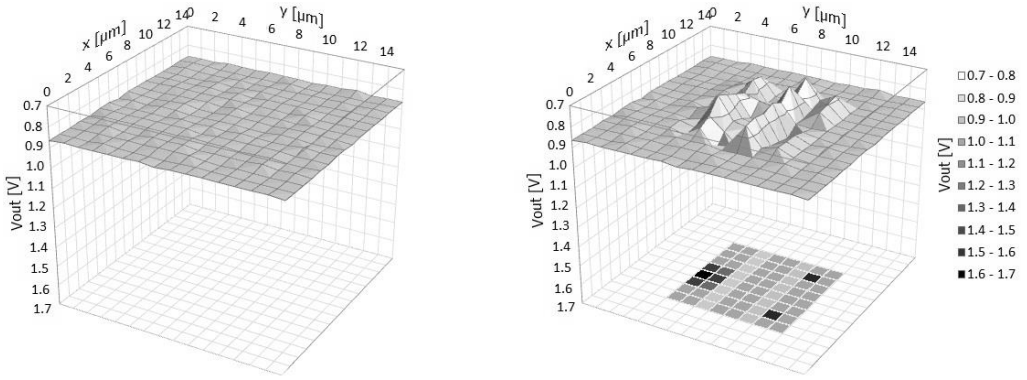
The illuminated circle at the imager surface in Fig. 6.10 has an area more than 12,000 times bigger than that of the imager array. The smoothness of the flat-field was verified in a small area mapped in the center of the circle, around the position where the imager array was placed. The mapped area in the center of the circle is square with area just four times bigger than the imager array.



(a) (b)

Figure 6.11- @OPTIMA – UFAM (a) Rear of the setup on the optical table; and (b) front of the setup on the optical table [art prepared by the author].

The square area was mapped under the irradiance of 4.37W/m^2. The mapping was performed by registering the voltage output of a single unaltered pixel of the array, pixel (1, 1), scanning the light field in 10-µm steps, as shown in Fig. 6.12(a). To attenuate temporal noise each point was measured 20 times and the average was taken for each different point. Placing the pixel array at the center of the square, the array response takes the form shown in Fig. 6.12(b), revealing the FPN distortions of the array for this irradiance. At the bottom of Fig. 6.12(b), the region where the array was placed is shown.



(a) (b)

Figure 6.12- (a) Profile of the uniform light field with $\sigma_{MEASURED}$ = 3.68 mV_{RMS}; and (b) the pixel-array response to that field with σ = 46.95 mV_{RMS}, and with the indication of the position of each pixel of the array on the bottom [art prepared by the author].

The measured standard spatial variance of the mapped square is $\sigma_{MEASURED}$ = 3.68 mV_{RMS}, and it was determined according to Eq. (4.2), where in this case M and N are 16 and n_p is 256. Just to compare this result with those that will be discussed later, for this irradiance the total standard spatial variance of the array is 46.95 mV_{RMS} and 18.98 mV_{RMS}, before and

after FPN compensation respectively. When the pixels with metal shielding are not taken in consideration the standard spatial variance of the array is 47.76 mV_{RMS} and 16.92 mV_{RMS}, before and after FPN compensation, respectively. And when only the 40 regular pixels of the array, i.e. those pixels without additional distortions, are taken into account, the standard spatial variance of the array is 26.28 mV_{RMS} and 14.38 mV_{RMS}, before and after FPN compensation, respectively. These results show that the standard spatial variance of the flat field is much lower than that produced by the distortions of the array, even when only the regular pixels are taken into account. Thus the measured results of the array suffer small influence of possible distortions introduced by the flat field non-uniformities.

The proposed DSRS technique was evaluated and also compared with the well-established CDS technique with the fabricated APS array operating in both linear and CMS modes of operation. In the linear mode CDS was applied to attenuate FPN, whereas in the CMS mode the proposed DSRS technique was applied for the same purpose.

Eight different flat-field irradiances within 60 dB were used to test the array operating in the linear mode, whereas for the complementary linear-logarithmic mode the array was tested under twelve different irradiances within 129.5 dB. All the resulting images captured by the array in this experiment are from static uniform illumination fields. Thus, the frame rate of the array will not be evaluated in this work.

The proposed control-signal scheme for the application of DSRS compensation technique is shown again in Fig. 5.17. The setup of the control signal schemes for the pixel array operating in both linear and complementary linear-logarithmic modes are presented in Table 6.1, respectively in the columns labeled as “LIN” and “CMS”. In the linear mode the first sample, s1, is taken 10μs after the beginning of t_{int} and the second sample, s2, 5 ms after the beginning of t_{int}. For the CMS mode the first sample, s1, is taken 5 ms after the beginning of tint and the second sample, s2, 20μs after the beginning of t_{ref}. This process is repeated for the 64 pixels of the array for each complete frame.

Table 6.1: Control Signal Setup

Control Signal Setup	**LIN**	**CMS**
Supply Voltage “V_{DD}”	3.3 V	3.3 V
Load Voltage “VL”	1.0 V	1.0 V
Integration Time “t_{int}”	6 ms	6 ms
RST low level	GND	2.2 V
RDR low level “V_{ref}”	GND	1.4 V
Reset Time “t_{rst}”	2 ms	1 ms
Reference Time “t_{ref}”	0 μs	160 μs
Pseudo-Flash Reset “P-FRST”	0 μs	1 ms

The ADC conversion rate of our data acquisition system limits the reference time t_{ref} for this experiment to a minimum of about 160μs. Nonetheless, as mentioned before, with the use of a faster ADC the reference time t_{ref} can be much shorter. For real-time imaging the

reset time, t_{rst}, and the pseudo-flash reset, P-FRST, can be much shorter. The pseudo-flash reset can also be applied to the pure linear mode by making P-FRST longer than 0 μs, as proposed in [16].

6.3 Analysis of the Experimental Results

The output results produced by the fabricated array with the experimental setup presented above are evaluated now to verify the ability of the proposed DSRS technique in attenuating fixed-pattern noise. Thus, spurious fluctuations of other sorts need to be minimized. To this purpose for each light condition 20 frames were captured and averaged to produce the base image for FPN analysis. This process reduces the effect of temporal fluctuations from either the light source or from the control and supply signals.

The resulting averaged frames for FPN analysis at some irradiance levels as well as at the dark condition, for both linear and complementary linear-logarithmic modes are presented in Fig. 6.13. The column identified as "LIN" represents the averaged frame in the linear mode before CDS compensation. The averaged frames in the linear mode after CDS compensation are shown in the column identified as "LIN CDS". The averaged frames, before and after the proposed DSRS compensation in CMS mode, are shown in the columns identified as "CMS" and "CMS DSRS" respectively.

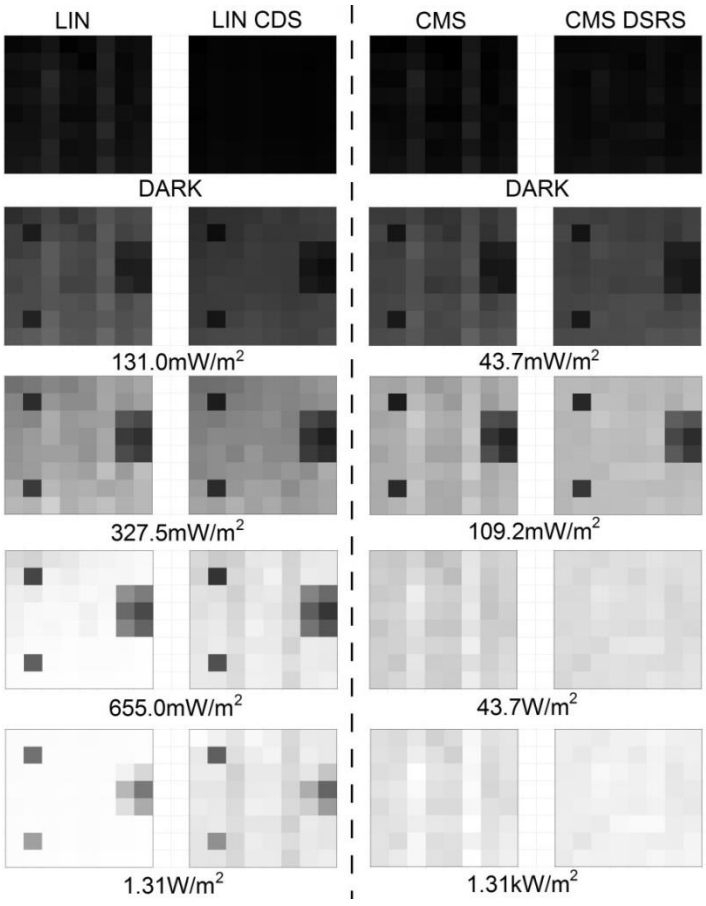


Figure 6.13- Averaged frames before and after FPN compensation: pairs of images on the left side for the linear mode and pairs of images on the right side for complementary linear-logarithmic mode [art prepared by the author].

The limits for the grayscale of the averaged frames presented in Fig. 6.13 that is the darker and brighter levels, stand for the measured voltage output limits in each mode of operation before and after FPN compensation. For the linear mode before CDS compensation the darker and brighter levels stand for 1.684 V and 0.239 V respectively, whereas after CDS compensation these levels stand for 0.093 V and 1.446 V respectively. For the CMS mode before DSRS compensation the darker and brighter levels stand for 1.655 V and 0.718 V respectively, whereas after DSRS compensation these levels stand for 1.042 V and 0.112 V respectively. Besides the limits, all other intermediate levels are grayscale variations between the limits of each mode, before and after FPN compensation.

The irradiance condition under which averaged frame was captured is shown under each pair of frames, before and after FPN compensation. The darker condition for both modes of operation is presented in the first row of Fig. 6.13.

For the linear mode, the second, third and fourth pairs of frames, before and after FPN compensation, are in the range of the light intensity for which the pixel array has the highest light sensitivity, as will be discussed next. The last pair of frames is that for which the regular pixels of the array reach the saturation level. It is important noticing that as the linear mode approaches the saturation level, the CDS technique adds FPN instead of attenuating it.

The second and third pairs of frames, for the complementary linear-logarithmic mode, lie in the range of highest sensitivity of this mode, which is inside the linear region, whereas the fourth and fifth pairs of frames lie within the logarithmic region. The fifth pair of frames was taken under the highest irradiance on which the array was tested. Differently from the pure linear mode, the CMS mode did not reach saturation even for the highest tested irradiance.

It is possible to verify that as the as the light intensity increases the proposed DSRS technique produces better results in the CMS mode than those of CDS in the pure linear mode. The experimental results show also that from the irradiance of 437 mW/m^2 and beyond, the designed partial optical shielding for those seven pixels with metal shield, in the positions (2, 2), (7, 2), (3, 7), (3, 8), (4, 7), (5, 7) and (5, 8), is rather ineffective. For these irradiance levels, the pixel with total metal shielding in the position (4, 8) is also shown to be ineffective.

6.3.1 Results of the Regular Pixels of the Array

The average of the output of all the pixels of the array is the usual way to determine the mean output value. However, as the fabricated array has 24 pixels with induced distortions, the effect of such pixels must be taken into account. Therefore, for the first set of analyses only the mean output value of the regular pixels of the array is considered. The regular pixels of the array are those without additional distortions, that is, all the pixels except those of the two different columns and those with metal shield. The process is the same for both uncompensated and compensated frames.

For each irradiance level x, the mean output value, μ_x, is calculated as shown in Eq. (6.1), where n_p is the number of pixels taken into account, which in this case is 40, since the other 24 pixels had additional induced distortions. When the array is operated in the CMS

mode, for the uncompensated frames, $V_{o,x}(m, n)$ in Eq. (6.1) stands for the samples of each pixel (m, n) of the array taken at s1 in Fig. 5.17. For the compensated frames $V_{o,x}(m, n)$ stands for the difference between the samples s1 and s2, (s1-s2), in Fig. 5.17. In the linear mode, for the uncompensated frames, $V_{o,x}(m, n)$ stands for the samples of each pixel taken at the end of the integration time, t_{int}, and for the compensated frames $V_{o,x}(m, n)$ stands for the difference between the samples taken at the beginning of t_{int} from those taken at the end of t_{int}.

The output results of the pixels with additional induced distortions appear in Eq. (6.1) as Σ_{col} and Σ_{shld}, where Σ_{col} stands for the sum of the voltage values of the 16 pixels on the two deviating columns as presented in Eq. (6.2), and Σ_{shld} stands for the sum of those additional 8 pixels with metal shield as presented in Eq. (6.3). Using this model, the output mean value curves versus irradiance is determined for both operation modes, before and after FPN compensation, as shown in Fig. 6.14.

$$\mu_x = \frac{1}{n_p}\left[\left(\sum_{m=1}^{M}\sum_{n=1}^{N} V_{o,x}(m,n)\right) - \Sigma_{col} - \Sigma_{shld}\right] \tag{6.1}$$

$$\Sigma_{col} = \sum_{m=1}^{M} V_{o,x}(m,3) + \sum_{m=1}^{M} V_{o,x}(m,6) \tag{6.2}$$

$$\begin{aligned}\Sigma_{shld} = {} & V_{o,x}(2,2) + V_{o,x}(7,2) + V_{o,x}(3,7) + V_{o,x}(3,8) \\ & + V_{o,x}(4,7) + V_{o,x}(4,8) + V_{o,x}(5,7) + V_{o,x}(5,8)\end{aligned} \tag{6.3}$$

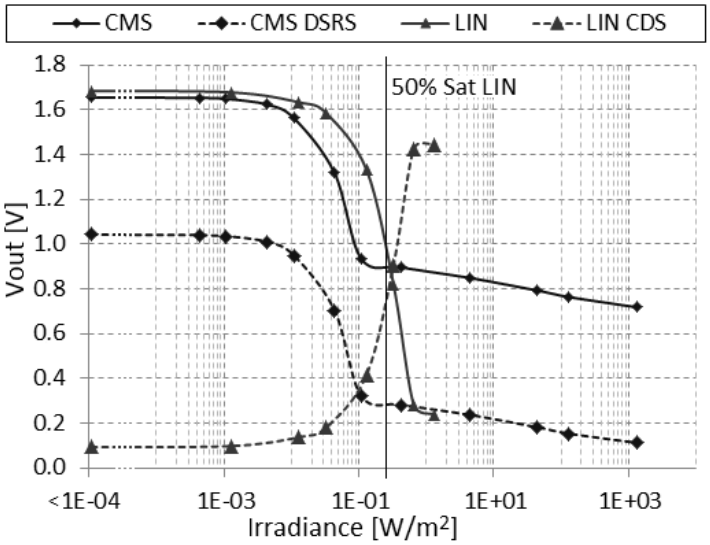


Figure 6.14- Regular pixels output mean value versus irradiance [art prepared by the author].

The mean values for twelve different irradiances in the complementary linear-logarithmic mode, before and after FPN compensation, are shown in Fig. 6.14 by the curves identified as “CMS” and “CMS DSRS”, respectively. The curves identified as “LIN” and “LIN CDS” in the same plot are the mean values for eight different irradiances for the linear mode, before and after FPN compensation, respectively. The irradiance for which

the array operating in linear mode reaches 50% of the saturation level is indicated by the line labeled as "50% Sat LIN".

The output signal swing, for both modes of operation, before and after FPN compensation is shown in Table 6.2. As the linear mode of operation reaches saturation for an irradiance of about 1.31W/m^2, the signal swing from the dark to the saturation level is the total signal swing for this mode before and after FPN compensation. On the other hand, for the CMS mode, the signal swing is not really the total output voltage variation because even for the highest tested irradiance of 1.31kW/m^2 the pixels of the array did not reach saturation.

The measured readout output temporal noise is also presented in Table 6.2. The temporal noise has the same level for both modes of operation before FPN compensation. These results show that after FPN compensation either CDS in the linear or the proposed DSRS in the CMS mode increases the noise level as shown in Table 6.2. The CDS technique causes an increase of temporal noise of about 0.5 mV_{RMS} in the linear mode, whereas the proposed DSRS technique causes an increase of temporal noise of about 0.7 mV_{RMS} in the CMS mode. Although the additional temporal noise introduced by the proposed DSRS technique is around 40% larger than that introduced by the classical CDS technique in the linear mode, it is still of the same order of magnitude of this well established technique.

Table 6.2: Signal Swing and Temporal Noise

	Before FPN Compensation	**After FPN Compensation**
Signal Swing		
Linear mode $_{TOTAL}$	1.445 V	1.353 V
CMS mode $_{MEASURED}$	938 mV	930 mV
Temporal Noise RMS		
Linear mode	1.8 mV_{RMS}	2.3 mV_{RMS}
CMS mode	1.8 mV_{RMS}	2.5 mV_{RMS}

The fixed-pattern noise of the array is determined by the standard spatial deviation of the output voltage of the pixels of the array. When only the regular pixels of the array are taken into account, the FPN is estimated as in Eq. (6.4). In this model $(\sigma_x)^2$ is the spatial variance and σ_x is the standard spatial deviation. The estimation of the variance is done using the number of pixels n_p minus one $(n_p - 1)$, in this case n_p is 40. For both modes of operation $V_{o,x}(m, n)$ has the same meaning as in Eq. (6.1). The effects of the two different columns and eight shielded pixels are expressed as $\Sigma_{\Delta col}$ and $\Sigma_{\Delta shld}$ respectively, and are defined as in Eq. (6.5) and Eq. (6.6). The estimation of the variance in the general case, where no induced distortion is introduced, is done without considering the components $\Sigma_{\Delta col}$ and $\Sigma_{\Delta shld}$ in (6.4). The FPN of the array must be recalculated for each different light condition.

The output FPN of the array versus irradiance of the regular pixels of the array, for both modes of operation, before and after compensation is presented in Fig. 6.15. The FPN values of the CMS mode for twelve different irradiances, before and after the proposed DSRS compensation, are presented by the curves identified as "FPN CMS" and "FPN CMS DSRS" respectively. For the linear mode before and after CDS compensation, the FPN

values for eight different irradiances are presented by the curves identified as “FPN LIN” and “FPN LIN CDS” respectively.

The FPN curves of the array of both modes of operation feature a peak in their respective range of high sensitivity due to photo-response non-uniformity (PRNU). After compensation, both residual FPN curves present some degree of attenuation in the range of high sensitivity however the peak remains in both modes. The attenuation of PRNU demands more accurate and complex compensation techniques as the one presented in [54] for the linear mode, and those proposed in [55] and [58] for the logarithmic mode.

$$\sigma_x^2 = \frac{1}{n_p - 1}\left[\left(\sum_{m=1}^{M}\sum_{n=1}^{N}\left(V_{o,x}(m,n) - \mu_x\right)^2\right) - \Sigma_{\Delta col} - \Sigma_{\Delta shld}\right] \tag{6.4}$$

$$\Sigma_{\Delta col} = \sum_{m=1}^{M}\left(V_{o,x}(m,3) - \mu_x\right)^2 + \sum_{m=1}^{M}\left(V_{o,x}(m,6) - \mu_x\right)^2 \tag{6.5}$$

$$\begin{aligned}\Sigma_{\Delta shld} = {} & \left(V_{o,x}(2,2) - \mu_x\right)^2 + \left(V_{o,x}(7,2) - \mu_x\right)^2 \\ & + \left(V_{o,x}(3,7) - \mu_x\right)^2 + \left(V_{o,x}(3,8) - \mu_x\right)^2 \\ & + \left(V_{o,x}(4,7) - \mu_x\right)^2 + \left(V_{o,x}(4,8) - \mu_x\right)^2 \\ & + \left(V_{o,x}(5,7) - \mu_x\right)^2 + \left(V_{o,x}(5,8) - \mu_x\right)^2\end{aligned} \tag{6.6}$$

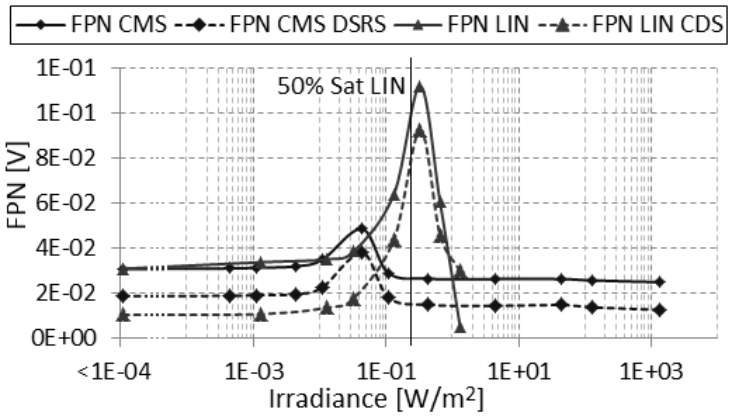


Figure 6.15- FPN versus irradiance of the regular pixels of the array [art prepared by the author].

The total FPN is composed by two components as shown in the model presented in Eq. (5.11), which are the dark signal nonuniformity (DSNU) or offset FPN, and the photo-response nonuniformity (PRNU) or gain FPN. The offset FPN is the value measured at dark condition that is the first value in the far left of each of the four curves presented in Fig. 6.15. The gain FPN is determined by decomposing the total FPN for each irradiance level from that of the dark condition according to the model presented in Eq. (5.11).

The offset FPN and the peak of gain FPN of the array in relation to the signal swing for the linear mode and for the linear region of the CMS mode are presented in table 6.3. For the logarithmic region of the CMS mode the maximum and minimum total FPN are also presented in table 6.3. It is important recalling that whereas for the linear mode the total

signal swing is determined, for the CMS mode it was not possible to determine the total signal swing. This must be taken into account for the analysis of these ratios.

Although in a non-optimized way, the proposed DSRS technique is able to attenuate the raw FPN within the whole range of operation of this linear-logarithmic combination as shown by the results in Fig. 6.15. These results show also that CDS is more effective for the linear mode of operation than the proposed DSRS technique for the linear region of the CMS mode.

Table 6.3: FPN in relation to the Signal Swing

	Before FPN Compensation	**After FPN Compensation**
Linear Mode		
σ_{Offset}	2.13%	0.76%
$\sigma_{Gain,PEAK}$	7.46%	6.80%
CMS Mode Linear Region		
σ_{Offset}	3.28%	2.00%
$\sigma_{Gain,PEAK}$	4.00%	3.56%
CMS Mode Logarithmic Region		
$\sigma_{TOTAL,\max} = \sqrt{\sigma_{Offset}^2 + \sigma_{Gain}^2}$	2.81%	1.59%
$\sigma_{TOTAL,\min} = \sqrt{\sigma_{Offset}^2 + \sigma_{Gain}^2}$	2.65%	1.34%

Using the model presented in Eq. (5.6) for the linear mode or region and in Eq. (5.15) for the logarithmic mode or region the signal-to-noise ratio (SNR) curves were plotted. However, as discussed before when both temporal noise and spatial distortions are considered to calculate this ratio, it is more adequate to call it signal-to-noise-and-distortion ratio (SNDR), as is done in [13]. This is done because the FPN is rather a fixed spatial distortion associated to the pixel array than a dynamic quantity fluctuating over time. Different from the previous chapter where only the spatial distortion FPN was considered, yielding therefore the signal-to-distortion ratio (SDR), now the complete SNDR curves are determined using the temporal readout noise of the array, presented in table 6.2.

The SNDR versus irradiance curves of the regular pixels of the array for both operating modes, before and after FPN compensation, are presented in Fig. 6.16. These results show that the proposed DSRS technique is able to improve the SNDR response of the array within the whole range of illumination. Both techniques improve the dynamic range of the array towards low illumination whereas towards high illumination it remains the same as before compensation. The improvement of dynamic range towards low illumination is of 8.28 dB with CDS in the linear mode and of 4.03 dB with the proposed DSRS technique in the CMS mode.

It is worth noticing that in the range of irradiance where the array presents the highest sensitivity in each operation mode, it is also the range where the array presents the highest SNDR in each mode. This fact basically minimizes the effects of the PRNU peak

presented in Fig. 6.15, showing that PRNU is not as detrimental at high irradiances as the offset FPN is for low irradiances.

At low irradiance the SNDR is primarily limited by the offset FPN, which in this case is much higher than the temporal readout noise for both modes of operation either before or after compensation. This can be verified by analyzing the SNDR model presented in Eq. (5.6) with the measured readout temporal noise presented in table 6.2 and the FPN results presented in Fig. 6.15.

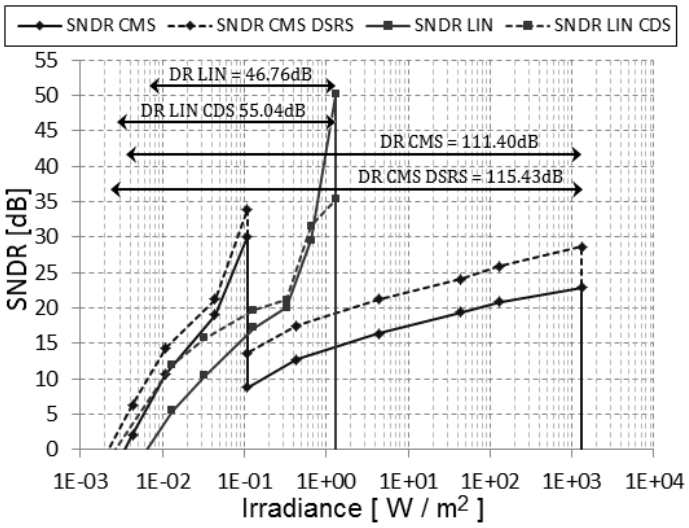


Figure 6.16- SNDR versus irradiance of the regular pixels of the array [art prepared by the author].

Now, comparing the results of Fig. 6.15 with the simulation results presented in section 5.7 in Fig. 5.27, it is clear that both the raw and the residual FPN of the experimental results are much higher than those predicted by the simulations. First of all it was already expected some increase of the measured FPN due to the additional FPN introduced by mismatches of the photodiodes and also PRNU not taken into account in the simulations. However a much higher increase is observed in the experimental results in relation to the simulation results both in the raw and in the residual FPN.

Although the sources of the additional FPN level are not yet well determined, it might be connected to the reasonable increase of temperature in the chip observed during the experiments. It was observed that the simple act of biasing the chip with the 3.3 V power supply makes a constant current of about 200 mA to flow through its supply voltage terminals. This high current level is connected to the operation of many of the digital circuit structures integrated in the chip that do not belong to this specific project.

This produces an increase of temperature on the chip of more than 10 ^{o}C above room temperature. This provokes the increase of the dark current of the photodiode, resulting in higher levels of DSNU, increasing thus the total offset FPN. This problem will be subject of future investigations and it must be taken into account in future multi-user integrated circuit design of our team.

6.3.2 Results with the Additional Columns with Induced Distortions

The effects of the two columns with induced distortions are now considered altogether with the regular pixels. In this case the mean value, μ_x, for each irradiance level must be recalculated using Eq. (6.1) without considering the component containing the sum of the values of the pixels of these columns, Σ_{col} defined in Eq. (6.2). Also the spatial variance must be recalculated for the present case using Eq. (6.4) without considering the component $\Sigma_{\Delta col}$ defined in Eq. (6.5).

The resulting mean value versus irradiance curves present no relevant difference from those curves presented in Fig. 6.14 with only the regular pixels, thus this plot will not be repeated here. The output signal swing, for both modes of operation, before and after FPN compensation for the present case are presented in table 6.4.

The signal swing results presented in table 6.4 also show small deviation from the previous results presented in table 6.2. Similarly to the previous case, as the linear mode of operation reaches saturation for an irradiance of about 1.31W/m^2, the signal swing from the dark to the saturation level is the total signal swing for this mode before and after FPN compensation. Likewise, for the CMS mode the signal swing is not really the total output voltage variation, because even for the highest tested irradiance of 1.31kW/m^2 the pixels of the array did not reach saturation.

All the pixels of the array, whether with or without additional distortion, use the same readout data acquisition system. Therefore, for the present case the measured readout output temporal noise for both operation modes, before and after FPN compensation is the same already the presented in table 6.2.

The FPN versus irradiance curves for the present case, for both modes of operation, before and after compensation, are shown in Fig. 6.17. Comparing the curves in Fig. 6.17 with those presented in Fig. 6.15, it is verified that that besides the PRNU peak, the additional distortion of the two different columns almost doubles the raw FPN in both modes of operation. Also in both modes, the residual FPN after their respective compensation remains almost at the same level as when the addition distortion was not considered. However, in the linear-logarithmic mode, the residual FPN presents a slight increase in relation to that of the previous case.

The array offset FPN and the peak of gain FPN in relation to the signal swing for the linear mode and for the linear region of the CMS mode for the present case are presented in table 6.5. The maximum and minimum total FPN for the logarithmic region of the CMS mode are also presented in table 6.5.

These results confirm that the additional columns distortion almost doubles the raw offset FPN, whereas the gain FPN remains close to the same level as in the previous case presented in table 6.3. In the logarithmic region of the CMS mode the total is also almost doubled, showing that the effect of the two columns with addition distortions basically affects the raw offset FPN.

In all cases the offset FPN after compensation is brought to almost the same level as those of the previous case. This indicates that the attenuation of the offset FPN caused by

distortions in the column amplifies is very effective for both techniques. Nevertheless, the CDS technique is shown to be a bit more effective for the linear mode than the proposed DSRS for the linear region of the CMS mode. On the other hand, attenuation of gain FPN with both techniques is shown to be of little or none effect for both modes of operation.

Table 6.4: Signal Swing with the Two Modified Columns and Temporal Noise

	Before FPN Compensation	**After FPN Compensation**
Signal Swing		
Linear mode $_{TOTAL}$	1.415 V	1.321 V
CMS mode $_{MEASURED}$	931 mV	925 mV

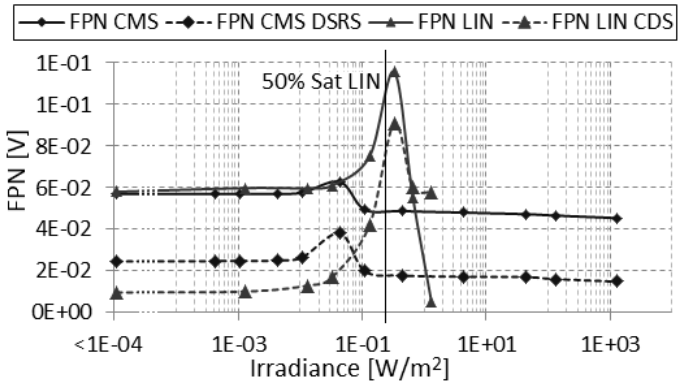


Figure 6.17- FPN of the regular pixels plus two columns with induced FPN [art prepared by the author].

In the present case the SNDR versus irradiance curves of the array for each mode of operation, before and after FPN compensation, are presented in Fig. 6.18. These SNDR curves were produced using the same model and temporal readout noise level of the previous case, and the FPN results shown in Fig. 6.17.

Table 6.5: FPN in relation to the Signal Swing with the Two Modified Columns

	Before FPN Compensation	**After FPN Compensation**
Linear Mode		
σ_{Offset}	4.08%	0.71%
$\sigma_{Gain,PEAK}$	7.08%	6.84%
CMS Mode Linear Region		
σ_{Offset}	6.09%	2.62%
$\sigma_{Gain,PEAK}$	2.86%	3.15%
CMS Mode Logarithmic Region		
$\sigma_{TOTAL,\max} = \sqrt{\sigma_{Offset}^2 + \sigma_{Gain}^2}$	5.21%	1.89%
$\sigma_{TOTAL,\min} = \sqrt{\sigma_{Offset}^2 + \sigma_{Gain}^2}$	4.85%	1.57%

The SNDR results before FPN compensation show that the additional distortions introduced by the two modified columns are reasonably reduced within the whole

illumination range when compared with the results presented in Fig. 6.16. On the other hand the compensated SNDR curves are brought to almost the same level as the compensated curves presented in Fig. 6.16 showing the efficacy of the two FPN compensation techniques.

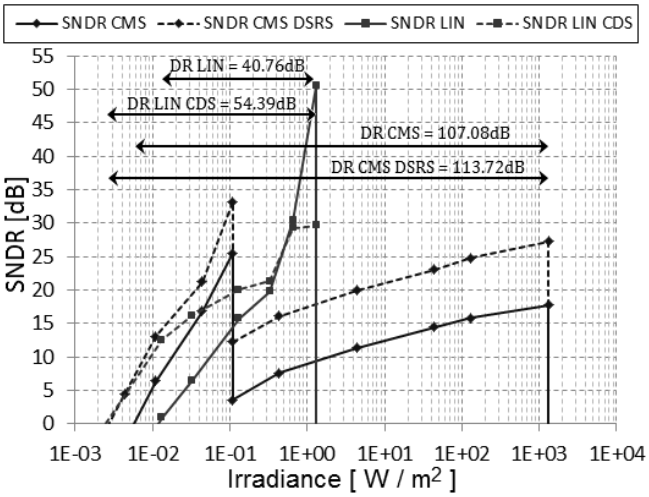


Figure 6.18- SNDR of the regular pixels plus the two columns with induced FPN [art prepared by the author].

As in the previous case, both techniques improve the dynamic range of the array towards low illumination, whereas towards high illumination it remains the same as before compensation. The improvement of dynamic range towards low illumination is 13.63 dB with CDS in the linear mode and 6.64 dB with the proposed DSRS technique in the CMS mode. The dynamic range reduction due to the additional column distortions, from the present to the previous case before and after FPN compensation in the linear mode is 6.00 dB and 0.65 dB respectively, and in the CMS mode is 4.32 dB and 1.71 dB respectively.

In the previous case the dynamic range improvement ratio between the CDS technique in the linear mode and the proposed DSRS technique in the CMS mode is 2.0527 times, whereas in the present case this ratio is of 2.0546 times. This shows that the expected improvement ratio is kept almost the same regardless the level of distortion of the array. However this might not be taken as a rule before further investigations.

6.4 Comparison between Different FPN Attenuation Techniques

Based only on the results presented in [56], [19], [44], [57], [59], [60], and [61], it is a very hard job to perform fair comparison between the different FPN compensation techniques. This happens because all these techniques are applied to pixels with different circuit topology, different fabrication technology, different pixel size, and different array size.

Therefore before uttering judgment based solely on the results presented in the respective works, some important characteristics should be taken into account considering the ideal case where at least: all the pixels were designed with the same size, all the arrays had the same dimension, the imagers were fabricated in the same CMOS

technology, they all employed the same data acquisition system, and all experiments were performed under the same conditions. Some of these characteristics are presented in Table 6.6.

Table 6.6: Qualitative comparison between the eight Lin-Log FPN attenuation techniques.

	2001 [56]	**2005 [19]**	**2006 [44]**	**2007 [57]**	**2009 [59]**	**2013 [60]**	**2014 [61]**	**THIS WORK**
APS Topology	4T	4T-PPD	7T	5T	7T	4T-PPD	5T	3T
On pixel automatic Lin-Log transition point	Yes	Yes	No	Yes	No	Yes	Yes	Yes
Possible Lin-Log transition point Adjustment	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Image Lag Suppression	Yes	*NA	Yes	*NA	*NA	*NA	Yes	Yes
Number of Readout Operations	2	4	≧ 4	*D2	4	3	2	2
Needs data recording for FPN Compensation	No	Yes	*D1	Yes	No	No	No	No
Needs to identify the region of operation to perform FPN compensation	No	No	Yes	Yes	Yes	Yes	No	No
Solution claims to compensate for FPN								
Linear Region	*NA	No	Yes	Yes	Yes	Yes	Yes	Yes
LOG Region	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Trans Region	*NA	No	*NAP	*D3	*NAP	Yes	Yes	Yes
Presents results of (raw VS residual) FPN								
Linear Region	No	Yes	No	No	No	No	No	Yes
LOG Region	No	Yes	Yes	No	Yes	Yes	No	Yes
Trans Region	No	Yes	*NAP	No	*NAP	Yes	No	Yes
Presents FPN results for the whole range of illumination	No	Yes	Yes	Yes	Yes	Yes	No	Yes
Provides SNDR or SNR analysis	No	No	Yes (SNR)	No	No	No	No	Yes (SNDR)

*NA – Information not available;
*D1 – Depends on how to apply two point calibration;
*D2 – Depends on the region of operation;
*D3 – Depends on the chosen technique;
*NAP – Not applicable;

In Table 6.6, the first row indicates the expected fill factor difference between the techniques if all the pixels were designed with the same size. The second row indicates if the lin-log transition point is performed in pixel using linear-logarithmic operation via low level reset modulation or externally using independent linear and logarithmic operation that combines two frames to produce the wide DR image. The third row indicates if it is possible to adjust the lin-log transition point, i.e. by modifying low level of the reset signal in CMS mode. The fourth row indicates if the technique deals with the image lag problem. The fifth row indicated the number of readout operations necessary to perform the respective compensation, this reflects directly on the speed of operation of the technique. The sixth row indicates if the technique requires external memory to perform FPN compensation. The seventh row indicates if it is necessary to identify the region of operation of the pixel to apply the compensation technique, what further reduces the operation speed of the technique.

It is also important to evaluate the claims and types of results presented by the authors of each different technique. From the eighth to the eleventh rows in Table 6.6 it is indicated in which region of the linear-logarithmic operation each technique is really useful to attenuate FPN. The four following row indicates if the authors of the respective techniques provide results of both raw and residual FPN, without which it is impossible to really tell how much of the raw FPN was attenuated or else if it really yields any attenuation. The following row indicates if the results presented by the authors evaluate FPN within the whole illumination range they claim their pixels to operate or if only for a single irradiance per region of operation, this is important because the FPN level may vary with the illumination level. The last row indicates if the DR of the respective technique was evaluated with or without the SNR of SNDR curves, this is important because as shown in [13] and along this work the right way to determine the DR of an imager is through its SNDR curve.

Details of the design and experimental results presented by the author of the different compensation techniques are presented in Table 6.7. Being aware of the details expounded above it is simple to perceive that these pieces of information alone are not sufficient to make a fair comparison between the different compensation techniques. As shown in Table 6.7 many of them do not present the raw FPN results, thus it is not possible to tell how much attenuation the technique really produced. A good example of the importance of such information is the results presented in [19] of 2005, where the author present the raw and residual FPN in the linear region showing that the technique actually added FPN in this region instead of attenuating it.

Table 6.7: Design and Experimental Information.

	2001 [56]	**2005 [19]**	**2006 [44]**	**2007 [57]**	**2009 [59]**	**2013 [60]**	**2014 [61]**	**THIS WORK**
CMOS Technology	AMS 0.8 µm DPDM CMOS	0.35 µm 1P3M CMOS	0.18 µm 1P4M CMOS	AMS 0.35 µm 2P4M CMOS	AMI 0.5 µm 2P3M CMOS	Samsung 0.13 µm CIS	0.18 µm 1P6M CMOS	AMS 0.35 µm 2P4M CMOS
Pixel Size	30 µm x 30 µm	7.5 µm x 7.5 µm	5.6 µm x 5.6 µm	10 µm x 10 µm	23.40 µm x 27.15 µm	2.25 µm x 2.25 µm	6 µm x 6 µm	10 µm x 10 µm
Fill Factor	*NA	37%	33%	44%	24.56%	*NA	32.54%	56.5%
Array Size	160 x 120	640 x 480	352 X 288	100 x 10	16x16	320 x 240	100 x 100	8 x 8
Raw/Residual FPN Lin Region	*NA / *NA	1 mV / 6.5 mV	*NA / *NA	*NA / 2% *RCT	*NA / 13.8 mV	*NA / *NA	*NA / 12 mV	30.8 mV / 18.6 mV
Raw/Residual FPN Log Region	*NA / 6.5 mV	13 mV / 5 mV	36 mV / 3.08 mV	*NA / 2% *RCT	27.6 mV / 19.1 mV	33 *LSB / 6 *LSB	*NA / **4 mV	26.4 mV / 14.8 mV
Measured DR	120 dB	124 dB	143 dB	120 dB	121.26 dB	105 dB	143 dB	***111.40 dB / 115.43 dB

*NA – Information not available;
*RCT – Relative Contrast Threshold [59];
*LSB – Of a 10-bit ADC [60];
** – This value is reached for V_{log} = 2.2V [61];
*** – BEFORE / AFTER FPN Compensation using SNDR Analysis;

Also as the presentation of the results is not made in a standard way, further hindrances are imposed to evaluate either the effectiveness of the technique itself or to compare it with other techniques. For example in [57] the results are presented in term of percentage of contrast threshold and it does not provide the necessary information to make the conversion of the results. In [60] the results are presented in LSB of a 10-bit ADC but it does not tell how much a LSB represents in millivolts in order to compare it with other results, however in this case it is possible to tell how much FPN attenuation is produced by the technique.

In summary, the presented results are good enough in some cases to evaluate the effectiveness of the respective technique. However, they are of little usefulness to compare it with another compensation method. Previously in this chapter it was presented the results of the proposed technique against the CDS technique applied to the linear mode in the same fabricated array. Using this approach it is reasonable to tell if the results are acceptable or not against each other, otherwise it is not fair.

6.5 Final Considerations and Future Works

The results so far presented assert the ability of the proposed technique in reducing FPN and especially column FPN in the complementary linear-logarithmic mode of operation, and also that these results are compliant to those yielded by the classical CDS technique in the linear mode. It might be recalled that the classical CDS technique cannot be directly applied to the CMS mode of operation, but rather only to the linear region as is done in [57], requiring additional computational verification.

The ability of the proposed technique to attenuate FPN in the CMS mode can also be verified when comparing the resulting images of the five pairs of frames on the right in Fig. 6.13, before and after FPN compensation. And though the proposed DSRS technique is not as optimized as those techniques, applied selectively per mode or region of operation, presented in [44] and [57], the proposed compensation can be executed at least at the same rate of a regular CDS operation in the linear mode.

Further experimental results with the shielded pixels of the array are presented and discussed next, as well as further considerations on the current and future works.

6.5.1 The Eight Shielded Pixels of the Array

Concerning the pixels with metal shielding, it was observed that from the irradiance of 437 mW/m^2 and beyond, the designed partial optical shielding for those seven pixels in the positions (2, 2), (7, 2), (3, 7), (3, 8), (4, 7), (5, 7) and (5, 8), is rather ineffective. The ineffectiveness of the metal shielding is yet under investigation, but we suppose that this happens especially due to the large number of photons reaching the photodiode on the small but finite exposed area, by metal-edge diffraction, and also due to the large number of charge carriers diffused through the bulk, coming from the surrounding pixels or through the edge of the array, reaching these pixels and also the pixel (4, 8).

The expected response for the shielded pixels was one like of a pixel with reduced fill factor, however this kind of response was observed just for a short range of illumination. On the other hand, the responses of those pixels with additional column distortions were

exactly as expected within the whole range of illumination, that is column FPN. The behavior of the shielded pixels is not treated in this work and the analyses of the unexpected shielding effects are to be discussed in future works.

The two last pairs of frames of the CMS mode, before and after compensation, presented in Fig. 6.13 are examples of the low efficacy of inducing FPN through metal shielding for high irradiances. Notwithstanding, at such high irradiances, other sources of FPN as well as the induced column FPN are still visible, and the proposed technique is shown to be efficient in reducing them.

6.5.2 The Array Histograms

The histogram of the array is a graphical method of analysis that shows the Gaussian distribution of the output of the pixels taken into account in the analysis around the mean output value. This method produces a single curve for each irradiance level. It shows both the raw FPN of the array and also how significant the FPN attenuation is for a given technique. The thinner the curve, the more significant the FPN attenuation is.

The total spatial variation of the 64 pixels of the array for the pure linear and CMS modes, before and after FPN compensation, for the dark condition is shown by the histogram of Fig. 6.19. These results show that before FPN compensation both curves have almost the same mean value and after compensation their mean values are very different. They show the ability of each compensation technique in attenuating FPN in each mode, and that CDS for the linear mode is more efficient for the low light level than the proposed DSRS for the CMS mode at the same illumination level.

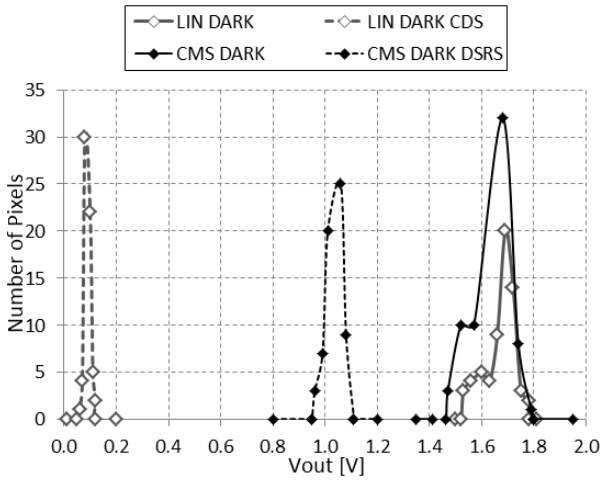


Figure 6.19- Histogram for linear and CMS modes at dark condition [art prepared by the author].

The histograms presented in Fig. 6.20 show the total spatial variation of the 64 pixels of the array for the pure linear mode, before and after FPN compensation, for the dark condition and for the irradiance level of 13 mW/m^2. These results show that the mean values are near each other either before or after compensation, and they show also the efficacy of the CDS technique in attenuating FPN in the linear mode for low irradiance levels.

The histograms presented in Fig. 6.21 show the total spatial variation of the 64 pixels of the array for the CMS mode, before and after FPN compensation, for the dark condition

and for two different irradiance levels. These results show that the mean values before and after FPN compensation move to the same direction as the irradiance increases. They show also that the proposed DSRS technique is able to attenuate FPN either for low or high irradiance levels.

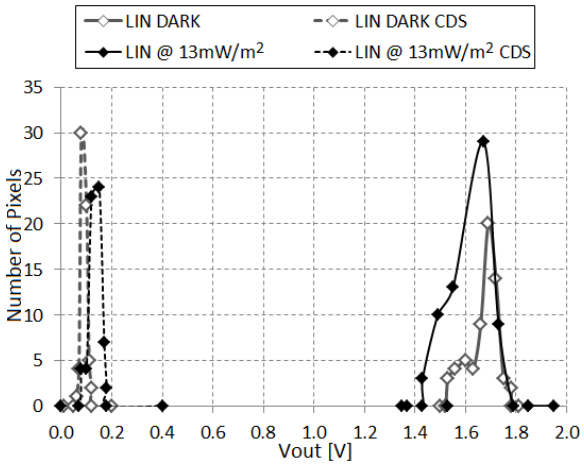


Figure 6.20- Histogram for linear mode at dark and low light conditions [art prepared by the author].

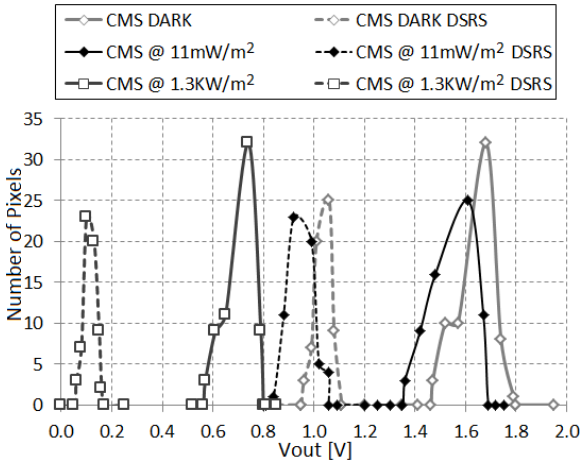


Figure 6.21- Histogram for CMS mode at Dark, Low, and High Light Conditions [art prepared by the author].

These results show how the output values of all the pixels of the array are distributed around the mean level for each illumination level. It gives an insight of how much the output of some pixels of the array are away from the mean value. The presented results complement the results presented in the previous sections, showing again the ability of the proposed DSRS technique in attenuating FPN in the CMS mode.

6.5.3 FPN in the literature

In this work the raw and residual FPN of the array was measured and treated for each irradiance level at which the array was tested. The standard way of analysis [52], defined only for the linear mode, is measuring the FPN distortions for dark level DSNU and for the irradiance at which the array reaches 50% of the saturation level DSNU. The DSNU used is a constant quantity within the whole illumination range, whereas the PRNU is used as a parameter of a linear function that varies with illumination. However, as shown by the

results presented in Fig. 6.15 and 6.17, the linear model for the PRNU can deviate considerably from the real response.

There is no standard way to present and analyze FPN neither in the logarithmic nor in the complementary linear-logarithmic modes. As shown in section 6.4, most of the works in the literature present only the residual FPN and not the raw FPN, making it hard to know how much it was attenuated. The lack of an standardized way to present the FPN results in the seven different works presented in the literature dealing with FPN in the linear-logarithmic mode [56], [19], [44], [57], [59], [60] and [61], make it hard to compare the results among those techniques. Also they use different pixels and array size, thus hindering fair comparisons.

In order to perform a fair comparison between the various FPN compensation approaches, more accurate results from the various techniques applied to the same pixel array are needed. It is also interesting that these experiments be performed with the standard method to produce flat illuminated fields using an integrating sphere. Doing this it will be easier to propose a more general way to analyze FPN in the CMS mode.

6.5.4 FPN versus Array Size

Another interesting point worth of further investigations is the raw and residual FPN as a function of the array size. Due to the high level of the measured FPN before and after compensation, especially in the pure linear mode, in relation to those presented in the literature, there is a strong feeling that the FPN level strongly depends on the size of the array. Though the introduction of FPN is a random process during fabrication, it seems that as the number of pixels in the array increases, the standard deviation approaches the mean level. Although it cannot be proved by the results presented in this work, because of the use of such small array, it is an interesting point to be investigated with larger pixel arrays.

6.5.5 Future Works

Future works on wide dynamic range CMOS image sensor with the proposed technique include: more elaborate comparisons between the existing compensation techniques using the same array or at least an array with different pixel topologies, but fabricated in the same chip and with the same size, because it is not fair to compare different techniques in either different technologies or different array sizes, as it is usually done in the literature; the design of an imager with a higher pixel density to evaluate the proposed technique with static and dynamic images; evaluation of the aging effects in imager arrays using the method to attenuate image lag, featured in the proposed DSRS technique, against that of the LINLOG^{tm} method presented in [47]; investigation on the automatic adjustment of the low level of the reset signal in order to improve signal swing of the imager; and the application of the proposed technique to other image sensor technologies as infrared sensors to both increase the dynamic range and attenuate FPN.

Conclusions

A simple way to improve the image quality of the basic 3T APS operating in the complementary linear-logarithmic operation was presented in this work. The technique proposed in this work is applied mainly for suppressing fixed-pattern noise in such imager, and also for suppressing image lag without the need of more complex techniques which either reduce the fill factor of the pixel or the imager life time.

The ability of the proposed technique to reduce image lag was demonstrated only through simulation results, where it was shown that the application of the pseudo-flash reset technique is well fit for the array operating in the linear-logarithmic mode. The use of the pseudo-flash reset helps keeping the fill factor of the pixel as small as possible because it does not need the use the PMOS reset transistor. Moreover, it does not require the hard reset approach that reduces the imager life time due to gate-oxide voltage overstress in the reset transistor of the pixel.

It was shown that a simple extension of the pseudo-flash reset technique would be applied to produce a voltage reference point that would be employed to compensate the FPN spatial distortions of the array operating in linear-logarithmic mode. The ability of the proposed technique in attenuating FPN was demonstrated either by simulations and experimental data. To this intent a small pixel array with eight rows and eight columns was fabricated in a standard 4-metal 2-poly n-well 0.35μm CMOS technology.

The implementation of such technique requires only a minor modification to the conventional three-FET pixel design and control-signal scheme. Thus the pixel complexity is kept low and its size small, rendering its fill factor as high as that of the basic 3T APS, except for a slight reduction due to the additional connection line for the reset-transistor drain terminal RDR. In the proposed solution the drain terminal of the reset-transistor of the pixel is used both to supply the reset level of the photodiode and also to impose the reference level applied to compensate the array FPN.

The experimental results presented in this work confirm that the proposed technique is able to attenuate FPN in a quite steady ratio within the whole tested illumination range. The efficacy of the proposed technique in attenuating FPN is proven even when additional column distortion is deliberately introduced in the pixel array. Some shielded pixels were also deliberately designed in the pixel array in order to emulate other sources spatial FPN. And though the distortions introduced by the shielded pixels were not accurately investigated in this work, the some histograms presented in this work show that even the FPN introduced by these pixels is somehow attenuated by the proposed technique.

The proposed technique is proven to work well even under a non-customized electrical environment as that of the experimental setup presented in section 6.2. Therefore it is expected to work even better on a customized printed circuit board.

The technique was compared with well-established CDS technique applied to attenuate FPN in the linear mode of operation. The results yielded by the CDS technique in the linear mode of operation of the fabricated array are not far from those yielded by the

proposed technique in the linear region of the array operating in linear-logarithmic mode. Though the CDS technique is shown to produce better results in the low light range, it cannot be directly applied to the linear-logarithmic mode of operation, but only to its linear region, yet requiring additional computational verification.

Unfortunately, due to silicon area limitation for this project, a larger array could not be implemented. The small size of the array imposed some limitations, such as producing high quality images showing the results before and after FPN compensation. Also because of the small size of the array, and the lack of a standard way to present FPN results in CMS mode, it was not possible to produce more detailed comparisons with different techniques found in the literature.

The presented work shows that the proposed solution to reduce both image lag and FPN in the APS operating in linear-logarithmic mode, based on a simple modification revisiting a well-established pixel topology, leads to an improved CMOS image sensor at no additional fabrication cost.

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