Paper

Minimization of Column FPN in linear-logarithmic CMOS Image Sensors by Reset-Drain Actuation

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Abstract Active-pixel-sensors (APS) operating in linear-logarithmic mode yield high-dynamic-range images. However, fabrication non idealities result in fixed-pattern noise (FPN) across the focal-plane array and cannot be reduced by conventional techniques as correlated double sampling. Alternative techniques may be used to reduce FPN but they increase the complexity of either the pixel or the external circuitry. Column FPN is of particular concern in CMOS imagers because they produce undesirable vertical stripes in the image. In this work a simple technique is proposed to reduce column FPN in a modified 3T APS operating in the liner-logarithmic regimen. Simulations show that the proposed technique can reduce the column FPN by more than 80% in range larger than 120dB.

Key words: Image Sensor, APS, FPN, Wide Dynamic Range.

1. Introduction

Active-Pixel Sensors (APS) operate often in either of two modes: linear or logarithmic. The linear mode promotes good sensitivity at low illumination but low dynamic range (DR) towards high illumination. On the other hand, the logarithmic mode features high DR towards high illumination but quite poor sensitivity at low illumination.

In order to achieve both good sensitivity to low illumination and high DR towards high illumination, the APS can be operated in the combined linear-logarithmic mode [1]. There are many techniques to achieve high DR that combine linear and logarithmic response [2], but they either increase the pixel complexity or reduce frame rate, by performing multiple-frame captures.

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An important note, however, is that when a conventional 3T APS is operated in the logarithmic mode, classical correlated double sampling (CDS) cannot be deployed, leaving the focal-plane array with a sometimes unacceptable amount of Fixed-Pattern Noise (FPN) uncompensated. FPN is caused by pixel-to-pixel output variation under uniform illumination due to component and interconnection mismatches across the array. Column FPN, produced by the column amplifier, is the most serious source of FPN in CMOS imagers because while the other sources of FPN usually produce non-uniformities randomly distributed across the image, it produces annoying vertical stripes in the image [7].

Several techniques have been proposed to reduce FPN in the logarithmic mode, as storing the pixel offsets [2], at the cost of added memory and liability to temperature variations; or applying double sampling readout subtraction (DSRS), by producing a voltage or current reference at the sense node of the pixel [3], [4], [5] and [6]; or by multimode readout pixel architectures [7, 8]. Such techniques require more complex pixel circuitry, which therefore reduces its fill factor.

In this work we present extended investigation results of a modified and simple DSRS technique to reduce FPN in the 3T APS operating either in logarithmic or in linear-logarithmic modes [9] and [10]. As the proposed technique can be applied directly to the 3T APS, the fill factor can be kept as large as possible.

The proposed technique will be described in section II. Simulations results asserting the solution are shown in section III. The pixel implantation is discussed in section IV. Finally, conclusions drawn from this work are given in section V.

2. Minimizing Fixed-Pattern Noise

The technique consists in letting the drain of the reset transistor, RDR connection of M1 in fig. 1, free to be connected at any voltage level and using this particular connection to establish a voltage reference at the sense node for the second output voltage readout during the reference time, tref fig. 2. By double sampling the output voltage, the first sample, s1 in fig. 2, registers the signal and the offset FPN, and the second, s2 in fig. 2, registers the voltage reference and also great part of the offset FPN. The subtraction of the first sample from the second suppresses the common offset FPN, which is present invariably in both samples.

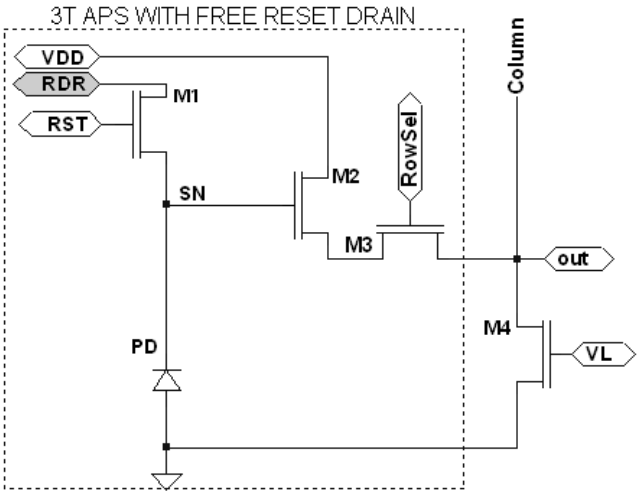

Fig.1 3T APS with free reset-transistor drain to apply the voltage reference

To implement the proposed solution, the set of signal controls shown in fig. 2 can be used to establish the voltage reference. The upper waveform, V_{SN}, represents the sense-node signal under five different levels of illumination. When exposed to the three higher levels of illumination V_{SN} reaches the logarithmic region in the beginning of integration time, t_{int}; and for the other two lower levels, the respective signals remain fairly linear until the end of the integration time. In the same figure, V_{RST} represents the reset signal with modulated low level; and V_{RDR} represents the signal applied at the drain of M_1 to either bias this transistor, high level, or to produce the voltage reference for the second sampling, low level. P-FRST pseudo-flash reset, meant to reduce image lag [9], and t_{rst} stand for the reset time. It is important to notice that the low level of V_{RDR} must be lower than the lowest possible level of V_{SN} [9]. The lowest level of V_{SN} is reached when the pixel is under the highest illumination condition.

The effectiveness of this technique was evaluated by means of Monte Carlo simulations and the results are shown in the next section.

3. Simulations and Results

Monte Carlo simulations of the pixel, designed in the AMS CMOS 0.35μm technology, were performed to verify the total and reduced column FPN and the FPN across the array. Along a column all pixels share the same column amplifier, M4 fig. 1. The FPN across the array is determined by mismatches of M1, M2, M3 and M4. The FPN between columns is determined by mismatches of M4. Other sources of FPN as dark current variations and photo response non-uniformities were not considered in this study.

The setup of the signal control in fig. 2 for the linear-logarithmic operation is the following: the VDD voltage is 3.3V, the reset low level is fixed at 2.5V, and the low level of VRDR is 1.4V. The illumination level is represented here by photocurrents varying from 1fA to 10uA.

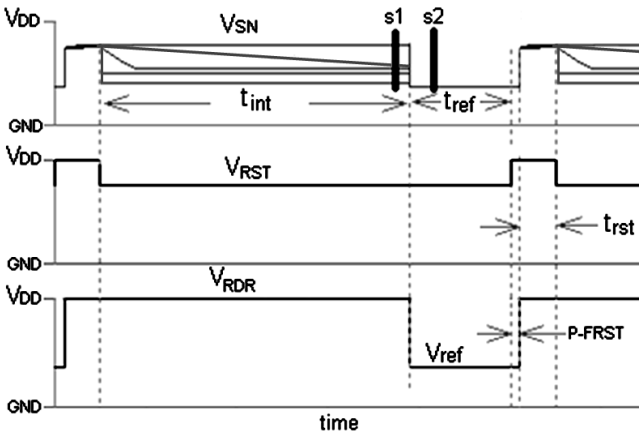

Fig.2 Double-sampling voltage reference, signal scheme

The results presented in this section are the mean and standard deviation of the output of the pixel, before and after FPN correction, of 256 Monte Carlo simulations for each photocurrent. An example of the pixel voltage output in the time for 10 Monte Carlo

simulations is given in fig. 3. Each time slot in fig. 3 shows alternately part of the integration and reference times of two different pixels. In the first pixel the mismatches of M1, M2, M3 and M4 were applied, while in the second pixel no mismatch was applied. To produce the results for each photocurrent as presented next, the output of pixel 1 was sampled twice, as shown in fig. 4, according to the scheme in fig. 2.

In the dynamic range of 120dB indicated in fig. 5, the output voltage swing after the FPN correction is 743mV that is almost the same before correction, 744mV, as shown in fig. 5. In this graph VOUT and C_VOUT stand for the output voltage variation for the pixel with illumination before and after FPN correction, respectively.

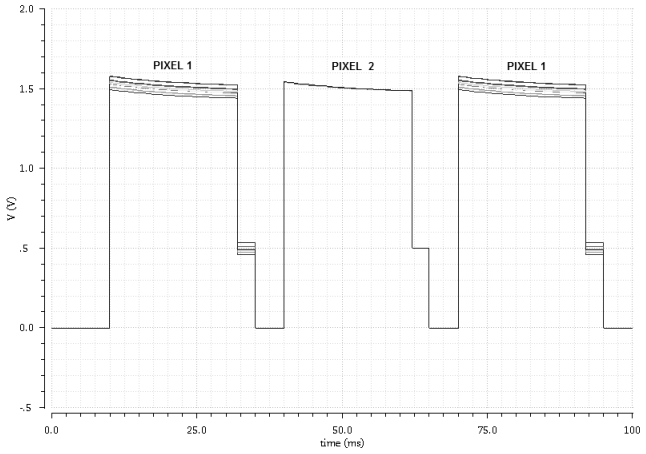

Fig.3 Ouput for 10 Monte Carlo simulations with Iph of 1pA

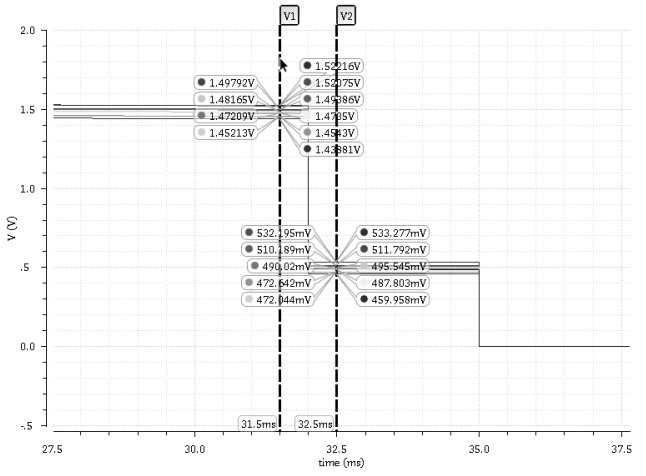

Fig.4 Sampling times

The total and reduced FPN across the array and between columns are shown in fig. 6. In this graph Array FPN and Column FPN stand for the FPN before correction across the array, and between columns respectively, and R Array FPN and R Column FPN stand for the FPN after correction across the array and between columns respectively.

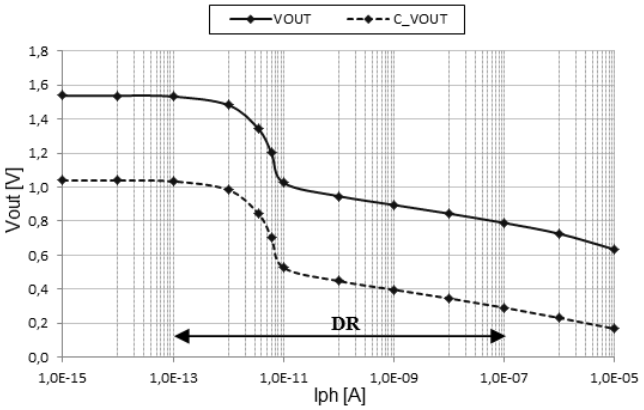

Fig.5 Linear-logarithmic output before and after FPN correction

The simulation results have shown a reduction better than 80% of the FPN across the array throughout the complete illumination range, R Array FPN in fig. 7. The FPN between columns can be reduced to better than 80% in the low illumination range, and better than 90% in the high illumination range, R Column FPN in fig. 7.

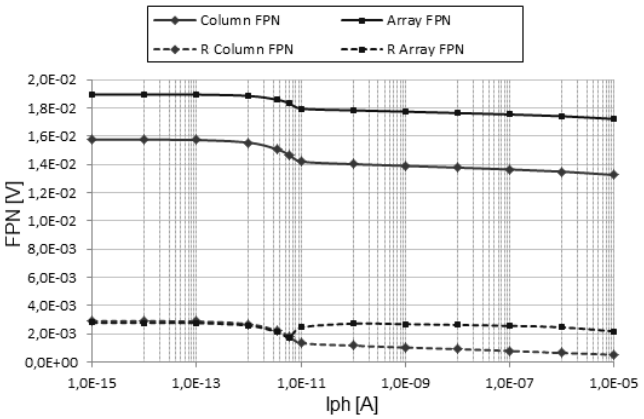

Fig.6 Total and reduced in linear-logarithmic mode

These results show that, in the linear-logarithmic mode, the maximum FPN across the array in the dynamic range indicated in fig. 5, without correction is about 2.54% of the signal swing in this range. While the maximum FPN across the array with correction is about 0.38% of the signal swing in this range. The column FPN before correction is 2.12% of the total signal swing and 0.39% after correction.

This technique can also be applied for the pixel operating in full-logarithmic mode with the reset signal, VRST in fig. 2, always in VDD. The VDD voltage level is still 3.3V, and the low level of VRDR is shifted to 2.0V. As in the previous case, the illumination level is

represented by photocurrents varying from 1fA to 10uA.

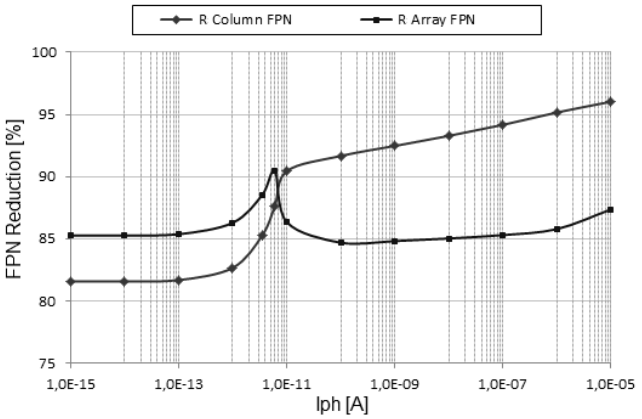

Fig.7 Percentage of FPN reduction in linear-logarithmic mode

In the dynamic range of 120dB indicated in fig. 8, the output voltage swing after the FPN correction is 246mV that, as in the previous case, is almost the same before correction, 247mV, as shown in fig. 8. In this graph VOUT and C_VOUT stand for the output voltage variation for the pixel with illumination before and after FPN correction, respectively.

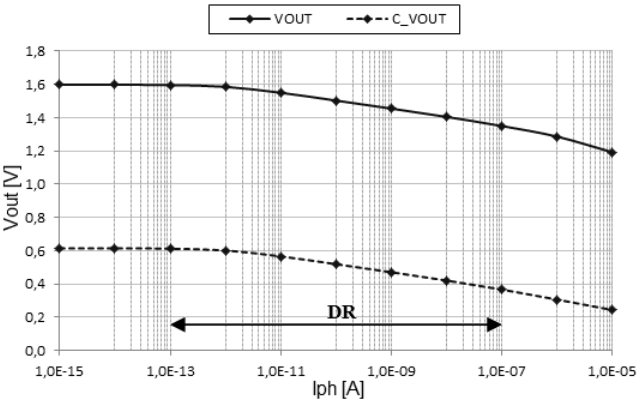

Fig.8 Full-logarithmic output before and after FPN correction

Comparing with the results of the linear-logarithmic mode, presented above, fig. 5, the full-logarithmic mode has reduced sensitivity especially in the low illumination region. The signal swing in linear-logarithmic mode is three times higher than that in full-logarithmic mode either with or without FPN correction.

The total and reduced FPN across the array and between columns are shown in fig. 9. In this graph Array FPN and Column FPN stand for the FPN before correction across the array, and between columns respectively, and R Array FPN and R Column FPN stand for the FPN after correction across the array and between columns respectively.

The simulation results have shown a reduction better than 80% of the FPN across the array throughout the complete illumination range, R Array FPN in fig. 10. The FPN between columns can be reduced to better than 85% in the complete illumination range, R Column FPN in fig. 10.

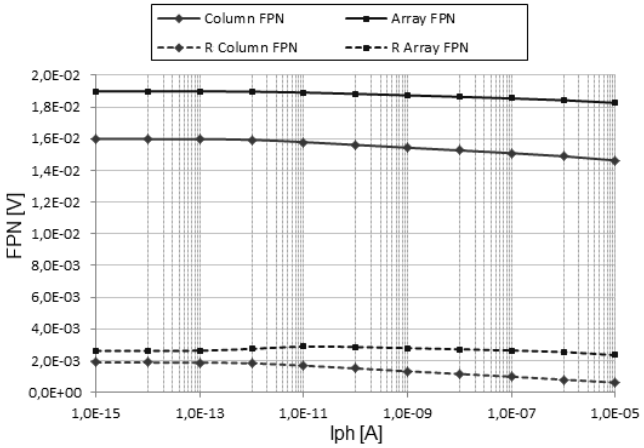

Fig.9 Total and reduced FPN in full-logarithmic mode

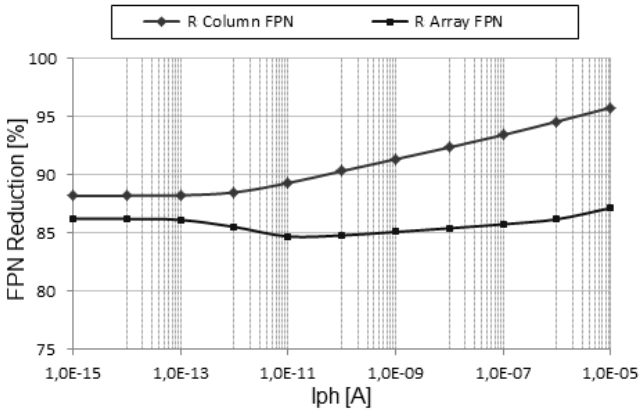

Fig.10 Percentage of FPN reduction in full-logarithmic mode

These results show that, in the full-logarithmic mode, the maximum FPN across the array in the dynamic range indicated in fig. 8, without correction is about 7.70% of the signal swing in this range. While the maximum FPN across the array with correction is about 1.17% of the signal swing in this range. The column FPN before correction is 6.48% of the total signal swing and 0.77% after correction.

These results show a true improvement in FPN reduction for active pixel sensors working in full-logarithmic mode when compared with some previous results in the literature. The solution in [4], using a 5T NMOS pixel in a CMOS 0.5μm technology, has a signal swing of 300mV in 120dB, and achieves a remaining FPN of 2.5% of the signal swing in this range. The solution in [5], using a 4T PMOS pixel in the same

CMOS 0.35µm technology, has a signal swing of 231mV in 120dB, and achieves a remaining FPN of 2.9% of the signal swing in this range. The solution in [6], using a 5T PMOS pixel in the same CMOS 0.35µm technology, has a signal swing of 705mV in 120dB, and achieves a remaining FPN of 2.1% the signal swing in this range.

The proposed pixel operating in linear-logarithmic regimen yields much better results, with a signal swing of 743mV in 120dB, and a remaining FPN of 0.38% of the signal swing in this range.

4. Pixel and Array Implementation

The greatest benefit of the proposed technique in relation to the previous solution is the use of only three FETs in the APS, exactly as in the basic 3T APS. However, the proposed pixel uses an additional line connection for the drain of the reset transistor, RDR in fig. 1. Due to this additional connection the fill factor of the proposed pixel may be slightly reduced compared to that of the basic 3T APS.

The proposed 3T APS, the schematic diagram of which is shown in fig. 1, has been designed in the AMS standard 4-metal 2-poly CMOS 0.35µm technology. The layout of pixel shown in fig. 11 has the following characteristics: pixel size 10µm x 10µm and fill factor of 56%.

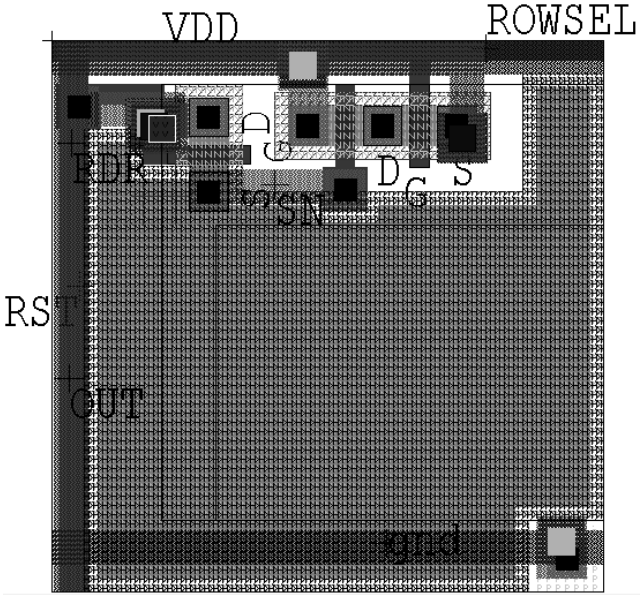

Fig.11 Layout of a 10µm x 10µm pixel with a fill factor of 56%

For further experimental evaluation of the proposed technique, a small array of eight rows and eight columns, fig. 12, has been sent for fabrication. In order to induce more column FPN two of the column-amplifiers have been designed with their channel width higher than the other six. The standard width of the column-amplifiers is 0.7µm while that of one of the two different columns is 1.0µm and that of the other is 1.2µm, which are indicated in fig. 12.

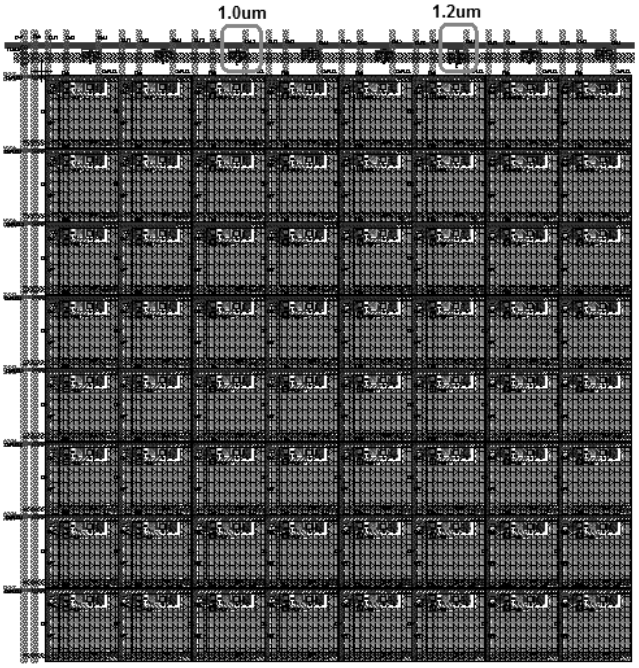

Fig.12 Layout of a small 8x8 array with the pixel of fig. 11, indicating the two columns where the column amplifier purposefully features different sizes for the gate of the buffer FET

5. Conclusions

The proposed technique provides a simple way to reduce both total and column FPN in the linear-logarithmic APS. This is achieved with a minor modification to the conventional 3T pixel design and control-signal scheme, and has been evaluated by Monte Carlo simulations. The technique is also effective to reduce FPN in the full-logarithmic APS. The pixel complexity and size is kept low, and its fill factor can be as high as that of the basic 3T APS, though it suffers a slight reduction due to the additional connection line for RDR. This solution, based on simple modification revisiting an established pixel topology, leads to improved CMOS image sensor at no additional fabrication cost.

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