# A 143dB 1.96% FPN Linear-Logarithmic CMOS Image Sensor with Threshold-Voltage Cancellation and Tunable Linear Range

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***Abstract*- This paper presents a high dynamic range (DR) linear-logarithmic (Lin-Log) CMOS image sensor (CIS) pixel with on-chip tunable linear range and threshold voltage cancellation scheme for reducing fix pattern noise (FPN). A column shared-OP with programmable gain was also applied to reduce the gain loss of source follower in conventional APS structure. A prototype chip with 100 x 100 pixel array and pixel pitch as 6 x 6 $um^2$ and 3.3V operation has been designed and fabricated in 0.18um TSMC 1P6M standard process. The measured results achieve a dynamic range of 143dB, a FPN related to sensitivity in log response (rms/log-sensitivity) of 1.96%, and a FPN related to full-swing in log response (rms/$V_{log\text{-}swing}$) of 0.45%, respectively.**

## I. INTRODUCTION

A high dynamic range (DR) CMOS image sensor (CIS) is widely used in biophysics and radiography. The conventional logarithmic CIS (Fig. 1) demonstrated a DR around 120dB with major drawbacks as follows: (1) limited voltage swing (0.2V~0.3V) degrades signal-to-noise ratio (SNR), and (2) large fix pattern noise (FPN) due to process variation. Linear-logarithmic (Lin-Log) architecture was proposed to increase DR and keep voltage swing like active pixel sensor (APS). The Lin-Log sensor keeps sensitivity of low-illuminated image and compress high-illuminated image with logarithmic response. It effective extends the DR by conserving the detail in low light and over-exposed area as well. The conventional high DR CIS is suffered from large FPN induced by the process-dependent logarithmic response. Off-chip compensation techniques are usually required to solve the FPN issue with additional signal processing effort and cost. Conversely, on-chip calibration in logarithmic CIS provides an efficient solution for FPN reduction. Therefore, a Lin-Log CIS with threshold voltage cancellation and tunable linear region is proposed to achieve a high dynamic DR imaging with on-chip FPN compensation.

In the other hand, how to decide the switching point between linear and logarithmic response is also an important issue in this type of CIS to get the best contrast under different environment. Some researches use off-chip decision [3], but it must take more effort to fit linear and logarithmic curve. For above reason, the on-chip decision was developed [5][6].

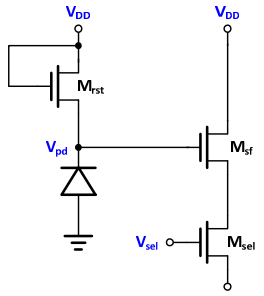


Fig. 1. Conventional logarithmic CMOS image sensor

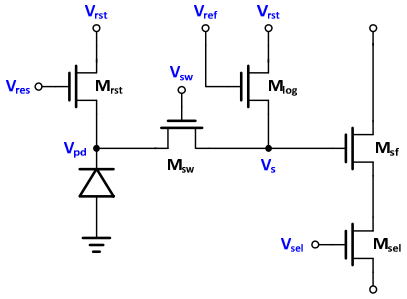


Fig. 2. Proposed Lin-Log CMOS image sensor

In this paper, a detail description of the design of a high DR Lin-Log CIS with FPN reduction by using threshold voltage cancellation scheme and tunable linear region is presented. This work also applies column shared-OP with programmable gain to reduce the gain loss of source follower in conventional APS structure. Column shared-OP also uses pixel transistors effectively.

The rest of this paper is organized as follows. The pixel circuit and column circuit designs are described in Section II. The experimental results of the realized prototype chip are shown in Section III. Finally, conclusions are drawn in Section IV.

## II. ARCHITECTURE

### *A. Conventional logarithmic CIS architecture*

A conventional logarithmic CIS imager is shown in Fig. 1. In this circuit, $M_{sf}$ and $M_{sel}$ act as source follower and select switch. The small current generated by photodiode makes $M_{rst}$ to operate in subthreshold region. In subthreshold region,

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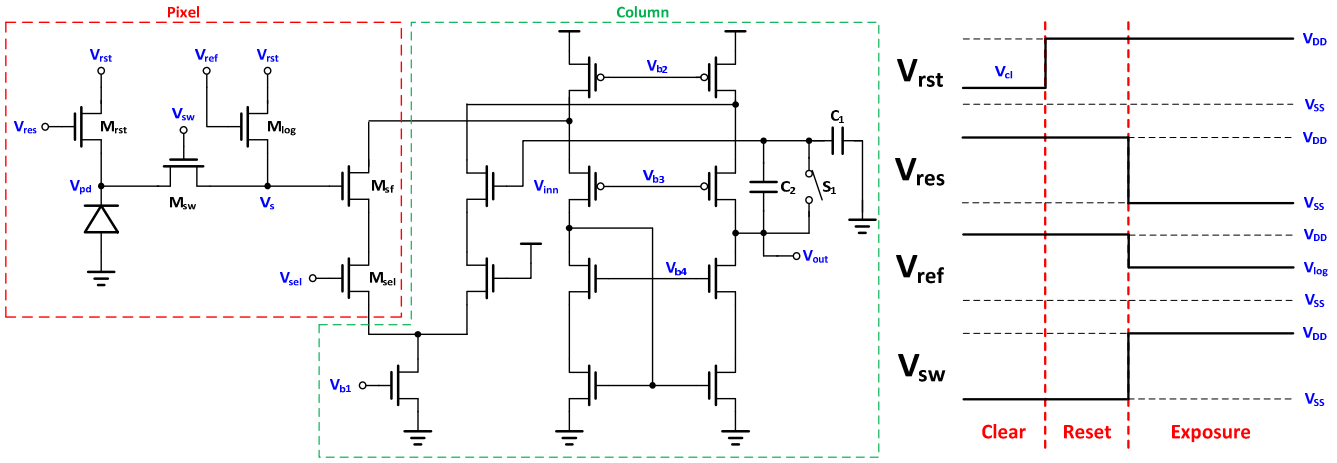


Fig. 3. Proposed pixel structure with column circuit and timing diagram

the gate-source voltage is proportional to logarithm of current flowing into $M_{rst}$. The output voltage at node $V_{pd}$ is determined by I-V equation in subthreshold region shown in (1):

$$V_{pd} = V_{DD} - V_{th,n} - nV_T \cdot ln\left(\frac{I_{ph}}{I_0}\right) \quad (1)$$

where $V_{th,n}$ is the threshold voltage of $M_{rst}$, $I_0$ is saturation current in subthreshold region, n is body-effect coefficient, and $V_T$ is thermal voltage. The output voltage includes a process dependent term $V_{th,n}$ from $M_{rst}$ and causes a large FPN in this type sensor.

### *B. Proposed Lin-Log CIS architecture*

A new 5T Lin-Log pixel design and readout scheme to solve FPN problem in conventional logarithmic CIS is shown in Fig. 2. Comparing to conventional logarithmic CIS, $M_{rst}$ and $M_{sw}$ were implemented to achieve threshold voltage cancellation. The pixel operation consists of three phases shown in Fig. 3 as clear phase, reset phase, and exposure phase.

**Clear phase:** $M_{rst}$ and $M_{log}$ are ON, $M_{sw}$ is OFF, and $V_{pd}$ and $V_s$ is charged to the voltage $V_{rst}$ ($V_{rst}$ = $V_{cl}$ during the clear phase). The main purpose in this phase is to eliminate the exposure value of last frame which will affect the reset voltage at reset phase.

**Reset phase:** $M_{rst}$ and $M_{log}$ are still ON. $M_{sw}$ remains OFF for isolating $V_{pd}$ and $V_s$ to prevent the logarithm related term in (1) being sampled at this phase. The voltage $V_{rst}$ is changed from $V_{cl}$ to $V_{DD}$. $V_s$ is pulled to a threshold voltage related term shown in (2):

$$V_1 = V_s = V_{DD} - V_{th,n} \quad (2)$$

As (2), $V_s$ is a threshold voltage drop from $V_{DD}$.

**Exposure phase:** The device $M_{rst}$ is OFF and $M_{sw}$ is ON. $V_{ref}$ is changed from $V_{DD}$ to $V_{log}$. The photodiode starts the integration. At low-illumination condition, the pixel behaves like a conventional 3T-APS by keeping $M_{log}$ OFF; and $V_s$ is discharged as linear response. At high-illumination condition, $V_s$ is discharged below the threshold to turn ON $M_{log}$ in subthreshold region. Thus $V_s$ is inversely proportional to photocurrent determined by I-V equation in subthreshold region of $M_{log}$ shown in (3):

$$V_2 = V_s = V_{pd} = V_{log} - V_{th,n} - nV_T \cdot ln\left(\frac{I_{ph}}{I_0}\right) \quad (3)$$

(3) shows that the signal voltage ($V_s$) in logarithmic response. By correlated double sampling (CDS), $V_1$ of (2) is subtracted from $V_2$ of (3) as shown in (4), the process dependent threshold voltage variation is canceled out.

$$\Delta V = V_1 - V_2 = V_{DD} - V_{log} + nV_T \cdot ln\left(\frac{I_{ph}}{I_0}\right) \quad (4)$$

where $\Delta V$ is output signal of CDS operation. $V_{DD}$ - $V_{log}$ is a preset linear range by tuning $V_{log}$ depends on environment. The rest term in (4) is logarithm related term. As shown in (4). FPN at logarithmic mode can be easily reduced by CDS operation.

### *C. Column circuit and readout scheme*

Fig. 3 shows the proposed pixel structure with column circuit. $M_{sf}$ is input device of column shared-OP enabled by $M_{sel}$ to avoid source follower's gain loss and provide a front-stage gain implemented by $1+C_1/C_2$. The column shared-OP acts like a unit gain buffer when $S_1$ is ON in exposure phase. After sampling the signal value by CDS circuit, the switch S1 turns OFF and pixel operation goes to clear and reset phase. Thus $\Delta V$ is multiplied by the gain of $1+C_1/C_2$ with column shared-OP.

### *D. Chip overview*

Fig. 4 shows the system architecture. This chip consists of pixel array, row select, read control, column shared-OP, OP bias, column-wise CDS, and column select. Row select was implemented by shift register for scanning each row of the pixel. Read control generates the control signals for pixels which are selected by row select. OP bias and column shared-OP are described in previous paragraph. Column CDS

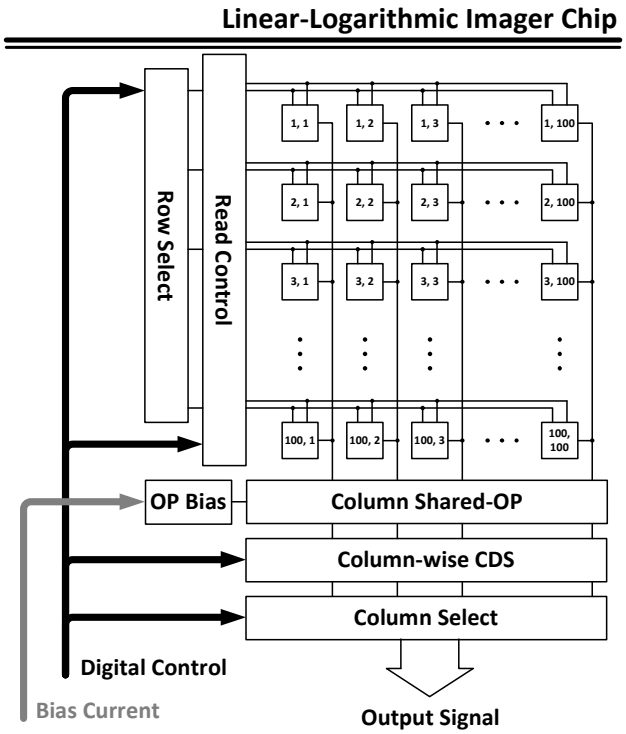


Fig. 4. System architecture of Lin-Log CMOS imager chip

achieve the subtraction for generating signal which is related to light intensity. Column select is used to mux the signal out serially to I/O pins.

## III. Measurement Results

Fig. 5 shows the chip microphotograph of the presented CMOS image sensor fabricated in 0.18um TSMC 1P6M standard process. The image array has 100 x 100 pixels with a pixel size of 6um x 6um. A column shared-OP and CDS is integrated at the bottom side of the image array. The chip size is 1.4mm x 1.4mm.

Fig. 6 shows the measured photoelectric conversion characteristics from 0.01lux to 156500lux with the tunable linear range. The blue line is measured with $V_{log}$ as 1.8v. The red line measured with $V_{log}$ as 2.5v. It shows that the linear region is tunable by varying $V_{log}$ as expected.

The measured performance of the developed CIS is summarized in Table. I. The achieved dynamic range and FPN in logarithmic region is 143dB and 1.96% respectively. Linear and logarithmic sensitivity are 651mV/lux-s and 55mV per decade of luminance. Temporal noise is 0.7462mV. And the average power consumption is 1.88mW at 50 fps.

Fig. 7 show sample images captured from prototype without any post-processing. The image (a) is captured in linear response. The tungsten filament is unrecognizable because the image around tungsten filament is saturated. The image (b) shows the doll and tungsten filament are cognoscible in Lin-Log response as expected. The measured performance comparison table of the proposed Lin-Log imager with state-of-the-art published works is summarized in Table. II.

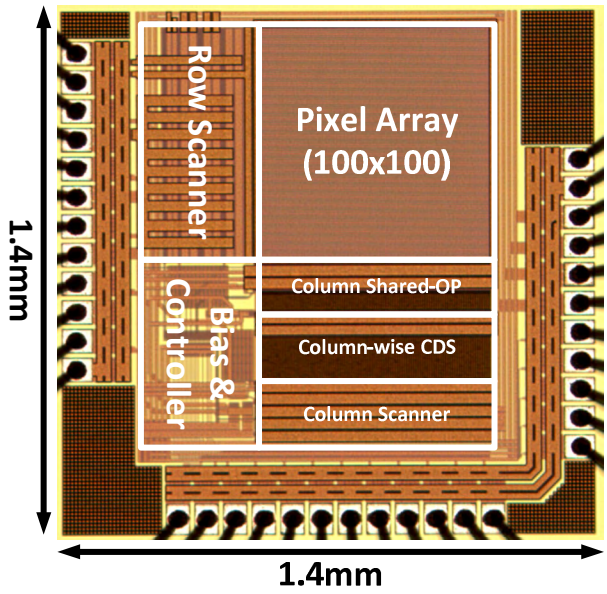


Fig. 5. Chip micrograph

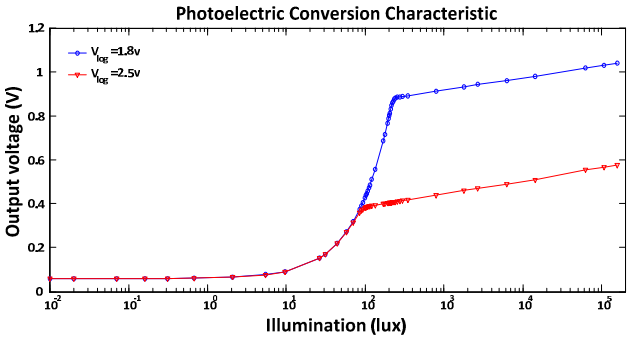


Fig. 6. Photoelectric conversion characteristic

TABLE. I
SENSOR MEASUREMENT

| | |
|---|---|
| **Technology** | **0.18um 1P6M CMOS** |
| **Power supply** | **3.3V** |
| **Array size** | **100×100** |
| **Pixel level transistors** | **5** |
| **Pixel size** | **6μm × 6μm** |
| **Fill factor** | **32.54%** |
| **Dynamic range** | **143.89dB** |
| **Linear sensitivity** | **651mV/lux.s** |
| **Logarithmic sensitivity** | **55mV/dec** |
| **Temporal noise** | **0.7462mV** |
| **FPN at linear** | **12mV** |
| **FPN at log** | **1.08mV** |
| **FPN at log [rms/(log sensitivity)]** | **1.96%** |
| **FPN at log [rms/$V_{logswing}$]** | **0.45%** |
| **Power comsuption** | **1.88mW @ 50 fps** |

TABLE. II
COMPARISON TABLE

| | [1] | [2] | [3] | [4] | [5] | This work |
|---|---|---|---|---|---|---|
| Technology | 0.8um | 0.25um | 0.18um | 0.35um | 0.5um | 0.18um |
| Array size | 160×120 | N/A | 352×288 | 640×480 | 16×16 | 100×100 |
| Pixel level transistors | 4 | 5 | 7 | 4 | 7 | 5 |
| Pixel size ($um^2$) | 30×30 | 10x10 | 5.6×5.6 | 7.5×7.5 | 23.4×27.15 | 6×6 |
| Fill factor | N/A | 43% | 33% | 37% | 24.56% | 32.54% |
| Dynamic range | >120dB | 140dB | 143dB | 124dB | 121.26dB | 143.89dB |
| High dynamic range technique | Lin-Log | Log | Lin-Log | Lin-Log | Lin-Log | Lin-Log |
| Linear-logarithmic switching | On chip fixed | N/A | Off chip | On chip fixed | On chip adjustable | On chip adjustable |
| Logarithmic sensitivity (mV/dec) | 53mV/dec | N/A | 77mV/dec | 66mV/dec | 79.98mv/dec | 55mV/dec |
| FPN at linear (mV) | N/A | N/A | N/A | N/A | 13.8mV | 12mV |
| FPN at log (mV) | 6.5mV | 32mV | 3.08mV | 5mV | 19.1mV | 1.08mV |
| FPN at log (%)[rms/(log sensitivity)] | 12.26% | N/A | 4.00% | 7.57% | 23.88% | 1.96% |
| FPN at log (%)[rms/$V_{logswing}$] | N/A | 2.46% | N/A | N/A | 8.34% | 0.45% |

## IV. CONCLUSION

This paper proposed a Lin-Log CIS with high DR. With threshold voltage cancellation and column shared-OP scheme, the imager achieves a DR and FPN in logarithmic region of 143dB and 1.96%. On-chip tunable response curve is proposed to control Lin-Log switching point properly without post-processing effort and cost. It shows the proposed design provides a promising solution of wide DR CIS chip.

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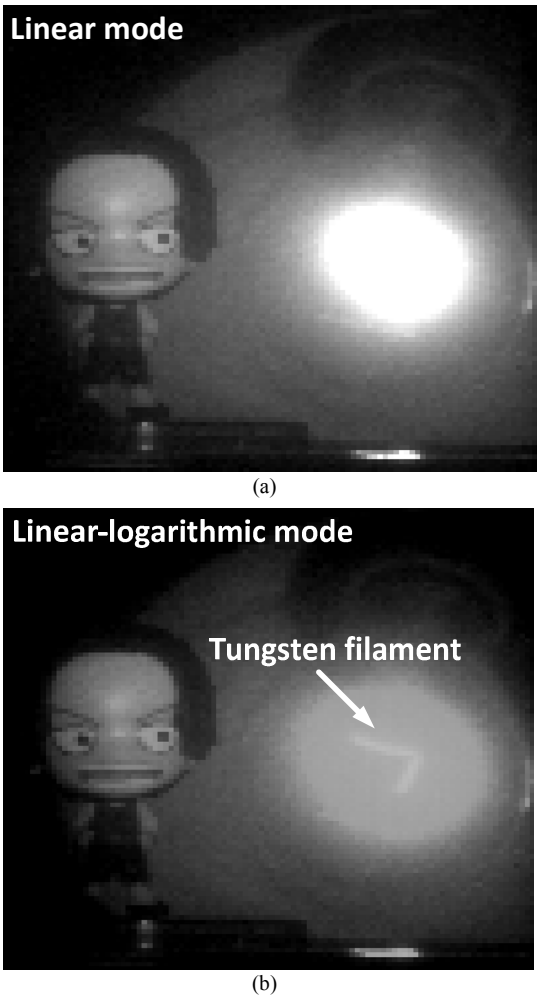


Fig. 7. Sample images (a) linear mode (b) linear-logarithmic mode