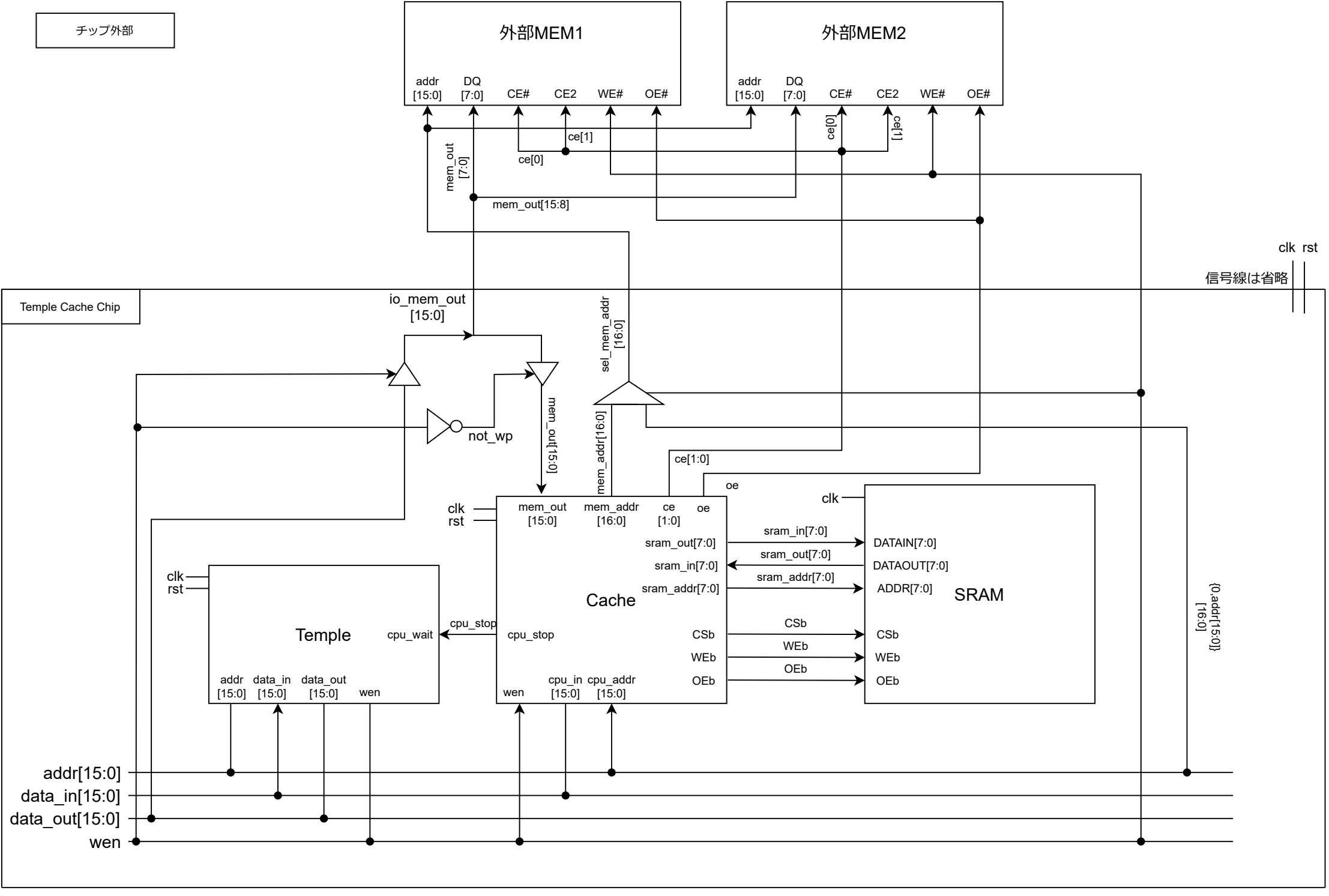
チップ外部
外部MEM1
addr [15:0]
DQ [7:0]
CE#
CE2
WE#
OE#
外部MEM2
addr [15:0]
DQ [7:0]
CE#
CE2
WE#
OE#
ce[1]
ce[0]
ce[0]
ce[1]
mem_out [7:0]
mem_out[15:8]
clk rst
信号線は省略
Temple Cache Chip
io_mem_out [15:0]
sel_mem_addr [16:0]
not_wp
mem_out[15:0]
mem_addr[16:0]
ce[1:0]
oe
clk
rst
mem_out [15:0]
mem_addr [16:0]
ce [1:0]
oe
sram_out[7:0]
sram_in[7:0]
sram_addr[7:0]
Cache
cpu_stop
cpu_stop
CSb
WEb
OEb
wen
cpu_in [15:0]
cpu_addr [15:0]
clk
DATAIN[7:0]
DATAOUT[7:0]
ADDR[7:0]
SRAM
sram_in[7:0]
sram_out[7:0]
sram_addr[7:0]
CSb
WEb
OEb
clk
rst
Temple
cpu_wait
addr [15:0]
data_in [15:0]
data_out [15:0]
wen
{0,addr[15:0]} [16:0]
addr[15:0]
data_in[15:0]
data_out[15:0]
wen