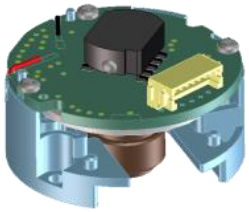
QS35-M40M-E12F

40Bits EHMT Multi-Turn Absolute Encoder with SIL3



Description and General Specification

This document provides an explanation of the ESL Safety protocol specification for the QS35 encoders.

Table 1 General Specification of the ESL Safety Serial Communication

Item	Specification	Note
Transmission Type	RS-485 Compliant Differential Transceiver	Recommended to use twisted pair shielded cable & grounding to chassis at both ends.
Communication Type	Half duplex	
Transmission Code Type	Binary, Non Return Zero (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	10 Mbps	
Frame Length	10 bits/Frame	
Transmission Error Checking	8 bits CRC (Non-Safety)	CRC Polynomial equation G(X) = $X^8 + X^{n-1}…+1$ (X = cr0 ~ cr7)
	16 bits CRC (Safety)	CRC Polynomial equation G(X) = $X^{16} + X^{n-1}…+ 1$ (X = cr0 ~ cr15)

Definition of Encoder Operating Mode

Table 2 Definition of Encoder Operating Mode

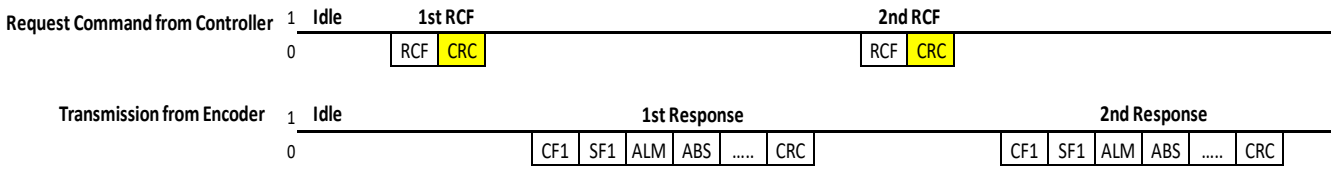
Mode	Definition	VCC (Typ)	Remarks
Power off mode	This is non-operation state of the encoder, where the main power supply, Vcc line is not connected.	0V	
Normal mode	This is normal operation state of the encoder, when main power supply Vcc is available. At this state, counting of single turn position, counting of multi-turn position and data transmission between encoder and Host are possible.	5V	

Transmission Frames between Host and Encoder

Overview of Communication

A one-to-one or one-to-many half-duplex serial communication established between the client encoder and the Host (e.g. servo driver). The communication is in a differential transmission format that complies with RS-485 electrical standard. The encoder will carry out specific operation based on the command request made by the ESL Host. Acknowledgment of the command request is necessary before the encoder executes the requested operation, i.e. by checking the Start bit, information data field, Stop bit & CRC frame. Upon failing this checking, the command request will not be acknowledged and executed

Figure 1 Typical RS-485 transmission frames format on half-duplex line



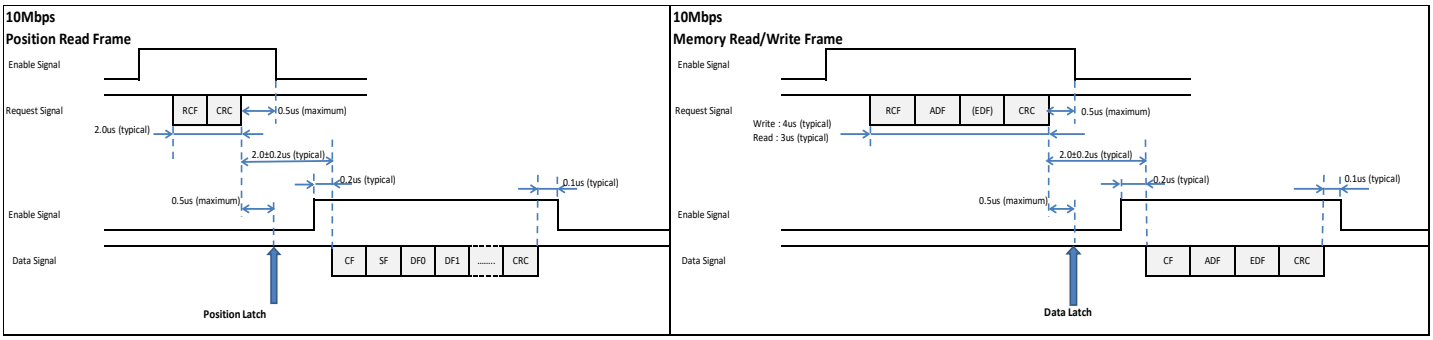
- **Start of transmission frames set:** The encoder will acknowledge as a valid Command Frame (CF) upon detecting
  - the first logic of Low state “0” on the transmission line after idling state, and
  - the following 3 bits conform to a valid encoder address, indicating the start of transmission frame set, else, it will continue to search for the next available logic of low state ”0”.

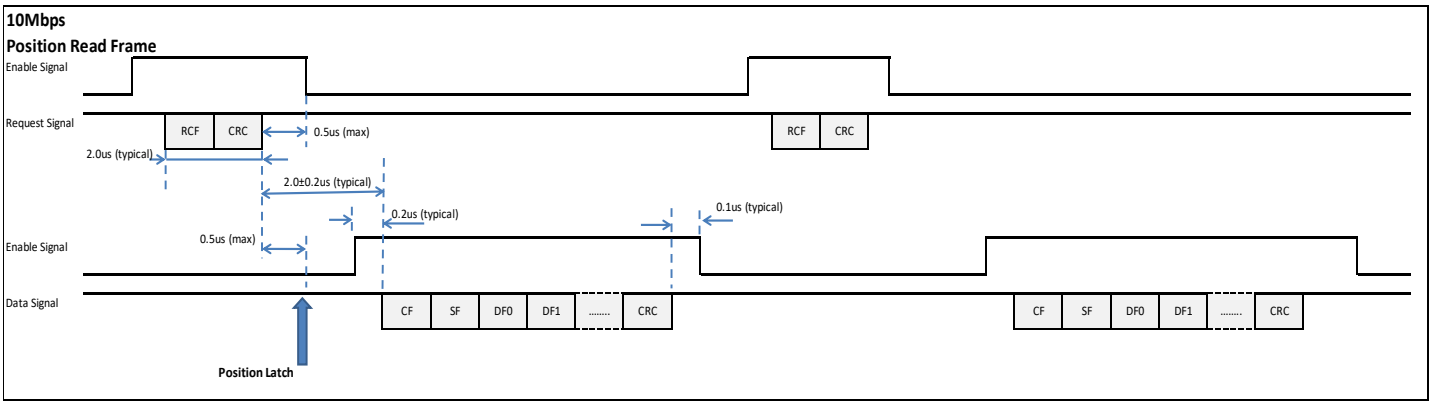
- **End of transmission frames set:** After the Command Frame detected, if there is no Start Bit after the End Bit of the last frame read, and subsequent CRC frame detected, end of transmission frame set concluded.
  - the valid 8-bit CRC value frame.

- **Idle state**: Idle state means a space between each transmission frames set and subsequent transmission frames. At idling state, logic of output in transmission line kept to high state “1”.

Encoder Data Read Out Frame Sets Format and Timing

Figure 2 Encoder Data Read Out Frame Set





Upon the Host issuing a RCF request, after 2.0 µs (typical), the encoder shall respond with Encoder Data Frames set with the following contents:

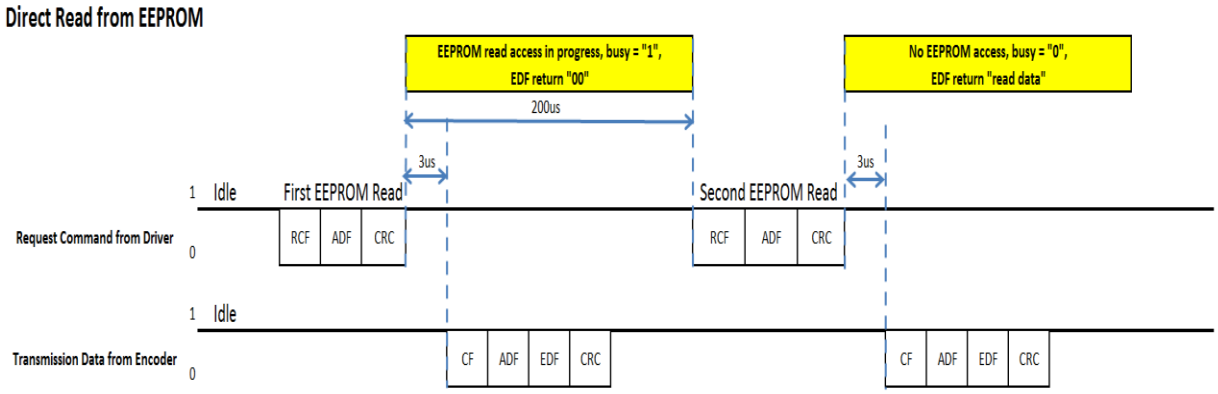
- CF: corresponds to the Command Frame issued by the Host
- SF: Status Frame
- DF0~DF7: Encoder Data Frames
- CRC: Cyclic Redundancy Check (CRC) frame

Encoder position calculation will be completed 4.3 µs (typical) after the end bit of Host request CF frame.

Notes: The encoder respond data frames set format are dependent on the requested operation by the ESL Host. Refer to Table 12.

EEPROM & Register Data Read Out Frames Set Format and Timing

Figure 3 EEPROM Data Read Out Frame Set



a) User needs consecutive transmit 2 memory read operation (same address) to read out physical EEPROM data.

   i) First memory read will direct read the physical EEPROM memory data then store into temporally register. Busy is “1” and EDF return “00”

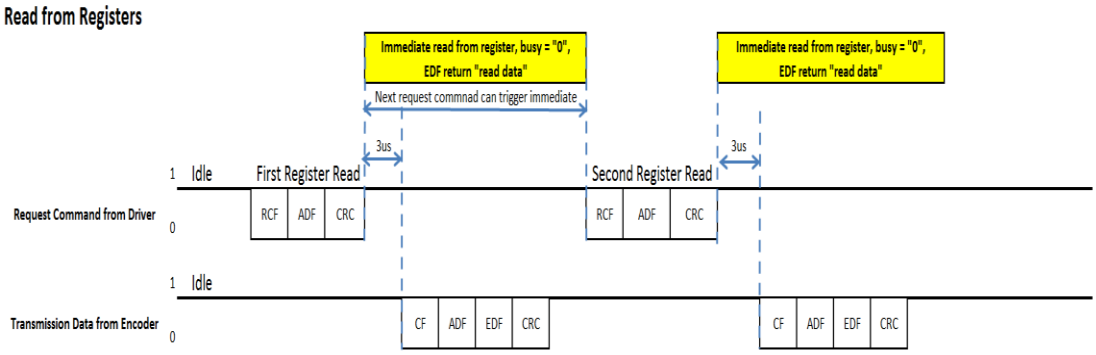
   ii) Second memory read will read from store registers. Busy is “0” and EDF return “memory data”.

b) User need to wait more than 200us between each memory read operation. The 200us is EEPROM read time.

Content of transmission frames:

- RCF: Request Control Frame (Host Command)
- CF: Control Frame (Encoder Response)
- ADF: Memory Address Data Frame indicates the EEPROM memory location to Read.
- EDF: Encoder Memory Data Frame contains the data read from EEPROM.
- CRC: Cyclic Redundancy Check (CRC)

Figure 4 Registers Data Read Out Frame Set

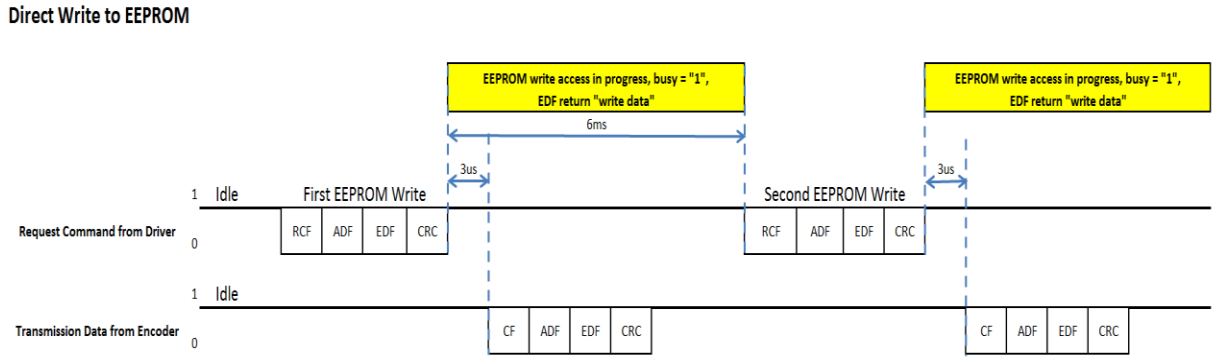


c) User only need transmit 1 memory read operation for reading registers content and can immediate trigger next read operation after register read operation.

d) As no EEPROM accessing, busy will remain low. Busy is "0" and EDF return "register data".

EEPROM & Register Data Write Frames Set Format and Timing

Figure 5 EEPROM Data Write Frame Set



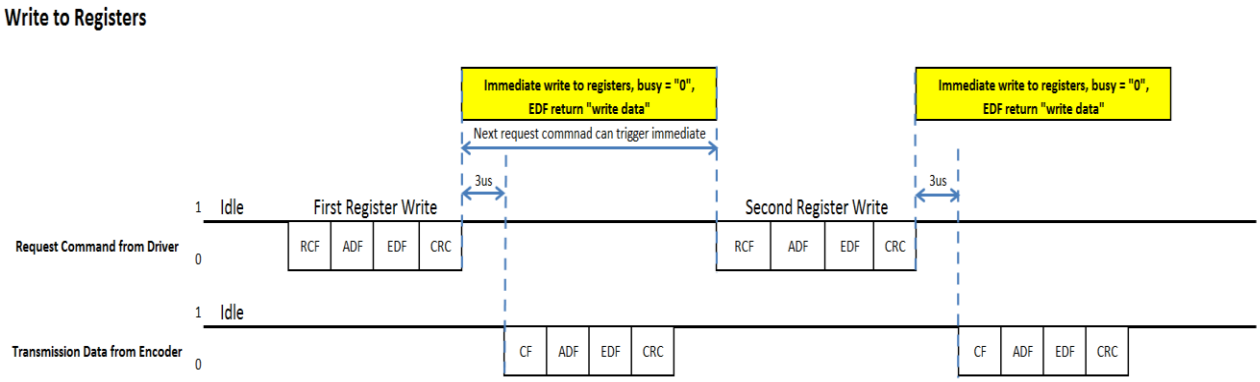
e) User need to wait more than 6ms between each memory write operation. The 6ms is EEPROM writing time and busy will return high.

f) User is recommend to perform memory read operation to confirm the physical EEPROM data has successful write in.

Content of transmission frames:

- RCF: Request Control Frame (Host Command)
- CF: Control Frame (Encoder Response)
- ADF: Memory Address Data Frame indicates the EEPROM memory location to write.
- CRC: Cyclic Redundancy Check (CRC) checking
- EDF: Encoder Memory Data Frame where the data write into EEPROM.

Figure 6 Registers Data Write Frame Set



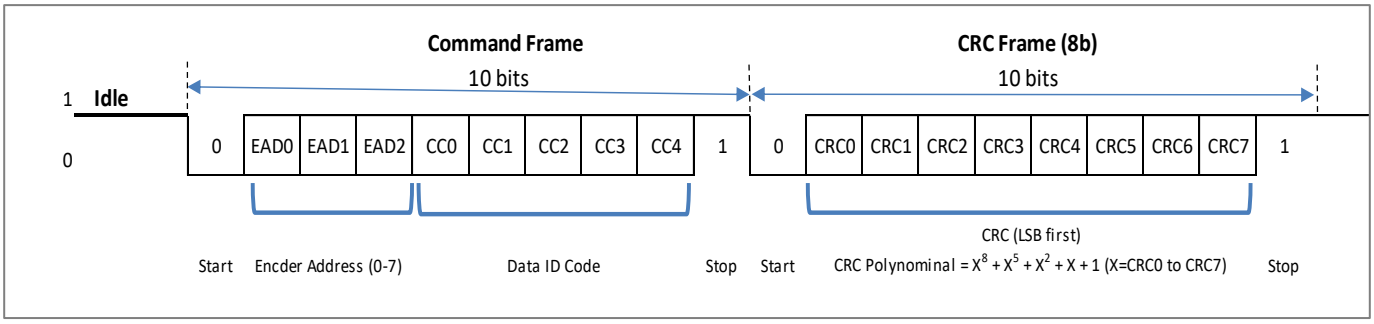
g) User can immediate trigger next write operation after register write operation. As it is not EEPROM accessing, busy bit will remain low.

h) User is recommend to perform memory read operation to confirm the register data has successful written in.

Detailed Description of Data Frames

Command Frame / Control Field (CF)

Figure 7 Command Frame / Control Field format



Content of CF frame:-

- Start Bit: Indicating the start of Frame, always “0”
- Encoder Address: Indicate encoder ID preset in factory or by user.
- Data ID: Combination of bits defining command instructions, refer to 0 and 0
- Parity Bit: Parity check bit for Command ID, refer to 0.
- End Bit: Indicating end of Frame, always “1”
- 8-bit CRC frame

Command ID and Encoder Operation Definition

Table 3 Definition of Encoder Operation Command Codes and Parity bit

	Encoder Address Code			Data ID Code				Parity	Remark
	BIT 0	BIT 1	BIT 2	CC0	CC1	CC2	CC3	CC4	
Data ID 1	EAD0	EAD1	EAD2	1	0	0	0	<odd>	Position Read command (Safety)
Data ID 2	EAD0	EAD1	EAD2	0	1	0	0	<odd>	
Data ID 4	EAD0	EAD1	EAD2	0	0	1	0	<odd>	Position Read command (Non Safety)
Data ID 5	EAD0	EAD1	EAD2	1	0	1	0	<odd>	
Data ID 8	EAD0	EAD1	EAD2	0	0	0	1	<odd>	Retrieve En_ID command
Data ID 9	EAD0	EAD1	EAD2	1	0	0	1	<odd>	Temperature Read command
Data ID A	EAD0	EAD1	EAD2	0	1	0	1	<odd>	Alarm Read command
Data ID B	EAD0	EAD1	EAD2	1	1	0	1	<odd>	Perform continuous 8times for ST clear command
Data ID C	EAD0	EAD1	EAD2	0	0	1	1	<odd>	Perform continuous 8times for alarm clear command
Data ID D	EAD0	EAD1	EAD2	1	0	1	1	<odd>	Perform continuous 8times for MT clear command
Data ID E	EAD0	EAD1	EAD2	0	1	1	1	<odd>	Memory or Register Read command
Data ID F	EAD0	EAD1	EAD2	1	1	1	1	<odd>	Memory or Register Write command

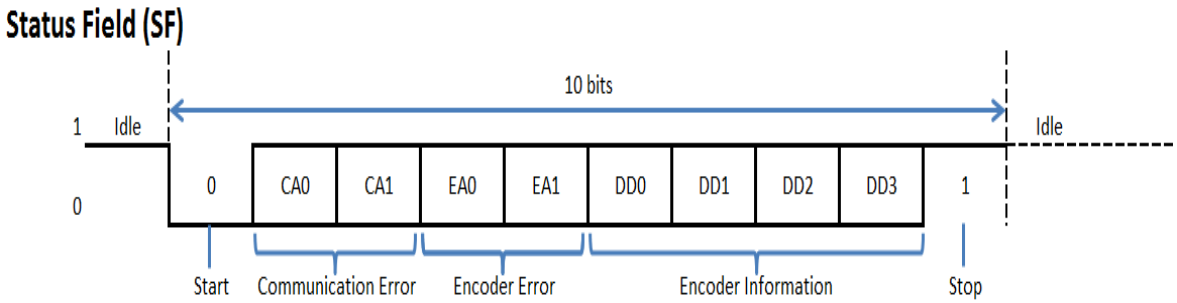
Description of Encoder Operation

Table 4 Description of encoder operation

Operation	Command ID	Description of Operation
Encoder Position Read (Safety)	1, 2	Position read out with safety related field.
Encoder Position Read (Non Safety)	4,5	Position read out with without safety related field.
Encoder ID	8	Encoder ID, auto generated by encoder & depends on safety, MT & ST settings.
Temperature Read	9	Temperature read out.
Alarm Read	A	Alarm read out.
Single-Turn Counter Reset	B	Transmit request minimum 8 times consecutively at a typical interval of 40µs to encoder, with motor shaft in stationary condition.
		Single turn Zero position can be set to any desired position.
		Upon successful completion of Zero Reset, the Zero position will be saved into encoder memory.
Clear All Error	C	Transmit request minimum 8 times consecutively at typical interval of 40µs to encoder, where the motor shaft is in a stationary condition.
		All latched errors as described in 0 will be cleared at the same time.
Multi-Turn Counter Reset	D	Transmit request minimum 8 times consecutively at typical interval of 40µs to the encoder, with motor shaft in stationary condition.
		Multi-turn counter will be cleared.
EEPROM Read	E	8 bits of data to be read from designated EEPROM address of User accessible memory area. Refer to Appendix A for recommended EERPOM read out process flow.
EEPROM Write	F	8 bits of data to be written into designated EEPROM address of User accessible area. Refer to Appendix B for recommended EERPOM writing process flow and Data content confirmation.

Status Response Frame (SRF)

Figure 8 SF frame format



Content of SF frame:-

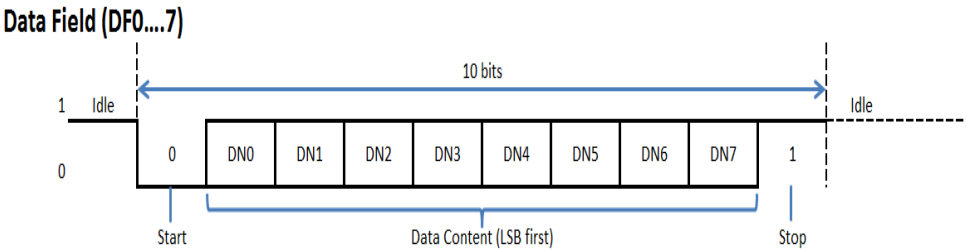
- Start Bit: Indicating the start of Frame, always “0”
- Communication Error Bits (CA): Return with state “1” if communication error detected, please refer to 0.
- Encoder Error Bits (EA): Return with state “1” if encoder error is detected, referring to 0
- Information Data (DD): Please refer to Table 5.
- End bit: Indicating the end of Frame, always “1”

Table 5 Encoder Error and Communication Error Descriptions

Status Field (SF)		
CA0	"0"	No Error
	"1"	Wrong Parity Bit in Request Control Frame
CA1	"0"	No Error
	"1"	Wrong Stop Bit in Request Control Frame
EA0	"0"	No Error
	"1"	Safety Error (ST/MEM/OV/UV/LED)
EA1	"0"	No Error
	"1"	Non Safety Error (MT/XC/LIS/OVSP)
DD0	"0"	No Warning
	"1"	Encoder Temperature Warning
DD1	"0"	CH1
	"1"	CH2
DD2	"0"	No Error
	"1"	Encoder Ready Status (ST-only or ST+MT)
DD3	"0"	No Forced Test
	"1"	Forced Test Passed

Encoder Data Frame (DF_n)

Figure 9 DF_n Frame Format



Content of DF_n frame:-

- Start Bit: Indicating the start of Frame, always “0”
- DN^0~DN^7: 8 bits data set with LSB first in sequence.
- End Bit: Indicating end of Frame, always “1”

Description of Data Frames with Respective Command ID

Table 6 Data frames content with respective Command ID

	DF0	DF1	DF2	DF3	DF4	DF5	DF6
Data ID 1	**ALM1**	**ABS0**	**ABS1**	**ABS2**	**ABM0**	**ABM1**	**SC1**
Data ID 2	**ALM1**	**ABS0**	**ABS1**	**ABS2**			**SC1**
Data ID 4	ABS0	ABS1	ABS2	ABM0	ABM1		
Data ID 5	ABS0	ABS1	ABS2				
Data ID 6	ABS0	ABS1	ABS2				
Data ID 8	ENID						SC1
Data ID 9	TEMP						
Data ID A	ALM1						
Data ID B	ALM1	ABS0	ABS1	ABS2			SC1
Data ID C	ALM1	ABS0	ABS1	ABS2			
Data ID D	**ALM1**	**ABM0**	**ABM1**				
Data ID E	EDF						
Data ID F	EDF						

Note: Rows highlighted in yellow are Functional Safety related format.

ABS(n): Absolute Single Turn counts, LSB of the Single Turn counts is located in ABS0 and MSB of the counts data is located in ABS2. Combining ABS0~ABS2 will provide a total to 24 bits of Absolute Single Turn data.

ABM(n): Multi Turn counts, LSB of the multi-turn counts is located in ABM0 and MSB of the counts data is located in ABM2. Combining ABM0~ABM1 will provide a total to 16 bits of multi-turn data. For 16 bits multi-turn counting, ABM2 are fixed to “00”.

ENID: Encoder Single Turn bits identification. Follow ST resolution and able to configure in EEPROM. {1'b<safety>, 2'b<MT-#-byte>, 5'b<ST-#-bit>}, ST={1, 00, 11000} , MT={1, 10, 11000}

EDF: Memory data frame

SC1/2: CH1/2 Sequence Counter (8b)

ALM1: Encoder Error Flags. Refer to 0
RS0 to RS1: 9bits of ST data. RS0 & RS1 combined for 9bit of ST2.

Table 7 Error Flag Bits Definition

Bit Value	DF7-0	DF7-1	DF7-2	DF7-3	DF7-4	DF7-5	DF7-6	DF7-7
0	No Error	No Error	No Error	No Error	No Error	No Error	No Error	No Error
1	XC Error	MT Error	LED or LIS Error	Overspeed Error	Mem Error	ST Error	UV Error	OV Error

Table 8 Encoder Alarms Description

Error Flags	Detection Mode	Description	Reset Method
XC Error	EHMT mode	Indicating MT Miss Count by comparing MT Counter vs. SW Counter. (Miss count means delta >1) 1: Consecutive 5x miss count. 0: No consecutive 5x EHMT miss count.	Perform all error clear
MT Error	EHMT mode	Check on the integrity of multi turn position data counting. The error flag latched. 1: Error detected in multi turn position counting 0: No Error detected	Perform MT counter reset and all error clear
LED or LIS Error	Normal mode	To indicate if LED current is out of operating range. 1: LED out of operating range. 0: LED within operating range. or To check integrity of ADC Sin and Cos signals by means of LIS (Lissajous) specifications. 1: Lissajous out of specification. 0: Lissajous within specification. In order to determine whether LED or Lis error triggered, please read via ESL interface Page 8, address 0x1A. Bit3 = Lis Err & Bit1 = LED Err.	Power cycle encoder
Overspeed Error	Normal mode	To check if an Overspeed condition has occured. 1: Encoder rotation speed >10k rpm 0: Encoder rotation speed <10k rpm	Power cycle encoder
Mem Error	Normal Mode	Verify if loading of internal and external EEPROM content upon encoder power up is successful. 1: Failure in loading internal encoder memory with external EEPROM memory data. 0: Loading of internal encoder memory with external EEPROM memory data successful.	Power cycle encoder
ST Error	Normal mode	Checking on the integrity of single-turn position data computation. 1: Error detected in single-turn position counting. 0: No Error detected.	Power cycle encoder
UV Error	Normal mode	Checking if Under Voltage condition occurred. 1: Supply voltage is lower than 2.9 ±0.1V 0: Supply voltage is higher than 2.9 ±0.1V	Error flag automatically cleared once voltage return to normal
OV Error	Normal mode	Checking if Over Voltage condition occurred. 1: Supply voltage is higher than 3.7 ±0.1V 0: Supply voltage is lower than 3.7 ±0.1V	Error flag automatically cleared once voltage return to normal

Cyclic Redundancy Check Frame (CRC)

Figure 10 16 Bit CRC Frame Format

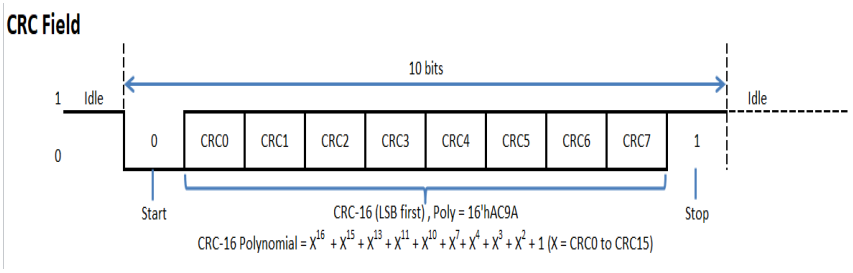
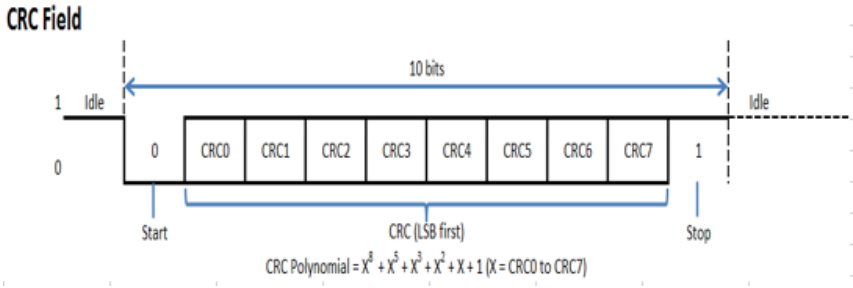


Figure 11 8 Bit CRC Frame Format



Content of CRC frame:-

- Start Bit: Indicating the start of frame, always “0”
- $cr^{0\sim cr15}$: 16 bits of CRC data set with LSB first in the sequence.
- $cr^{0\sim cr7}$: 8 bits of CRC data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always “1”

Note: The CRC calculation is as shown below:

16 Bit

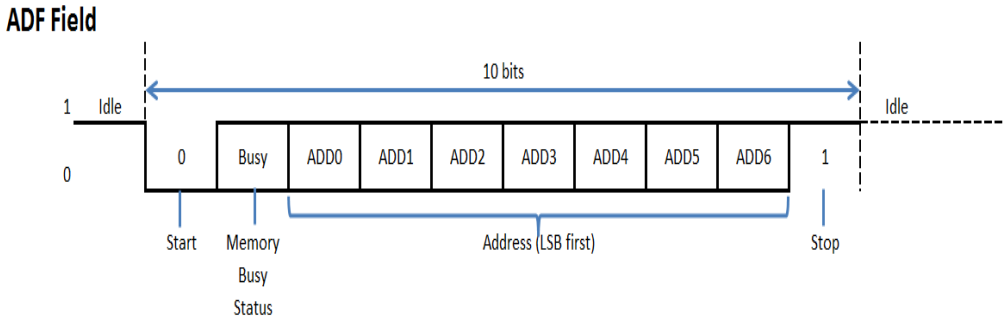
- Full CRC (16b) = {CRCx.2, CRCx.1}
- CRC-16 Polynomial = X16 + X14 + X12 + X11 + X8 + X5+ X4 + X2 + 1 (X = CRC0 to CRC15, Poly = 16'hAC9A)
- CH1 CRC initial value = 16'h0000 ; CH2 CRC initial value = 16'hFFFF
- CRC Field is transmitted from LSB first
- The code calculated from all bits without Start and Stop bit of all fields except CRC field.
- If # of field is odd number, the last 8-bit will be padded with 0's

8 Bit

- Full CRC (8b) = {CRCx}
- CRC-16 Polynomial = X8 + X5 + X3 + X2 + X + 1 (X = CRC0 to CRC7, Poly = 8’h97)
- CH1 CRC initial value; CH2 CRC initial value = 8'h00; CH2 CRC initial value = 8'h00
- CRC Field is transmitted from LSB first
- The code calculated from all bits without Start and Stop bit of all fields except CRC field.

Address Frame (ADF)

Figure 12 Address Data Frame Format (ADF)



Content of MAF frame:

- Start Bit: Indicating the start of frame, always “0”
- Busy: Memory Access busy status flag, refer to Table 9
- Add^0~Add^6: 7 bits Memory Address data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always “1”

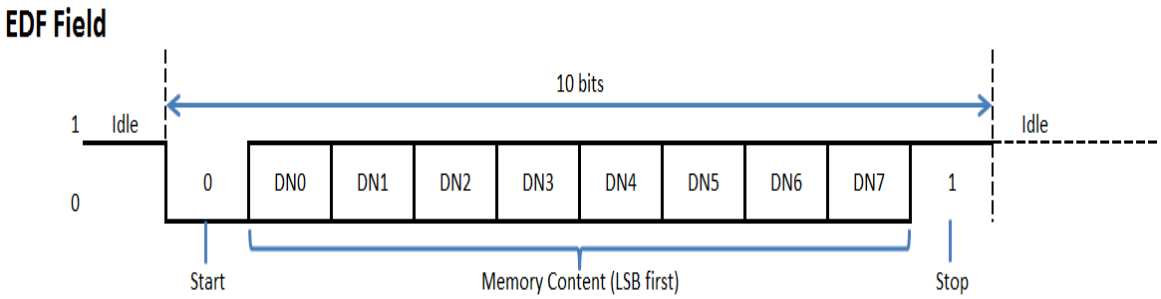
Table 9 Busy Status Definition

Busy Status become "1" during Memory access

Address	Definition
00h ~ 7Eh	Memory Data
7Fh	Page Selection. Default Page after power on is Page 8

EEPROM Data Frame (EDF)

Figure 13 EEPROM Data Frame Format (EDF)



Content of EDF frame:

- Start Bit : Indicating the start of frame, always “0”
- DN0~DN7: 8 bits EEPROM Memory data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always “1”

Table 10 Relationship between Request Command, Busy Status & Transmission Data

Relationship between Request Command, Busy Status and Transmission Data					
Request Command from Driver		Transmission Data from Encoder			Description
RCF	Busy	Busy	ADF	EDF	
Data ID E (Read)	0	0	ADF from Driver Request	Valid Memory Data	Reading is valid.
		1	ADF from Driver Request	“00”	Reading is invalid.
Data ID F (Write)	0	0	ADF from Driver Request	EDF from Driver Request	Writing is valid.
		1	ADF from Driver Request	“00”	Writing is invalid.

Register, Memory & EEPROM User Accessible Memory Area

Table 11 User Accessible Memory & Register Area

ESL Page	Start ESL Address	End ESL Address	#byte	Level	Description	Type
0	0x00	0x7E	512	N/A	User area (4kB)	EEPROM
4	0x00	0x7E	128	Level 1	IEC table	
5	0x00	0x7E	128	Level 1	OAC table	
6	0x00	0x03	4	Level 1	Remaining IEC, OAC & CH2 delta (for ST offset)	
	0x04	0x07	4	Level 1	IEC/OAC LRC	
	0x08	0x0B	4	Level 1	Temperature Offset (with invert)	
8	0x00	0x1F	32	N/A	CH1 Frame, FT Commands	Register
	0x1A	N/A	1	N/A	Encoder Error Info	
	0x20	0x2F	16	N/A	CH2 Frame info, FT command	
14	0x00	0x0F	16	Level 1/2	MTP 1	ASIC Memory (MTP)
	0x10	0x1F	16	Level 1/2	MTP 2	
14	0x20	0x2F	16	Level 1/2	Internal Register for Cal & Test	Register
	0x30	0x3F	16	Level 1/2	Internal Register for Lock Bit & Miscellaneous	

NOTE

1. All User accessible addresses are pre-programed with “00” prior to shipment.
2. The active page numbers are specified in address 7Fh, bank change is done by writing to address 7Fh.
3. Once the page value is changed, allow a 18ms delay.
4. Typical EEPROM Read time is 200µs minimum.
5. Typical EEPROM Write time is 6ms minimum.
6. Permissible MTP writing cycle is 100,000 times.
7. Permissible EEPROM writing cycle is 1,000,000 times.

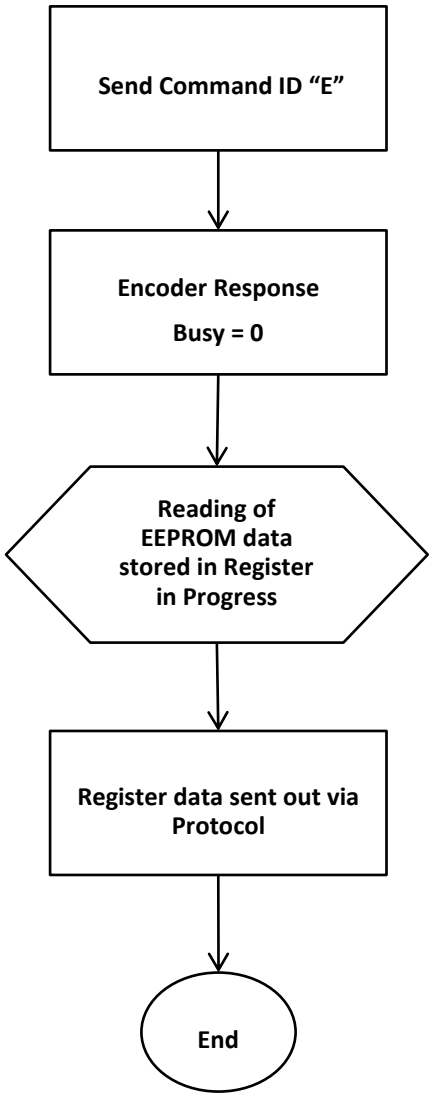
Internal temperature readout

Read internal temperature via ESL command ID.

	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	CRC1.1	CRC1.2
Data ID 9	CF1	SF1	TEMP							CRC1	

- Send command ID 0x09 to read actual temperature in ºC.
- 8 bits temperature data

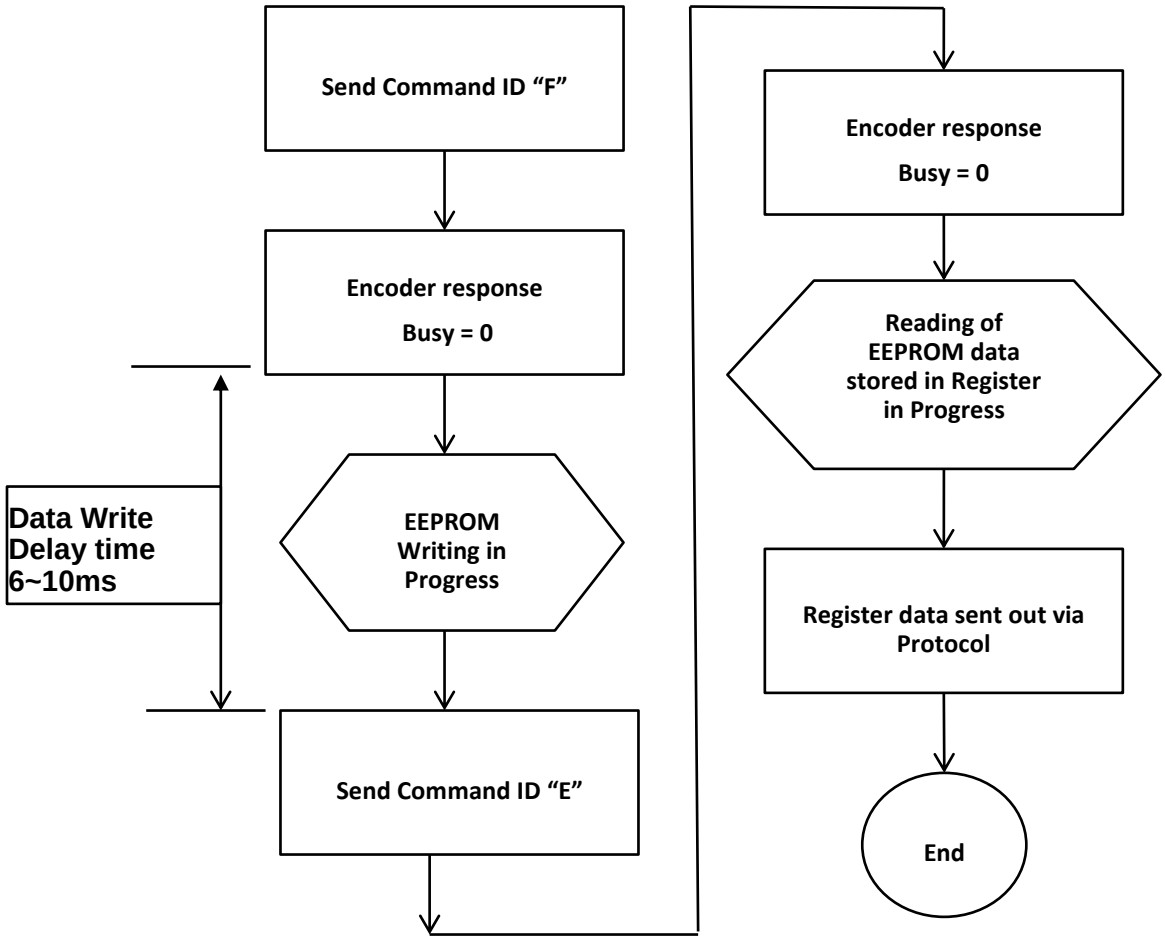
Figure 14 EEPROM Read Flow



NOTE

1. Each EEPROM reading requires sending a Command ID "E" from the ESL Host.
2. A Command ID "E" from ESL Host when initiate reading data from Register, Busy flag will return value "0".

Figure 15 EEPROM Write & Read Flow



NOTE

1. Each time when issuing of Command ID F request, the EDF content writing may not be confirmed even though the Busy flag returns a value of "0".
2. It is recommended to issue a Command ID "E" request 6~10ms after the issuance of EEPROM write request to read the designate EDF data for confirmation if the correct data has been successfully written.
3. The EEPROM read & write command is not for use in broadcast mode, only in 1 to 1 mode.

Table 12 Overview of ESL Protocol Format

	CF	SF	DF0	DF1	DF2	DF3	DF4	DF5	DF6	CRC1.1	CRC1.2	CF2	SF2	RF1	RF2	RF3	CRC2	CRC2	Remark	Frame Size	Safety Related?
Data ID 1	**CF1**	**SF1**	**ALM1**	**ABS0**	**ABS1**	**ABS2**	**ABM0**	**ABM1**	**SC1**	**{CRC1.1, CRC1.2}**		**CF2**	**SF2**	**ALM2**	**RS0**	**RS1, SC2**	**{CRC2.2, CRC2.1}**		**Position Read Command (Safety)**	**11+7**	**Yes**
Data ID 2	**CF1**	**SF1**	**ALM1**	**ABS0**	**ABS1**	**ABS2**			**SC1**	**{CRC1.1, CRC1.2}**		**CF2**	**SF2**	**ALM2**	**RS0**	**RS1, SC2**	**{CRC2.2, CRC2.1}**			**9+7**	**Yes**
Data ID 4	CF1	SF1	ABS0	ABS1	ABS2	ABM0	ABM1			CRC1									Position Read Command (Non-Safety)	8	No
Data ID 5	CF1	SF1	ABS0	ABS1	ABS2					CRC1										6	No
Data ID 6	CF1	SF1	ABS0	ABS1	ABS2					CRC1		CF2	SF2	RS0, RS1 (extend)			CRC2		Position Read Command (for calibration) **	6+5	No
Data ID 8	CF1	SF1	ENID						SC1	{CRC1.1, CRC1.2}		CF2	SF2	ENID		0,SC2	{CRC2.2, CRC2.1}		Perform continous 8times for Dynamic Addressing	6+6	Yes
Data ID 9	CF1	SF1	TEMP							CRC1									Temperature Read Command	4	No
Data ID A	CF1	SF1	ALM1							CRC1		CF2	SF2	ALM2			CRC2		Alarm Read Command	4+4	No
Data ID B	CF1	SF1	ALM1	ABS0	ABS1	ABS2			SC1	{CRC1.1, CRC1.2}		CF2	SF2	ALM2	RS0	RS1, SC2	{CRC2.2, CRC2.1}		**Perform continous 8times for ST clear command**	9+7	Yes
Data ID C	CF1	SF1	ALM1	ABS0	ABS1	ABS2				CRC1		CF2	SF2	ALM2	RS0	RS1	CRC2		Perform continous 8times for alarm clear command	7+6	No
Data ID D	**CF1**	**SF1**	**ALM1**	**ABM0**	**ABM1**					**CRC1**									**Perform continous 8times for MT clear command**	**6**	**No**
Data ID E	CF1	ADF	EDF							CRC1									Memory or Register Read Command (Non-Safety Related)	4	No
Data ID F	CF1	ADF	EDF							CRC1									Memory or Register Write Command (Non-Safety Related)	4	No

* For Position Read Command's Data Field, add Ch1 Sequence Counter (SC1) before CRC

* For Position Read Command, add Redundant (Safety) Fields : Redundant Single-Turn Position (RS0,1), Ch2 Sequence Counter (SC2) & CRC2 (for CH2)

RS0 to RS1: 9bits of ST data. RS0 & RS1 combined for 9bit resolution of ST2. RS0 MSB [Bit8:1] & RS1 is LSB [Bit0].

* For QS35 Memory Access, non-SR memory refer to Page 8 (0x00-7F); the rest are categorize as SR memory.

Encoder Connection Topology

Figure 16 Daisy Chain (Bus Topology)

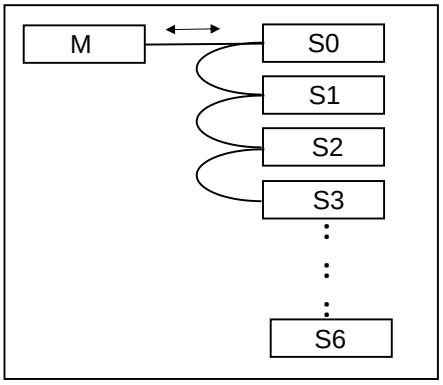
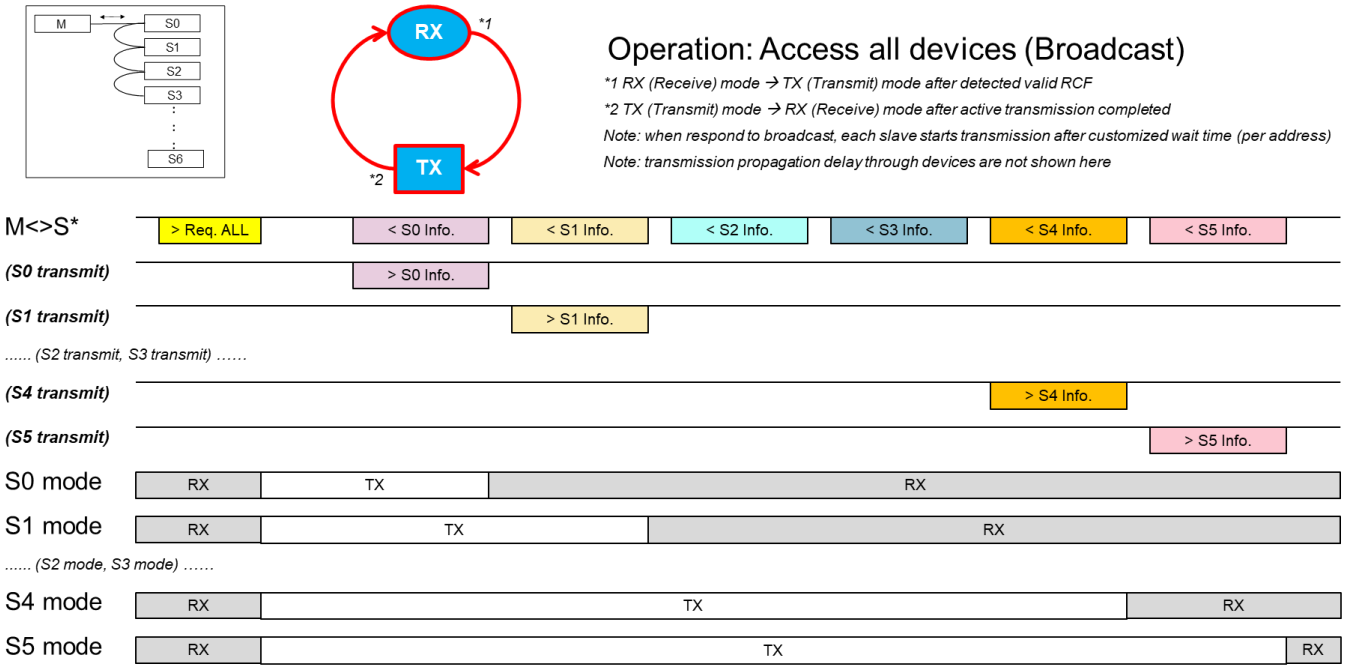
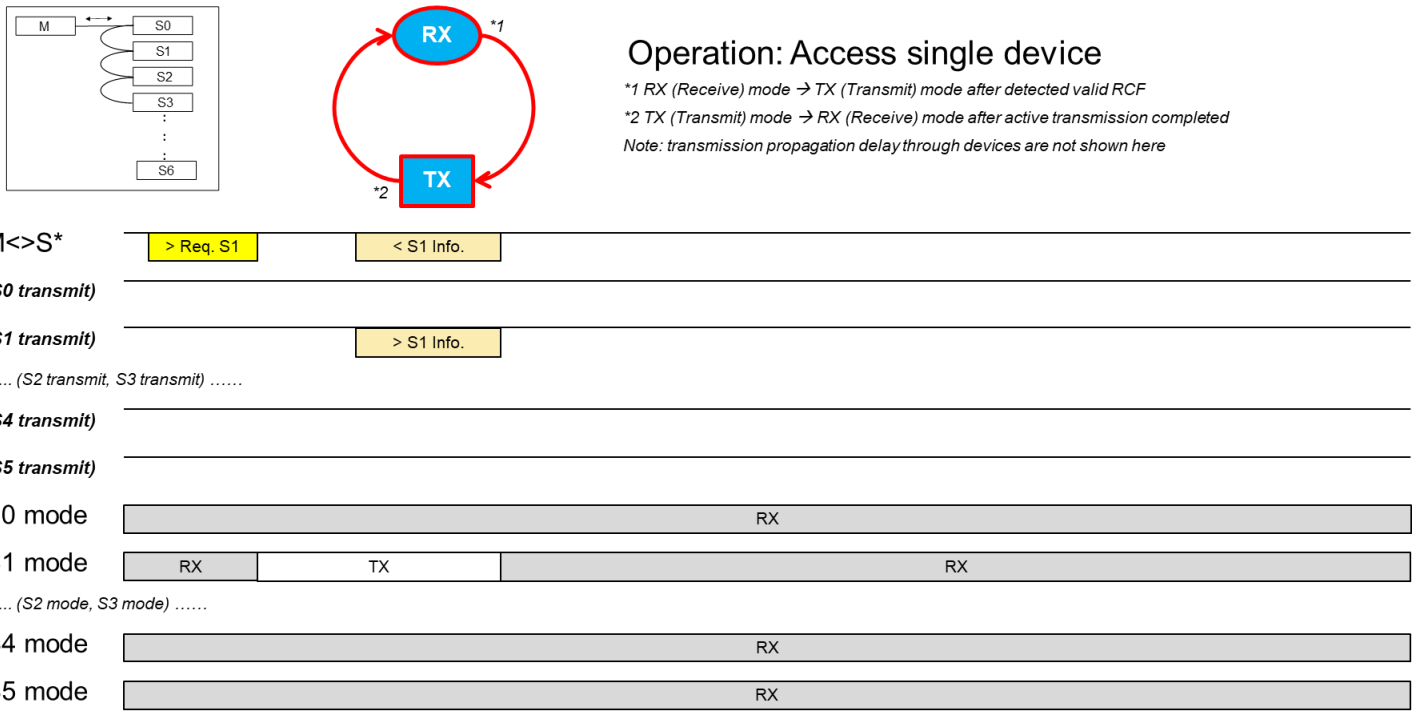


Figure 17 Daisy Chain Connection (Bus) – Access all devices



Note: Memory read and write Not applicable for Broadcast mode

Figure 18 Daisy Chain Connection (BUS) – Single device access



NOTE: Memory read and write only applicable for single device point to point connection

ESL Connection & Termination (Transmit and Receive)

Figure 19 Point to Point connection

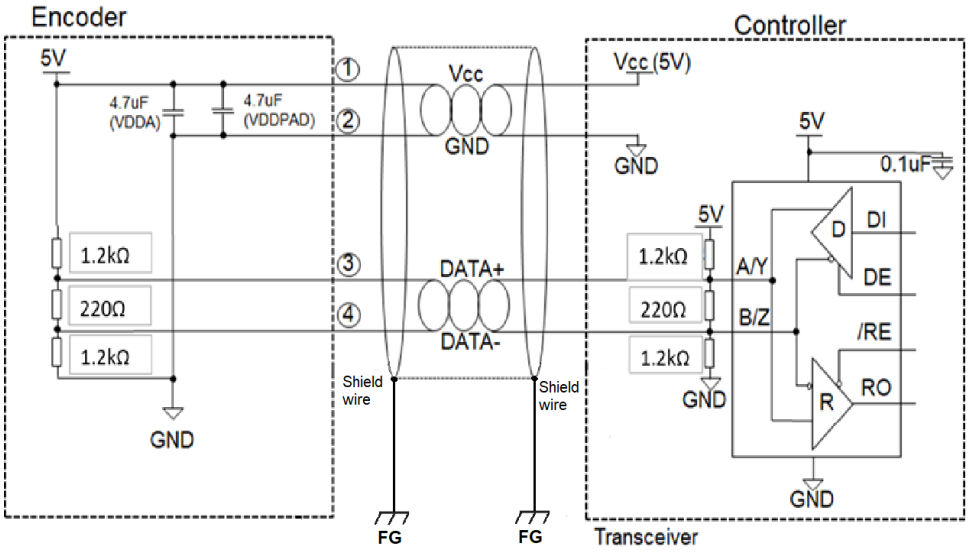
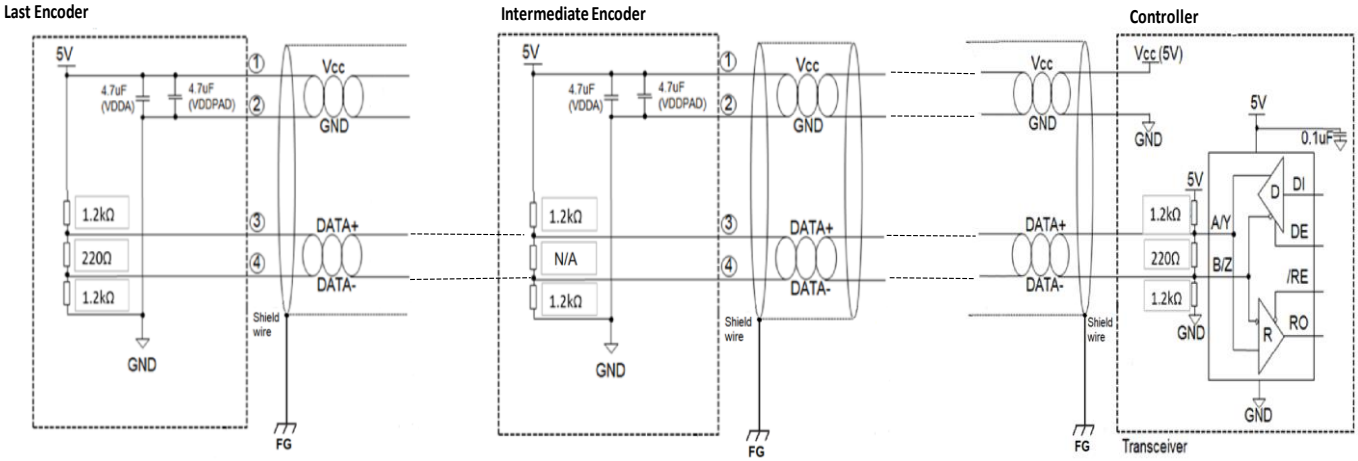


Figure 20 Bus Topology Connection



Change Control

Rev	Date	Changes	By
1.0	17 Dec 2021	Initial release	Andrew Kuan
1.1	27 Dec 2021	Pg10: Table 6 Notes- removed ABM2 Pg18: Table 12: Add RS0 & RS1 description under notes below table Pg21: Figure 20 update with the correct pull up & pull down resistor values for intermediate encoders	Lim Chiang Hee
1.2	28 Dec 2021	Pg12 8bit CRC Poly update to value 8'h97	Lim Chiang Hee
1.3	25 Jan 2022	Pg21: Figure 19 and 20 update with new pull up, pull down and termination resistor Pg15: Add Internal temperature read out	Andrew Kuan
1.4	27 Apr 2022	Pg7: Command ID D add ST position clear description Pg8: Command ID D add ST position clear description Pg18: Table 12, update Command ID D description to add ST position reset	Lim Chiang Hee
1.5	11 Oct 2022	Whole document - change the word "master" to "host" Pg1: Table 1 Insert the sentence under Note column "Recommended to use twisted pair shielded cable & grounding to chassis at both ends." Pg2: Figure 1 Typical RS-485 transmission frames format on half-duplex line. Add CRC frame requirement to Command Frame Pg3: Figure 2 Encoder Data Read Out Frame Set Pg6: Command Frame/Control Field (CF) add in CRC frame requirement Pg8: Table 4 Description of encoder operation Pg10: Table 6 Data frames content with respective command ID Pg12: Table 7 Error Flag Bits Definition Pg12: Table 8 Encoder Alarms Description Pg16: Table 11 User Accessible Memory & Register Area Pg19: Table 12 Overview of ESL Protocol Format Pg22: Figure 19 Point to Point connection & Figure 20 Bus Topology Connection	Lim CH & Tan HA