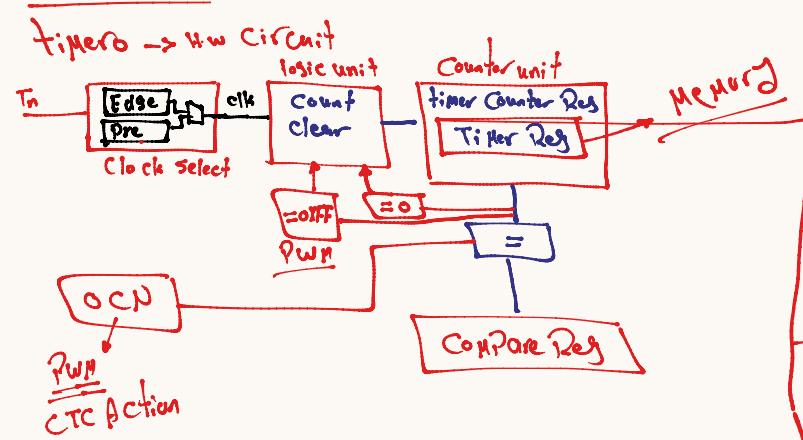


timers

- ↳ single compare unit
- ↳ CTC - Mode
- ↳ Support PWM
- ↳ Count outside → ① Clock
② event
- ↳ overflow interrupt →
 - ↳ OVF → TOV → Interrupt Enable
- ↳ Compare Match Interrupt →
 - ↳ OCFO → Interrupt Enable



* Timer0 Register

↳ ① TCCR0

* Bit 7: Force output compare

↳ in CTC mode

↳ simulate the output on
ff. width → OC0
↳ set
clear
toggle

↳ Debugging mode

* Bit 6, 3 → Select the timer mode

- normal = 0 0 0 0
- CTC = 1 0
- PWM
 - ↳ Fast = 1 1
 - ↳ Phase = 0 1

* Bit 5:4 in TCCR0

* Select the action on How Pin

↳ CTC → Non PWM

5	4
0	0
0	1
1	0
1	1

0 → Disable
0 → Toggle
1 → Clear
1 → Set

↳ PWM

↳ Fast

(NON Inver) 5 4
0 → Low Compare, High over
Compare = D.C $\times 2^n$

(Inver)

1 1 → High Compare
Low over Pl
Compare = $2^n (1 - D.c)$

* Bit 2,1,0 Select the Internal / External Clock & Prescaler

2	1	0	
0	0	0	→ No Clk (Disable timer)
0	0	1	→ Prescaler = 1
0	1	0	→ " = 8
0	1	1	→ " = 64
1	0	0	→ " = 256
1	0	1	→ " = 1024
1	1	0	→ External Clock Pin To Falling
1	1	1	→ External Clock Pin To rising

[2] TCNT0 → The time / Counter Register

[3] OCR0 → The Output Compare Register



④ TIMSK [Set for timer]

$\text{Bit 1} \rightarrow \text{OCIE0}$
 ↳ Enable Interrupt for Compare Match

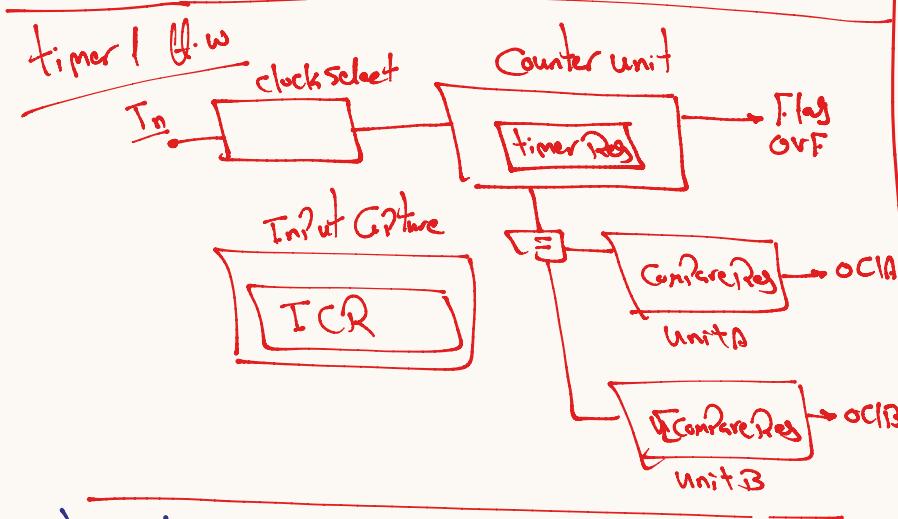
$\text{Bit 1} \rightarrow \text{TOIE0}$
 ↳ Enable Interrupt for overflow

timer 1 → 16-bit size
 → 2 Compare Unit
 ↳ Compare unit A → 16-bit
 ↳ Compare unit B → 16-bit

→ ICR, → CTC
 → PWM
 Fixed  Max Compare

→ External CLK / Event

→ 4 Interrupt
 ↳ overflow interrupt
 ↳ Compare Match unit A interrupt
 ↳ " " " + B interrupt
 ↳ Input Capture unit interrupt



① timer 1

↳ datasheet

- ↳ ① Modes
- ↳ ② PWM options
- ↳ ③ Register

Motor
 Servo
 DC-Motor

⑤ TIFR → [PIF for timer]
 $\text{Bit 1} \rightarrow \text{out compare match flag}$
 (OCFO)
 $\text{Bit 0} \rightarrow \text{overflow flag}$
 (TOVO)

