Eternal Interruit (Specific) Atmega32 Lain Atmega have 3 5 Perated Lo Cirmit -> Flag set when Pin low level -> [lag set when 1 Which even & Pire Plag Pin Hish (2) Which Ist WIM Sens -> Flet 5ct Whe 3 Action Pin visig MCMCiz OXL - Scleet sens Control - EXIII سما An-1 chens Felling Visi-g

Bit 1, 0 -> select sens Control
For EXIIO

MC4 CSR -> 5 La Rit 6 La seus Gutrol Per EXII2. La coma Palling GICX Biti- Intl - SIE For Wolls to the company of the contraction of the cont 13: tb > Into > SIE For FXIIO

FXIIO LBit5-INT2-SIEPON ExtI2

Lo > potallow

Lo 1 > allow GIPR -> Seneral Intermot Play Reg Ly Bit 7 - PeriDherd Internot Plag Lo Bit 6 Int F20 3:15 Int Fo

→ SIE → Into, Int, Int → PIF → Intro, Intro → GIE → Common between all Internet Derigher

> SREA

La void on GTE_Enable (): La void on GTE_Disable (); La structre -> EXTI -> Driver

Pin → Su?Port INto → PD3

INt1 → PD3

INt2 → PB2