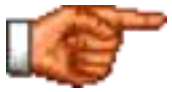
数字逻辑设计

Digital Logic Design

张春慨
School of Computer Science
ckzhang@hit.edu.cn

Unit 5 Multi-Level Gate Circuits NAND and NOR Gates



- 多级门电路（**Multi-Level Circuits**）
- **两级门电路的设计**
- **多输出电路的设计**
- **Some Examples**

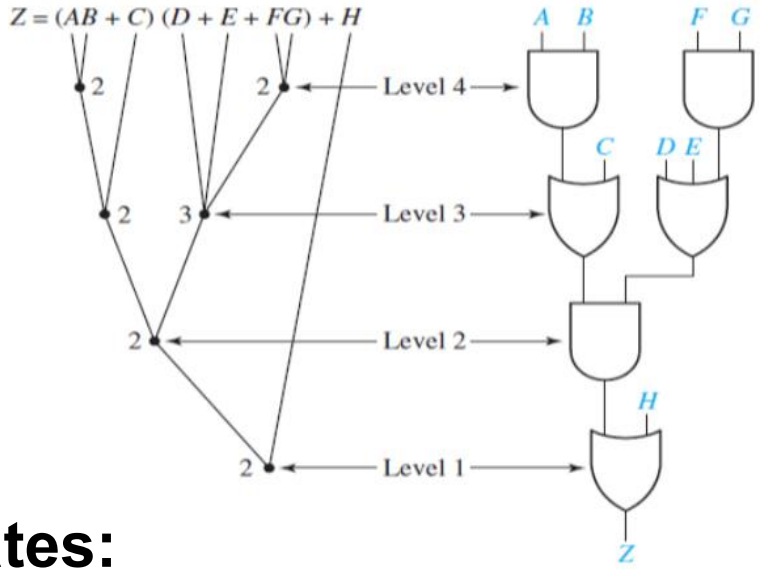
Multi-Level Gate Circuits

前提： 忽略输入端原、反变量的差别.

门的级数——

电路输入与输出之间串联的门的最大数值

- **二级电路**
  - *AND-OR* 电路（积之和）
  - *OR-AND* 电路（和之积）
- **三级电路**
  - *OR-AND-OR* 电路



- **Circuit of AND and OR gates:**
  - no particular ordering of the gates;
  - the output gate may be either AND or OR.

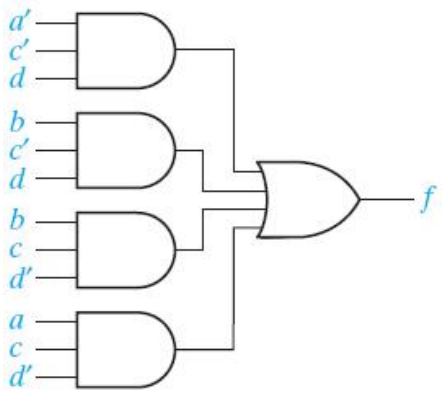
Multi-Level Gate Circuits

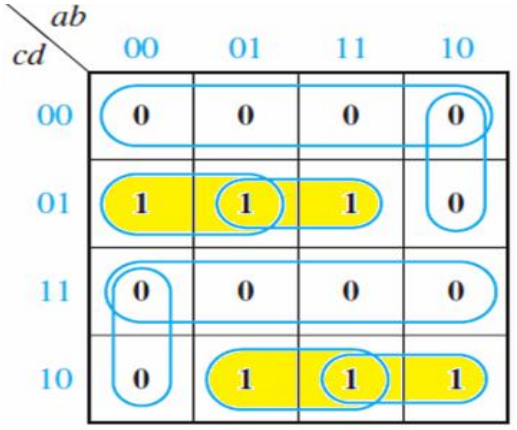
1. 二级电路

AND-OR 电路（积之和）

$$f = a'c'd + bc'd + bcd' + acd'$$

5个门, 16 个输入端

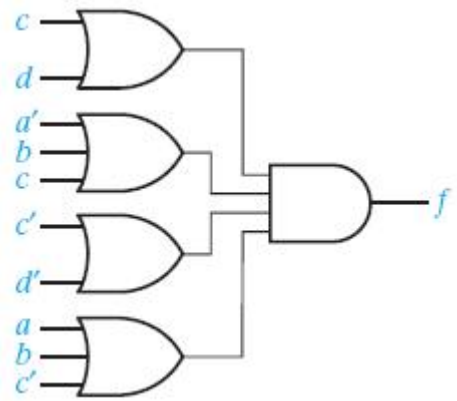




OR-AND 电路（和之积）

$$f = (c + d)(a' + b + c)(c' + d')(a + b + c')$$

5个门, 14 个输入端



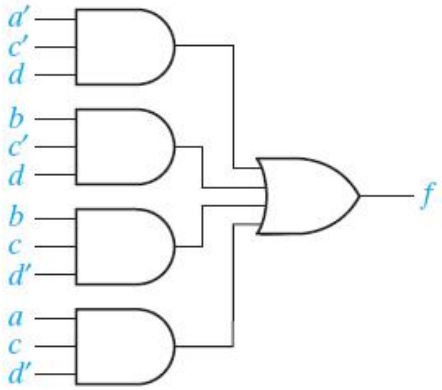
Multi-Level Gate Circuits

1. 二级电路

AND-OR 电路（积之和）

$$f = a'c'd + bc'd + bcd' + acd'$$

5个门, 16 个输入端

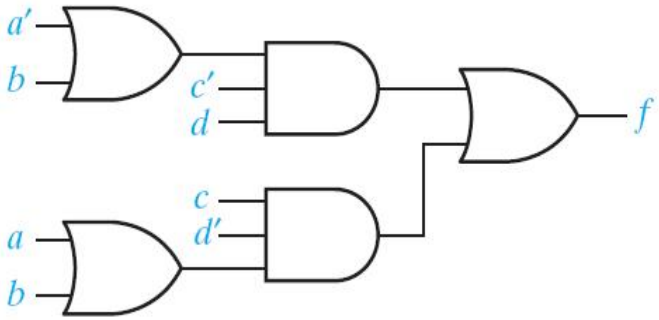


2. 三级电路

OR-AND-OR 电路

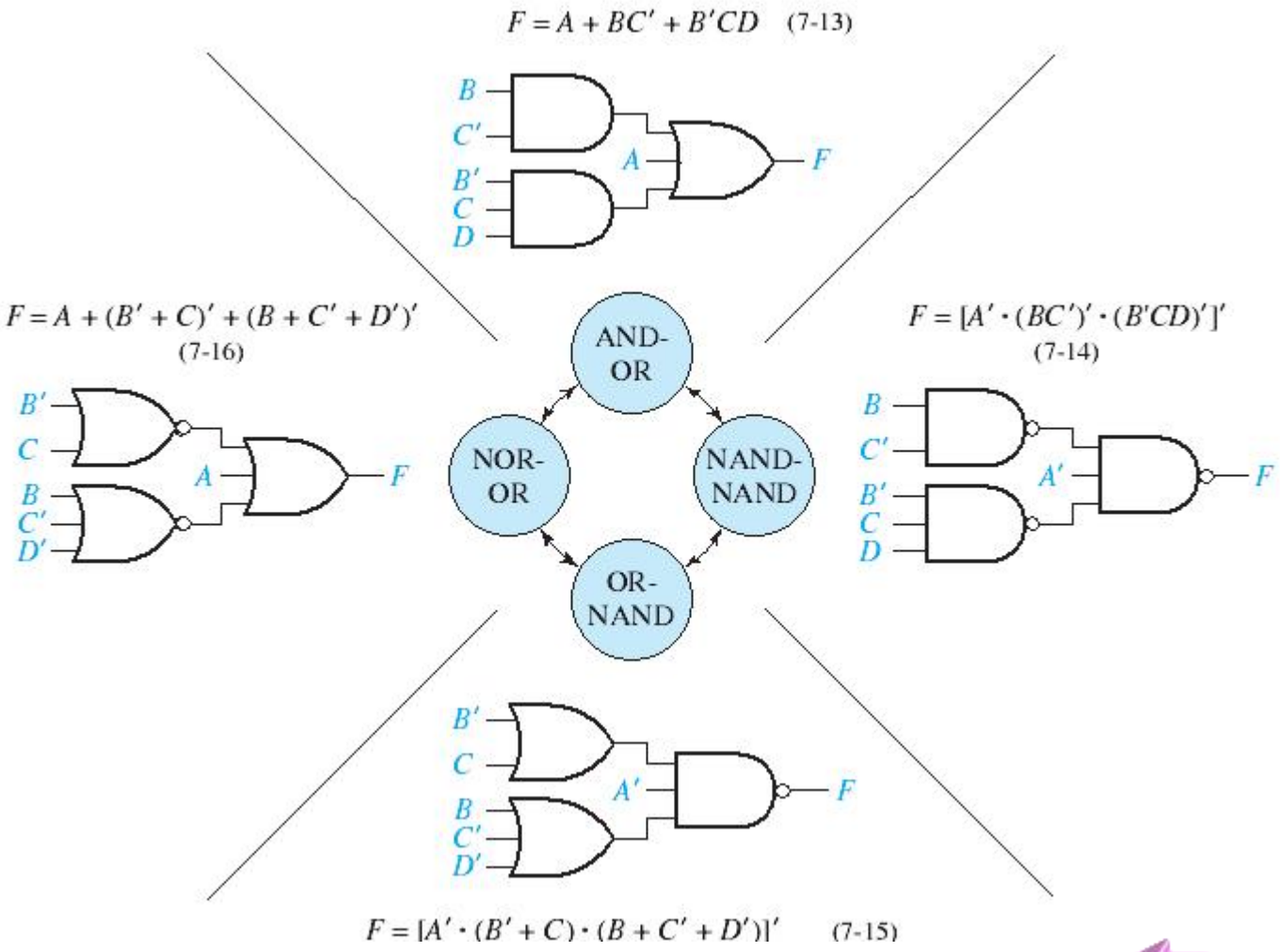
$$f = c'd(a' + b) + cd'(a + b)$$

5个门, 12 个输入端



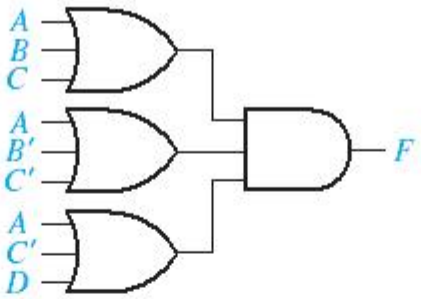
Multi-Level Gate Circuits

二级电路的8种基本形式

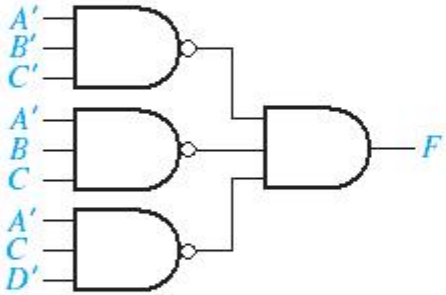


二级电路的8种基本形式

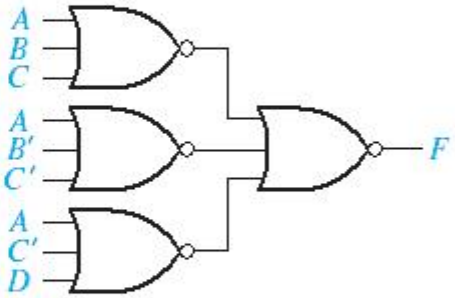
$$F = (A + B + C)(A + B' + C')(A + C' + D) \qquad (7\text{-}18)$$

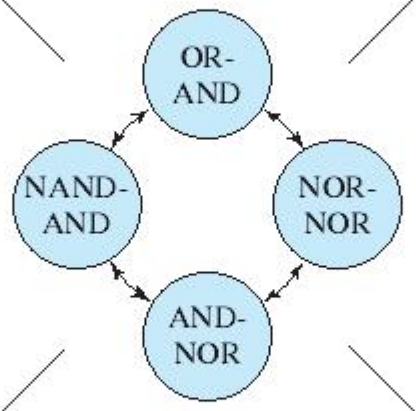


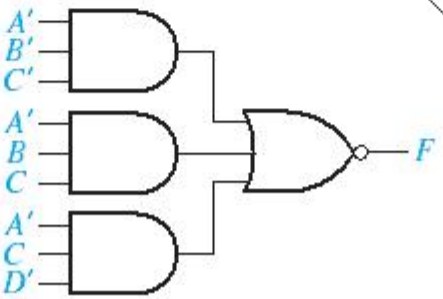
$$F = (A'B'C')' \cdot (A'BC)' \cdot (A'CD')' \qquad (7\text{-}21)$$



$$F = [(A + B + C)' + (A + B' + C')' + (A + C' + D)']' \qquad (7\text{-}19)$$







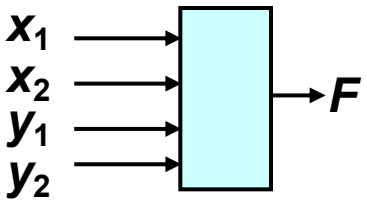
$$F = (A'B'C' + A'BC + A'CD')' \qquad (7\text{-}20)$$

Multi-Level Gate Circuits

Example

设计组合电路，对输入的2个二进制数 $X=X_1X_2$和 $Y=Y_1Y_2$ 比较，当$X>Y$, 输出$F=1$；否则，$F=0$.

① 确定输入输出



② 真值表

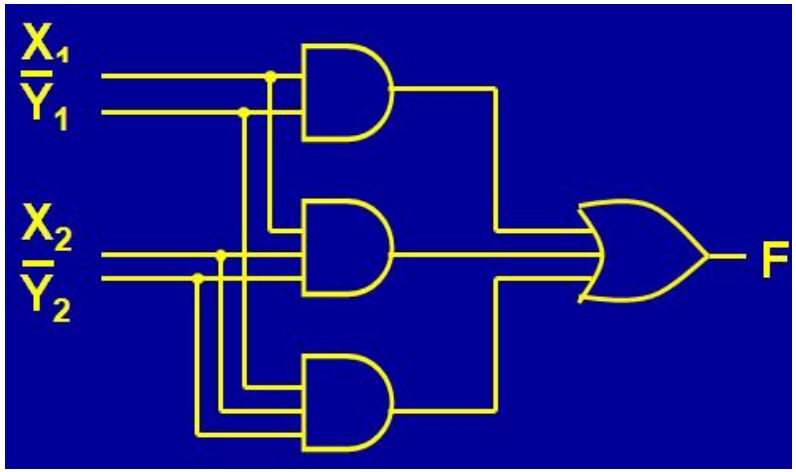
X_1 X_2 Y_1 Y_2	F	X_1 X_2 Y_1 Y_2	F
0 0 0 0	0	1 0 0 0	1
0 0 0 1	0	1 0 0 1	1
0 0 1 0	0	1 0 1 0	0
0 0 1 1	0	1 0 1 1	0
0 1 0 0	1	1 1 0 0	1
0 1 0 1	0	1 1 0 1	1
0 1 1 0	0	1 1 1 0	1
0 1 1 1	0	1 1 1 1	0

Multi-Level Gate Circuits

③ 最简二级与或电路

$$F = X_1\bar{Y}_1 + X_2\bar{Y}_1\bar{Y}_2 + X_1X_2\bar{Y}_2$$

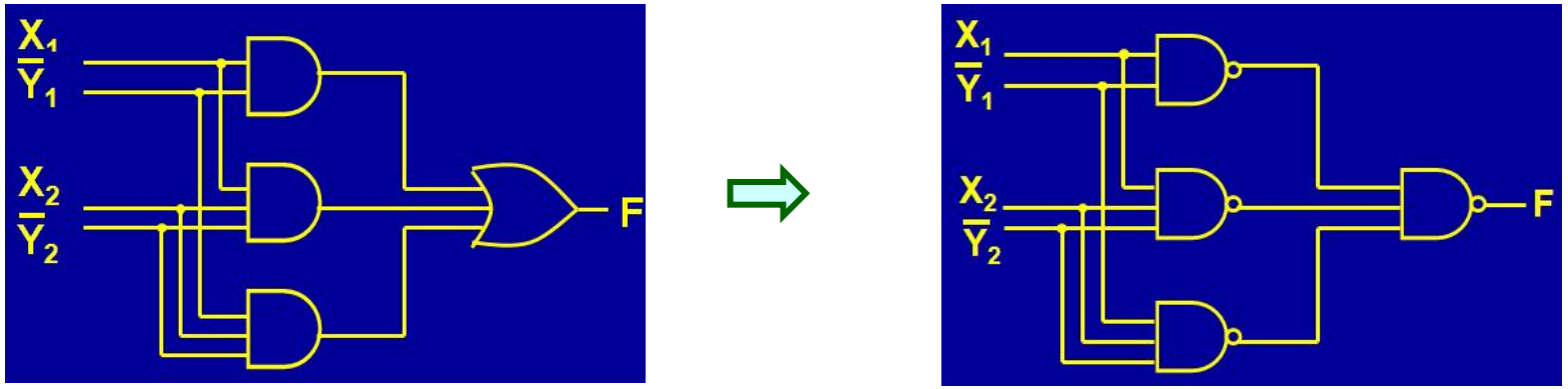
X_1X_2 \ Y_1Y_2	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0



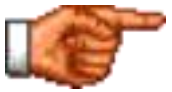
Multi-Level Gate Circuits

④. 采用单一逻辑门(与非门)设计

$$F = X_1\bar{Y}_1 + X_2\bar{Y}_1\bar{Y}_2 + X_1X_2\bar{Y}_2 = \overline{\overline{(X_1\bar{Y}_1)}\ \overline{(X_2\bar{Y}_1\bar{Y}_2)}\ \overline{(X_1X_2\bar{Y}_2)}}$$



Unit 5 Multi-Level Gate Circuits



- 多级门电路
- 两级门电路的设计
- 多输出电路的设计
- Some Examples

Design of Two-Level Circuits

Any logic can be realized in two level circuit :

$$F(X,Y,Z)=\sum_{XYZ}(1,6,7)=\prod_{XYZ}(0,2,3,4,5)$$

$$F'(X,Y,Z)=\sum_{XYZ}(0,2,3,4,5)=\prod_{XYZ}(1,6,7)$$

NAND and **NOR** gates:
相比与门、或门——速度更快；价格便宜；使用的器件更少

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一个与非门的功能至少要用一个与门或若干个或门及反相器(德蒙根定律：与门 = 或门+非门)才能实现。对相对复杂的电路而言问题则更加突出。元件数量越多，电路的延时就越长，整个电路的频响性能就会变差，对高频电路而言则更加不划算。

Design of Two-Level Circuits

1. 使用单一逻辑门（与非门）设计最简二级电路

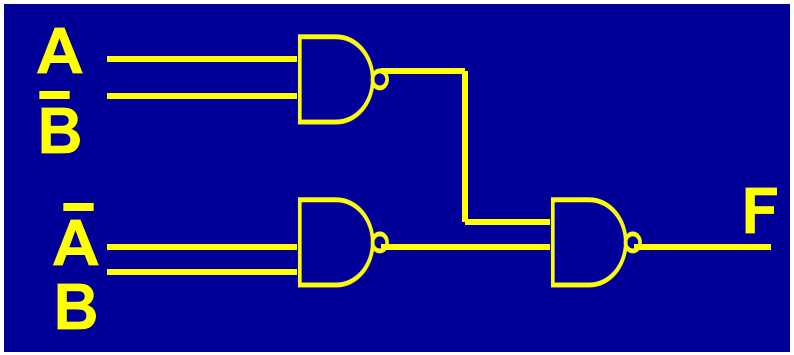
Given: 最简与或式

- Method 1： **(F')'**

$$F=\bar{A}B+A\bar{B}$$

$$=\overline{\bar{A}B+A\bar{B}}$$

$$=\overline{\bar{A}B}\cdot\overline{A\bar{B}}$$



Design of Two-Level Circuits

Given: 最简与或式

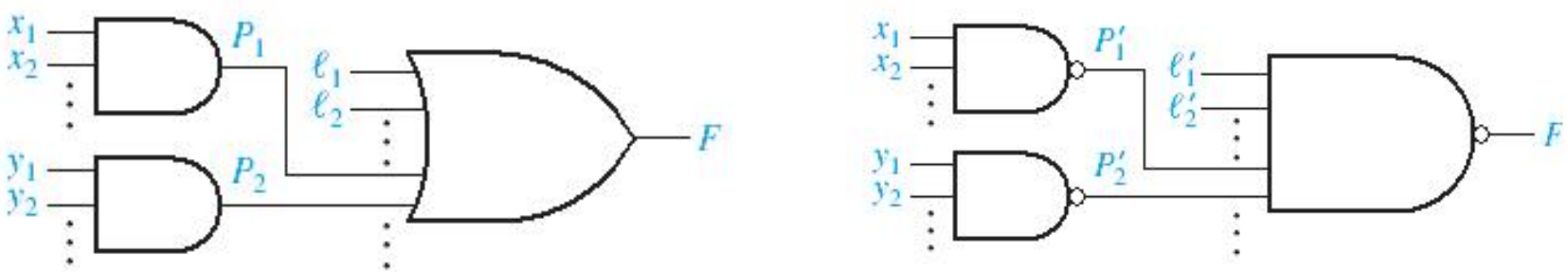
- Method 2:

1. 找出F的最简与或式（最简积之和）式.

2. 画出二级与或电路（*AND-OR*）.

3. 用与非门替换所有逻辑门.

4. 将连接输出门的所有单个变量取反



Design of Two-Level Circuits

2. 使用单一逻辑门（或非门）设计最简二级电路

Given: 最简与或式

- Method 1： $(F^D)^D$

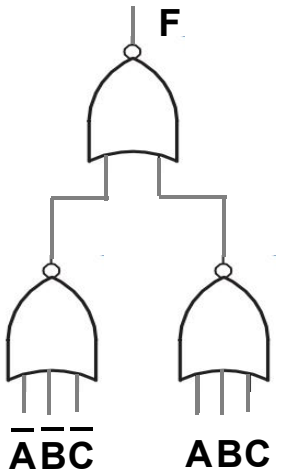
$$F=\bar{A}C+B\bar{C}+A\bar{B}$$

$$F^D=(A+\bar{B})\cdot(B+\bar{C})\cdot(\bar{A}+C)$$

$$=\bar{A}\bar{B}\bar{C}+ABC$$

$$=\overline{\bar{A}\bar{B}\bar{C}}\cdot\overline{ABC}$$

$$F=(F^D)^D=\overline{\overline{(A+B+C)}+\overline{(\bar{A}+\bar{B}+\bar{C})}}$$



Design of Two-Level Circuits

Given: 最简与或式

- Method 2:
  1. 找出F的最简与或式（最简和之积）.
  2. 画出二级或与电路（*OR-AND*）.
  3. 用或非门替换所有逻辑门.
  4. 将连接输出门的所有单个变量取反

Design of Two-Level Circuits

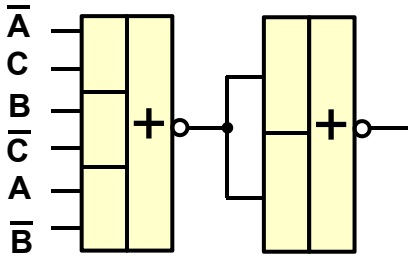
3. 使用单一逻辑门（与或非门）设计最简二级电路

Given: 最简与或式

- Method： **(F')'**

$$F=\bar{A}C+B\bar{C}+A\bar{B}$$

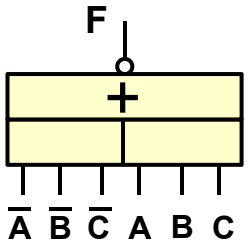
$$\overline{\overline{F=\bar{A}C+B\bar{C}+A\bar{B}}}$$



$$\overline{F}=\overline{\bar{A}C+B\bar{C}+A\bar{B}}$$

$$=\bar{A}\bar{B}\bar{C}+ABC$$

$$F=\overline{\bar{A}\bar{B}\bar{C}+ABC}$$

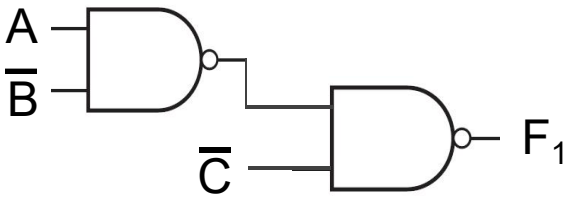


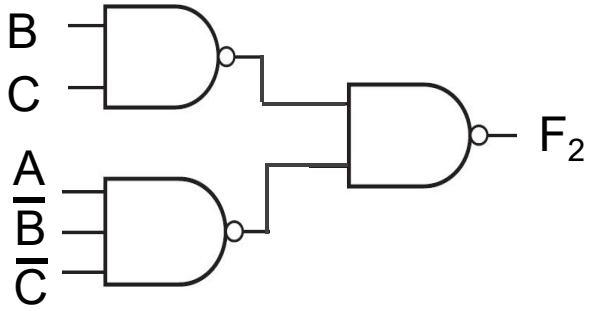
Unit 5 Multi-Level Gate Circuits

- 多级门电路
- 两级门电路的设计
- 多输出电路的设计

Design of Multiple-Output Circuits

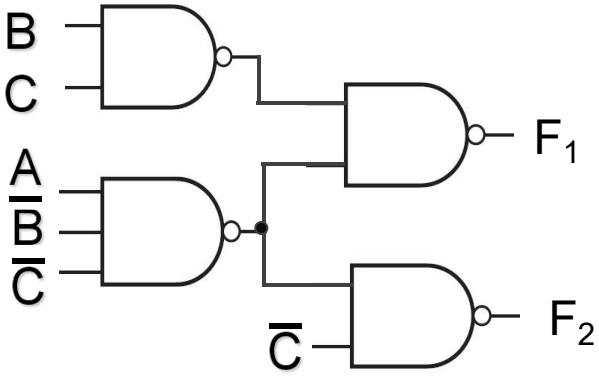
利用与非门设计二级电路：　$F_1 = C + A\bar{B}$，　$F_2 = BC + A\bar{B}\bar{C}$





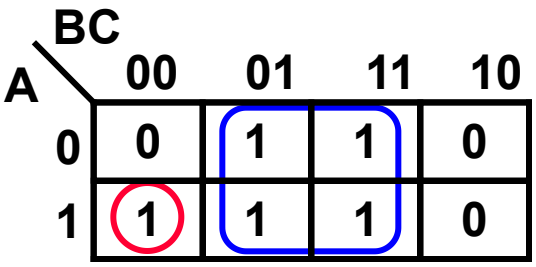
关键：寻找共享项，追求整体最简

$$
\begin{aligned}
F_1 &= C + A\bar{B} \\
&= C + A\bar{B}(C + \bar{C}) \\
&= C + A\bar{B}C + A\bar{B}\bar{C} \\
&= C + A\bar{B}\bar{C}
\end{aligned}
$$

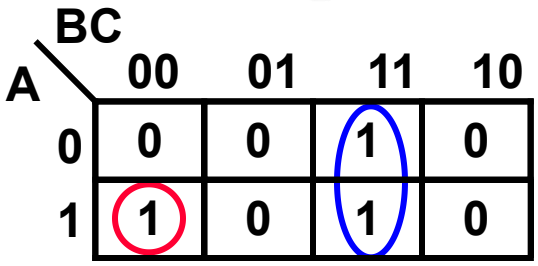


Design of Multiple-Output Circuits

F_1



F_2

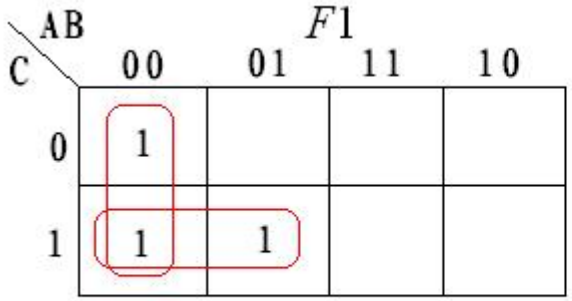


$F_1 = C + A\bar{B}\bar{C}$

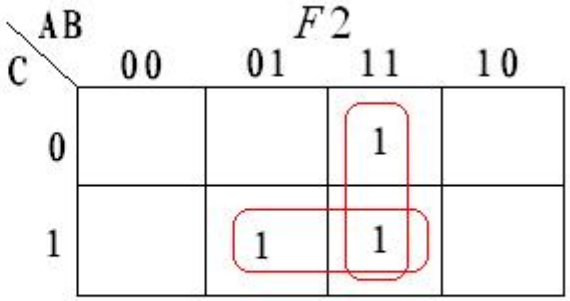
$F_2 = BC + A\bar{B}\bar{C}$

关键：寻找共享项，追求整体最简

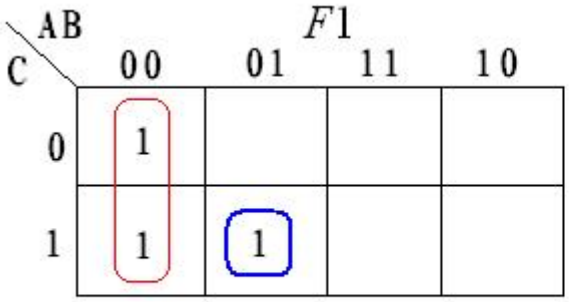
Design of Multiple-Output Circuits



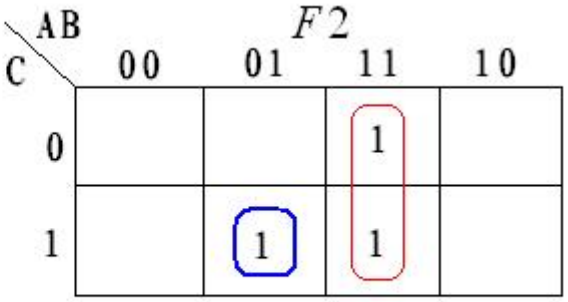
$$F1 = A' \cdot B' + A' \cdot C$$



$$F2 = A \cdot B + B \cdot C$$



$$F1 = A' \cdot B' + A' \cdot B \cdot C$$



$$F2 = A \cdot B + A' \cdot B \cdot C$$

小　　结

- 多级门电路（Multi-Level Circuits）
- 两级门电路的设计
- 多输出电路的设计
- 多级门电路实例