Assignment -2

CSA

Q1. What are differences b/w among sequential access, direct access & random access? What is locality of reference What is distinction b/w spatial locality & and temporal locality? What are strategies for exploiting spatial locality & temporal locality?
Consider following code

```
for (i=0; i<20; i++)
    for (j=0; j<10; j++)
        a[i] = a[i] * j;
```

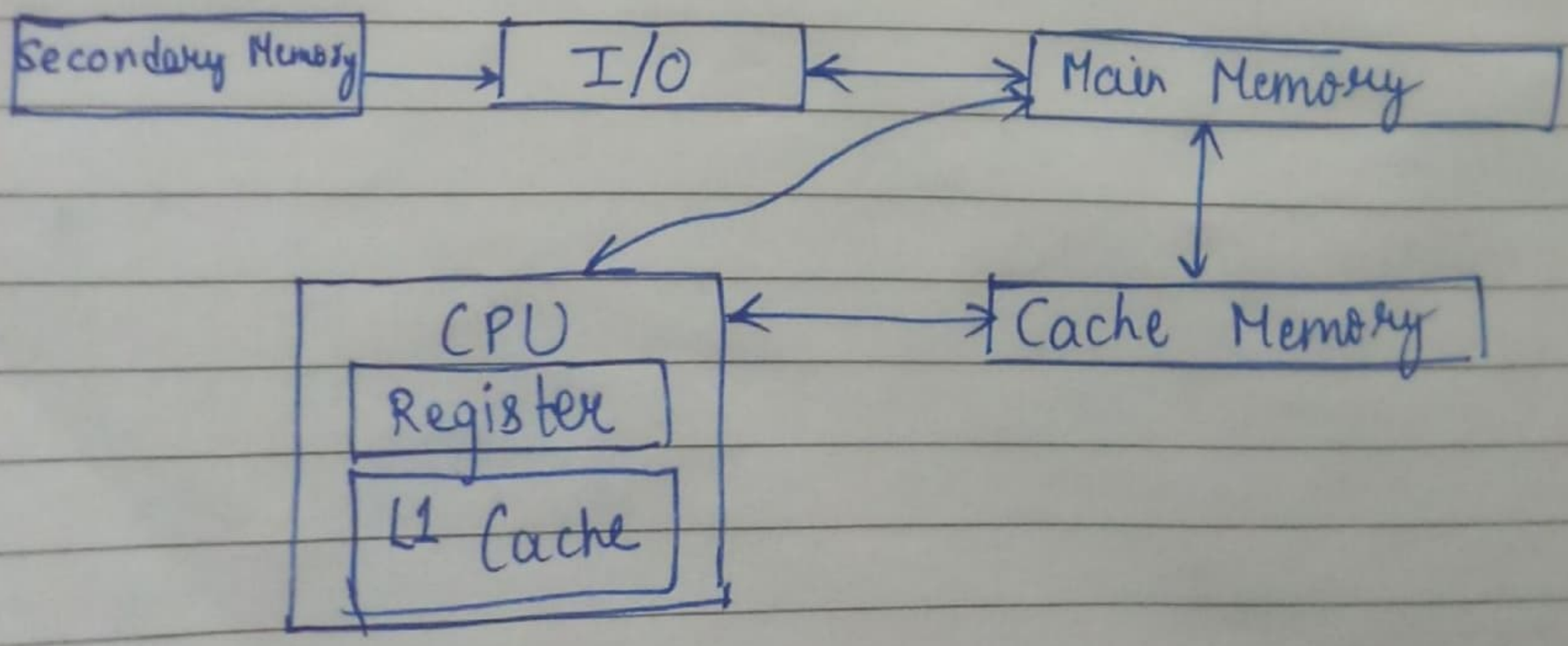
Give one example of spatial locality in the code and also provide one example of temporal locality in code.

Ans → Sequential access is accessing data in a specific linear sequence (example: tapes)

→ Direct access has data address based on physical location.

→ Random access, any location can be selected at random and addressable locations in memory have unique, physically wired-in-addressing mechanism.

→ Locality of Reference reference to a phenomenon in which computer program tends to access same set of memory locations for particular time period. Property of locality of reference is mainly shown by loops & subroutine calls in a program.



→ Spatial locality refers to tendency of execution to involve a number of memory locations that are clustered, while temporal locality deals with tendency for a processor to access memory locations that have been used recently.
Larger cache blocks & prefetching mechanisms are used to exploit spatial locality. Temporal locality is exploted by keeping recently used instructions & data values in cache memory, & by exploiting a cache hierarchy.

→ a[1] is accessed after a[0] both are near memory locations & hence example of spatial locality.
→ a[0] is accessed for j=0 & j=1 ; same memory location accessed in nearby time & hence example of temporal locality.

Q2* Set-associative cache has block size of four 16-bit words & set size of 2. Cache can accomodate a total of 4096 words. Main memory size that is cacheable of 64K 32 bits. Design cache structure & show how processor's addresses are interpreted.

Ans. Give that Set size → 2
Main Memory size → 64K X 32 bits

Calculate bits needed for each field:
Set size given is 2. So 2-bit set associative

Main memory size = 64 KB X 3 bits
= 64 KB X 32/8 B
= 64 KB X 4B

$= 256\ KB$

$= 2^{18}$

address format requires 18 bits in total.

Q4. A digital computer has memory units 64K x16 & a cache memory of 1K words. The cache uses direct mapping with block size of four words.

a) How many bits are there in tag, index, block & word fields of address format?
b) How many bits are there in each word of cache & how are they divided into functions? Include valid data.
c) How many blocks can cache accomodate?

Ans a) Main memory has $64K = 64 \times 1024 = 2^6 \times 2^{10} = 2^{16}$ words
Cache memory has $1K = 1024 = 2^{10}$ words

Cached address consists of index & tag part. Index & tag together make main memory address. Index part addresses cache memory & tag part represents rest of main memory address.
In this case to address main memory we need 16 bits (2^{16}) and to address cache memory we need 10 bits (2^{10}). Index is 10 bits wide & Tag is bits wide (16-10=6).

When using blocks the index is divided into "Block" part & the "Word" part. Block part addresses blocks of cache memory & word part addresses individual words in block.
In this case, the block is 4 words long for what we need 2 bits (2^2) and that leaves 8 bits (10-2=8) for addressing blocks.

Tag = 6 bits
Index = 10 bits
Block = 8 bits
Word = 2 bits

b) for above example a cache word with Valid bit would contain.

Valid bit = 1 bit
Tag = 6 bits
Data = 16 bits
Total bits = 23 bits

c) If cache has 1K words and block size is 4 words then number of ~~block~~ blocks is 1K/4 = 1024/4 = 256 ~~block~~ blocks.

Q5. Access time of cache memory is 100 ns & that of main memory 100 ns. It is estimated that 80% of memory requests are for read and remaining 20% are for write. Hit ratio for read access only is 0.9. A write through procedure is used.

a) What is average access time of system for considering only memories reads cycles?
b) Average access time of system for both read & write requests?
c) What is hit ratio taking into consideration the write cycle?

Ans a) Average access time read = Hit ratio X Cache access time + (1 - hit ratio) X Main memory access time

= 0.9 X 100 ns + (1 - 0.9) X 100 ns = 90 ns X 100 ns = 190 ns

b) If we take in account both read & write accesses then we have to sum averages for read & write

Read average would take those 80% of all these overall requests & average read access time of 190 ns we calculated in a) to get 0.8 X 190

Write average would take those 20% of overall requests and main memory access time of 1000 ns to get 0.2 X 1000ns.

We get :- 0.8 X 190ns + 0.2 X 1000 = 152 ns + 200 ns = 352ns

c) Hit ratio read = Read requests % X Hit ratio =
0.8 X 0.9 = 0.72

Q. What are key properties of semiconductor memory? What is difference b/w DRAM & SRAM in terms of application? What is difference b/w DRAM & SRAM in terms of characteristics of such as speed, size & cost? What are applications for ROM? What are difference b/w optical Magnetic Tape & Magnetic Disk?

Ans :- → They exhibit two stable states, which can be used to represent binary 1 or 0.
They are capable of being written into (at least once) to set state.
They are capable of being read to sense state.
→ SRAM is used for cache memory (both on & off chip), & DRAM is used for main memory.
→ SRAMs generally have faster access times than DRAMs. DRAMs are less expensive and smaller than SRAMs.

→ Microprogrammed control unit memory, library subroutines for frequently wanted functions, systems programs, function tables.

→ Magnetic Tape	Magnetic Disk
1. Cost of magnetic tape is less.	1. Cost of magnetic disk is high.
2. Realibility of magnetic tape is less.	2. Realibility of magnetic disk is more.
3. Access time for magnetic tape is more.	3. Access time for magnetic tape is less.
4. Data transfer rate for magnetic tape is comparatively less.	4. Data transfer rate for magnetic disk is more.
5. Magnetic tape is used for backups.	5. Magnetic disk is used as secondary storage.
6. Magnetic tape data accessing rate is slow.	6. Magnetic disk data accessing rate is high or fast
7. Magnetic tape data can't be updated after fed-up of data.	7. Magnetic disk data can be updated.
8. Magnetic tape is more portable.	8. Magnetic disk is less portable.

Q7. A computer use RAM chips of 1024 X 1 capacity.

a) How many chips are needed, and how many should their address lines be connected to provide a memory capacity of 1024 bytes?

b) How many chips are needed to provide memory capacity of 16K bytes?

c) Explain in words how chips are connected to address bus?

Ans a) We have to obtain memory whose capacity is 1024 bytes or (1024 × 8) bits

= No. of chips required to obtain memory capacity of 1024 bytes are :-

$$= \frac{1024 \times 8}{1024} = 8 \quad \text{Ans}$$

$\therefore 2^{10} = 1024$ so a memory chip capacity of 1024 bytes connected with 10 address lines

b) Capacity of chip = $(1024 \times 1) = 1024$ bits

We have to obtain whose capacity is 16 K bytes or (16 X 1024 X 18) bits

Hence,

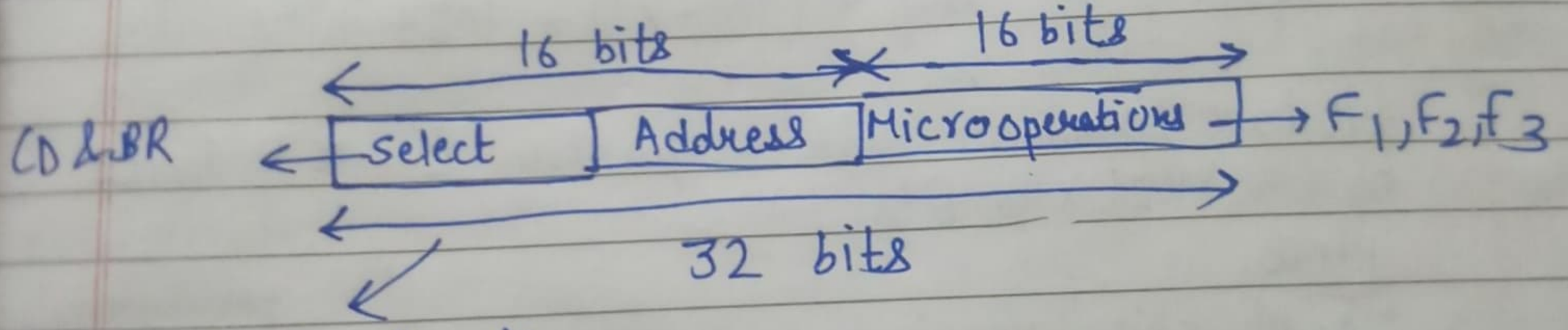
No. of chips required to obtain a memory capacity of 16 K bytes are :-

$$\frac{16 \times 1024 \times 8}{1024} = 128 \quad \text{Ans}$$

Q8 System uses a control memory of 1024 words of 32 bits each. Microcoinstruction has 3 fields and 16-bit micro-operations.

a) How many bits are there in the branch address field and selection field?
b) If there are 16 status bits in system, how many bits of branch logic are used to select status bit?
c) How many bits are left to select an input for multiplexer?

Ans
- Keywords : A system uses a control memory of 1024 words of 32 bits each. Microinstruction has 3 fields and 16-bits micro-operations.



Microcoinstruction diagram

- Control memory has 1024 words (2^{10}). The required address field for each word is 10 bits.
- Selection field consists of status bits & branch bits.
- Selection field will be: 32 - (16 + 10) = 6 bits

Microoperations total bits

Bit for address fie

a) Selected field will be 32 - (16+10) = 6 bits

b) 16 states means 4 bits are required for it (2^4)

c) Input for multiplexer = Selection field bits - Status bits = 6-4 = 2 bits

Q9 a) Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. Operations code has six bits. & control memory has 2048 words.

Ans OpCode = 6 bit

Control memory = 2048 words = 11 bits of address

mapping from 6 bits = 11 bit

XX XXXX

Ans = 00XXXXXX00

b) Show a 9-bit microoperation field in a microinstruction can be divided into subfields to specify 46 micro-operations. How many micro-operations can be specified in one-~~microcoin~~ microinstruction?

Ans. 5-bits $2^5 - 1 = 31$ micro operations

4-bits $2^4 - 1 = 15$ " "

Total = 46 " "

c) Explain the steps that are performed during address sequencing in detail.

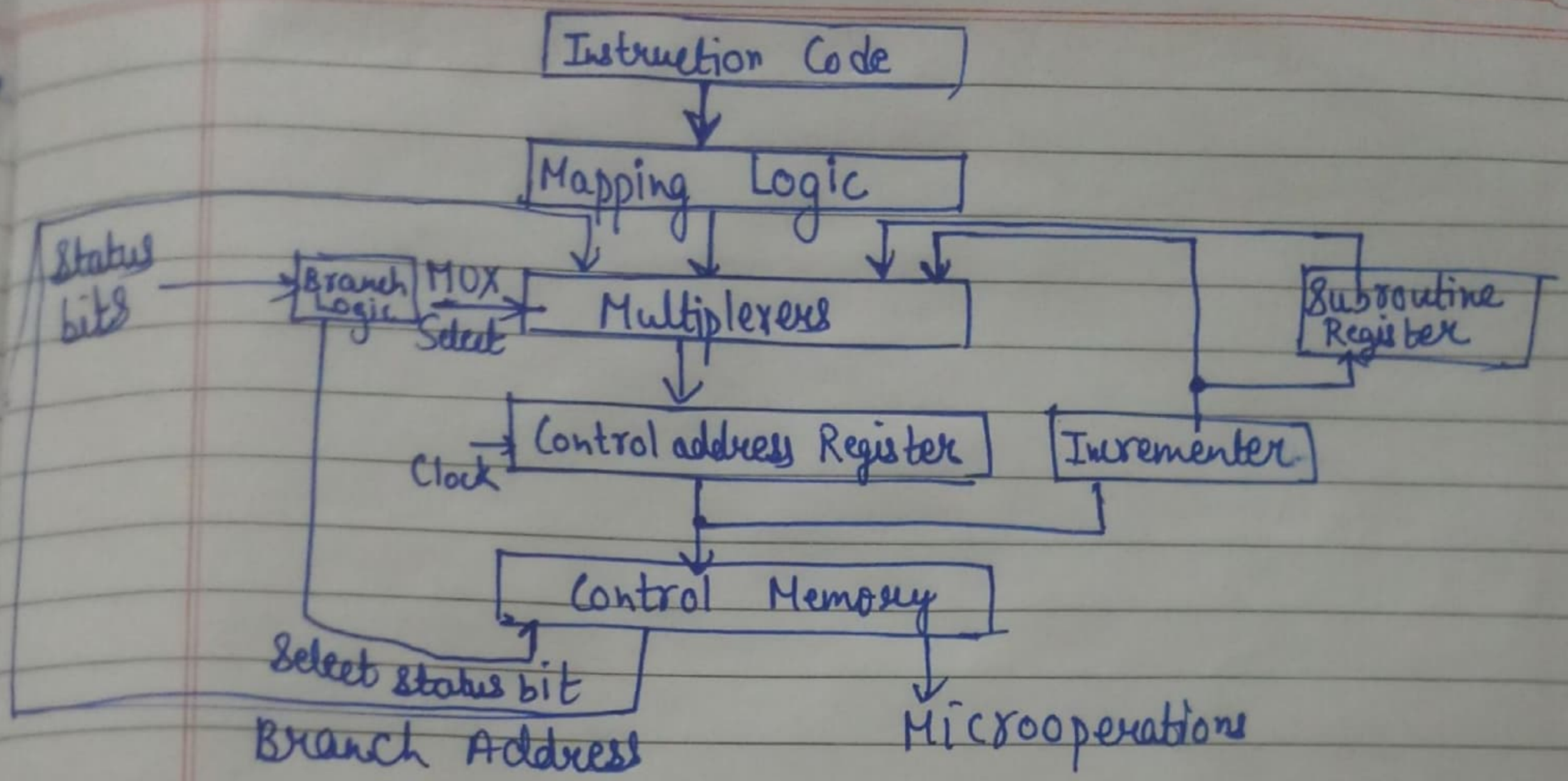
Ans Microinstructions in groups is used to store by control memory. Each group is used to specify a routine. Control memory of each computer has instructions which contains their micro-programs routine. Micro-programs are used to generate the micro-operations that will be used to execute instructions

Ans - 10 Suppose address sequencing of control memory is controlled by hardware. In that case, hardware must be capable to branch forom one routine to another routine and also able to apply sequencing of microinstructions within a routine. When we try to execute a single instruction of computer, control must undergo the following steps :-

① When power of computer is turned on, we have to first load an initial address into control address register. Address can be defined as first microinstruction address. With help of this address, we are able to activate the instruction fetch routine.
② Control memory will go through routine, which will be used to find out the effective address of operand.
③ In next step, a micro-operation will be generated which will used to execute instruction fetched from memory.

We are able to transform bits of instruction code into an address with help of control memory when routine is located. Process can be called mapping process. Control memory required the capabilities of address sequencing, which is described as follows :-

- On ~~status~~ of status bits conditions, address sequencing selects conditional branch or unconditional branch basis
- Addressing sequence is able to increment the control address register
- It provides facility for ~~subroutines~~ subroutines calls and returns.
- Mapping process is provided by addressing sequence from instructions bits to a control memory address.



b) What is Nano-Programming?

Ans A micro-instruction is in primary control-store memory, it then has control signals generated for each micro-instruction using a secondary memory is called nano-instruction.

c) What is superscalar processing?

Ans A superscalar processor is a processor designed to exploit Data-level Parallelism combined with Instruction level Parallelism, through implementation of pipeline with multiple executing Units.