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Ans-1- ① Moore's law is the observation that the number of transistors in a device integrated circuit (IC) doubles about every 2 years.

Moore's Law is an observation / projection of a historical trend. Rather than law of physics.

The basic organization of a computer system are:-

1) CPU (Central Processing Unit) - CPU is the brain of Computer.

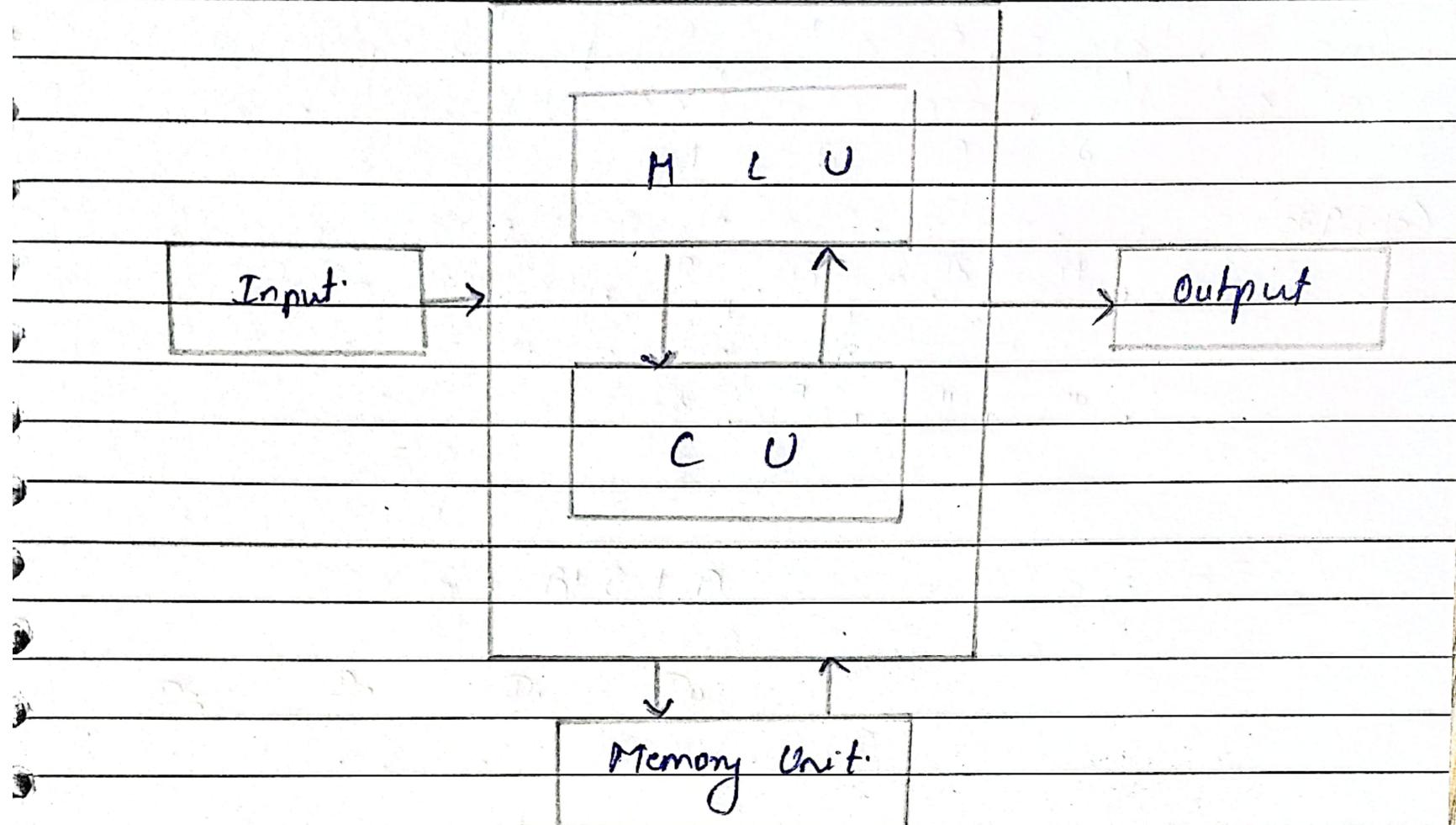
2) Arithmetic and logical unit - This is a part of CPU which perform mathematical calculations.

3) Input unit and Output unit - This unit controls input and output devices.

System design is the process of designing the components, modules, interfaces and data for a system to specified requirement. Functional unit are a part of a CPU that performs the operation called for by the computer program.

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Input

ALU

I/O

Memory

Processor

Output

Control Unit

- b) Virtual Memory: → It is a memory management technique that provides an idealized abstraction of the storage resources that are actually available on a given machine.

Advantages:-

- More process may be maintained in the main memory.
- A process may be larger than all of the main memory.
- It allows greater multiprogramming level by using less of available (primary) memory for each process.
- Virtual memory provides many functions, including multitasking (multiple task executing at one on one CPU), allowing multiple process to access the shared library in memory swapping and others.

Cache Memory

Virtual Memory

- 1) Cache memory is a memory unit and is very easy to access.
- 1) Virtual memory is a technique and involve Hard disk & is slower to access.
- 2) The size of cache memory is less than the virtual memory.
- 2) The size of virtual memory is greater than the code cache memory.
- 3) Hardware manages the cache memory.
- 3) Operating System manages the virtual memory.
- c) The Von - Neumann architecture consist of a single, shared memory for programs and data, shared memory for programs and a single bus for memory access, an arithmetic unit and a program control unit. The von Neumann processor operating fetching and execution cycles seriously.

The von - Neuman processor operate fetching and execution cycles seriously.

It's important due to control unit retrieves data and instruction in the same manner from one memory. The von Neumann is a bottleneck throughout caused by the standard personal Computer Architecture.

Ans-2- a)

$$\text{Q. } f(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$$

	$C'D$	$\bar{C}D$	$\bar{C}D$	CD	CD	$C\bar{D}$
AB	00					
$\bar{A}\bar{B}$	00	1	1	0	1	1
$\bar{A}B$	01	0	1	1	0	0
$A\bar{B}$	10	0	1	1	0	0
AB	11	0	1	1	1	1
$A\bar{B}$	10	0	1	0	1	1
$\bar{A}\bar{B}$	00	1	1	0	1	1

Now, $f(A, B, C, D) = (A'B + AB)(C'D + CD) +$
 $(A'B' + A'B + AB + AB')(C'D + CD) +$
 $(A'B' + AB')(CD' + CD') = B$
 $\Rightarrow BD + C'D + B'D'$

$$f(A, B, C, D) = BD + C'D + B'D'$$

② $f(A, B, C, D) = \sum m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \sum d(0, 2, 14)$

	$C'D$	$\bar{C}D$	$\bar{C}D$	CD	CD	$C\bar{D}$
AB						
$\bar{A}\bar{B}$	X	0	1	3	1	X ₂
$\bar{A}B$	1	1	0	5	0	7
$A\bar{B}$	0	1	1	1	1	1
AB	12	13	13	15	15	X
$A\bar{B}$	1	1	1	1	0	0
$\bar{A}\bar{B}$	8	9	9	11	10	10

$$\begin{aligned}
 \text{Now, } F(A, B, C, D) &= (AB + AB') (C'D + CD) \\
 &\quad + (CA'B' + AB') (C'C'D + CD) \\
 &\quad + (CA'B') (AB) (CD' + C'D) + \\
 &\quad (CA'B' + A'B) (C'C'D' + CD') \\
 \Rightarrow F(A, B, C, D) &= AB + B'D + B'C' + A'D'
 \end{aligned}$$

iii) $F(A, B, C, D) = (3, 5, 7, 8, 11, 12, 13)$

AB	CD	00	01	11	10
00	1	1	0	3	12
01	1	4	0	5	16
11	0	2	0	3	15
10	0	8	0	11	0

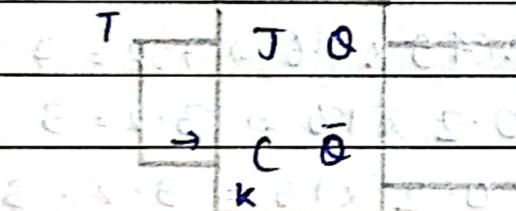
$$F(A, B, C, D) = (A + \bar{C}) \cdot (\bar{A} + \bar{B})$$

b) flip flop is a circuit that maintains a state until directed by input to change state. A flip flop can be constructed by 4 NAND or 4 NOR gates.

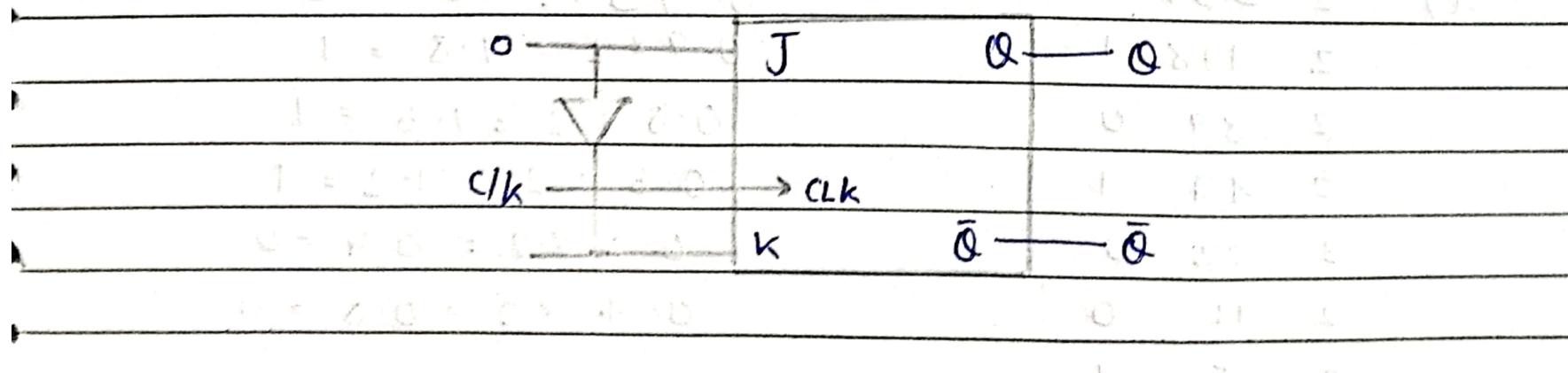
Types of Flip Flops:

- T Flip Flop
- JK Flip Flop
- D Flip Flop

In order to convert J-k flip flop to T- flip flop one can make both the input same i.e., $J = k$.



In order to convert JK flip flop to D types JK input pins with D input and its negation. Thus additional hardware component required would be a not



(Further implementation)

$$Ans-3-i) a) (357 \cdot 45)_{10} = (4)_8$$

8 357			
			$0.45 \times 8 = 3.6 \quad 3$
8 44 5			$0.6 \times 8 = 4.8 \quad 4$
8 5 4			$0.8 \times 8 = 6.4 \quad 6$
			$0.1 \times 8 = 3.2 \quad 3$
0 5			$0.2 \times 8 = 1.6 \quad 1$

$$(357 \cdot 45)_{10} = (545.346\overline{31463146})_8$$

$$b) (357 \cdot 45)_{10} = (4)_{16}$$

16 357			
			$0.45 \times 16 \Rightarrow 7.2 = 7$
16 23 7			$0.2 \times 16 \Rightarrow 3.2 = 3$
16 1 7			$0.2 \times 16 = 3.2 = 3$
0 1			

$$(357 \cdot 45) = (177.73333)_{16}$$

(i) 2 357		$0.45 \times 2 = 0.9 = 0$
2 178 1		$0.9 \times 2 = 1.8 = 1$
2 89 0		$0.8 \times 2 = 1.6 = 1$
2 44 1		$0.6 \times 2 = 1.2 = 1$
2 22 0		$0.2 \times 2 = 0.4 = 0$
2 11 0		$0.4 \times 2 = 0.8 = 0$
2 5 1		
2 2 0		
2 1 0		
0 1		

$\Rightarrow (101100101.01110011001)_2$

ii) $(AJD)_{16} = (?)_{18}$

$(AJD)_{16}$ first base 16 to base 18.

$$= A \times 16^2 + 1 \times 16^1 + 0 \times 16^0$$

$$= (2589)_{10}$$

Now $(2589)_{10} \rightarrow (?)_8$.

divided by 8

$$\underline{2589} = 328 \text{ with rem } 5$$

8

$$\underline{328} = 40 \text{ with } 3$$

8

$$\underline{3} = 0 \text{ with } 5$$

0

So,

$$(5035)_8$$

b) $(86.5625)_{10} \rightarrow 0.1010101001 \times 2^n k^n$

$n_{15} \rightarrow 0's \text{ or } 1's$.

$$0.10101101001 \times 2^{11}$$

c) Total length is 38 bits (1 bit sign, 8 bit biased), 8 bits biased, 8 bits biased exponents 23 bits mantissa.

The number is 1.010110101×2^6 so exponent is biased.

from its $6 + 129 = 135$

$$\text{ii) a)} (AID)_{16} = (?)_8$$

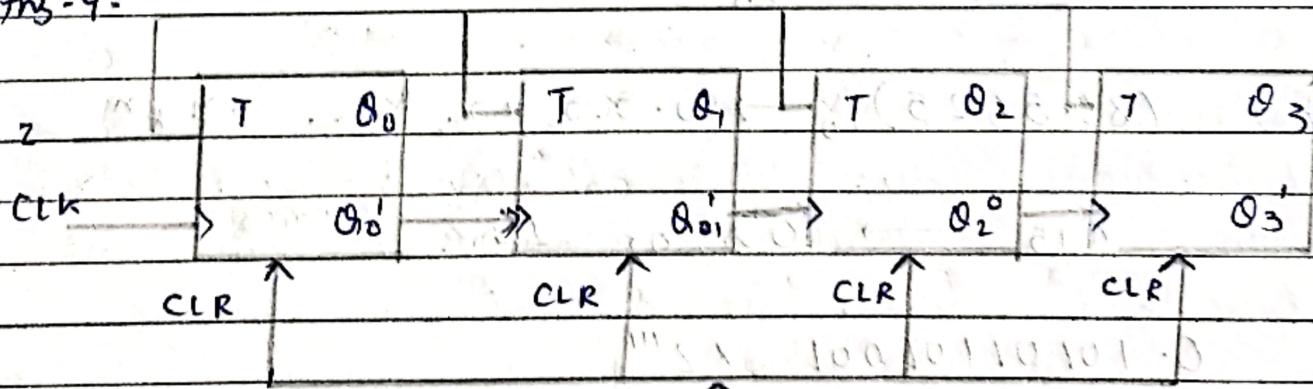
$$(AID)_{16} = 10 \times 16^2 + 1 \times 16^1 + 13 \times 16^0 \\ = (2589)_{10}$$

8	2 5 8 9		
8	3 2 9	5	$= (5035)_8$
8	4 0	3	
8	5	0	
	0	5	

$$\text{b) } 1010110 \cdot 1001$$

$$\text{c) } 56.9$$

Ans - 4.



Addition of Q_0 and Q_1 did not exceed total 10
Addition of Q_1 and Q_2 did not exceed total 10
Addition of Q_2 and Q_3 did not exceed total 10
Average Q_3 is 10. Addition of Q_3 and column 10
is 10. Total is 20. Second bit is 1

Ans-5- According to formula if there are n numbers of k bits register, then their should be k number of $N \times 1$ max.

- 1) a selection input are there in mux.
 - 2) 64 multiplexers are there in bus.
 - 3) 32×1 sized. multiplexer needed.

Ans - 6. a)

$$A \cdot B = B \cdot A$$

$$(A \cap B) \cap C = A \cap (B \cap C)$$

$$LHS = (ATB)TC \stackrel{?}{=} R.H.S \quad AT(BC)$$

$$\Rightarrow A \cdot B \cdot C = \overline{A} \cdot \overline{(B \cdot C)}$$

$$\Rightarrow AB + C = A + BC$$

$$\Rightarrow AB + \bar{C} = \bar{A} + BC$$

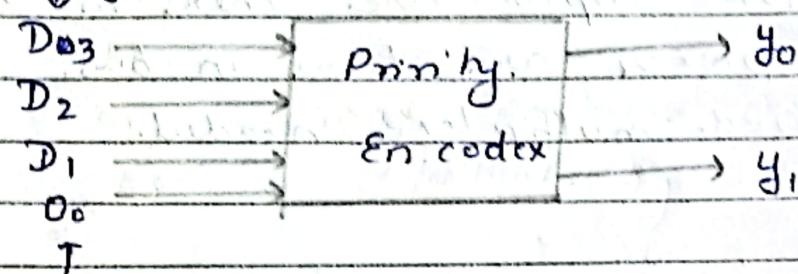
C-H-S ≠ R-H-S

Hence proved.

b) RISC processor CTSC.

- | | |
|------------------------|----------------------------|
| 1) force on software | 1) force on hardware |
| 2) code size is large. | 2) code size is small. |
| 3) fixed size instruc. | 3) variable sized instruc. |

Ans-7. Priority Encoders. Priority encoder takes one of their data input one at a time and convert them into binary code at its output.



Block diagram

Highest Input Lowest Output

D_3	(D_3)	D_2	(D_2)	D_1	(D_1)	D_0	(D_0)	y_1	y_0
0	0	0	0	0	0	0	0	x	x
0	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	x	1	1	1
0	0	0	1	1	x	x	0	0	0
1	1	x	x	x	x	x	1	1	1

Karnaugh Map
AB CD

0	1	3	1	
4	5	7	6	
1	1	1	1	SOP(15)

Priority encoder truth table

Input & output labels

Priority encoder address

Priority encoder address

12 13 15 14

1 1 1 1

8 9 11 10

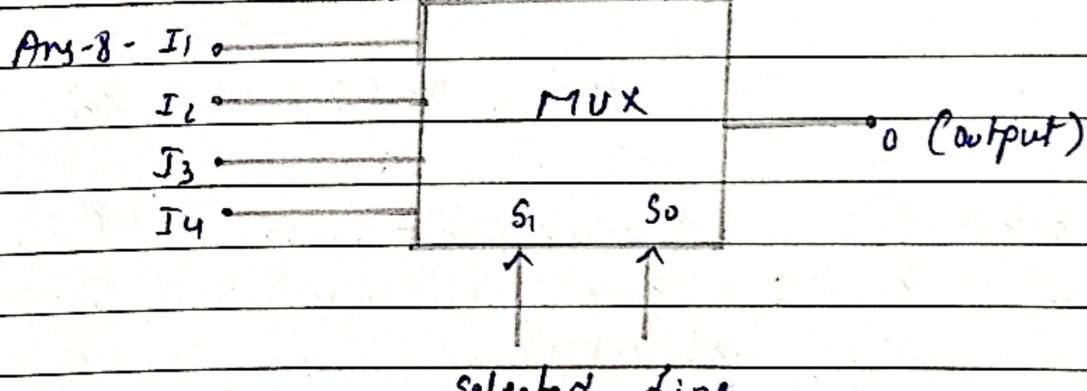
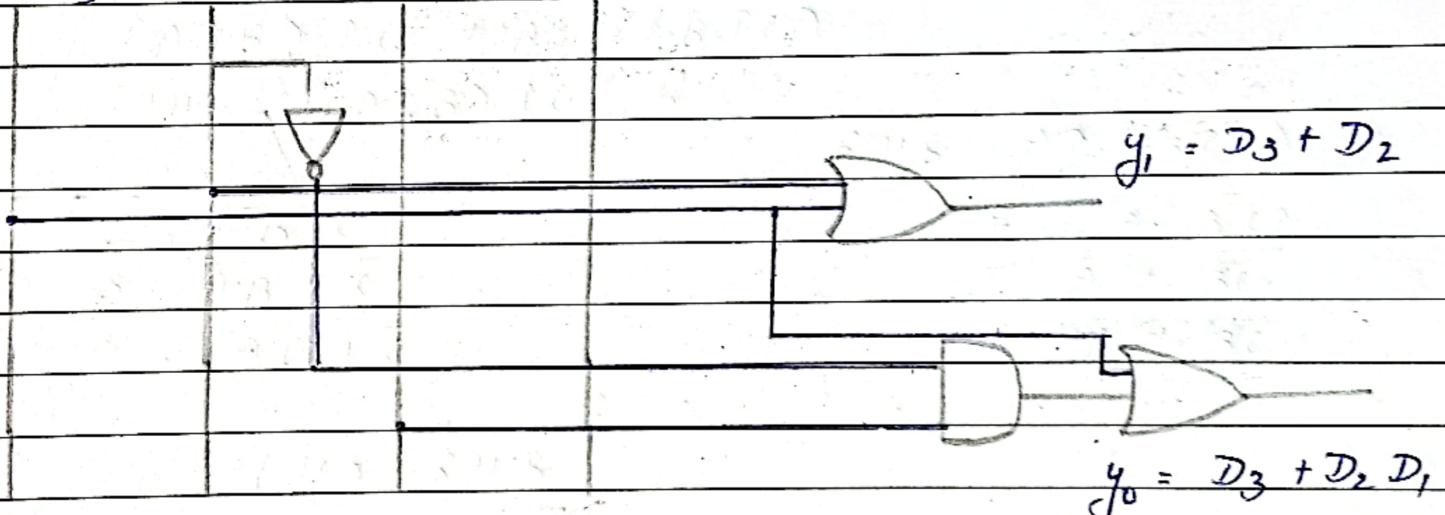
1 1 1 1

$$S = B + A$$

		CD		AB			
		0	1	3	2		
x						1	
4	5 = 0	3				6	
12	13		15	14			
8	9	1	11	10			

$$S = B' C + A$$

$D_3 \quad D_2 \quad D_1 \quad D_0$



Truth Table

$S_1 \quad S_0 \quad V$

$$O = S_1' S_0^2, I_0 = S_1' S_0' I_2 +$$

(or) $O = S_0 I_1$

$S_2 \quad S_0 \quad I_3$

0 1 I_1

1 0 I_2

max contains AND gate

1 1 I_3 follow by OR gate