Interrupts

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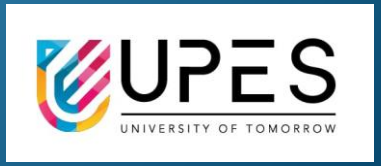


Introduction

- Interrupt is an internal or external signal which may disturb or alter the sequence of execution of processor.
- It is a method by which an I/O device informs the processor that it requires services of the processor.
- It is asynchronous.
- The response to an interrupt is controlled by the microprocessor.
- Interrupt can be classified as:

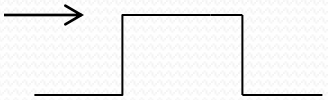
a. **Maskable –** Interrupt which can be avoided.

Non-Maskable - Interrupt which cannot be ignored or avoided.

b. **Vectored** – Interrupt which has specific address location in the memory.

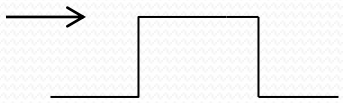
Non-vectored – Interrupt which do not have specific address location in the memory.

8085 Interrupt

Priority	Interrupt	Type of Triggering	Vector Address
1	TRAP		0024 H
2	RST 7.5		003C H
3	RST 6.5		0034 H
4	RST 5.5		002C H
5	INTR		

MASKABLE

VECTORED



Level Triggering

Edge Triggering

- The 8085 interrupt process is controlled by the Interrupt Enable flip-flop, which is internal to the processor and can be set or reset by using software instructions.

Flip-flop	Enabled	Microprocessor is enabled
INTR	High	

- The 8085 interrupt process is described in terms of following process:

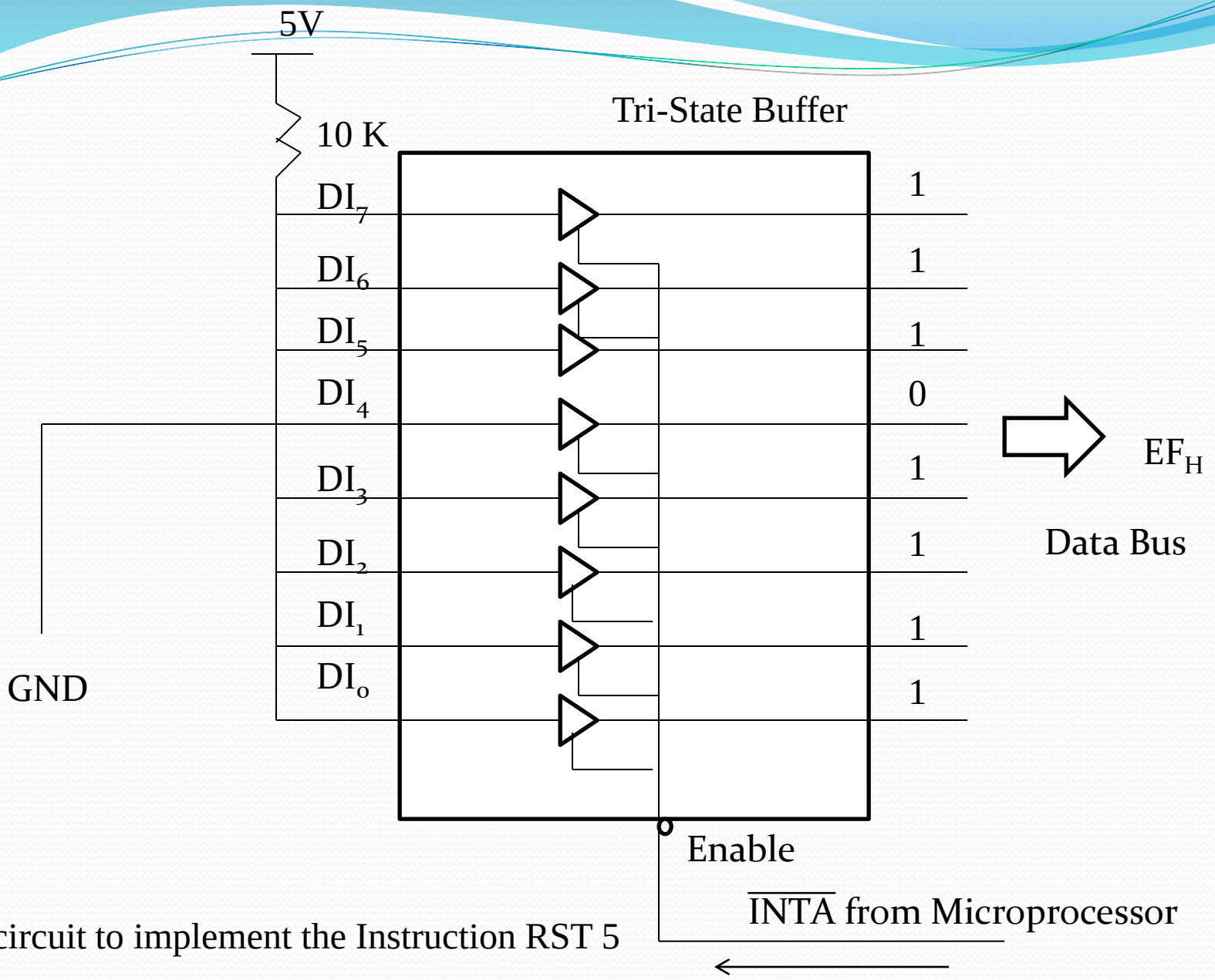
1. The interrupt is enabled using EI instruction in the main program. The DI resets the flip-flop and disable the interrupt process.

EI	Enable Interrupt
DI	Disable Interrupt

2. While executing the program, microprocessor checks the INTR line during the execution of each instruction.
3. If interrupt is enabled and INTR is high, the processor completes its present instruction and sends $\overline{INTA}$ signal.
4. The signal $\overline{INTA}$ is used to insert a restart (RST) instruction (Call instruction) through external hardware.
5. When the microprocessor receives an RST instruction it saves the memory address of the next instruction on the stack.
6. The program is transferred to CALL location and performs the task in the subroutine (service routine).
7. The subroutine contains the EI instruction.
8. At the end of the subroutine, RET instruction is used.

Restart Instructions

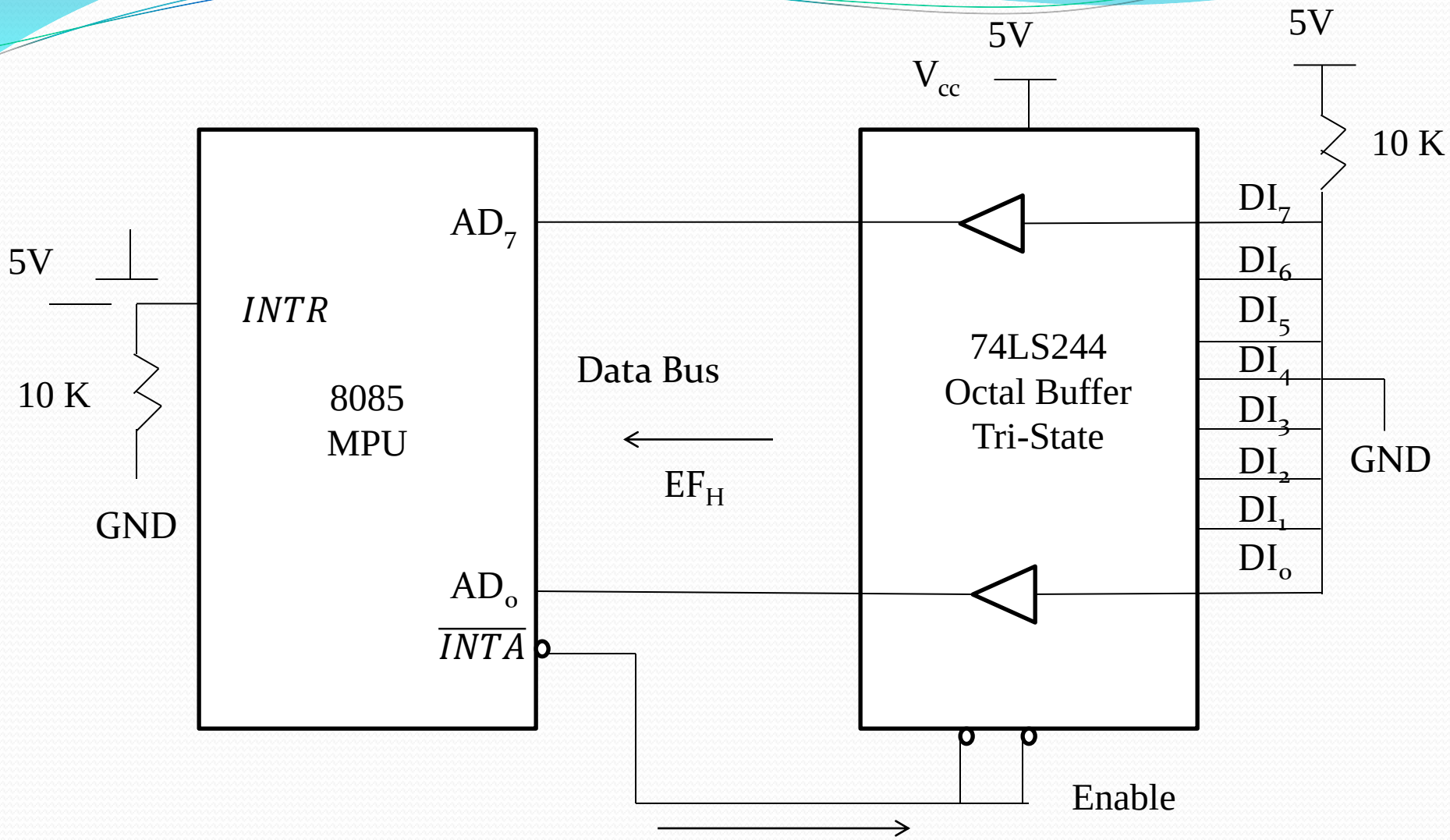
	Binary code									
Mnemonics	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex Code**	**Call Location In Hex**
RST0	1	1	0	0	0	1	1	1	C7	0000
RST1	1	1	0	0	1	1	1	1	CF	0008
RST2	1	1	0	1	0	1	1	1	D7	0010
RST3	1	1	0	1	1	1	1	1	DF	0018
RST4	1	1	1	0	0	1	1	1	E7	0020
RST5	1	1	1	0	1	1	1	1	EF	0028
RST6	1	1	1	1	0	1	1	1	F7	0030
RST7	1	1	1	1	1	1	1	1	FF	0038



A circuit to implement the Instruction RST 5

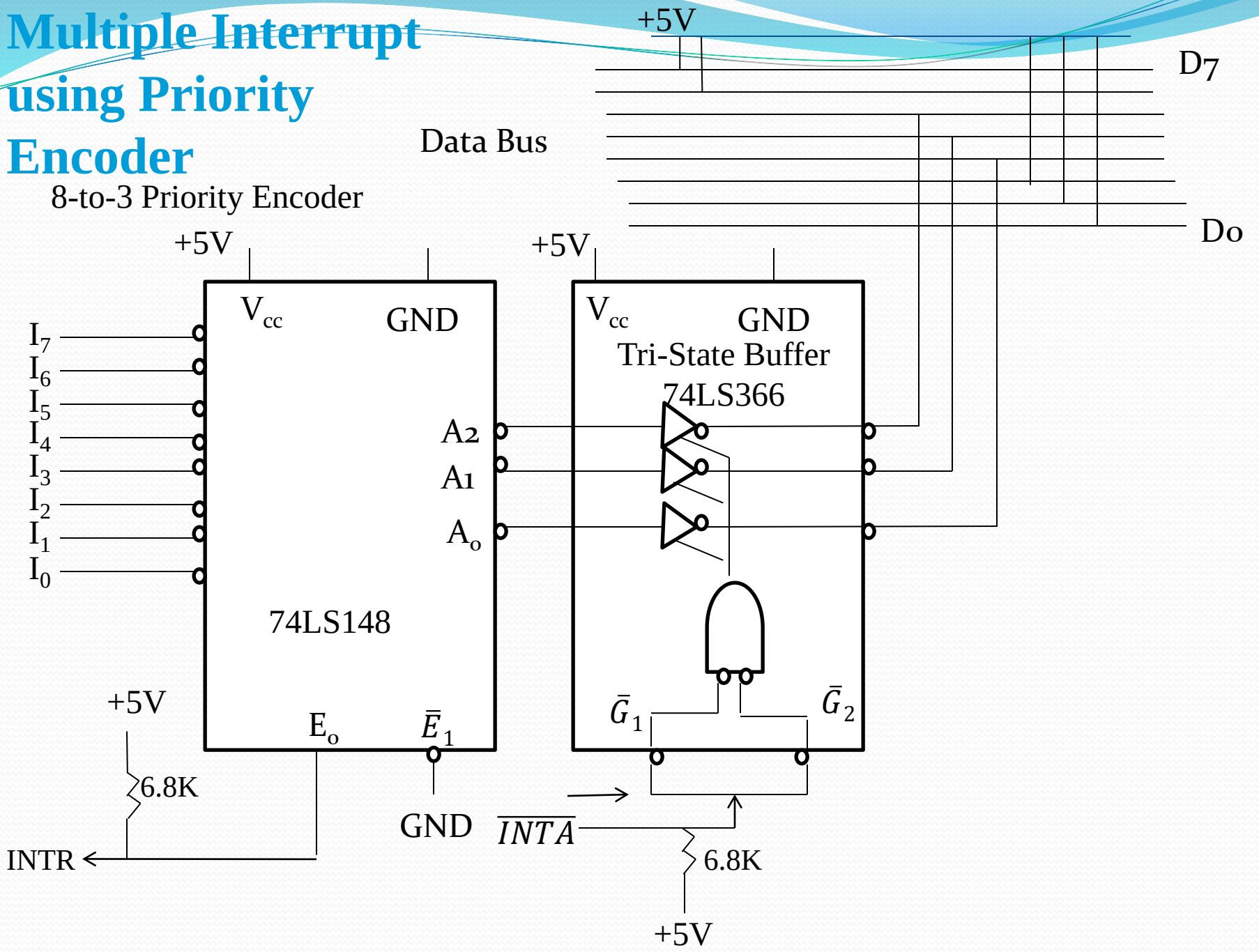
HOMEWORK

- WAP to count continuously in binary with a one second delay between each count.
- Write a service routine at XX70H to flash FFH five times when the program is interrupted, with some appropriate delay between each flash.



Schematic to Implement the 8085 Interrupt

Multiple Interrupt using Priority Encoder



Vectored Interrupt

- The four vectored interrupt of 8085 microprocessor don't require the $\overline{INTA}$ signal or an input port.
- The necessary hardware is implemented inside 8085 microprocessor.

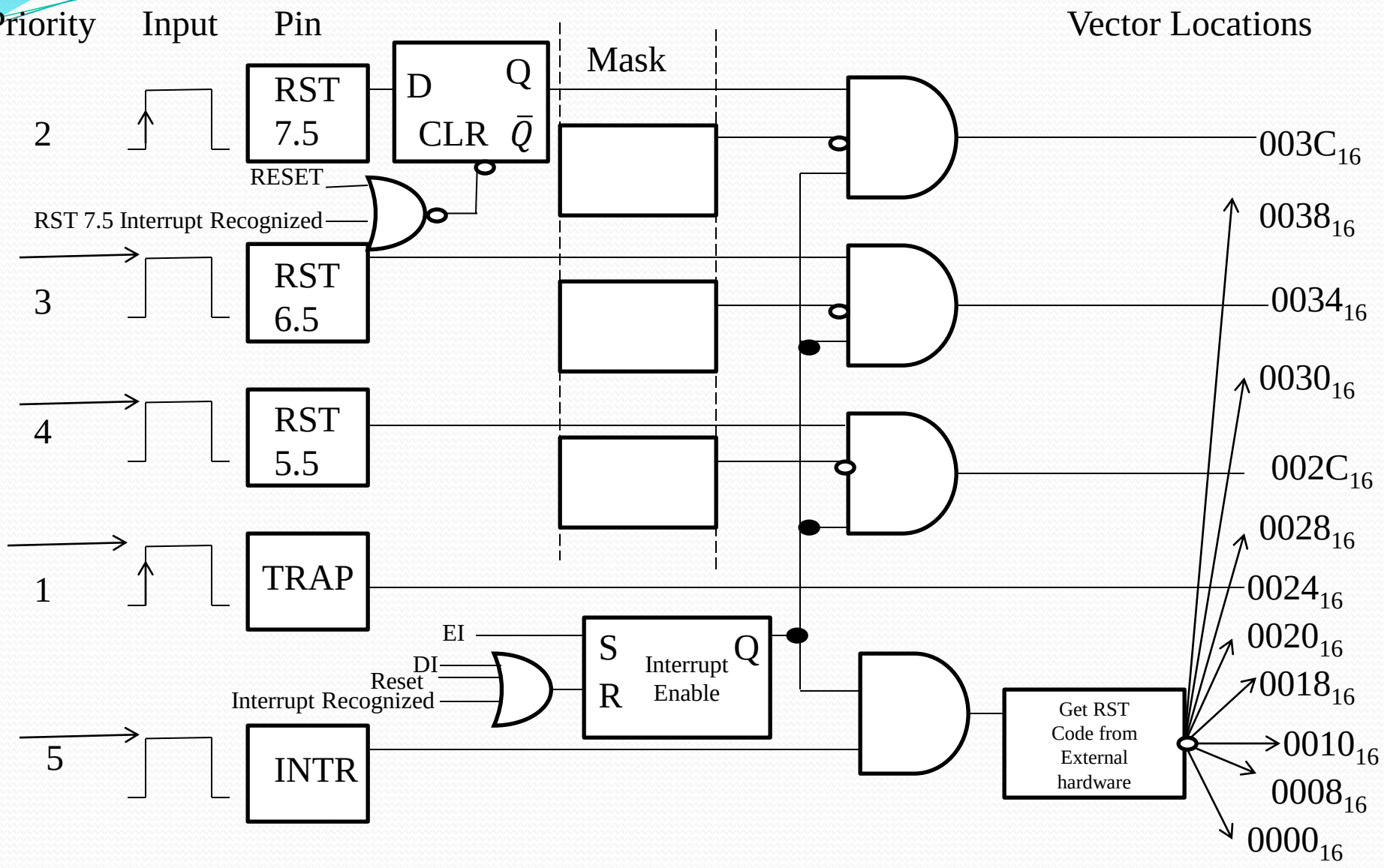
Interrupt	Call Location
TRAP	0024H
RST 7.5	003CH
RST 6.5	0034H
RST 5.5	002CH

- TRAP has highest priority among other interrupt but has lower priority than HOLD signal in DMA controller.

- EI instruction is used to enable the interrupt in the main program.
- DI instruction resets the interrupt enable flip-flop except the TRAP interrupt.

DI	Disable the interrupt enable flip-flop
RESET	
Interrupt recognized	

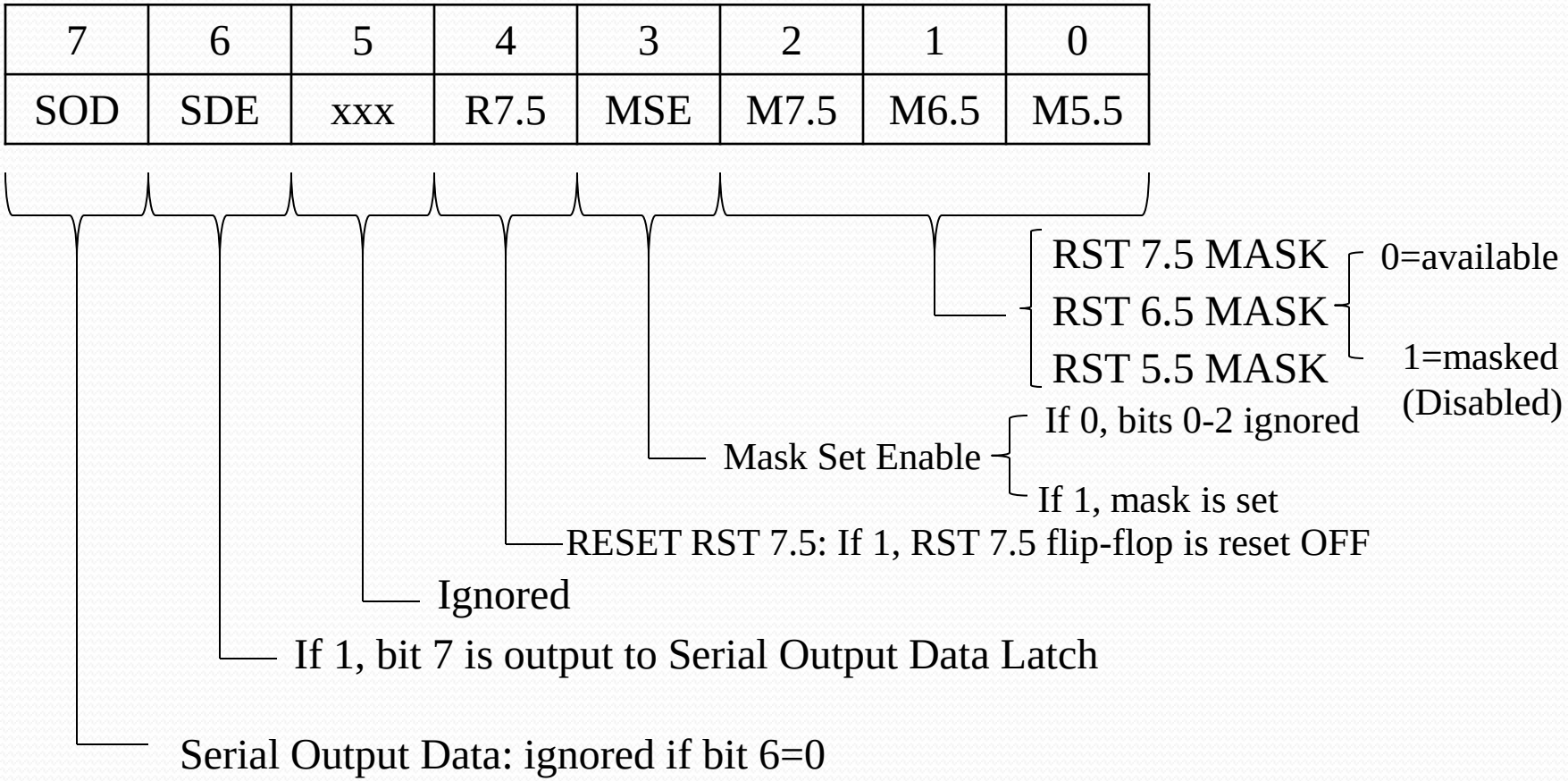
- Before the program returns back from ISS to the main program all the interrupts are enabled again using EI instruction before using the RET instruction.
- TRAP is a nonmaskable interrupt which cannot be enabled or disabled and is not accessible to user. It is used for emergency situation such as power failure and energy shut-off.



8085 Interrupts and Vector Locations

RST 7.5, 6.5, 5.5

- These are maskable interrupt and are enabled by software using the instruction
  - EI
  - SIM (Set Interrupt Mask)
- The execution of the instruction SIM enables/disables interrupt according to the bit pattern of the accumulator.



Interpretation of the Accumulator Bit Pattern for the SIM Instruction

- Write instructions to enable all the interrupts of Intel 8085.
- Write instructions to enable RST 6.5 and disable RST 7.5 and RST 5.5.
- WAP to interrupt Intel 8085 using RST 7.5.

Pending Interrupt

- When one interrupt is served by microprocessor, then other interrupt resulting in a pending request.
- The interrupt having highest priority is served first and remaining are left pending.
- In 8085 programmer uses the instruction RIM to know the current status of the pending interrupt.

Accumulator content after the execution of RIM