EXPERIMENT – 8

AIM

To study and design a 4-bit BCD adder.

PLATFORM/TOOL USED

- Simulator: https://circuitverse.org/simulator

THEORY

The digital systems handle the decimal number in the form of ***binary coded decimal numbers (BCD)***. A BCD Adder Circuit that adds two BCD digits and produces a sum digit also in BCD. BCD numbers use 10 digits, 0 to 9 which are represented in the binary form 0 0 0 0 to 1 0 0 1, i.e., each BCD digit is represented as a 4-bit binary number. When we write BCD number say 526, it can be represented as

5	2	6
↓	↓	↓
0 1 0 1	0 0 1 0	0 1 1 0

Suppose we have two 4-bit numbers A and B. The value of A and B can vary from 0(0000 in binary) to 9(1001 in binary) because we are considering decimal numbers.
The output will vary from 0 to 18 if we are not considering the carry from the previous sum. But if we are considering the carry, then the maximum value of output will be 19 (i.e., 9+9+1 = 19).

The BCD addition procedure as follows:

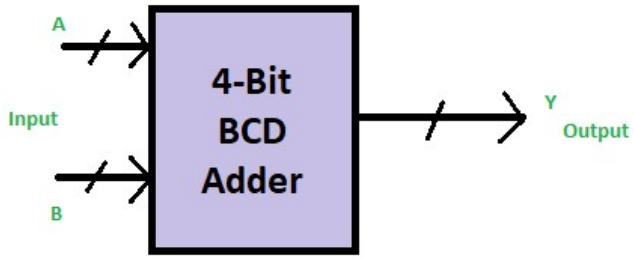
1. Add two BCD numbers using ordinary binary addition.
2. If four-bit sum is equal to or less than 9, no correction is needed. The sum is in proper BCD form.
3. If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.
4. To correct the invalid sum, add 01102 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

Thus, to implement BCD Adder Circuit we require:

- 4-bit binary adder for initial addition
- Logic circuit to detect sum greater than 9 and
- One more 4-bit adder to add 01102 in the sum if sum is greater than 9 or carry is 1.

The logic circuit to detect sum greater than 9 can be determined by simplifying the Boolean expression of given BCD Adder Truth Table.
The Logic Diagram and Truth Table of a 4-bit BCD Adder is given in the table.

Block Diagram for BCD Adder



Truth Table for BCD ADDER

Decimal	Binary Sum					BCD Sum				
	C'	S_3'	S_2'	S_1'	S_0'	C	S_3	S_2	S_1	S_0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	1	1	0
7	0	0	1	1	1	0	0	1	1	1
8	0	1	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	1	0	0	1
10	0	1	0	1	0	1	0	0	0	0
11	0	1	0	1	1	1	0	0	0	1
12	0	1	1	0	0	1	0	0	1	0
13	0	1	1	0	1	1	0	0	1	1
14	0	1	1	1	0	1	0	1	0	0
15	0	1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1	0	1	1	1
18	1	0	0	1	0	1	1	0	0	0
19	1	0	0	1	1	1	1	0	0	1

The K-map for the expression to check whether the BCD sum values greater than 9, up to decimal number 15 is given below:

K-Map for BCD Adder

For Y

I_3I_2 \ I_1I_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

$$Y = S_3S_2 + S_3S_1$$

For Binary sum values greater than 15, the carry bit is 1 (high), which updates the expression obtained to –

$$\boxed{Y = C' + S_3S_2 + S_3S_1}$$

The Boolean Expressions for the conditions detecting that the Binary Sum is greater than 9 to convert it to BCD by considering the carry bit as 1 in BCD representation for the ten's place BCD digit.

Boolean Expressions for BCD Adder

$$\boxed{S_3S_1 = 1d} \ (Condition\ 10 \text{ and } 11)$$

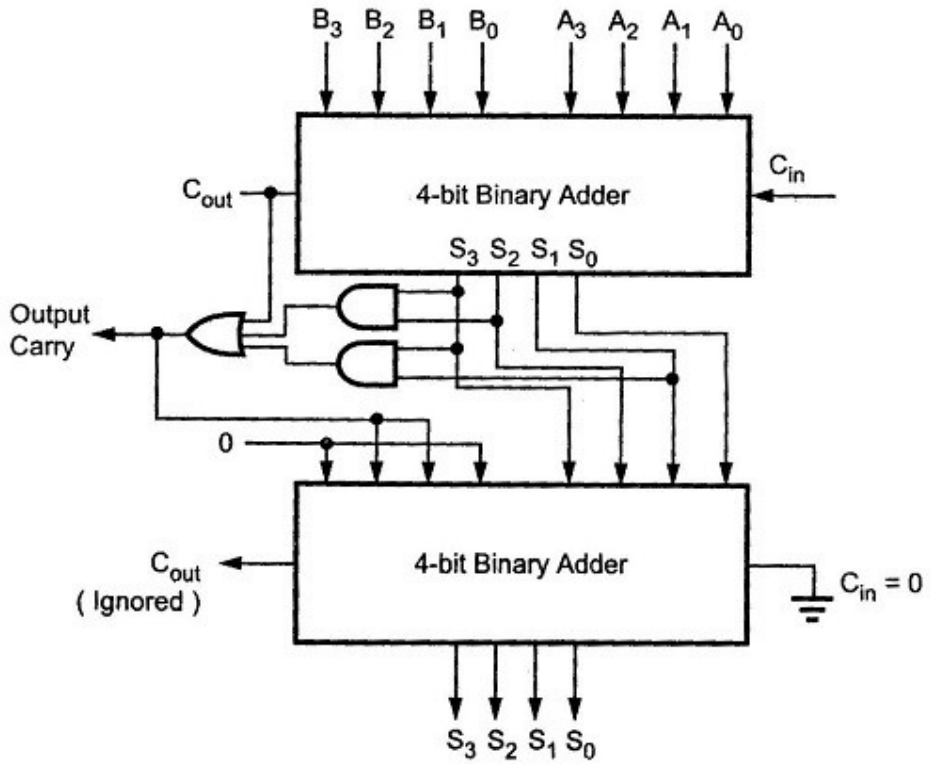
$$\boxed{S_3S_2 = 1} \ (Condition\ for\ 12 - 15)$$

$$\boxed{C' = 1} \ (Condition\ for\ 16 - 19)$$

Logic for the checking the INVALID SUM (greater than 9)

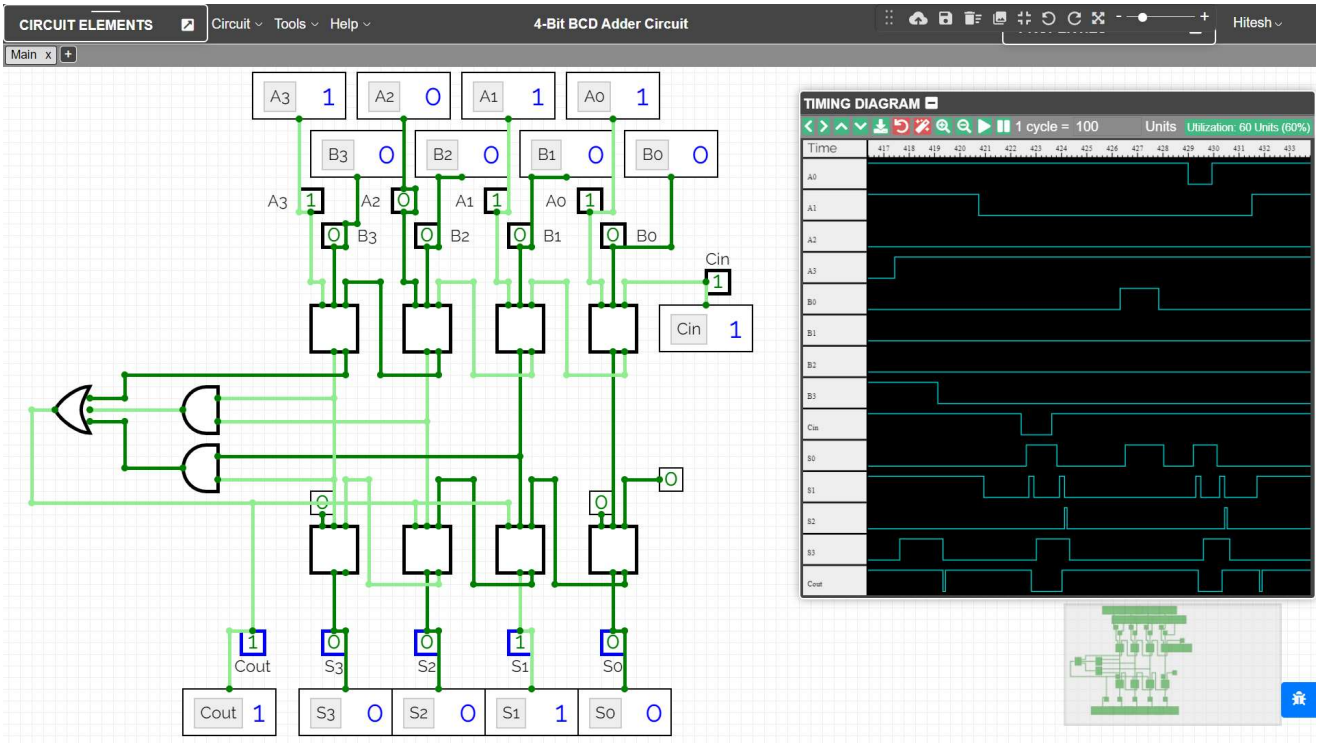
$$\boxed{Y = C' + S_3S_2 + S_3S_1}$$

Logic Diagram for BCD Adder



v

SIMULATED OUTPUT



RESULT

The Working of 4-bit Binary Coded Decimal (BCD) Adder combinational circuit have been analysed and the Truth Table and Boolean Expression of BCD Adder using Full Adders and OR & AND gates have been studied and verified using the online simulator.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		