# EXPERIMENT – 7

**AIM**

To design a 4-bit priority encoder.

**PLATFORM/TOOL USED**

- Simulator: https://circuitverse.org/simulator

**THEORY**

**Priority Encoder** is a combinational logic circuit for data transmission. It executes the priority function. The logic of the priority encoder is such that two or more inputs appear at an equal time, the input having the largest priority will take precedence.

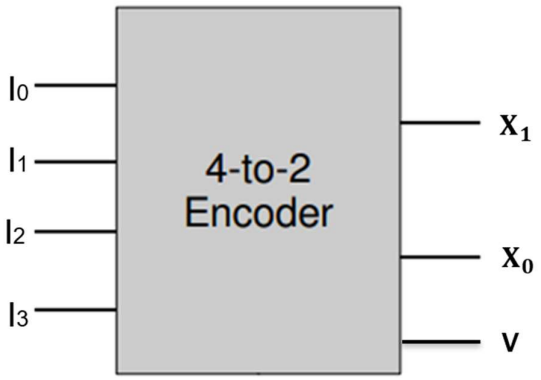
For instance, the 4-bit priority encoder is also referred to as 4- bit priority, which consists of 4 inputs and 2 output lines. Since an encoder contains 2^n input lines and n output lines. The third output is 'V', which is considered as a valid bit indicator, and it is set to 1 when more than one input line is high or active (1).

If the valid bit is equal to '0', then all the inputs are '0'. In this case, the other 2 output lines are considered as don't care conditions denoted by 'X'

- An encoder has 2n inputs, and n output lines. Only one input can be at logic 1 at any given time (active input). All other inputs must be 0's.
- If more than one input is active, the higher-order input has priority over the lower-order input. – The higher value is encoded on the output
- A valid indicator, V, is included to indicate whether the output is valid.
- Output is invalid when no inputs are active ● V = 0
- Output is valid when at least one input is active ● V = 1

The Logic Diagram and Truth Table of a four-input priority encoder is given in the table.

**Block Diagram for PRIORITY ENCODER**




**Truth Table for PRIORITY ENCODER**

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| $I_3$ | $I_2$ | $I_1$ | $I_0$ | $X_1$ | $X_0$ | V |
| 0 | 0 | 0 | 0 | × | × | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**K-Map for PRIORITY ENCODER**

**For $X_1$**

| $I_3I_2$ \ $I_1I_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| **00** | × | 0 | 0 | 0 |
| **01** | 1 | 1 | 1 | 1 |
| **11** | 1 | 1 | 1 | 1 |
| **10** | 1 | 1 | 1 | 1 |

$X_1 = I_2 + I_3$

**For $X_0$**

| $I_3I_2$ \ $I_1I_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| **00** | × | 0 | 1 | 1 |
| **01** | 0 | 0 | 0 | 0 |
| **11** | 1 | 1 | 1 | 1 |
| **10** | 1 | 1 | 1 | 1 |

$X_0 = I_3 + I_2'I_1$

**For V**

| $I_3I_2$ \ $I_1I_0$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| **00** | 0 | 1 | 1 | 1 |
| **01** | 1 | 1 | 1 | 1 |
| **11** | 1 | 1 | 1 | 1 |
| **10** | 1 | 1 | 1 | 1 |

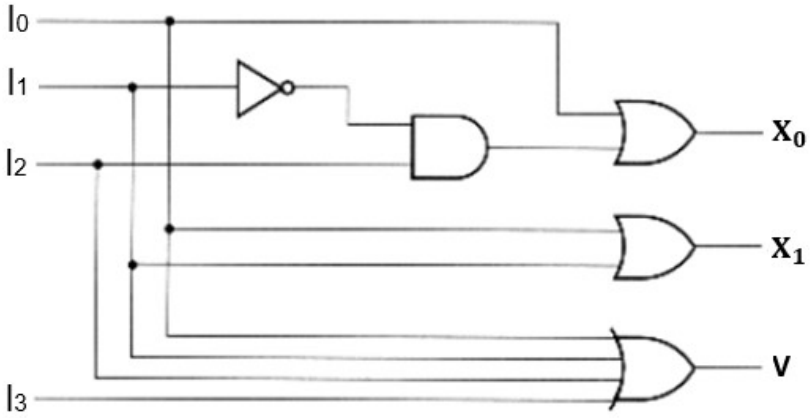
$V = I_0 + I_1 + I_2 + I_3$

**Boolean Expression for PRIORITY ENCODER**

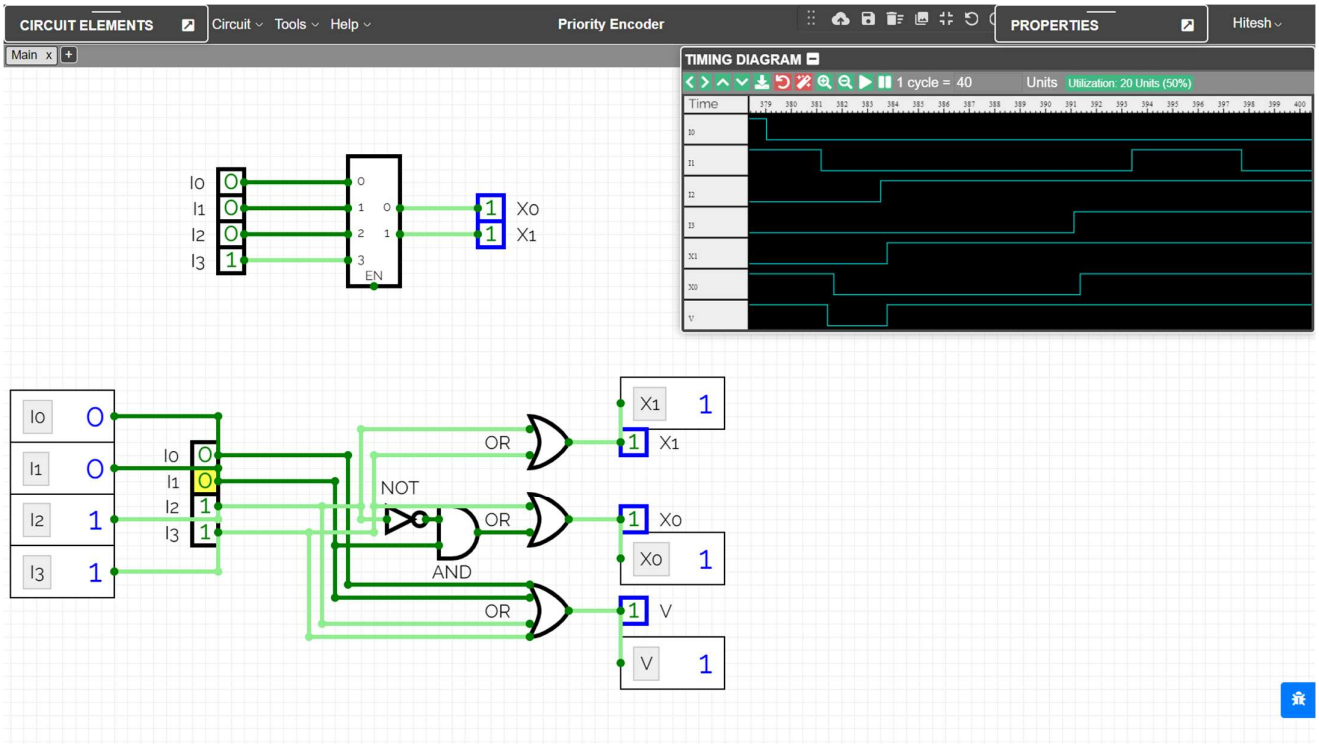
$\boxed{X_1 = I_2 + I_3}$ $\boxed{X_0 = I_3 + I_2'I_1}$

$\boxed{V = I_0 + I_1 + I_2 + I_3}$

**Logic Diagram for PRIORITY ENCODER**




**SIMULATED OUTPUT**




**RESULT**

The Working of Priority Encoder combinational circuit have been analysed and the Truth Table and Boolean Expression of Priority Encoder using NOT, OR & AND gates have been studied and verified using the online simulator.

| CRITERIA | TOTAL MARKS | MARKS OBTAINED | COMMENTS |
|---|---|---|---|
| Concept (A) | 2 | | |
| Implementation (B) | 2 | | |
| Performance (C) | 2 | | |
| Total | 6 | | |