# EXPERIMENT – 9

**AIM**

To study and design the 4-bit common bus system using Tri-State Buffer.

**PLATFORM/TOOL USED**

- Simulator: https://circuitverse.org/simulator

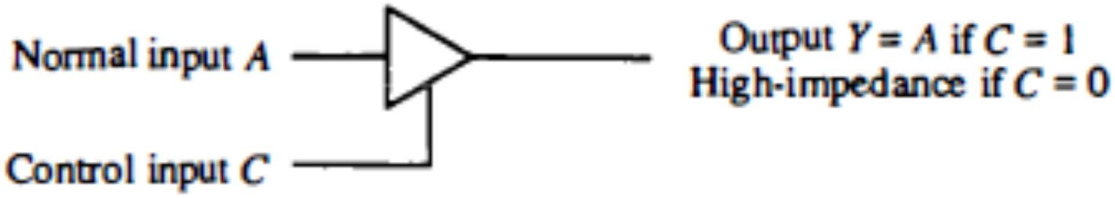
**THEORY**

A ***Tri-state Buffer*** can be thought of as an input-controlled switch with an output that can be electronically turned "ON" or "OFF" by means of an external "Control" or "Enable" (EN) signal input.

A three-state gate is a digital circuit which exhibits 3 states:

1. Logic 0
2. Logic 1
3. High impedance state (behaves like open circuit)

**Symbol for TRI-STATE Buffer**




Control input determines the output state.

**Truth Table for TRI-STATE Buffer**

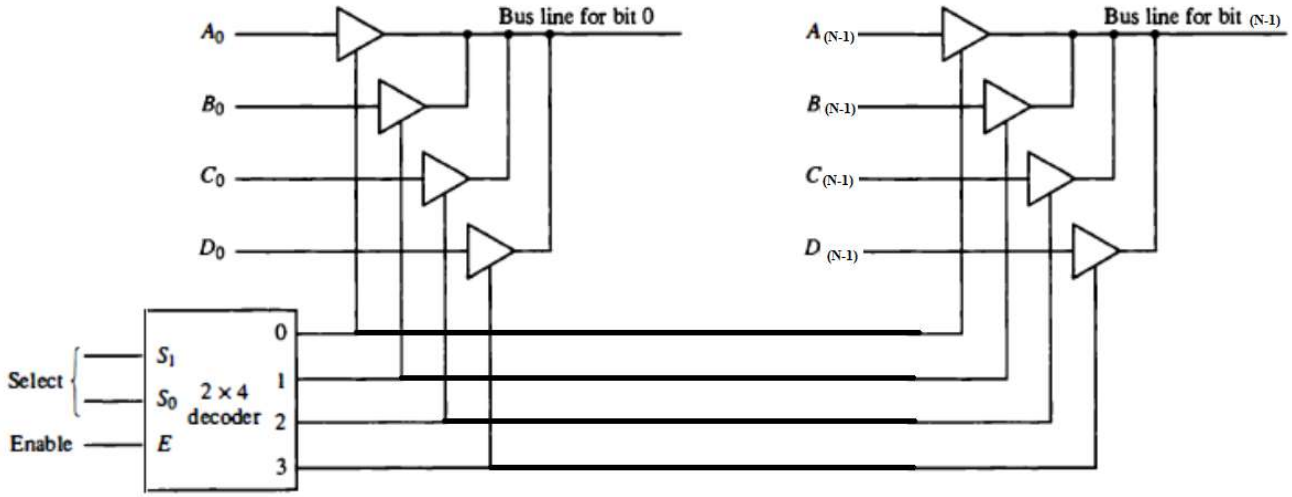
| EN | IN | OUT |
|---|---|---|
| 0 | X | Hi-Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

It may perform any type of conventional logic operations such as AND, OR, NAND, etc.

A typical computer has many registers, and the information is transferred between these registers. A way to transfer the information is using the common bus system.
A **Tri-state Bus Buffer** is an integrated circuit that connects multiple data sources to a single bus. The open drivers can be selected to be either a logical high, a logical low, or high impedance which allows other buffers to drive the bus.

The construction of such bus system for N registers is shown below for instance using *Tri-state Buffers*. The bus consists of Tri-state buffer having 1 input line, 1 control signal & 1 output line, and 4 registers with bits numbered 0 to 3. There are 2 select inputs S0 and S1 which are connected to the enable lines of the tri-state buffers.

**Logical Diagram for Common Bus using TRI-STATE BUFFER**




- The outputs of four buffers are connected to form a single bus line.
- The control inputs to the buffers determine which of the four normal inputs will communicate with the bus line.
- No more than one buffer may be in the active state at any given time.
- The connected buffers must be controlled so that only one three-state buffer has access to the bus line while all other buffers are maintained in a high impedance state.
- When the enable input of the decoder is 0, all its four outputs are 0, and the bus line is in a high-impedance state because all four buffers are disabled.
- When the enable input is active, one of the three-state buffers will be active, depending on the binary value in the select inputs of the decoder.

The output 1 of register A is connected to input of tri-state buffer bus line 1 and similarly other connections are made as shown in the diagram. The data transferred to the bus depends upon the select lines. A truth table for the various combinations of select lines is shown below.

**Truth Table for REGISTER Selection**

| Select Lines Combination | | Register Selected | Tri-state buffer line selected in each set of buffers connected to registers | Content transferred on 4-bit Common Bus |
|---|---|---|---|---|
| S1 | S0 | | | |
| 0 | 0 | Register A | 1st tri-state buffer line | $A_3A_2A_1A_0$ |
| 0 | 1 | Register B | 2nd tri-state buffer line | $B_3B_2B_1B_0$ |
| 1 | 0 | Register C | 3rd tri-state buffer line | $C_3C_2C_1C_0$ |
| 1 | 1 | Register D | 4th tri-state buffer line | $D_3D_2D_1D_0$ |

The transfer of information from some source register to a destination register is performed by transferring the content of the register to the bus and then the contents of the bus to a destination register. This can be accomplished by connecting the bus lines to the inputs of all destination registers and activating the load control of the desired destination register. The symbolic notation for this operation is shown as:

BUS <- C, R1 <- BUS
Or
R1 <- C

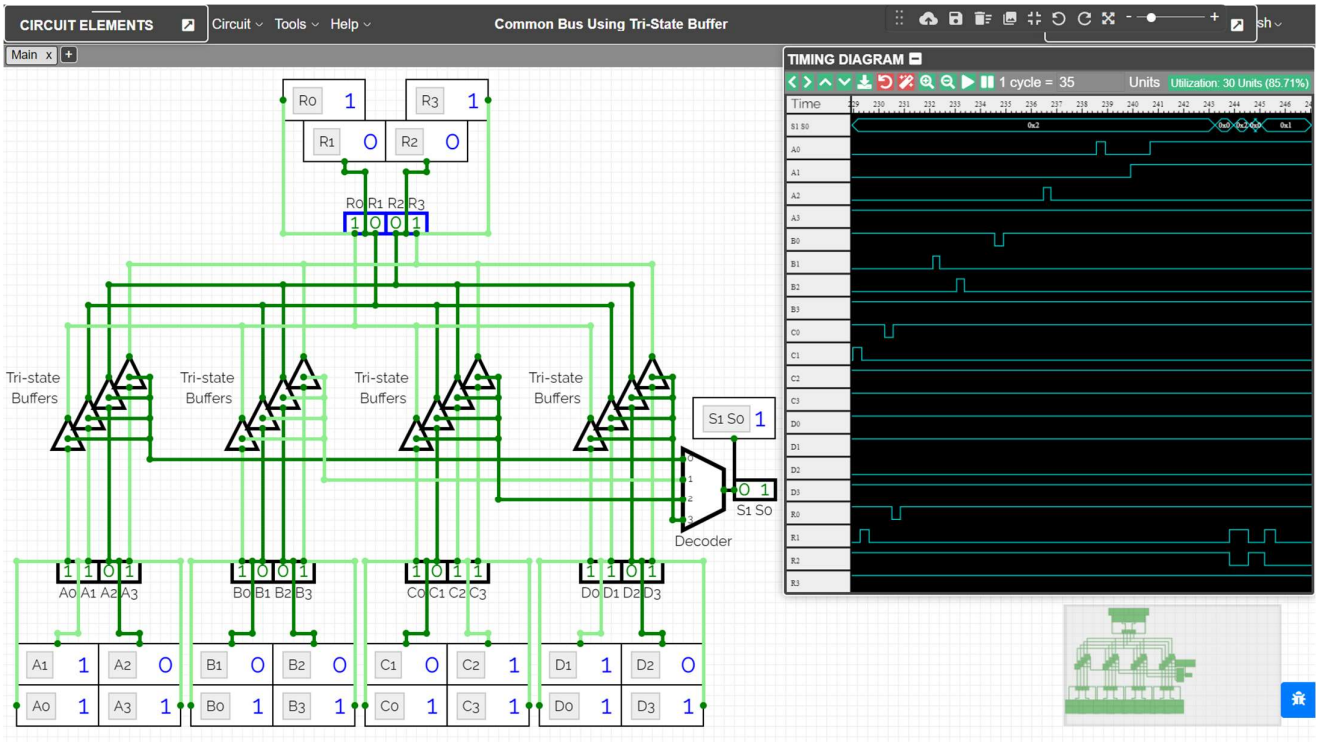
The number of tri-state buffers needed to construct the bus is equal to $(n \times k)$,

Where,

N → No. of bits in each register

K → No. of data lines it (or No. of Registers)

**SIMULATED OUTPUT**




**RESULT**

The combinational circuit 4-bit common bus system using Tri-state buffer have been implemented on the Online Simulator and its working has been studied and analysed.

| CRITERIA | TOTAL MARKS | MARKS OBTAINED | COMMENTS |
|---|---|---|---|
| Concept (A) | 2 | | |
| Implementation (B) | 2 | | |
| Performance (C) | 2 | | |
| Total | 6 | | |