B.TECH. (2020-24)
Artificial Intelligence

Lab File
(Experiment 3A & 3B)
on
DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION
[CSE207]

Submitted To
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EXPERIMENT – 3A

COMBINATIONAL CIRCUIT:

HALF SUBTRACTOR

EXPERIMENT – 3A

AIM

To study and design the single bit half subtractor combinational circuit for verifying and interpreting its logic and truth table and for analysing the working of half subtractor circuit by using the ICs of –

    (1) XOR, NOT and AND gates

    (2) NAND gates

PLATFORM/TOOL USED

➢ Simulator: https://circuitverse.org/simulator

➢ Virtual LAB: https://de-iitr.vlabs.ac.in/exp/half-full-subtractor/

THEORY

Subtractor is an electronic logic circuit for calculating the difference between two binary numbers which provides the difference and borrow as output.
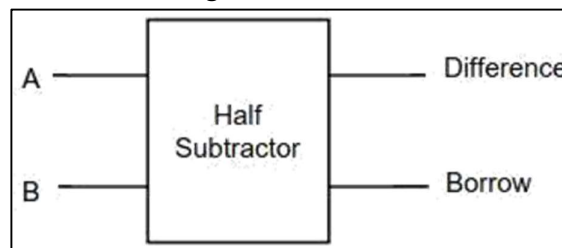
    Subtractor circuits take two binary numbers as input and subtract one binary number input from the other binary number input. Like adders, it gives out two outputs, difference and borrow (carry-in the case of Adder). There are two types of subtractors.

- Half Subtractor
- Full Subtractor

Half Subtractor

❖ The **Half Subtractor** is a combinational circuit which is used to perform subtraction of two bits.

❖ It has two inputs, A (minuend) and B (subtrahend) and two outputs Difference and Borrow.

❖ The logic symbol and truth table are shown below.

Block Diagram for HALF SUBTRACTOR

Truth Table for HALF SUBTRACTOR

INPUT		OUTPUT	
A	**B**	**Difference**	**Borrow**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-Map for HALF SUBTRACTOR

For DIFFERENCE

B A	0	1
0	0	(1)
1	(1)	0

$$Difference\ =\ AB' + A'B$$
$$Difference = A \oplus B$$

For BORROW

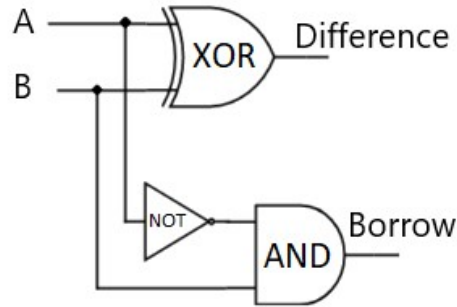| B A	0	1
0	0	(1)
1	0	0

$$Borrow\ =\ \bar{A}B$$

Boolean Expression for HALF SUBTRACTOR

$$Difference = AB' + A'B = A \oplus B \qquad Borrow = \bar{A}B$$
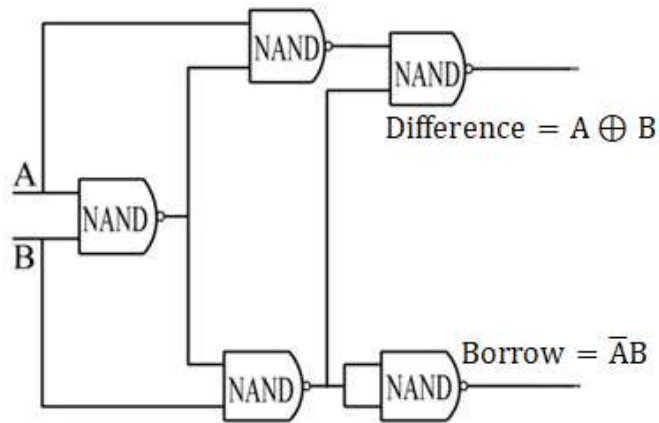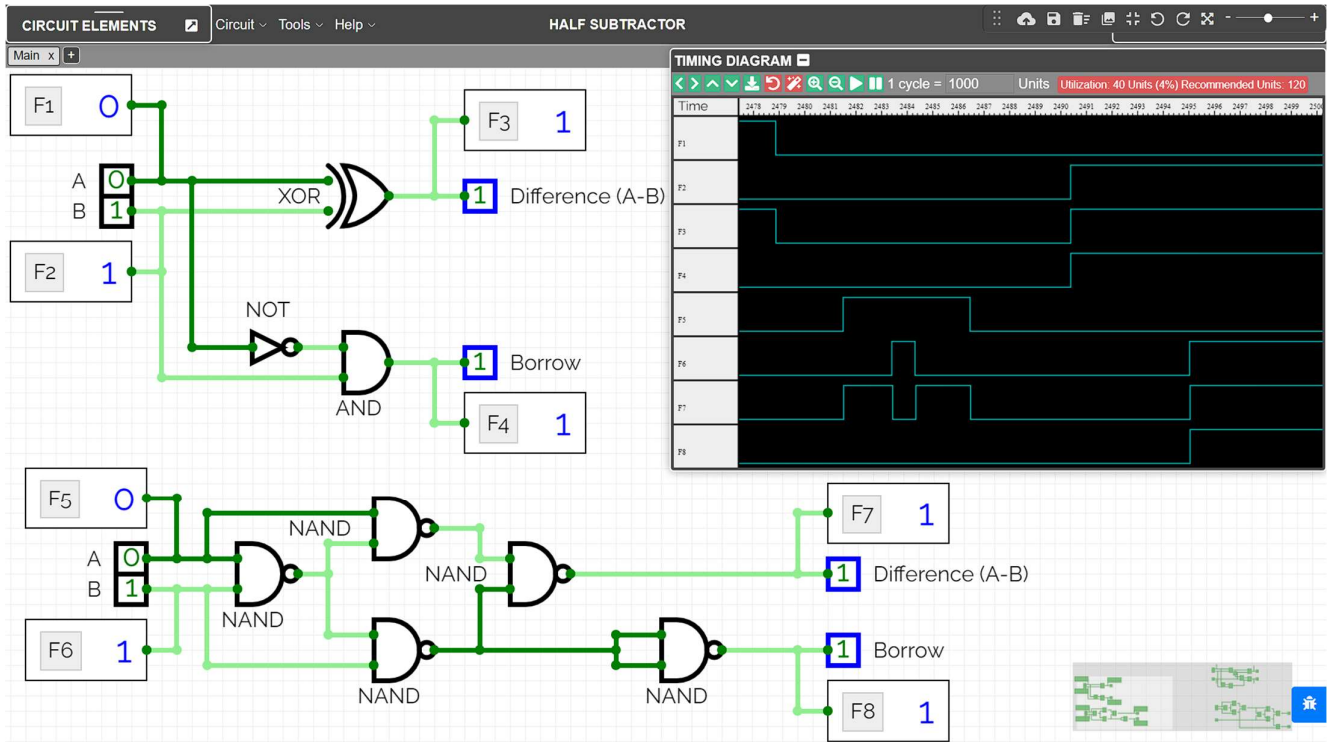
Logic Diagram for HALF SUBTRACTOR

❖ Five NAND gates are required to design a half subtractor.

Realization of Half Subtractor using 5 NAND gates

$$Difference = A \oplus B$$

$$Borrow = \bar{A}B$$

SIMULATED OUTPUT

RESULT

The Working of Half Subtractor combinational circuit have been analysed and the Truth Table and Boolean Expression of half subtractor using XOR, NOT & AND gates, and NAND gates have been studied and verified using the online simulator.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		

EXPERIMENT – 3B

COMBINATIONAL CIRCUIT:

FULL SUBTRACTOR

EXPERIMENT – 3B

AIM

To study and design the single bit full subtractor combinational circuit for verifying and interpreting its logic and truth table and for analysing the working of half subtractor circuit by using the ICs of –

     (1) XOR, AND, NOT and OR gates

     (2) NAND gates

PLATFORM/TOOL USED

➤ Simulator: https://circuitverse.org/simulator

➤ Virtual LAB: https://de-iitr.vlabs.ac.in/exp/half-full-subtractor/

THEORY

Subtractor is an electronic logic circuit for calculating the difference between two binary numbers which provides the difference and borrow as output.
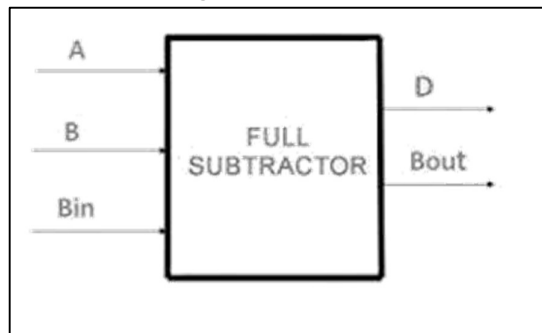
     Subtractor circuits take two binary numbers as input and subtract one binary number input from the other binary number input. Like adders, it gives out two outputs, difference and borrow (carry-in the case of Adder). There are two types of subtractors.

- Half Subtractor
- Full Subtractor

Full Subtractor

❖ A **Full Subtractor** is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend, considering 1 may be borrowed from the previous adjacent lower significant bit.

❖ It accepts three inputs: A (minuend), B (subtrahend) and a Bin (borrow bit) and it produces two outputs: D (difference) and Bout (borrow out).

❖ The logic symbol and truth table are shown below.

Block Diagram for FULL SUBTRACTOR

Truth Table for FULL SUBTRACTOR

INPUT			OUTPUT	
A	**B**	**B$_{IN}$**	**DIFFERENCE**	**B$_{OUT}$**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for FULL SUBTRACTOR

For Difference

BC_{IN} / A	00	01	11	10
0	0	(1)	0	(1)
1	(1)	0	(1)	0

$$Difference = A'B'B_{in} + A'BB'_{in} + AB'B'_{in} + ABB_{in}$$
$$Difference = A \oplus B \oplus B_{IN}$$

For Borrow_{out}

BC_{IN} / A	00	01	11	10
0	0	1	1	1
1	0	0	1	0

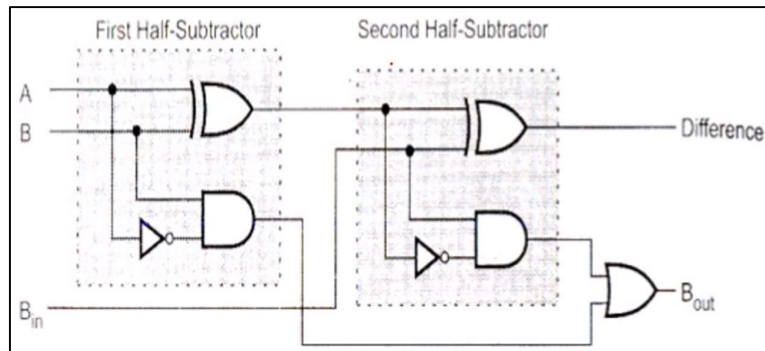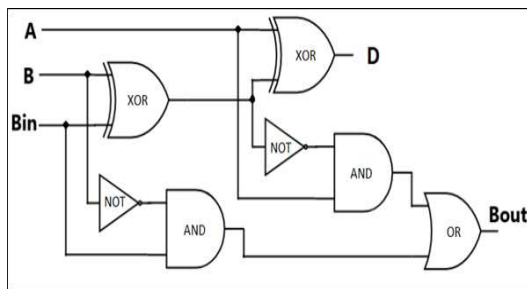$$B_{out} = \bar{A}B + \bar{A}B_{in} + BB_{in}$$
$$B_{out} = \bar{A}B + B_{in}\overline{(A \oplus B)}$$

Boolean Expression for FULL SUBTRACTOR

$$Difference = A'B'B_{in} + A'BB'_{in} + AB'B'_{in} + ABB_{in} = A \oplus B \oplus B_{IN}$$

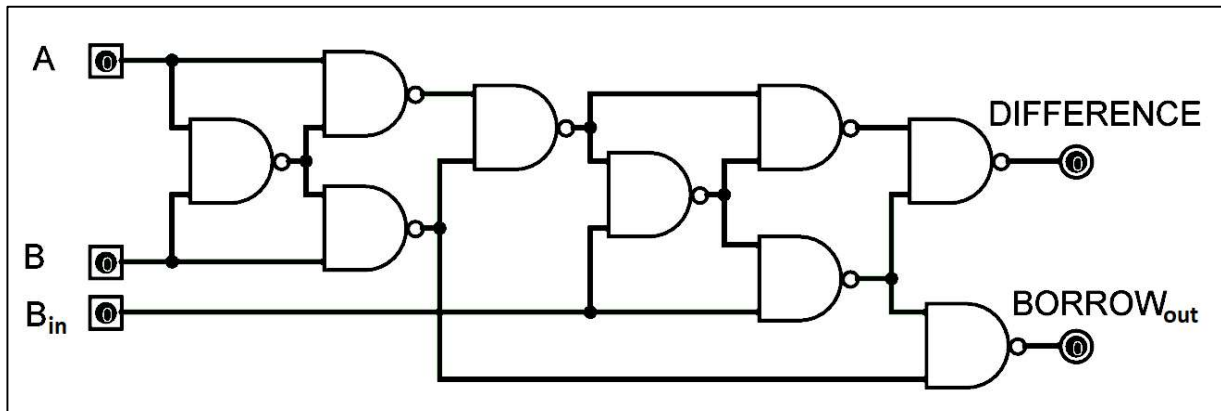$$B_{out} = \bar{A}B + \bar{A}B_{in} + BB_{in} = \bar{A}B + B_{in}\overline{(A \oplus B)}$$

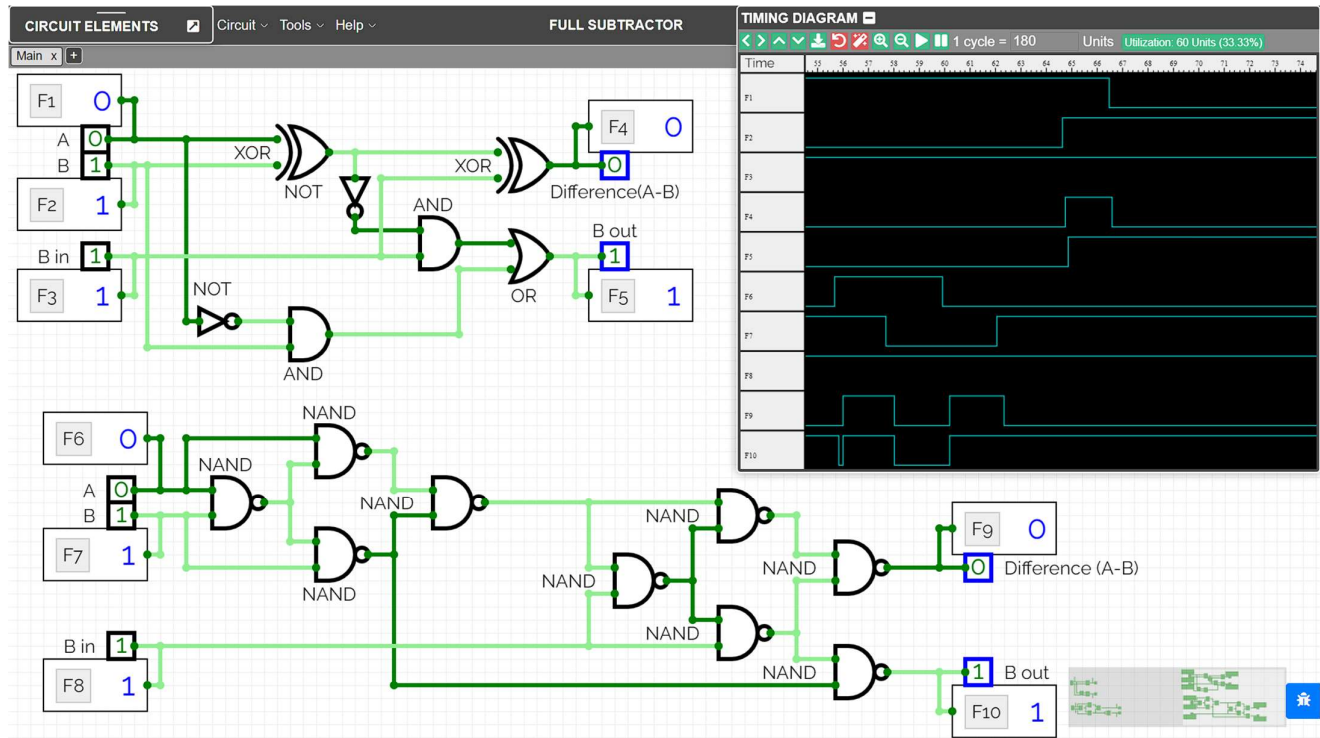## Logic Diagram for FULL SUBTRACTOR

❖ Nine NAND gates are required to design a full subtractor.

Realization of FULL SUBTRACTOR using 9 NAND gates

SIMULATED OUTPUT

RESULT

The Working of Full Subtractor combinational circuit have been analysed and the Truth Table and Boolean Expression of full subtractor using XOR, NOT,OR & AND gates, and NAND gates have been studied and verified using the online simulator.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		