EXPERIMENT – 6

AIM

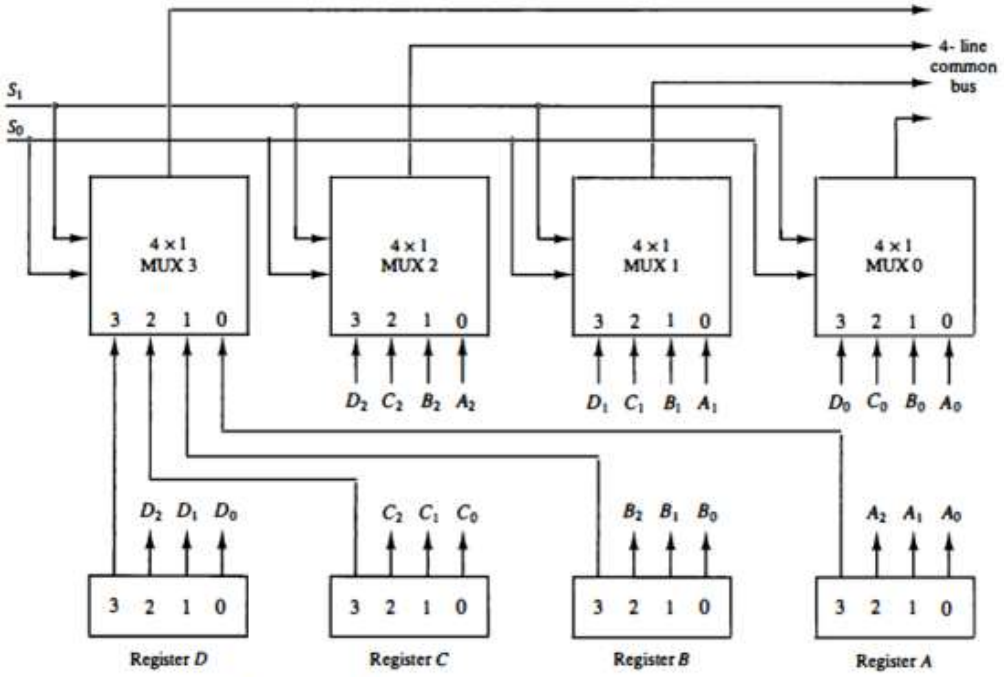
To design and simulate 5-bit common bus system using multiplexers.

PLATFORM/TOOL USED

- Simulator: https://circuitverse.org/simulator

THEORY

A typical computer has many registers, and the information is transferred between these registers. A way to transfer the information is using the common bus system.



A bus system for transfer of contents of four registers

The construction of such bus system for 4 registers is shown above. The bus consists of 4×1 multiplexers with 4 inputs and 1 output and 4 registers with bits numbered 0 to 3. There are 2 select inputs S0 and S1 which are connected to the select inputs of the multiplexers.

The output 1 of register A is connected to input 0 of MUX 1 and similarly other connections are made as shown in the diagram. The data transferred to the bus depends upon the select lines. A table for the various combinations of select lines is shown below.

Truth Table for REGISTER Selection

Select Lines Combination			Register Selected	MUX line selected in all MUXes	Content transferred on 5-bit Common Bus
S2	S1	S0			
0	0	0	Register A	1st input of all MUX	$A_4A_3A_2A_1A_0$
0	0	1	Register B	2nd input of all MUX	$B_4B_3B_2B_1B_0$
0	1	0	Register C	3RD input of all MUX	$C_4C_3C_2C_1C_0$
0	1	1	Register D	4TH input of all MUX	$D_4D_3D_2D_1D_0$
1	0	0	Register E	5TH input of all MUX	$E_4E_3E_2E_1E_0$

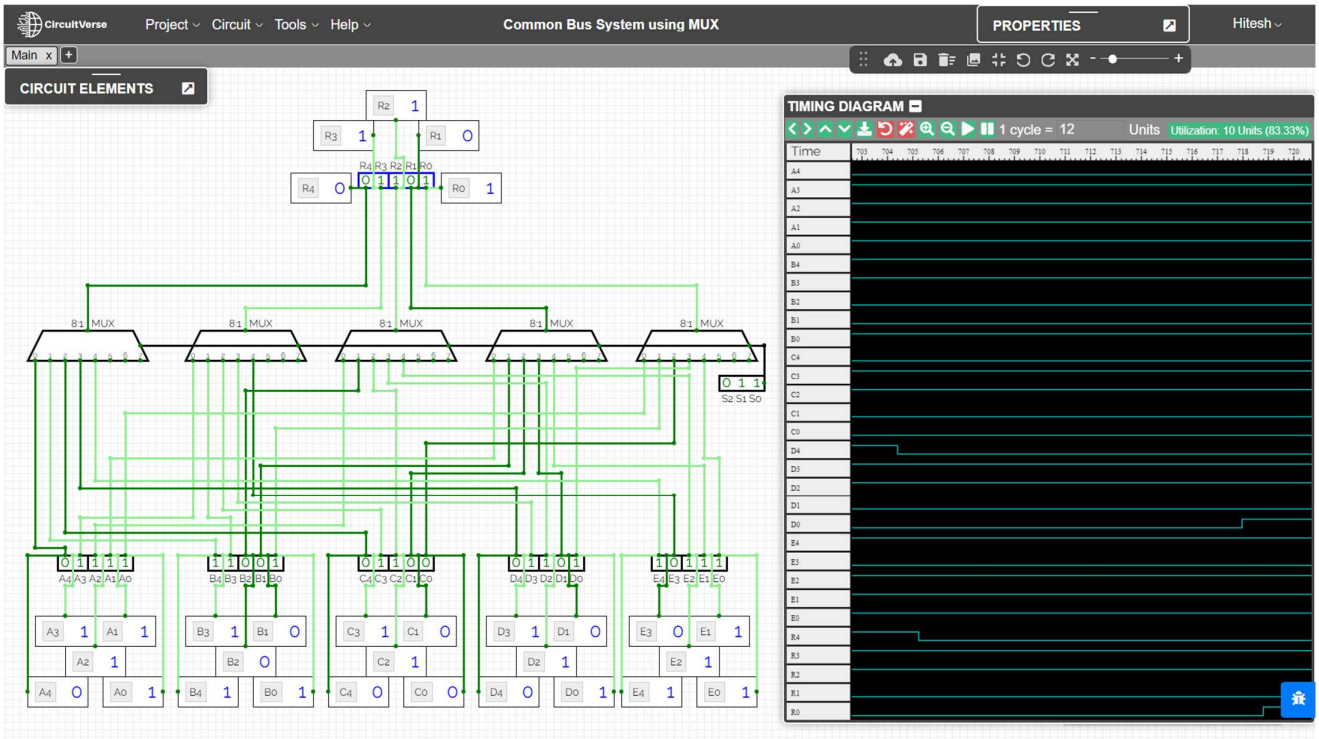
The transfer of information from some source register to a destination register is performed by transferring the content of the register to the bus and then the contents of the bus to a destination register. This can be accomplished by connecting the bus lines to the inputs of all destination registers and activating the load control of the desired destination register. The symbolic notation for this operation is shown as:

BUS <- C, R1 <- BUS
Or
R1 <- C

The number of multiplexers needed to construct the bus is equal to n, the number of bits in each register. The size of each multiplexer must be $(k \times 1)$ since it multiplexes k data lines (or simply the no. of registers)

- No. of MUX = No. of bits in each register
- Size of MUX = No. of data lines it multiplexes (or No. of Registers)

SIMULATED OUTPUT



RESULT

The combinational circuit 5-bit common bus system using multiplexers have been implemented on the Online Simulator and its working has been studied and analysed.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		