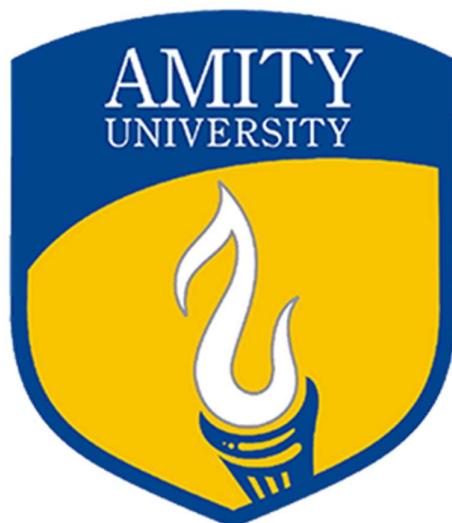


B.TECH. (2020-24)
Artificial Intelligence

Lab File
(Experiment 4)
on
DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION
[CSE207]



Submitted To
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EXPERIMENT – 4

COMBINATIONAL CIRCUIT:

PARALLEL ADDER SUBTRACTOR

EXPERIMENT – 4

AIM

To study and design the 4-bit Parallel Adder & Subtractor combinational circuit for verifying and analysing the working of parallel adder subtractor circuit by using the full adders.

PLATFORM/TOOL USED

- Simulator: <https://circuitverse.org/simulator>

THEORY

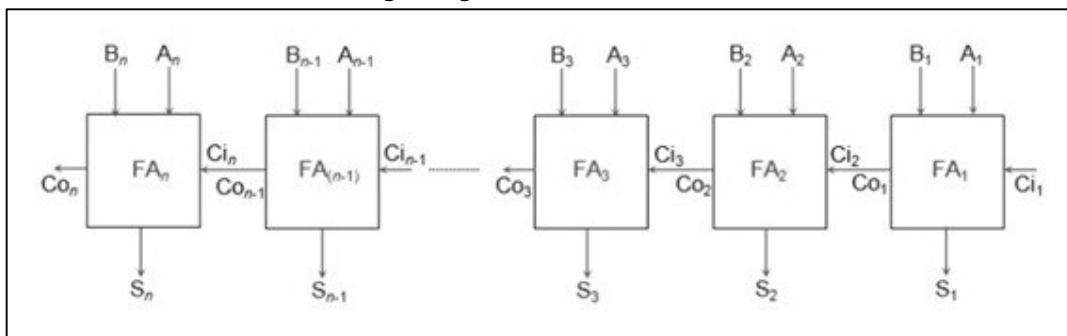
Additions and subtractions are fundamental operations in a digital system, control system & digital signal processing. These systems are influenced by the adders and subtractors by providing accurate as well as fast operations. Adders and subtractors play an essential role in digital systems due to their wide usage in other digital operations like multiplication, subtraction & division. Therefore, improving the performance of these will progress the execution of binary operations within a circuit.

Parallel Adder

- A single Full Adder performs the addition of two one-bit numbers and an input carry.
- But a **Parallel Adder** is a digital circuit capable of finding the arithmetic sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel.
- It consists of full adders connected in a chain where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain. A n-bit parallel adder requires n full adders to perform the operation. So, for the two-bit number, two adders are needed while for four-bit number, four adders are needed and so on. Parallel adders normally incorporate carry lookahead logic to ensure that carry propagation between subsequent stages of addition does not limit addition speed.

In modern Integrated Circuits, the most basic and widely used component are Binary Adders. Adder circuit is classified as Half Adder and Full Adder. The Adder circuit is expected to compute fast, occupy less space, and minimize delay. Hence Parallel Adders were implemented with the help of Full Adder circuits.

Logic Diagram for Parallel Adder



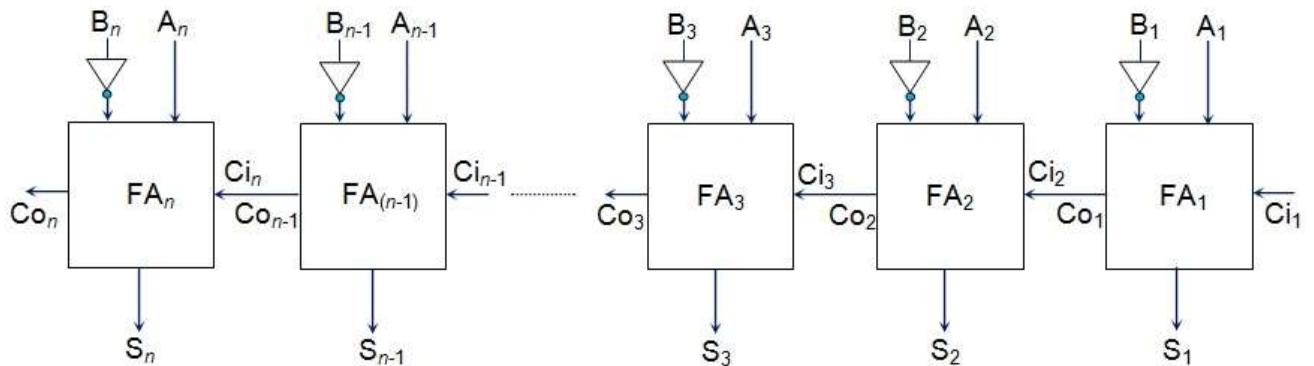
Working of parallel Adder –

1. Firstly, the full adder FA₁ adds A₁ and B₁ along with the carry C₁₁ to generate the sum S₁ (the first bit of the output sum) and the carry C_{o1} which is connected to the next adder in chain.
2. Next, the full adder FA₂ uses this carry bit C_{i2} to add with the input bits A₂ and B₂ to generate the sum S₂ (the second bit of the output sum) and the carry C_{o2} which is again further connected to the next adder in chain and so on.
3. The process continues till the last full adder FA_n uses the carry bit C_n to add with its input An and Bn to generate the last bit of the output along last carry bit C_{out}.

Parallel Subtractor

A Parallel Subtractor is a digital circuit capable of finding the arithmetic difference of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. The parallel subtractor can be designed in several ways including combination of half and full subtractors, all full subtractors or all full adders with subtrahend complement input.

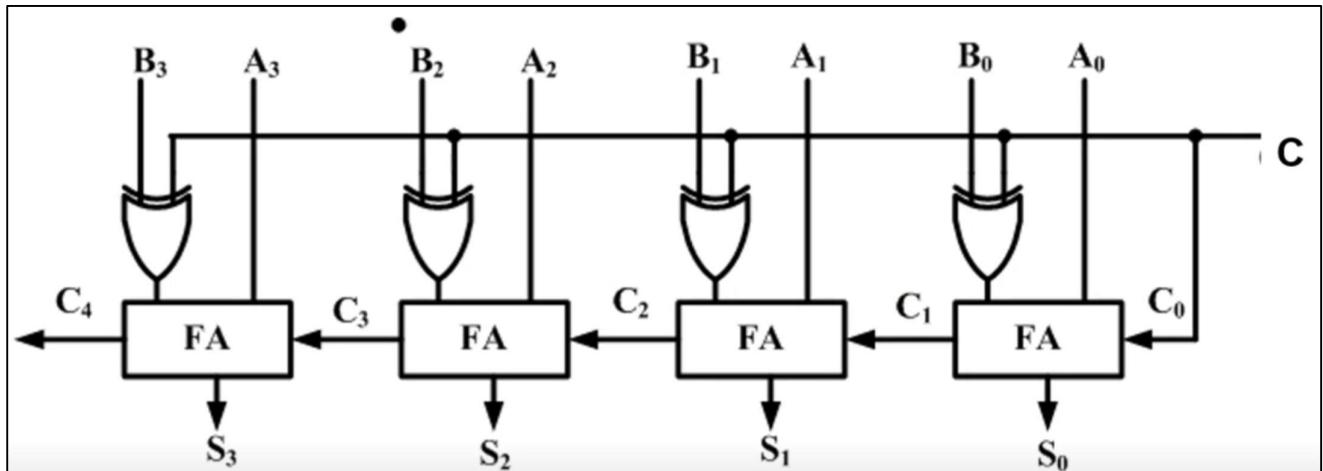
Logic Diagram for Parallel Subtractor



Working of Parallel Subtractor –

1. The parallel binary subtractor is formed by combination of all full adders with subtrahend complement input.
2. This operation considers that the addition of minuend along with the 2's complement of the subtrahend is equal to their subtraction.
3. Firstly the 1's complement of B is obtained by the NOT gate and 1 can be added through the carry to find out the 2's complement of B. This is further added to A to carry out the arithmetic subtraction.
4. The process continues till the last full adder FA_n uses the carry bit C_n to add with its input A_n and 2's complement of B_n to generate the last bit of the output along last carry bit C_{out}.

Realization of PARALLEL ADDER SUBTRACTOR in a single Combinational Circuit



Here, the combinational logic circuit of Parallel Adder Subtractor is shown where there are following modes:

- 1) Set C = 0 for ADDITION
- 2) Set C = 1 for SUBTRACTION

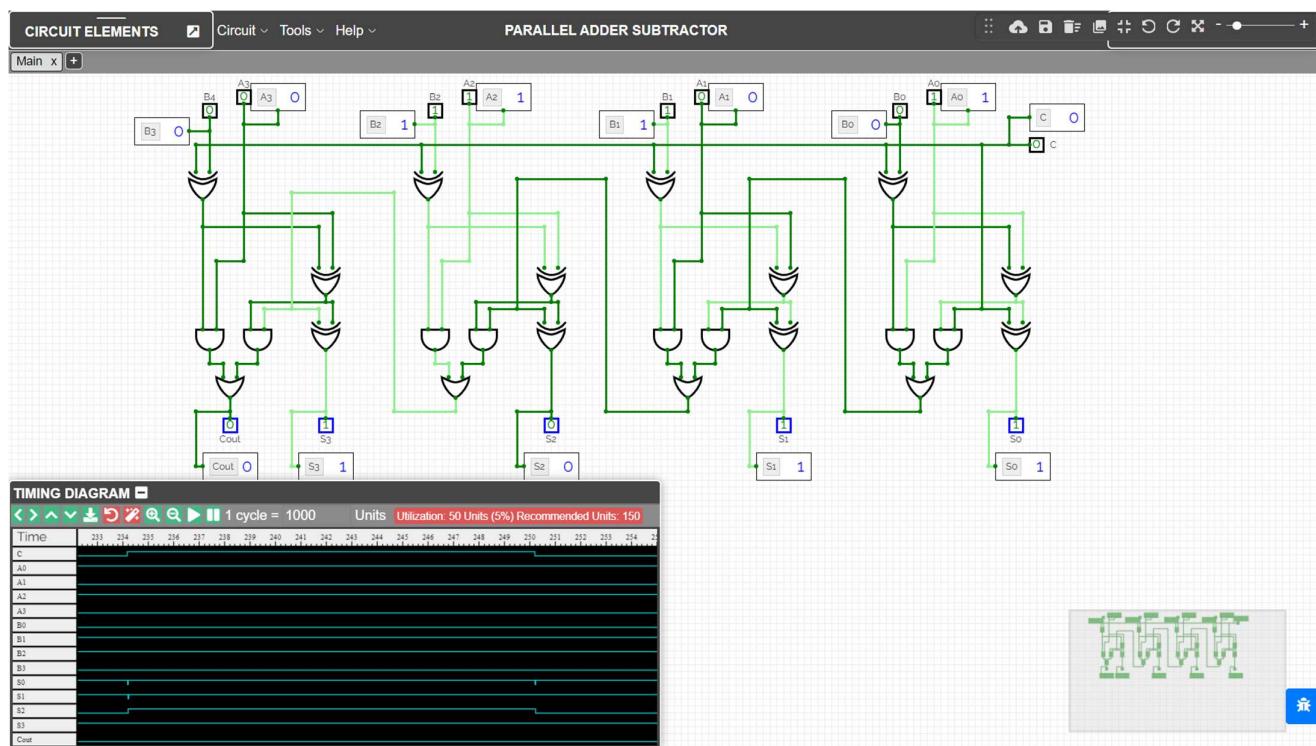
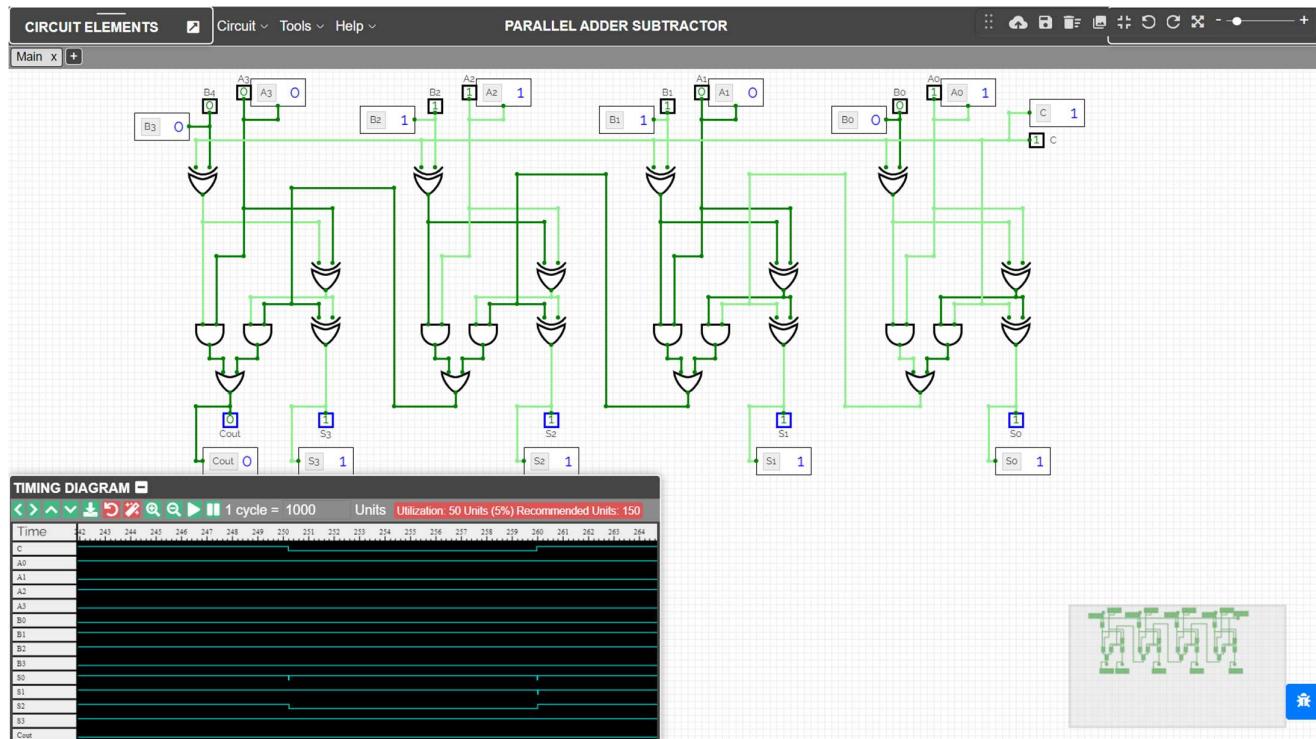
Advantages of parallel Adder/Subtractor –

1. The parallel adder/subtractor performs the addition operation faster as compared to serial adder/subtractor.
2. Time required for addition does not depend on the number of bits.
3. The output is in parallel form i.e., all the bits are added/subtracted at the same time.
4. It is less costly.

Disadvantages of Parallel Adder/Subtractor

The major drawback of Parallel Adder/Subtractor is the Propagation Delay. The delay is directly proportional to the length of binary numbers that are to be added.

SIMULATED OUTPUT



RESULT

The combinational circuits of Parallel Adder & Subtractor have been implemented on the Online Simulator and its working has been studied and analysed using full adders.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		