EXPERIMENT – 5

AIM

To study and design the Logical part Arithmetic Logic Unit ALU using:

1) MUX
2) Decoder

PLATFORM/TOOL USED

- Simulator: https://circuitverse.org/simulator

THEORY

In Digital electronics, an Arithmetic Logic Unit (ALU) is a combinational digital circuit that performs arithmetic and bitwise operations on binary digital signals.

The ALU is a component which can carry out a range of calculations on its inputs, including various standard arithmetic and logic operations. The choice of operation is made by setting control inputs appropriately; ultimately, the control inputs are determined by the instruction which the CPU is executing at any given time. We'll go further into this idea later in the course.

ALU is also known as an integer unit (IU) that is an integrated circuit within a CPU or GPU, which is the last component to perform calculations in the processor. It can perform all processes related to arithmetic and logic operations such as addition, subtraction, and shifting operations, including Boolean comparisons (XOR, OR, AND, and NOT operations). Also, binary numbers can accomplish mathematical and bitwise operations. The arithmetic logic unit is split into AU (arithmetic unit) and LU (logic unit).

The logic unit can perform the logical operations such as AND, OR, NOT, XOR, NOR, NAND, etc.

The combinational circuit of Logic Unit can be implemented using:

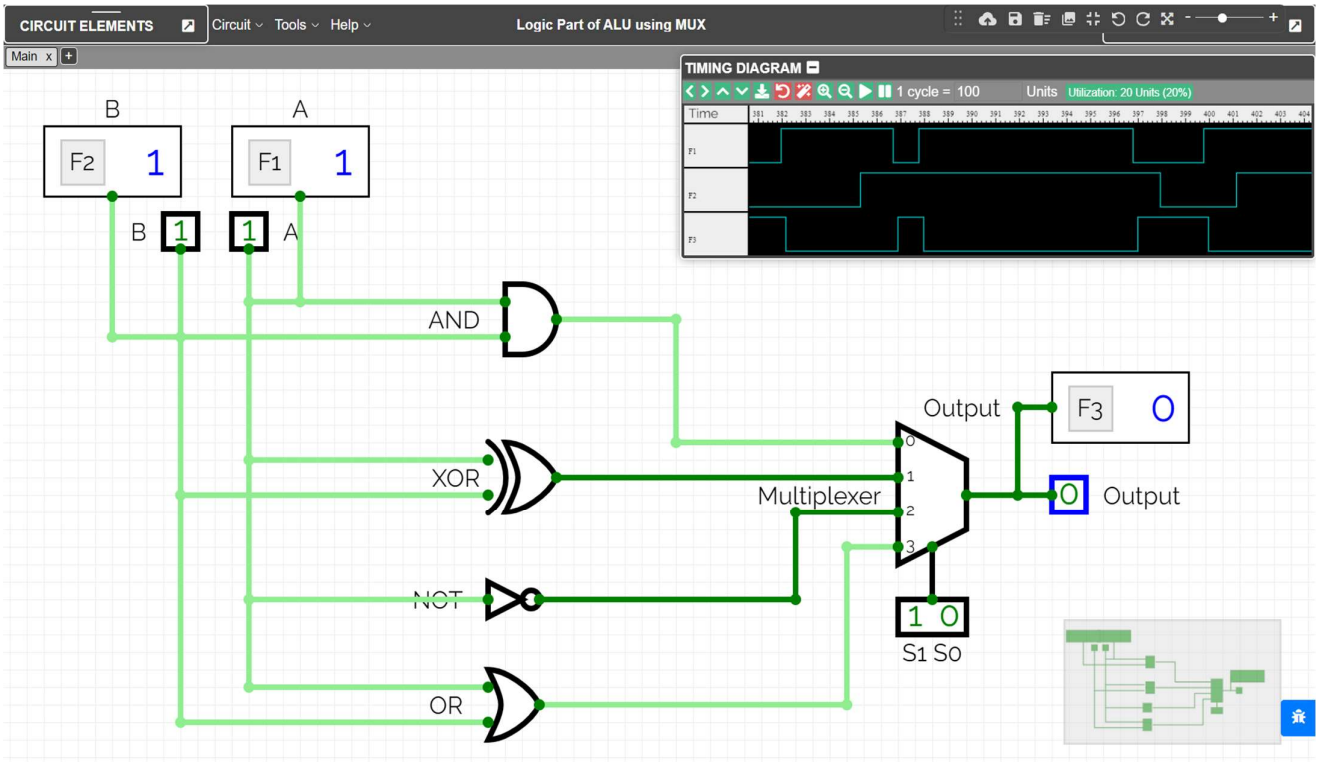
1) Multiplexer
   - The size of MUX is defined as such where the no. of input lines is same as the no. of logical operations to be performed.
   - Each input line will be connected with the respective logic gate for logical operation.
   - And the no. of select lines will be evaluated from the no. of input lines using formula 2^n, for instance, no. of inputs = 4, then no. of select lines = n = 2 since $2^2 = 4$.

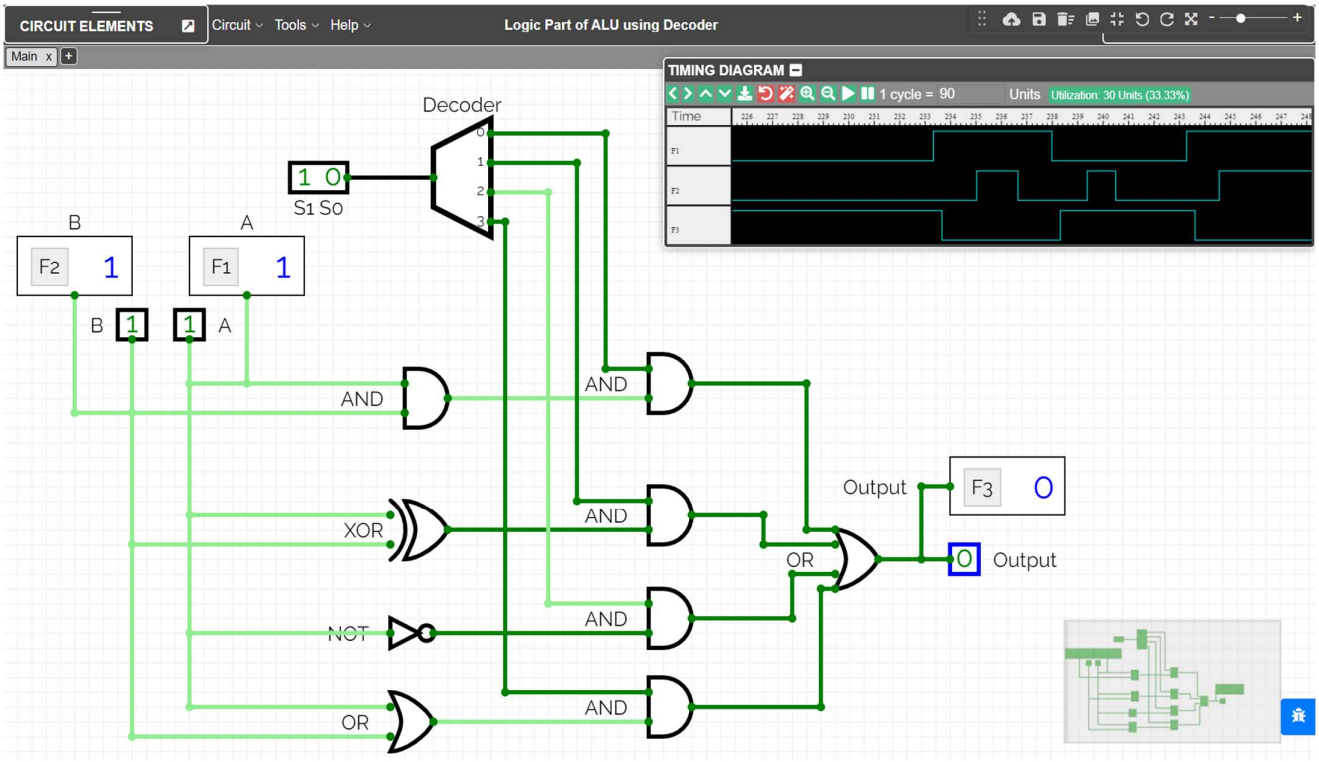
2) Decoder
   - The size of decoder will be described with the help of no. of logical operations that is same as 2^n which will be taken as the no. of output lines.
   - Each output line connected with an AND gate that is also joined with the output of logical operation given by the respective logic gate.
   - The no. of input lines can be found using formula 2^n, i.e., equal to no. of output lines where n = the no. of input lines.

Truth Table for LOGICAL Operation Selection

S_1	S_0	Logical Operation OUTPUT
0	0	AND
0	1	XOR
1	0	NOT
1	1	OR

SIMULATED OUTPUT





RESULT

The combinational circuits of the Logical Part of ALU using MUX and Decoder have been implemented on the Online Simulator and its working has been studied and analysed.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		