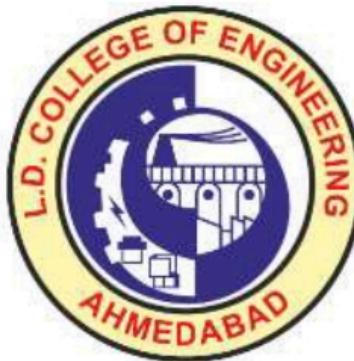




Laboratory Experiments

Back-End Design

VLSI Design (3151105)



Department of Electronics & Communication Engineering

Name: SIDDHARTH GOHIL

Enrollment No: 200280111012

Semester: 5th Div – A

Term Date: 26th July - 1st December, 2022

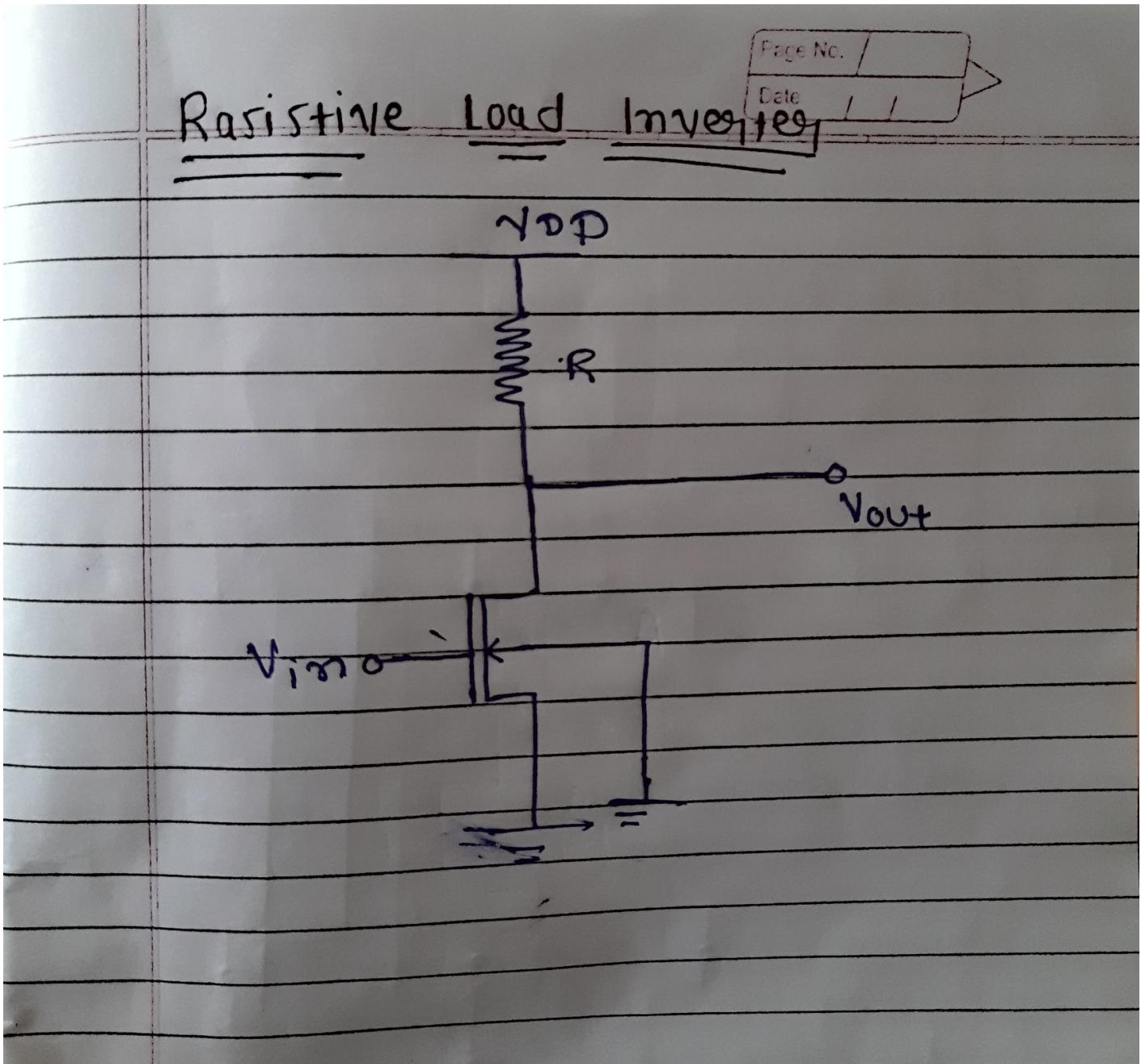
List of Experiments

Sr. No.	Title of the Experiment	Date	Sign
1	Introduction to Back-end Design Tool - Microwind.		
2	Draw layouts of Resistive Load Inverter with different values of load resistances of $10\text{ K}\Omega$, $5\text{ K}\Omega$ & $2\text{ K}\Omega$ Compare the all the three layouts in terms of Area, Power, Voltage Transfer Characteristics – V_{out} v/s V_{in} (VTC).		
3	Draw a layout of CMOS Inverter using CMOS $0.12\text{ }\mu\text{m}$ technology and simulate its Transient Characteristics- V_{out} v/s time, Voltage Transfer Characteristics – V_{out} v/s V_{in} (VTC). Note the Area and Power of the design.		
4	Draw a layout of CMOS NAND Gate using CMOS $0.12\text{ }\mu\text{m}$ technology and simulate its Transient Characteristics- V_{out} v/s time.		
5	Draw a layout of CMOS NOR Gate using CMOS $0.12\text{ }\mu\text{m}$ technology and simulate its Transient Characteristics- V_{out} v/s time.		
6	Draw a layout of CMOS XOR using CMOS $0.12\text{ }\mu\text{m}$ technology and simulate its Transient Characteristics- V_{out} v/s time. Use the Euler's path technique for designing.		
7	Draw a layout of CMOS Half Adder using CMOS $0.12\text{ }\mu\text{m}$ technology and simulate its Transient Characteristics- V_{out} v/s time. Use the Euler's path technique for designing.		
8	Draw a layout of CMOS Full Adder using CMOS $0.12\text{ }\mu\text{m}$ technology and simulate its Transient Characteristics- V_{out} v/s time. Use the Euler's path technique for designing.		
9	Compare the CMOS, Resistive Load, and <i>n</i> MOS Load Inverters in terms of Area, Power, and Voltage Transfer Characteristics – V_{out} v/s V_{in} (VTC).		
10	Draw a layouts of CMOS Inverter using CMOS $0.12\text{ }\mu\text{m}$ technology with different width (W_p) of <i>p</i> MOS transistors. <ul style="list-style-type: none"> • $W_n = 4\lambda$ & $W_p = 4\lambda$ $W_n = 4\lambda$ & $W_p = 6\lambda$ • $W_n = 4\lambda$ & $W_p = 10\lambda$ $W_n = 4\lambda$ & $W_p = 12\lambda$ and compare their Voltage Transfer Characteristics – V_{out} v/s V_{in} (VTC).		
11	Draw a layouts of CMOS Inverter using CMOS $0.12\text{ }\mu\text{m}$ technology. Apply different value of V_{SB} and observe the changes in Transient Characteristics- V_{out} v/s time, Voltage Transfer Characteristics – V_{out} v/s V_{in} (VTC) due to Substrate Bias (Body bias) effect. Herein, $V_{SB} = V_s - V_B$ (V_s = source voltage, V_B = body (substrate) voltage).		
12	Draw layouts of <i>n</i> MOS and <i>p</i> MOS as pass-transistors. Using the simulation results of Transient Characteristics – V_{out} v/s time demonstrate that <i>n</i> MOS (<i>p</i> MOS) is a good (bad) conductor of logic “0” (“1”) and bad (good) conductor of logic “1” (“0”).		
13	Draw a layouts of Transmission Gate (TG) as pass-transistors. Using the simulation results of Transient Characteristics – V_{out} v/s time demonstrate that TG is a good conductor of logic “0” and logic “1”.		
14	Draw a layout of any one sequential basic building block from the following: SR Latch, D Latch.		

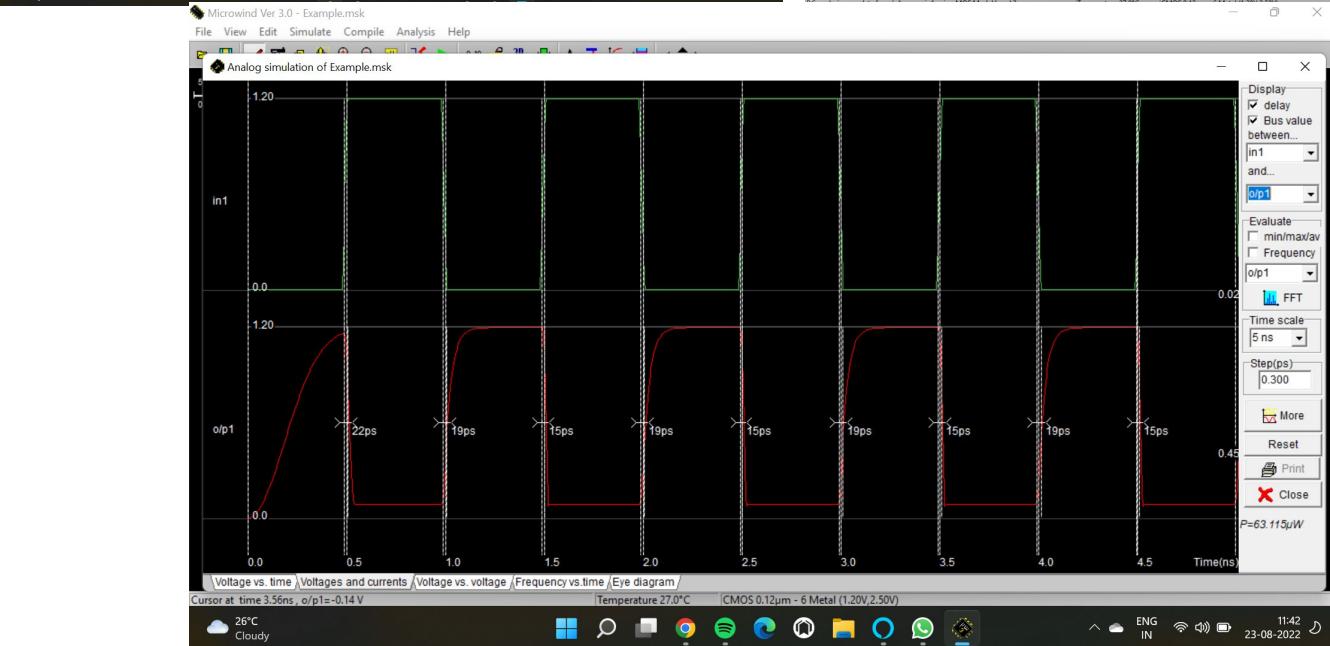
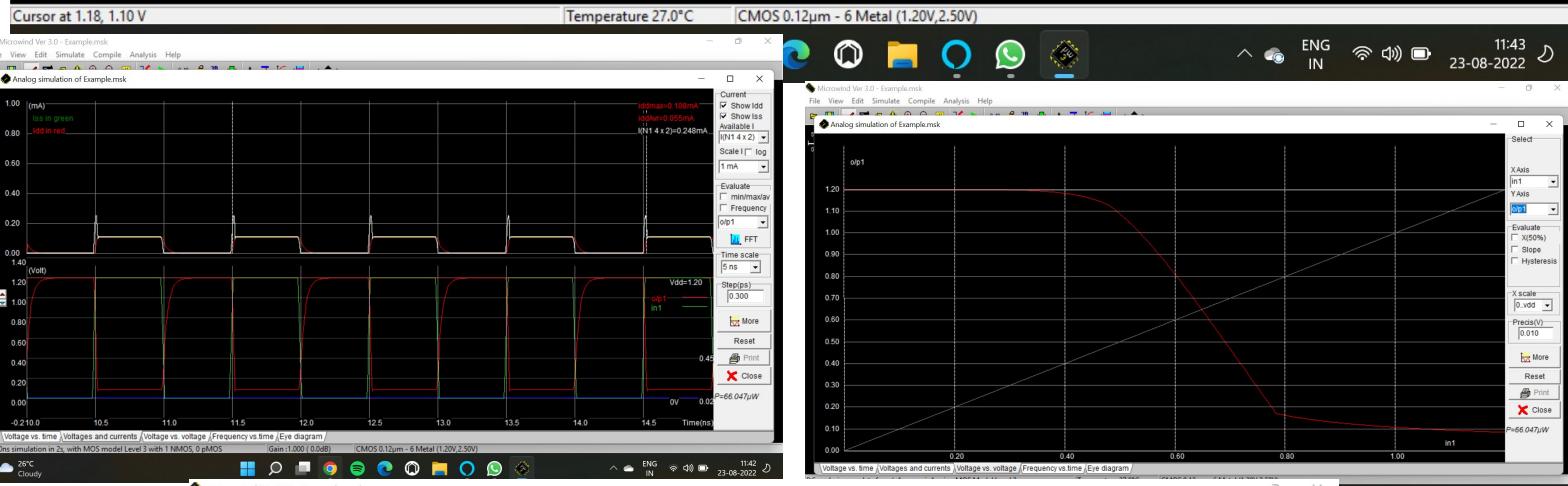
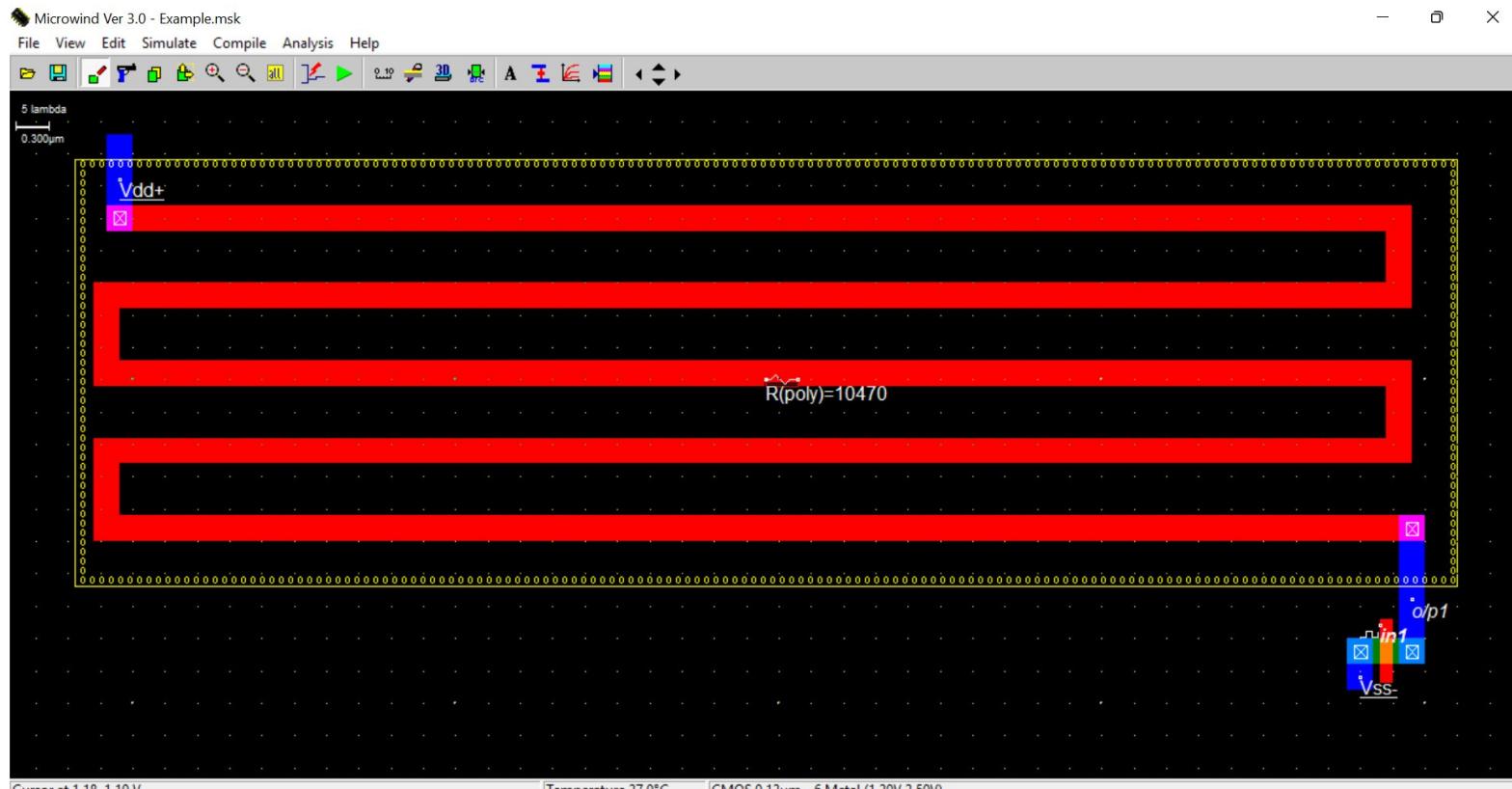
Note:

- At the end of semester, an individual student is required to submit a mini-project by completing a layout design and simulation of any combinational or sequential CMOS circuit during the semester. For example; Multiplexers, decoders, encoders, ALU, adders, multipliers, counters, shift-registers or any such kind of digital design.

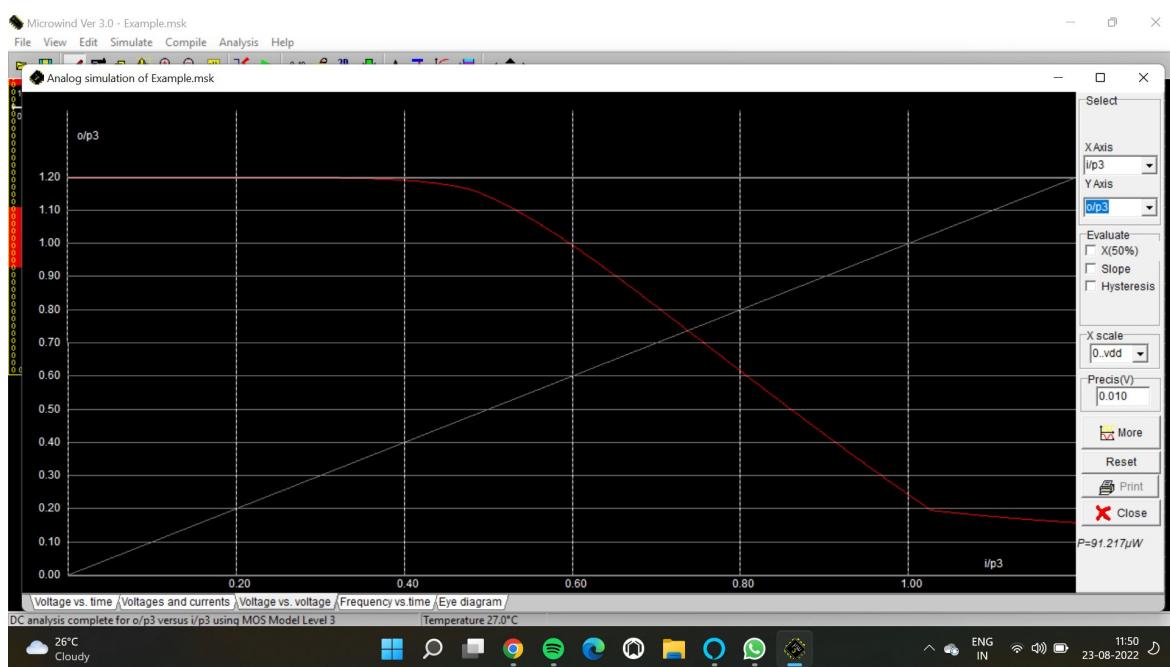
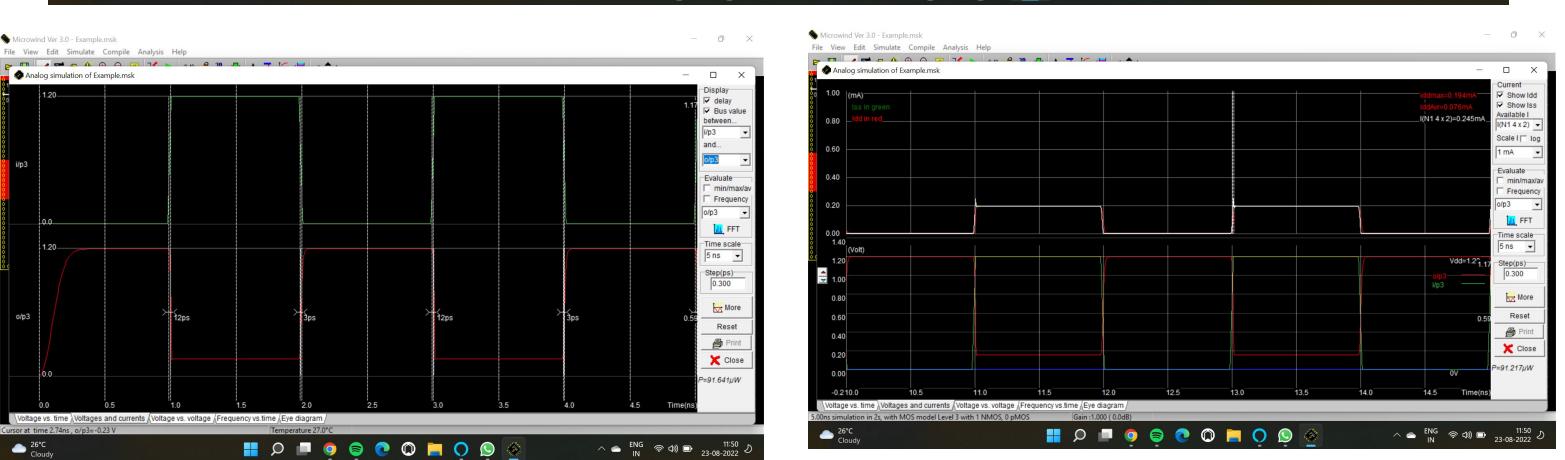
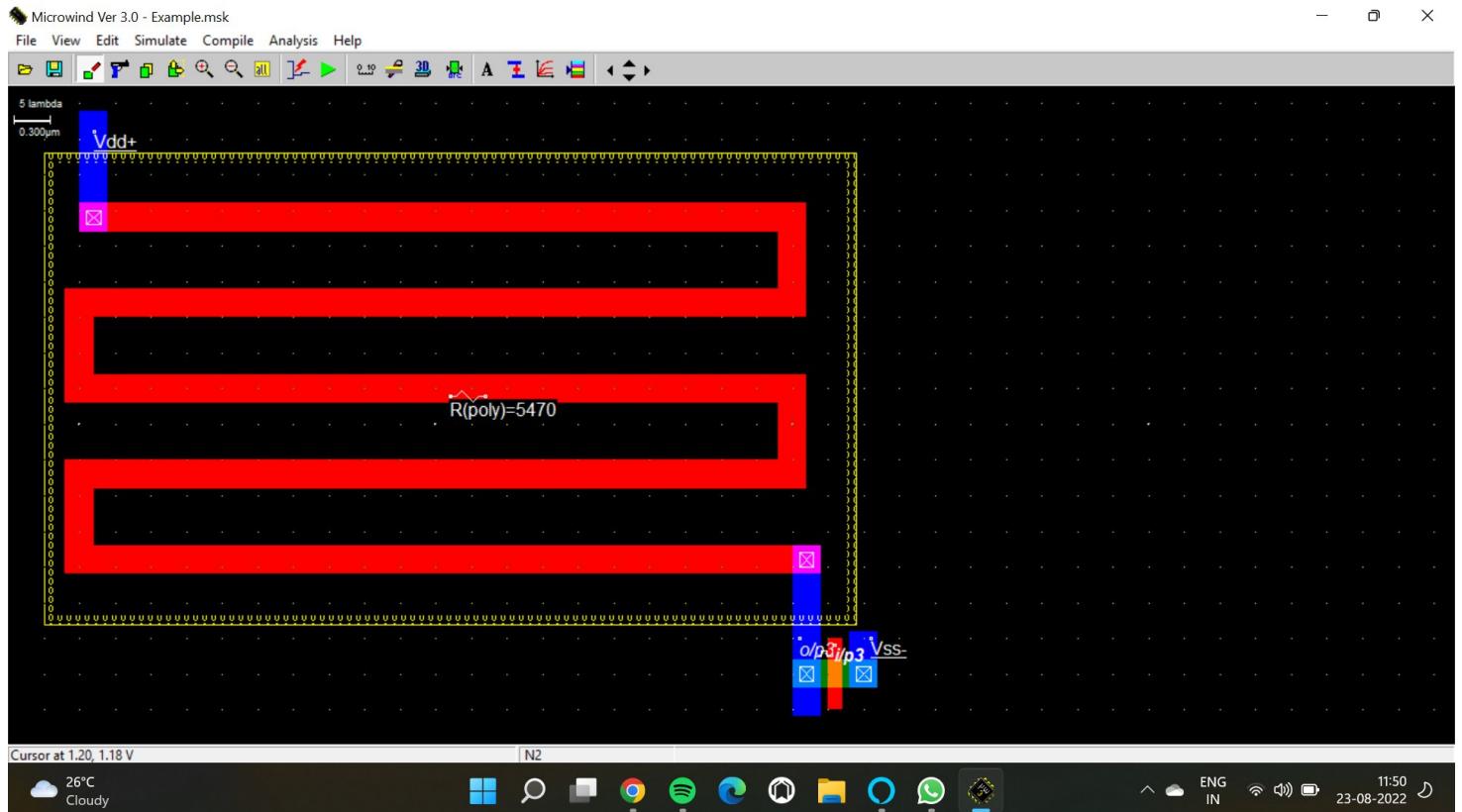
Experiment 2:RESISTIVE LOAD INVERTER



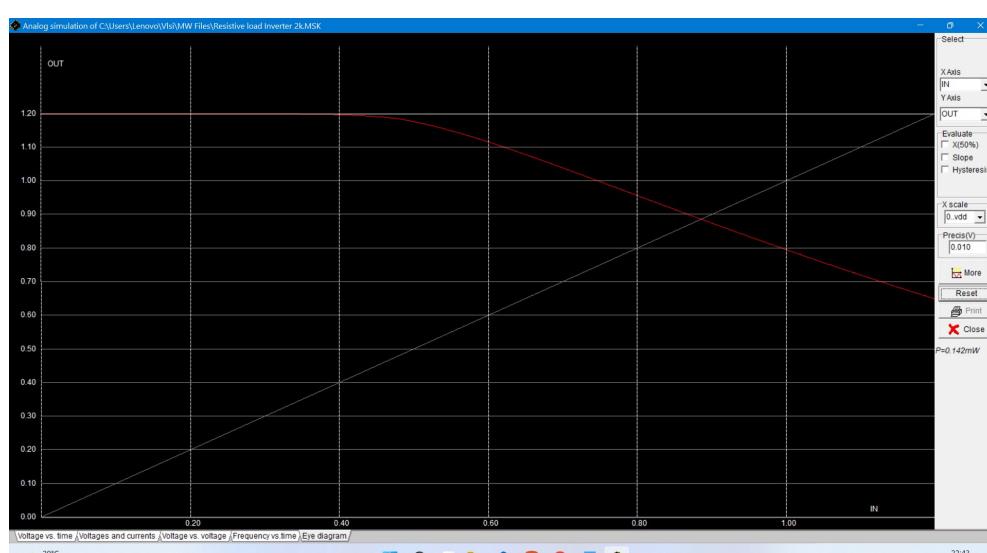
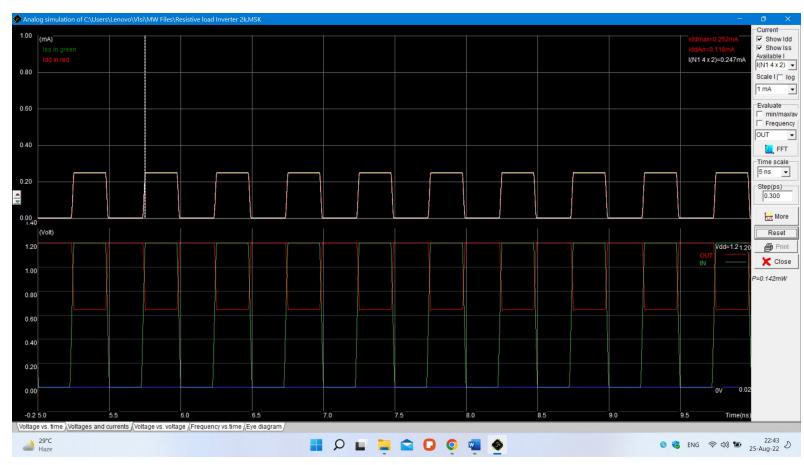
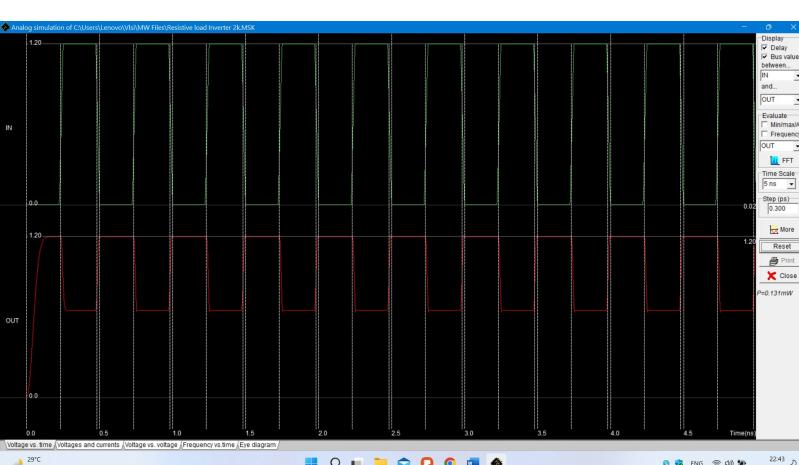
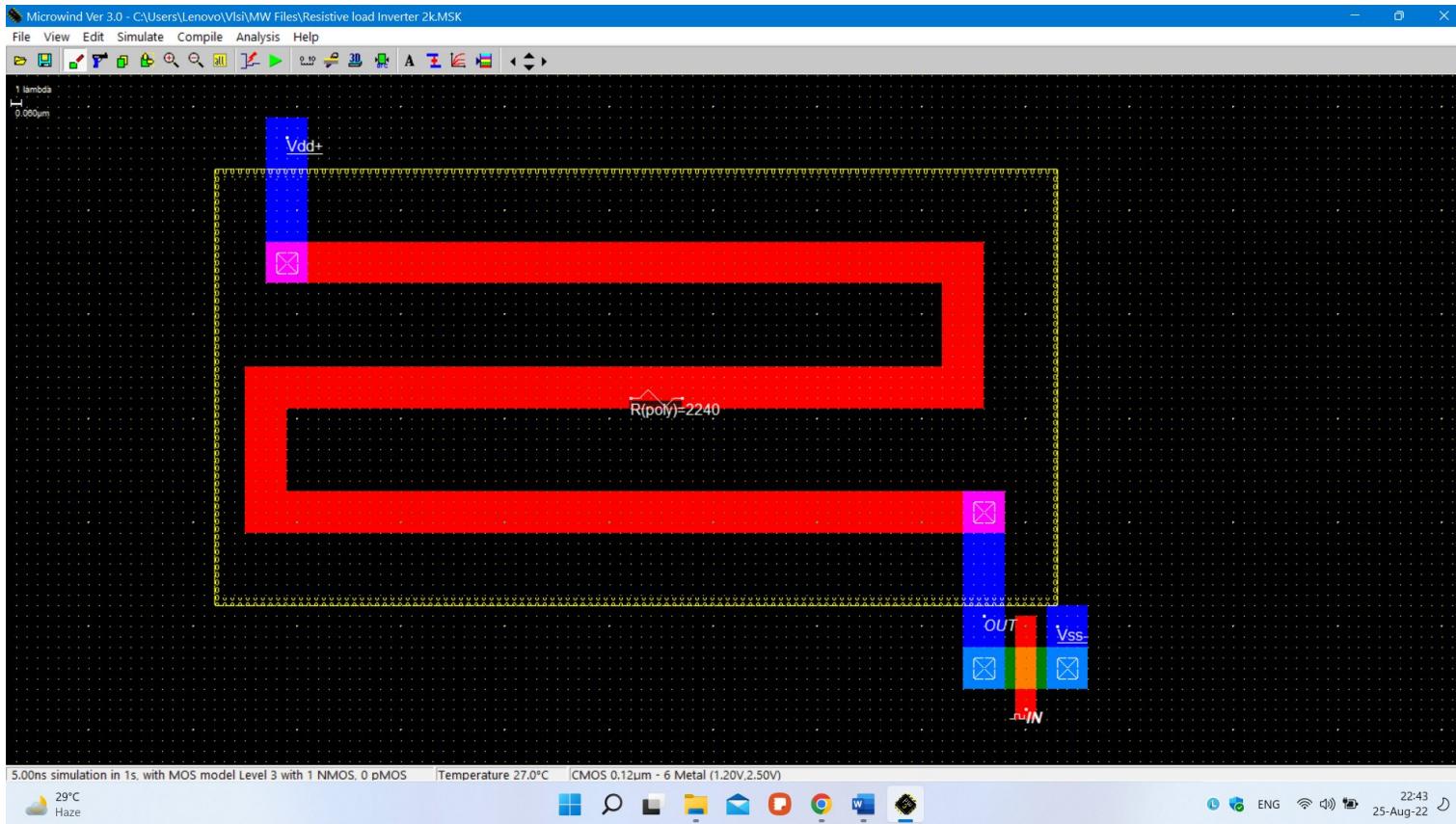
1) 10kohm



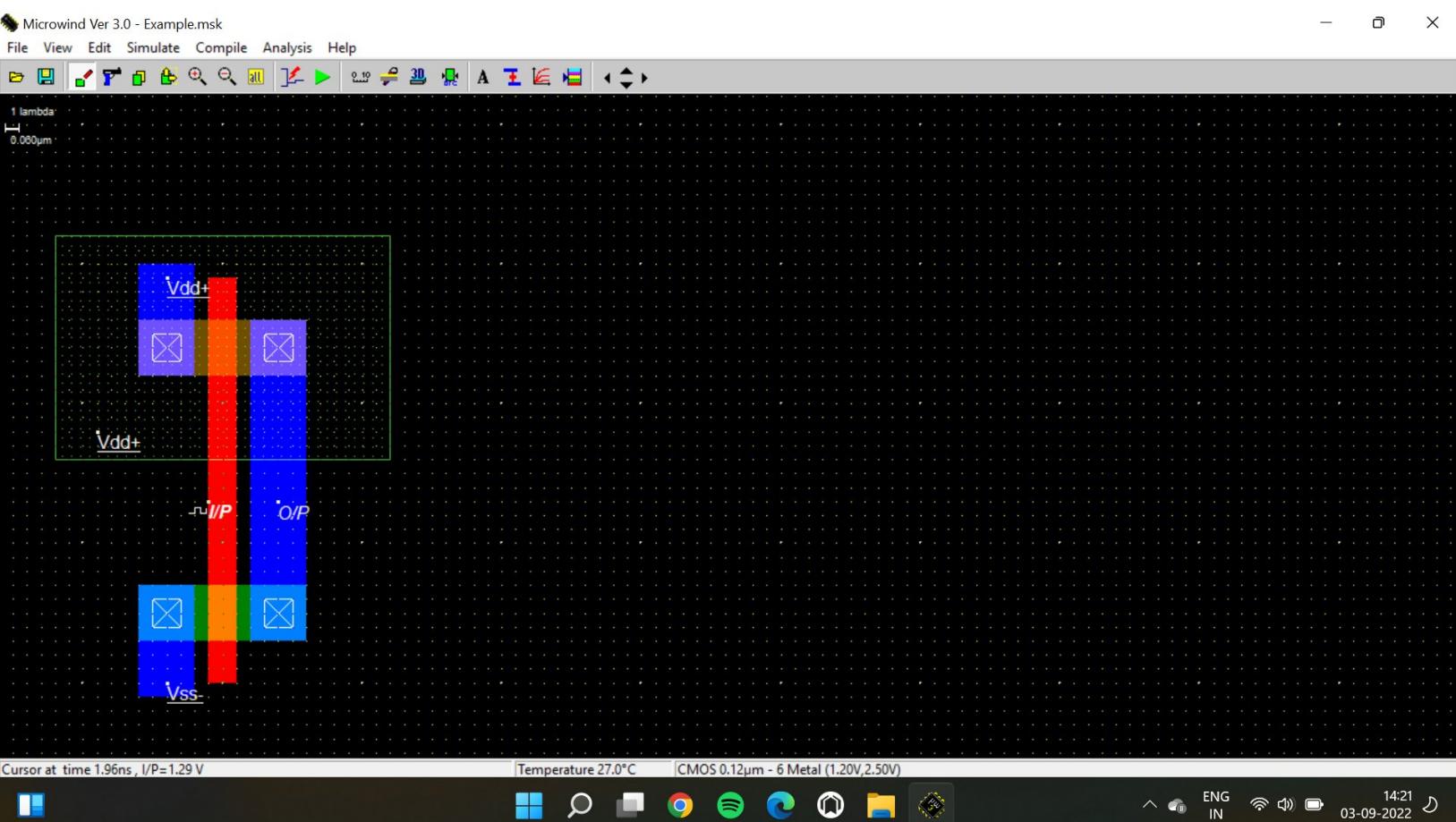
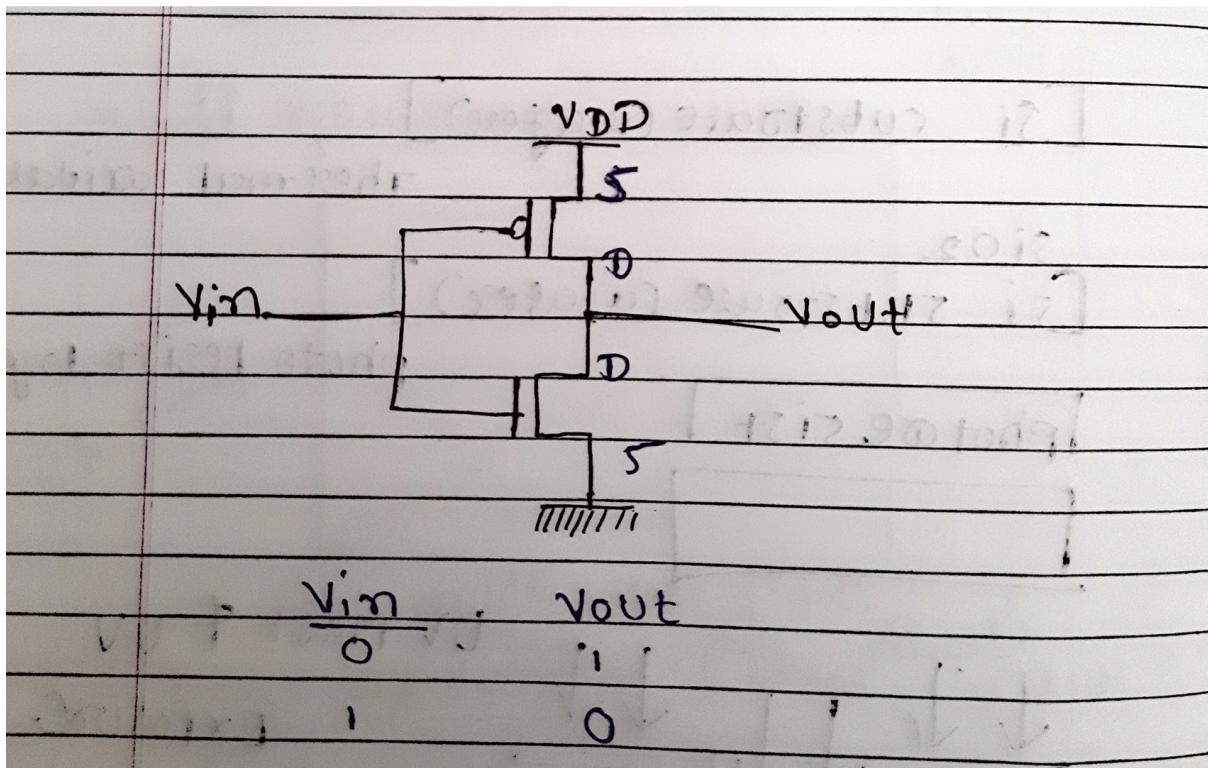
2) 5kohm



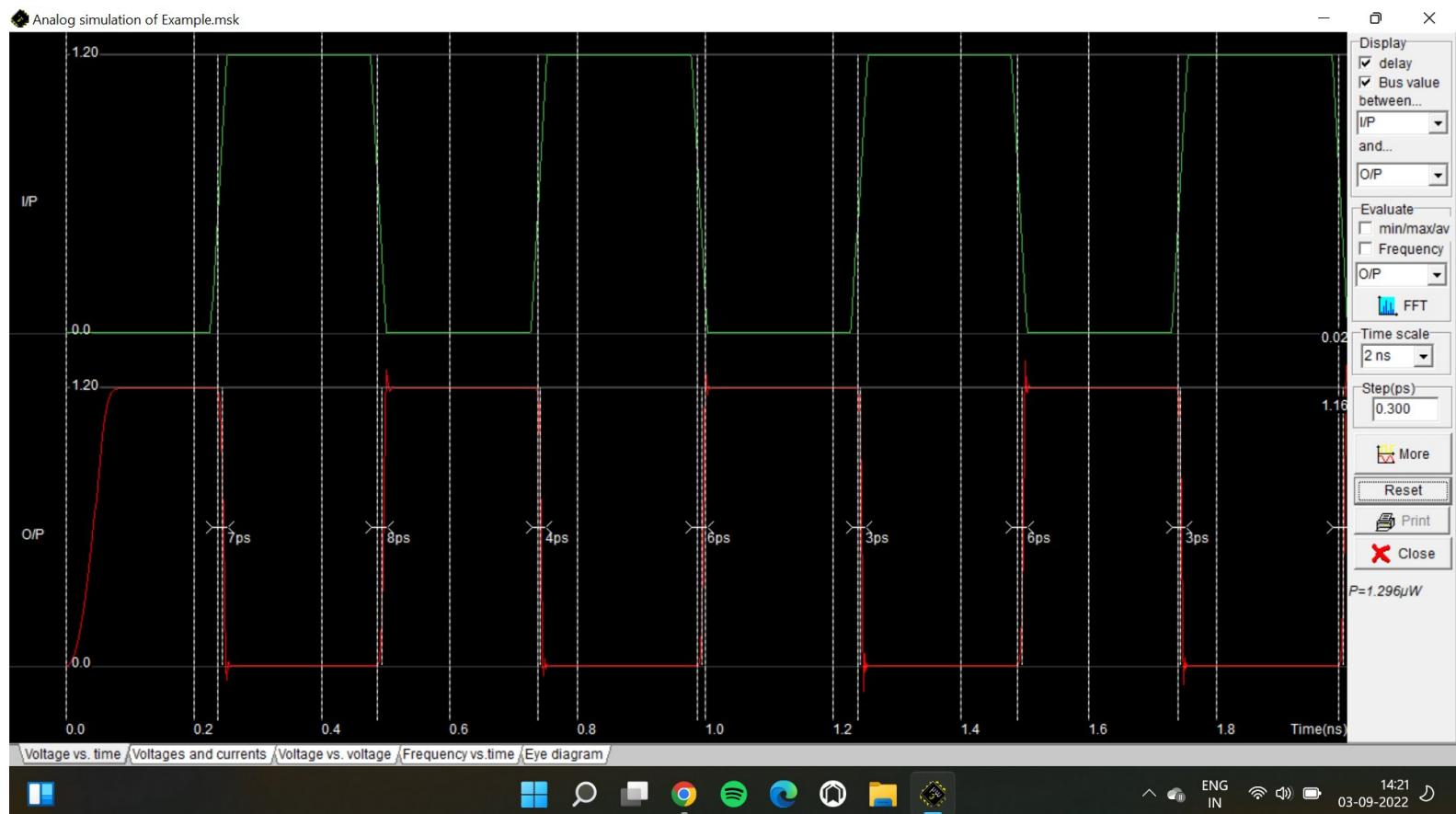
3) 2kohm



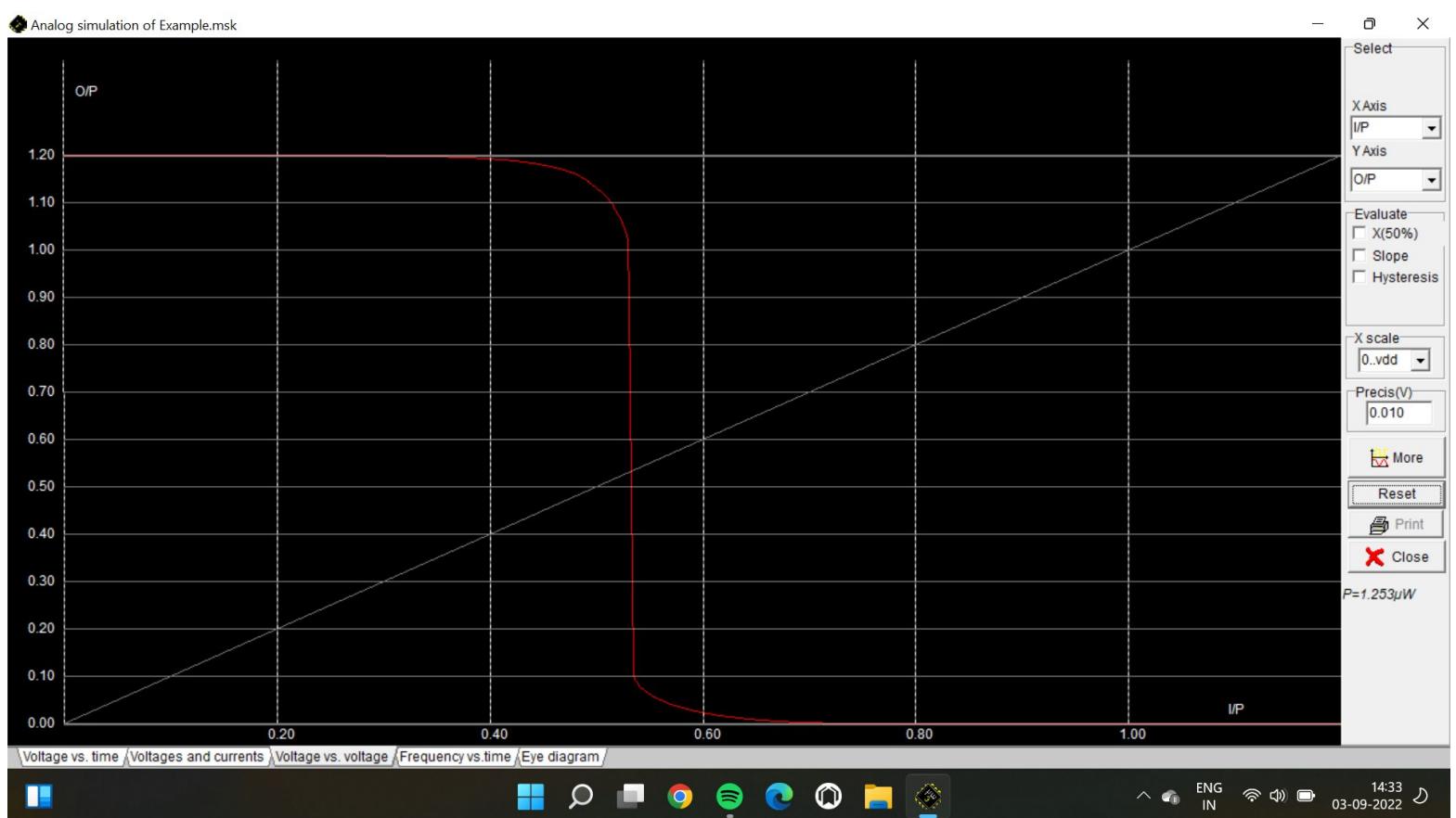
Experiment 3: CMOS



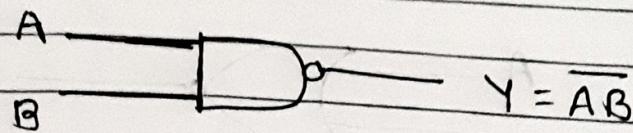
V->t



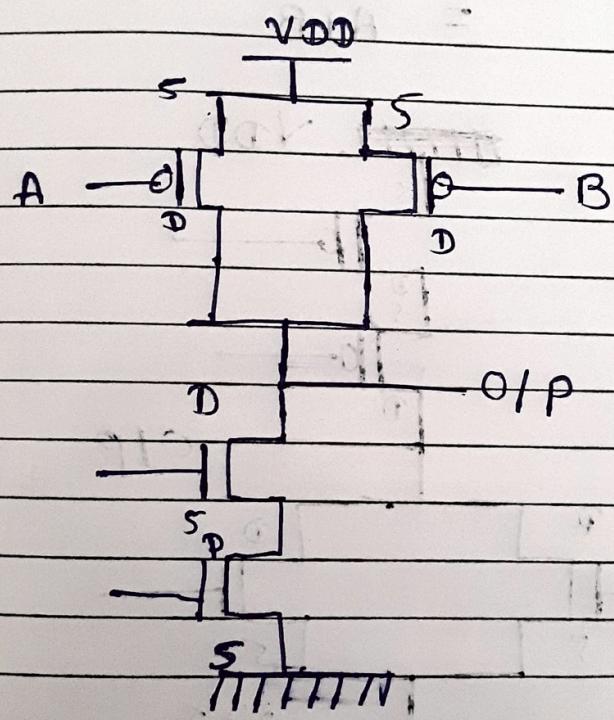
Vout->Vin



Experiment 4:NAND



$$(Y = \overline{\overline{AB}} = \overline{AB})$$



A	B	$(AB)'$
0	0	1
0	1	1
1	0	1
1	1	0

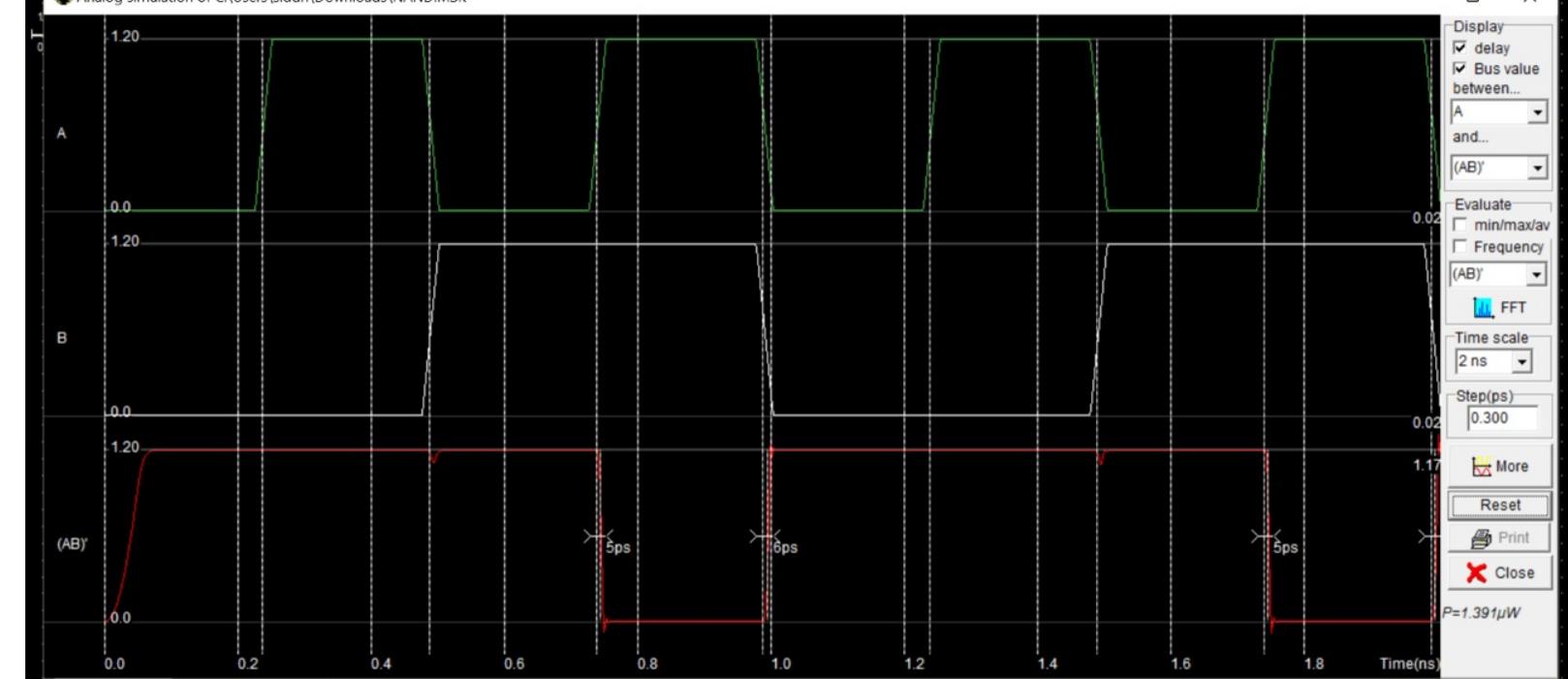
I
0.050μm

2.00ns simulation in 1s, with MOS model Level 3 with 2 NMOS, 2 pMOS

Temperature 27.0°C

CMOS 0.12μm - 6 Metal (1.20V,2.50V)

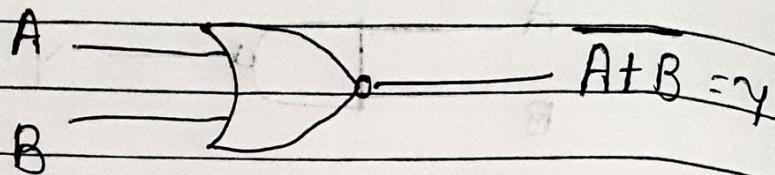
30°C ENG IN 23:20
Haze 02-09-2022



Temperature 27.0°C CMOS 0.12μm - 6 Metal (1.20V,2.50V)

30°C ENG IN 23:20
Haze 02-09-2022

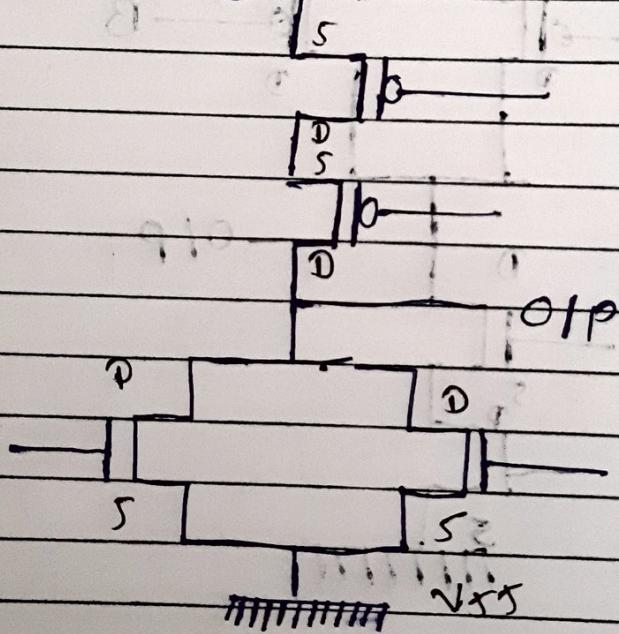
Experiment 5:NOR



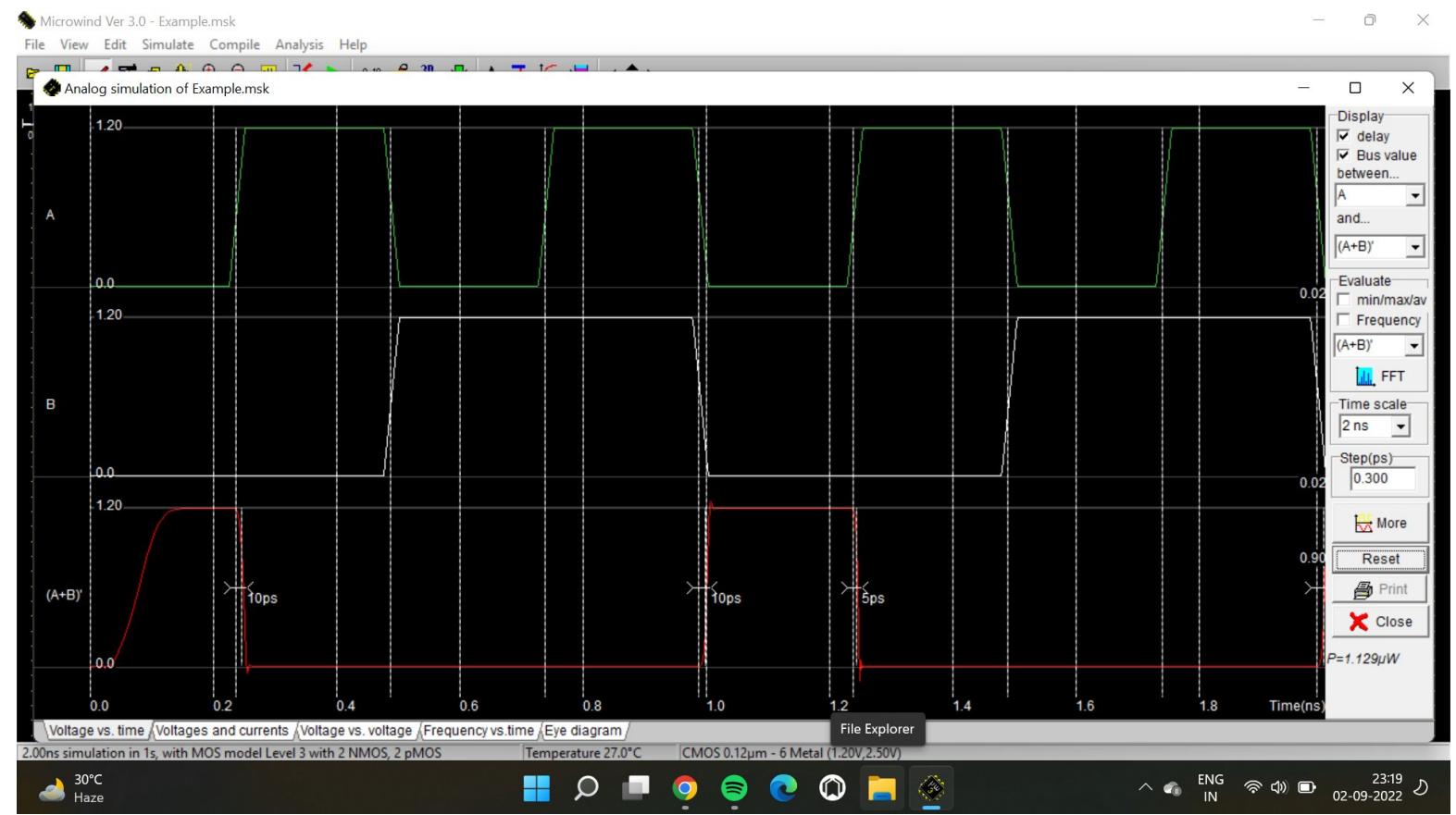
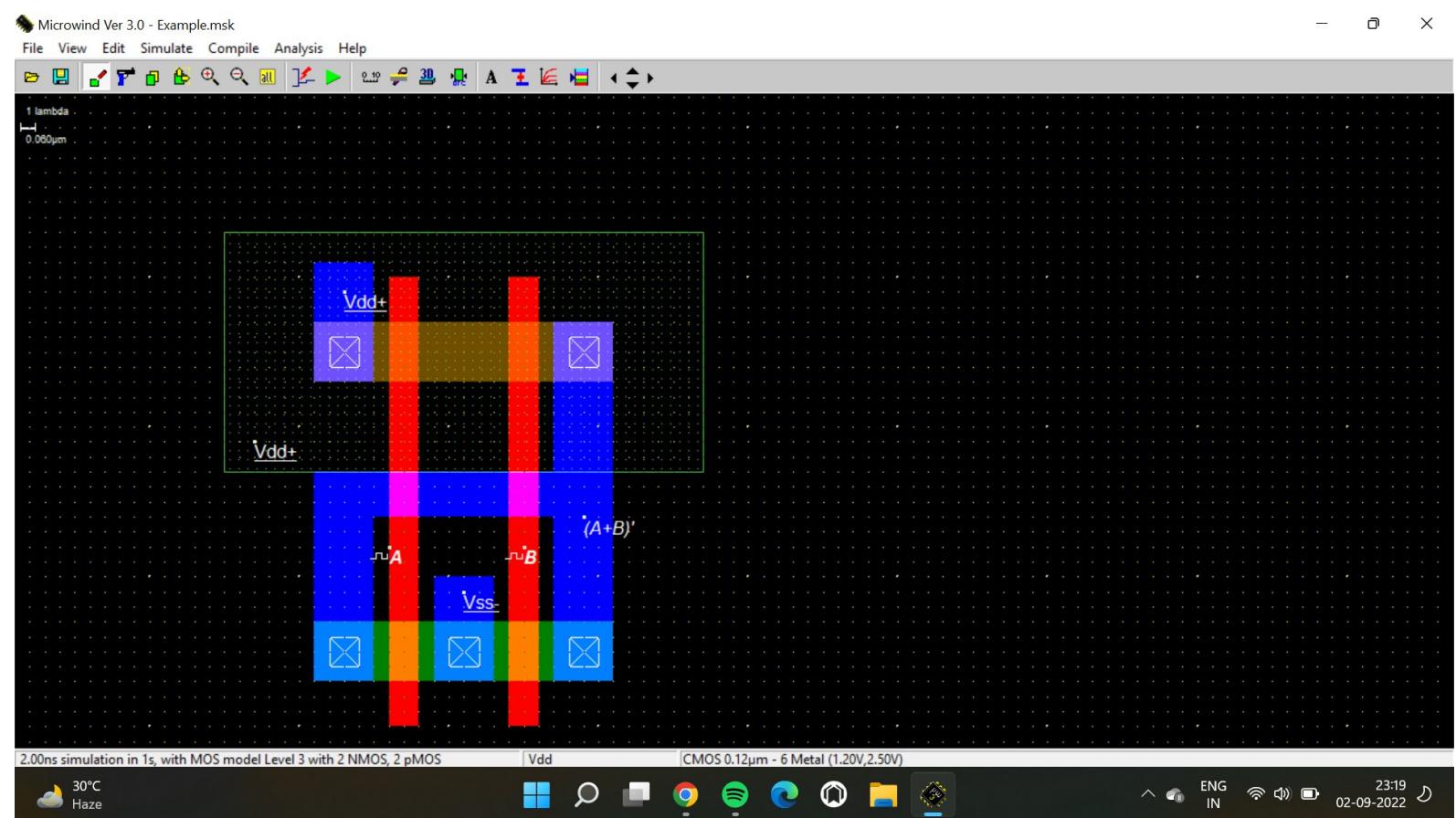
$$Y = \overline{A+B}$$

$$= \overline{A} \cdot \overline{B}$$

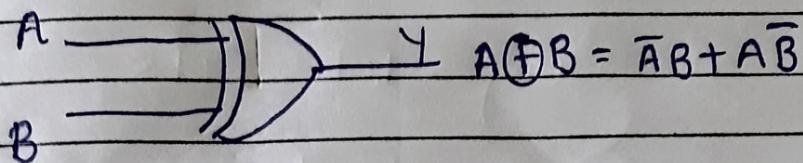
~~VDD~~ VDD



A	B	(A+B)
0	0	1
0	1	0
1	0	0
1	1	0



Experiment 6:XOR



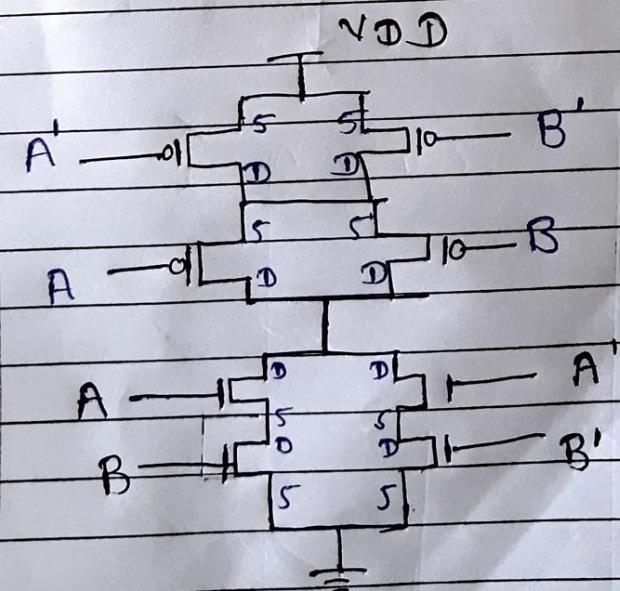
$$Y = \overline{\overline{AB} + \overline{A}\overline{B}}$$

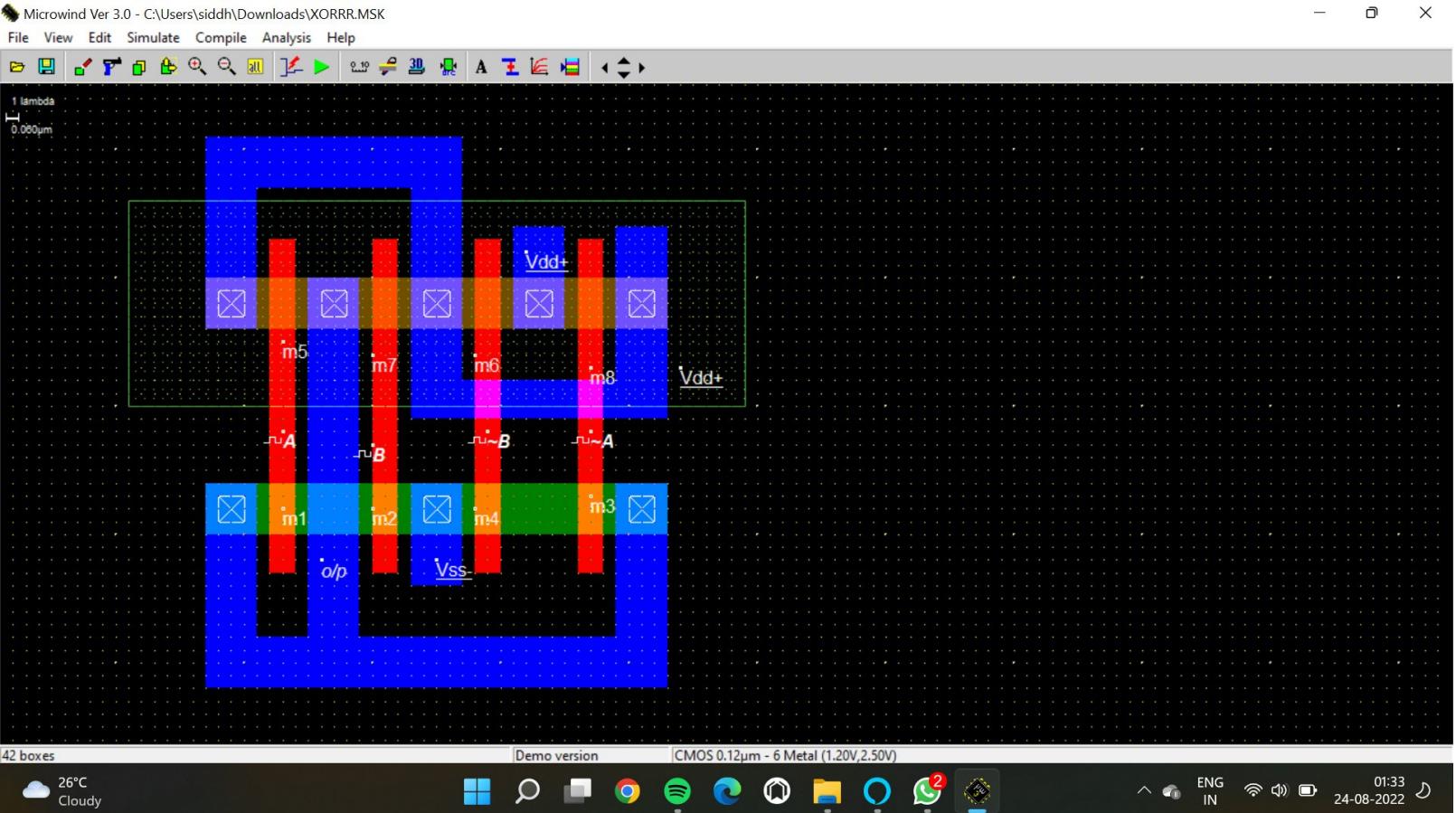
$$= (\overline{A} + \overline{B})(\overline{A} + B)$$

$$= \overline{AB} + \overline{A}\overline{B} \rightarrow 4 \text{ NMOS}$$

$\rightarrow 4 \text{ PMOS}$

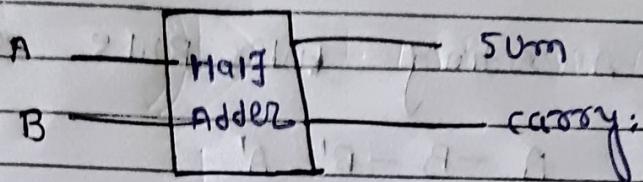
Gate Level diagram





Experiment 7: HALF ADDER

Half Adder

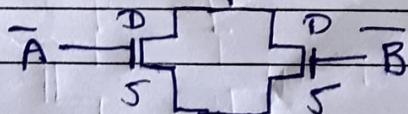
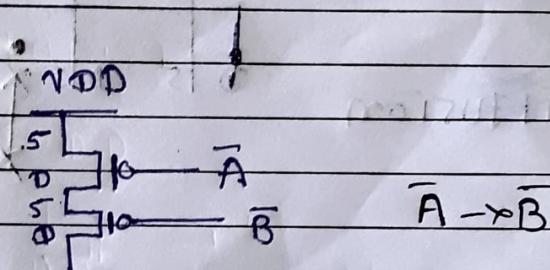


For Half Adder

$$\text{sum} = A \oplus B = \bar{A}\bar{B} + A\bar{B} \quad (\text{XOR}) ; \\ \text{carry} = A \cdot B$$

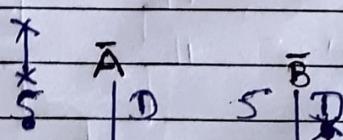
$$= \overline{\bar{A}\bar{B}} \\ = \overline{\bar{A} + \bar{B}}$$

Carry

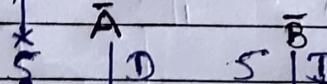


Stick Diagram

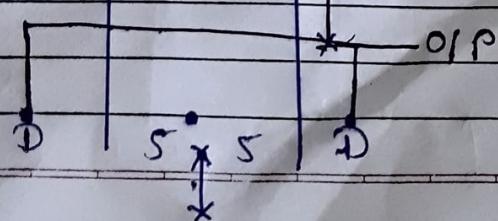
V_{DD} :



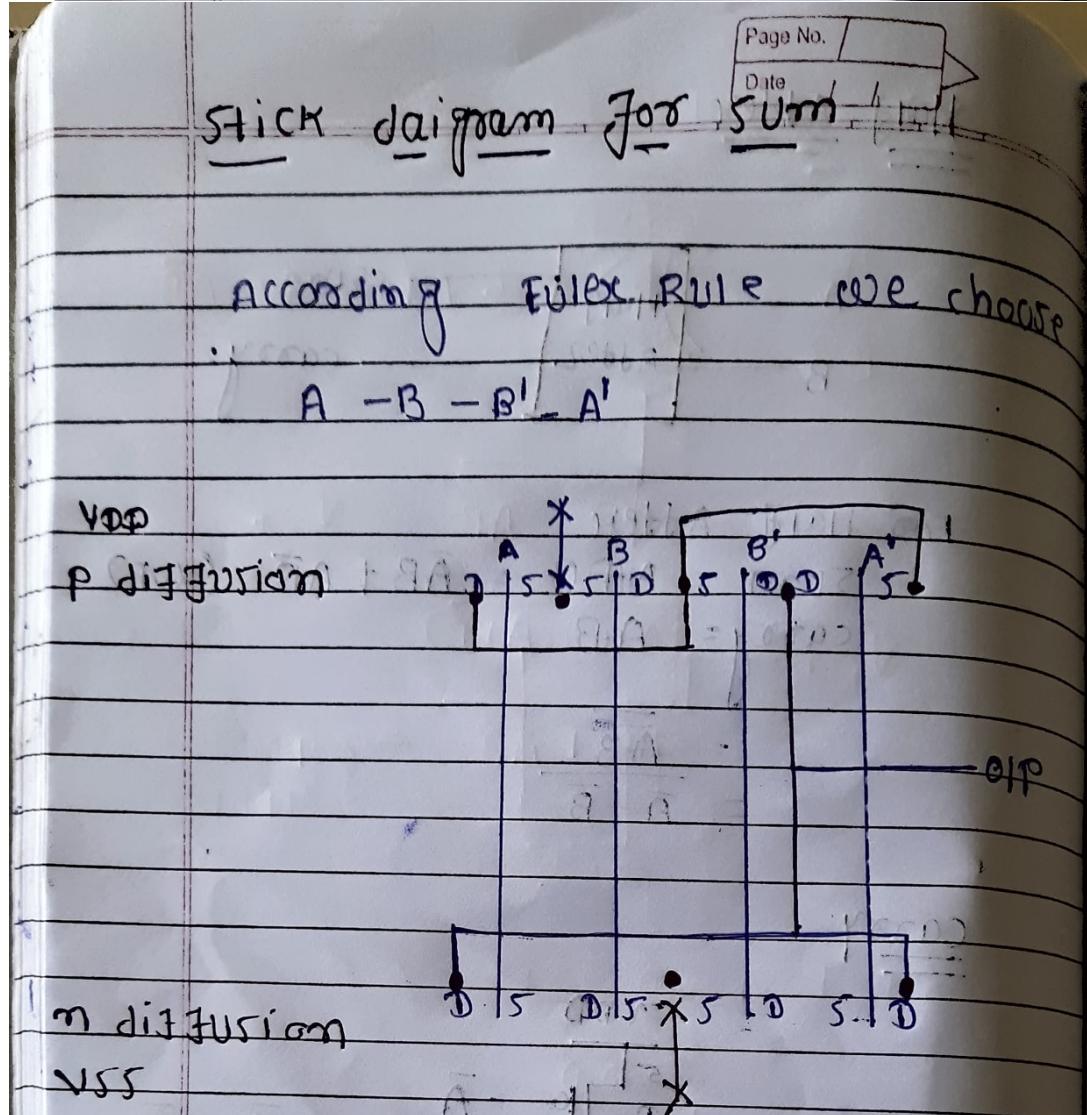
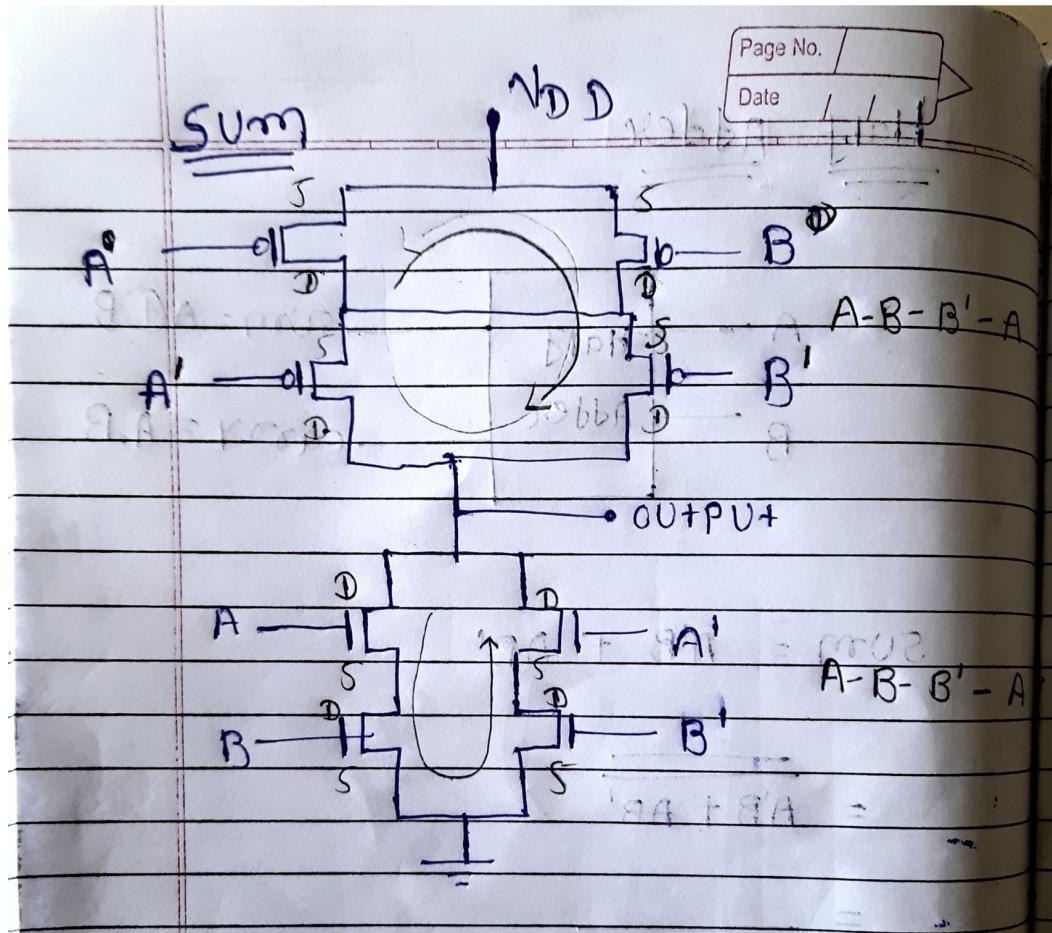
P diffusion :

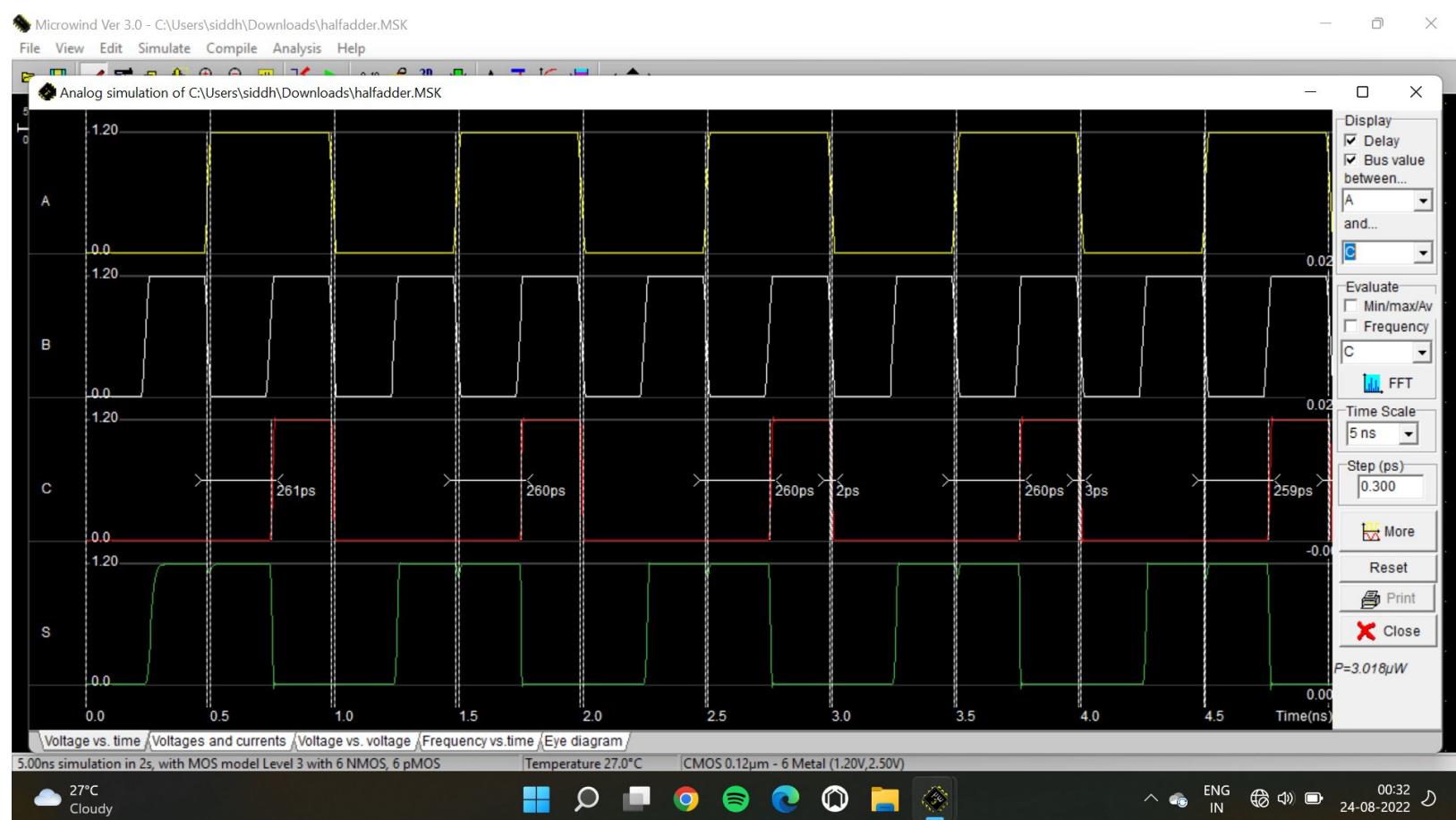
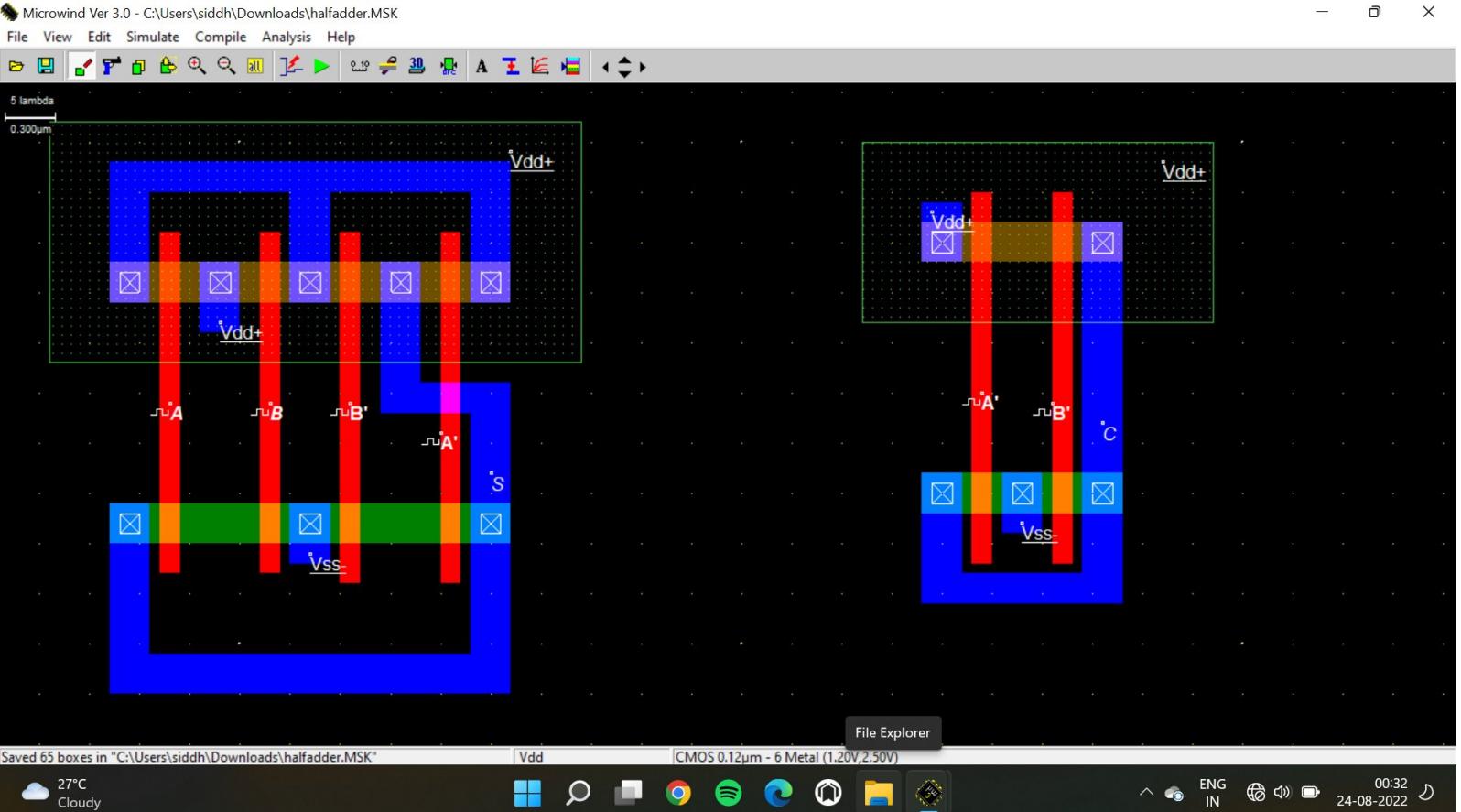


n diffusion



V_{SS}

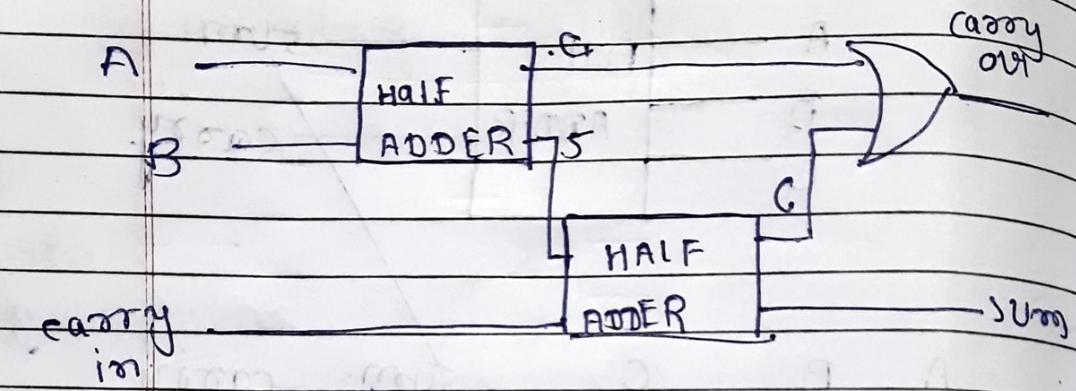




Experiment 8: FULL ADDER

Page No. / /
Date / /

FULL ADDER



A	B	Cin	S	Cout	\bar{C}_{out}
0	0	0	0	0	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
0	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	0

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

$$C_{out} = \bar{A}\bar{B}C_{in} + A\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + AB\bar{C}_{in}$$

$$= B(C_{in} + A(C_{in} + AB(1+C_{in}))$$

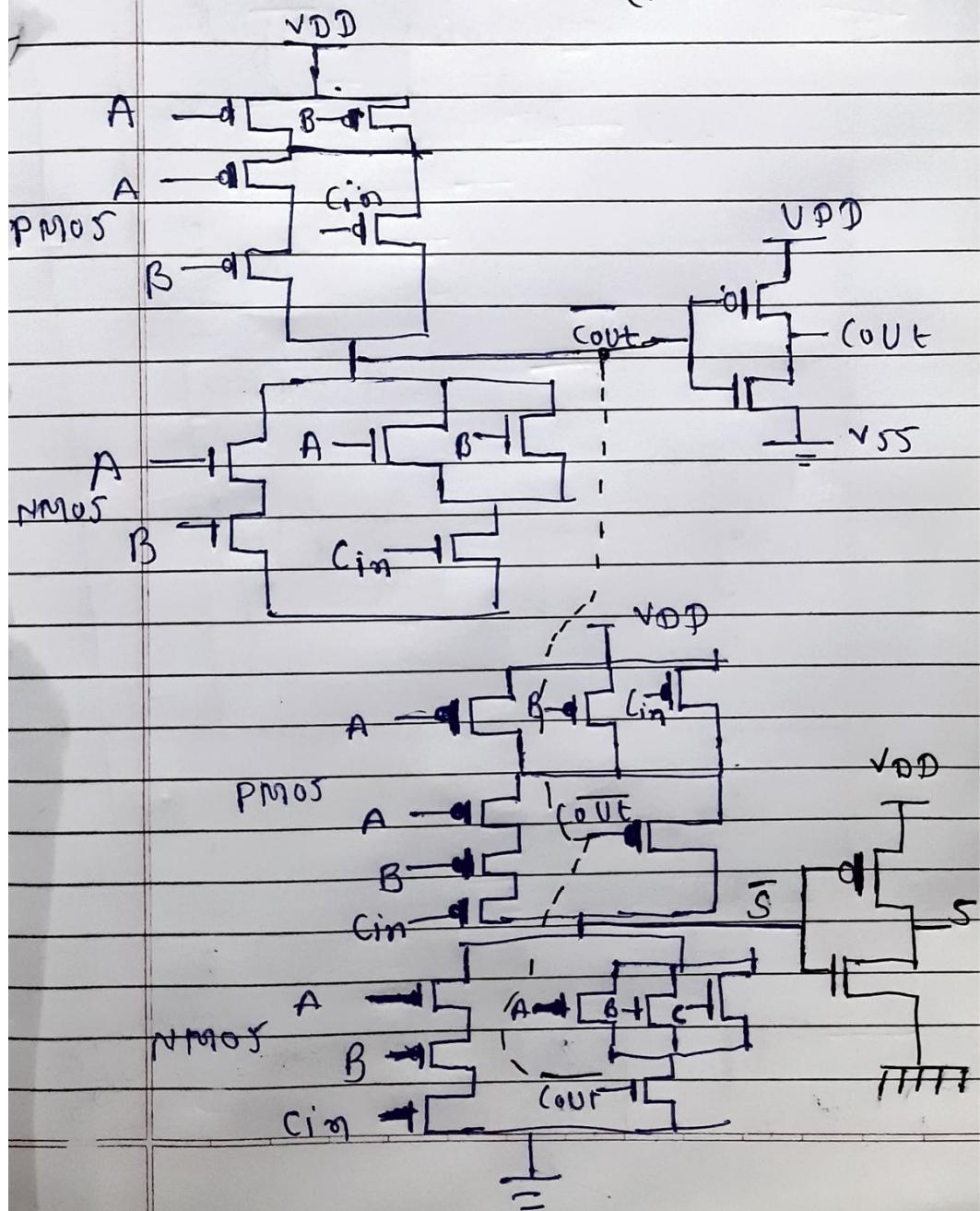
$$= (A+B)(C_{in} + AB(1+C_{in}))$$

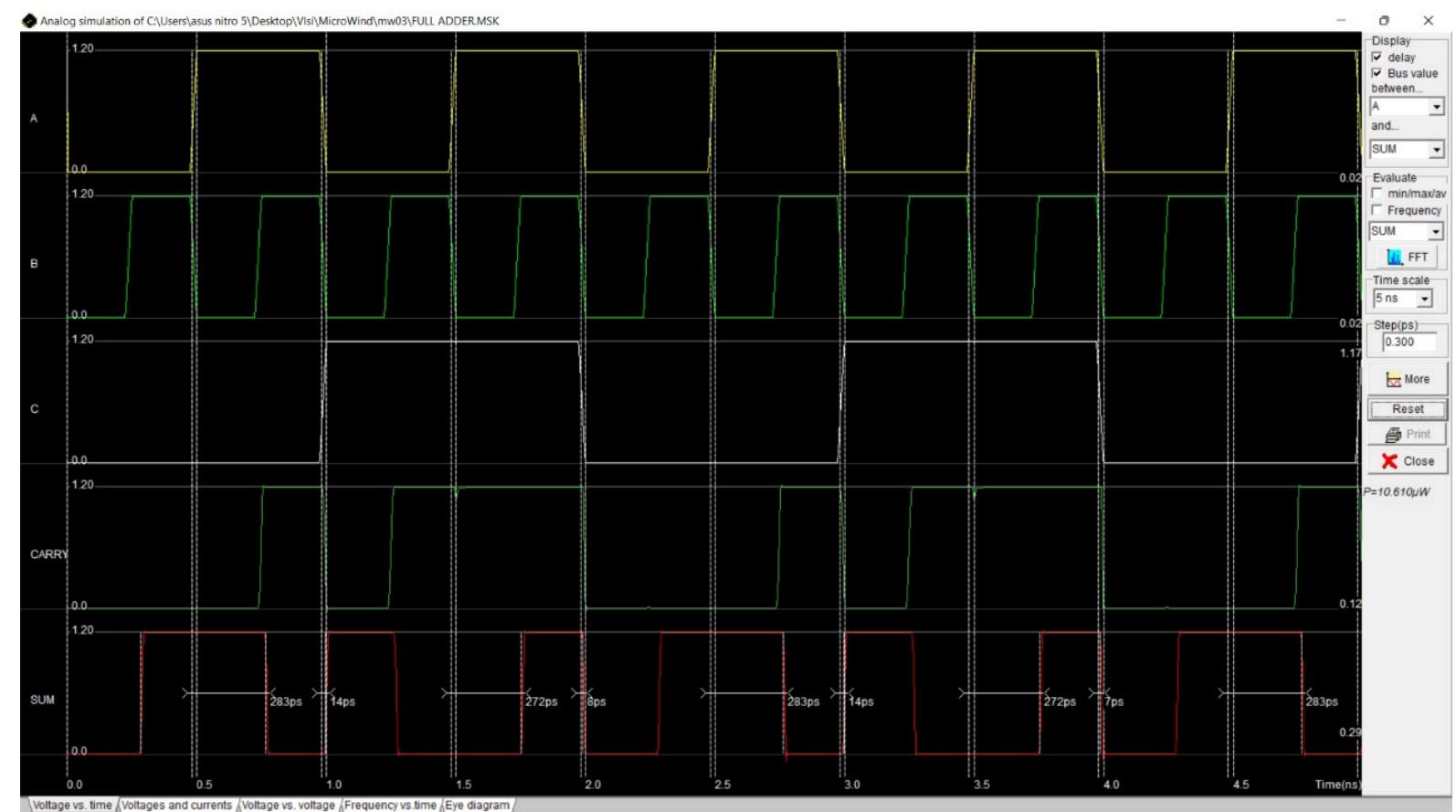
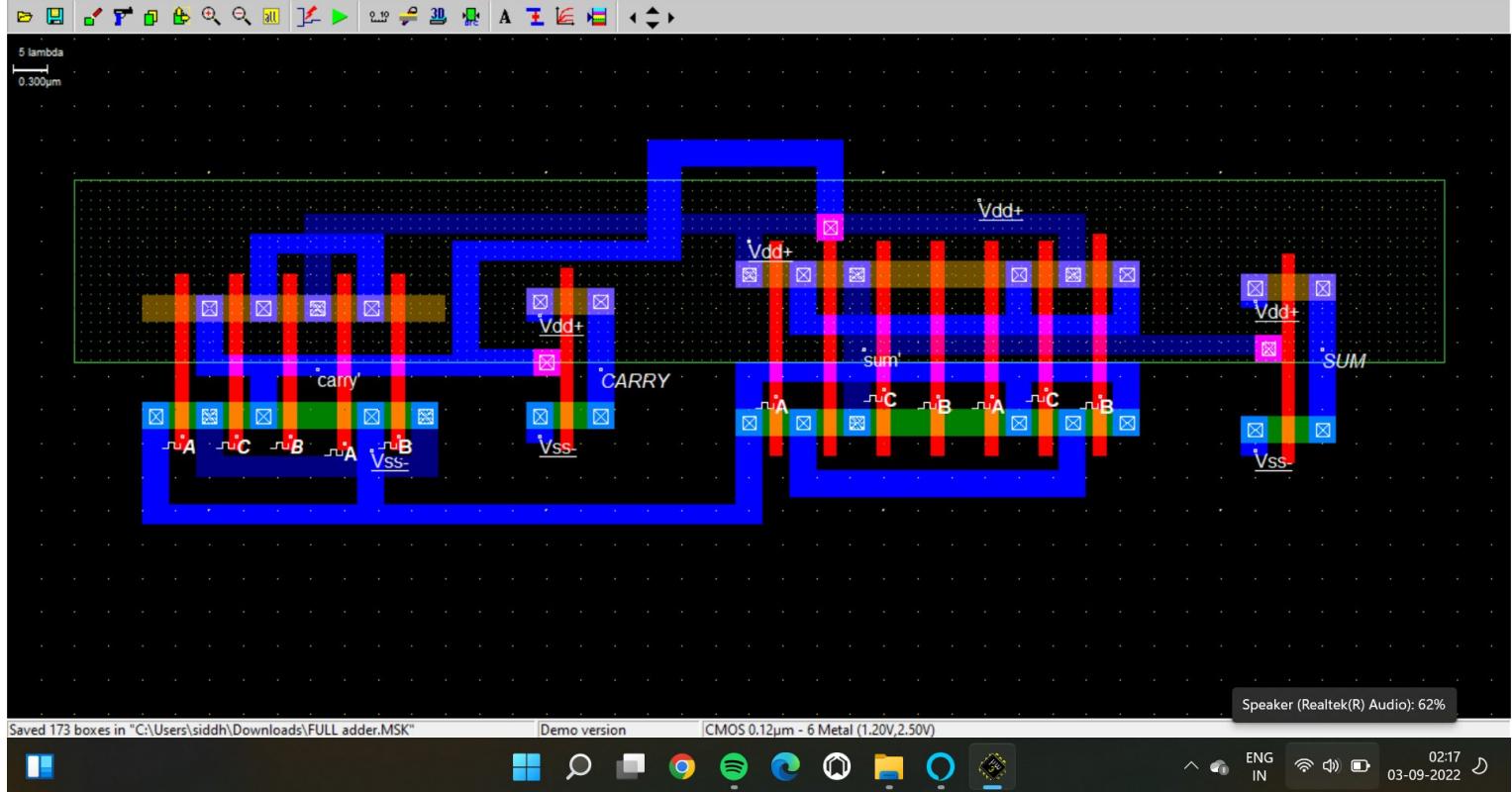
$$C_{out} = (A+B) C_{in} + AB$$

for sum

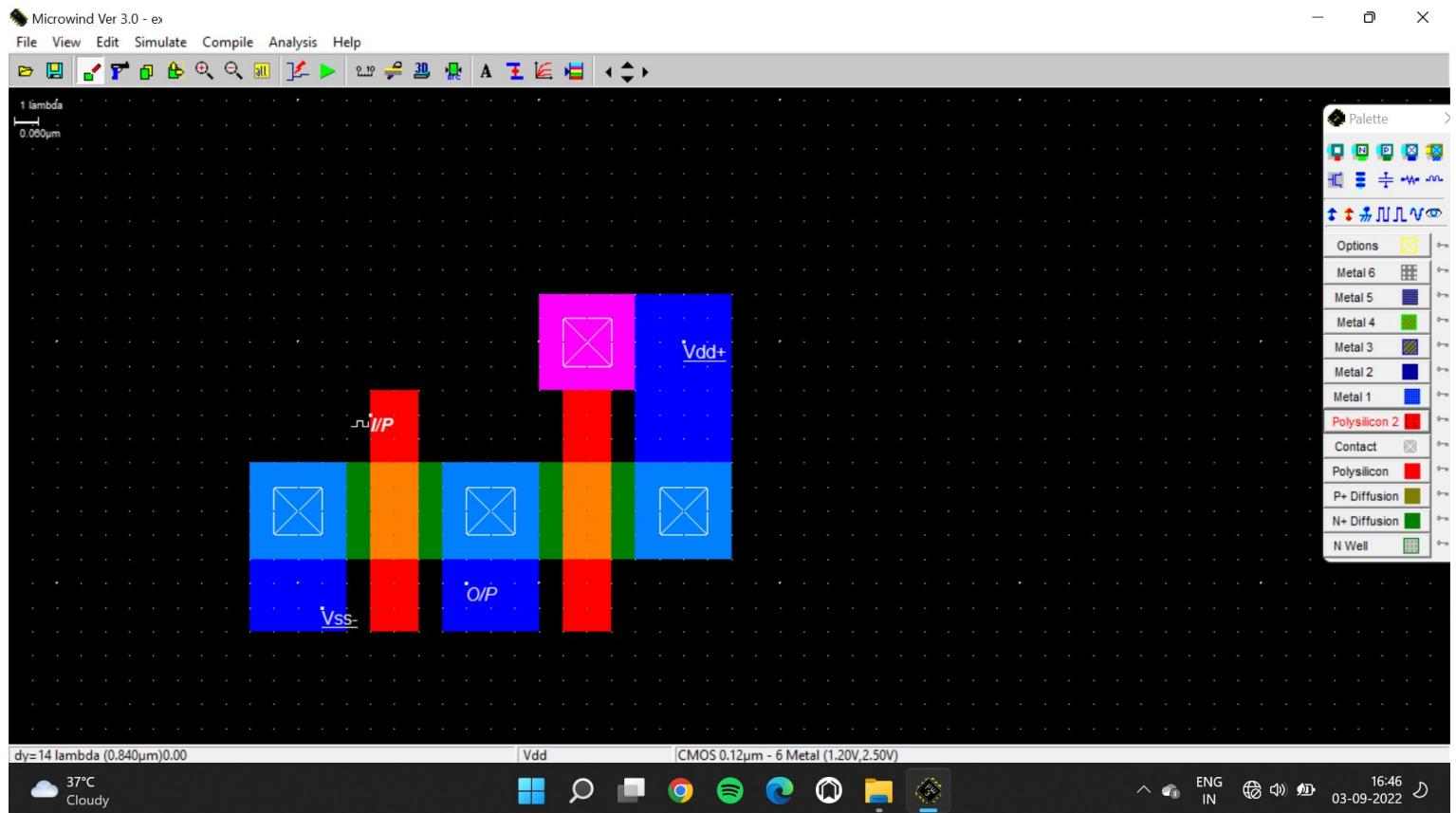
$$\textcircled{1} \quad \text{Sum} = C_{in} C_{out} + A C_{out} + B C_{out} \\ + AB + C_{in}$$

$$= ABC_{in} + (A+B+C_{in}) C_{out}$$



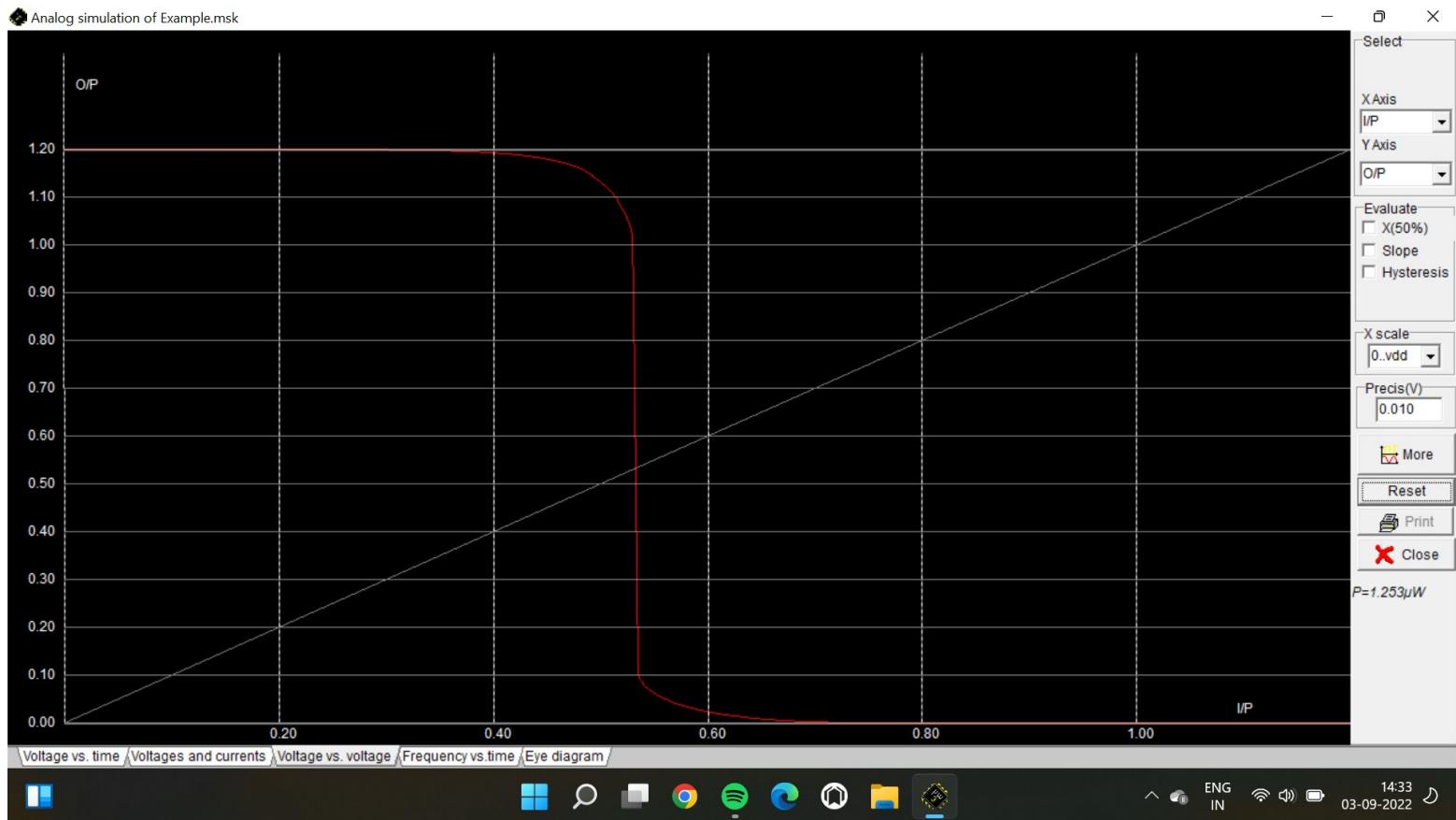


Experiment 9:nMOS INVERTER

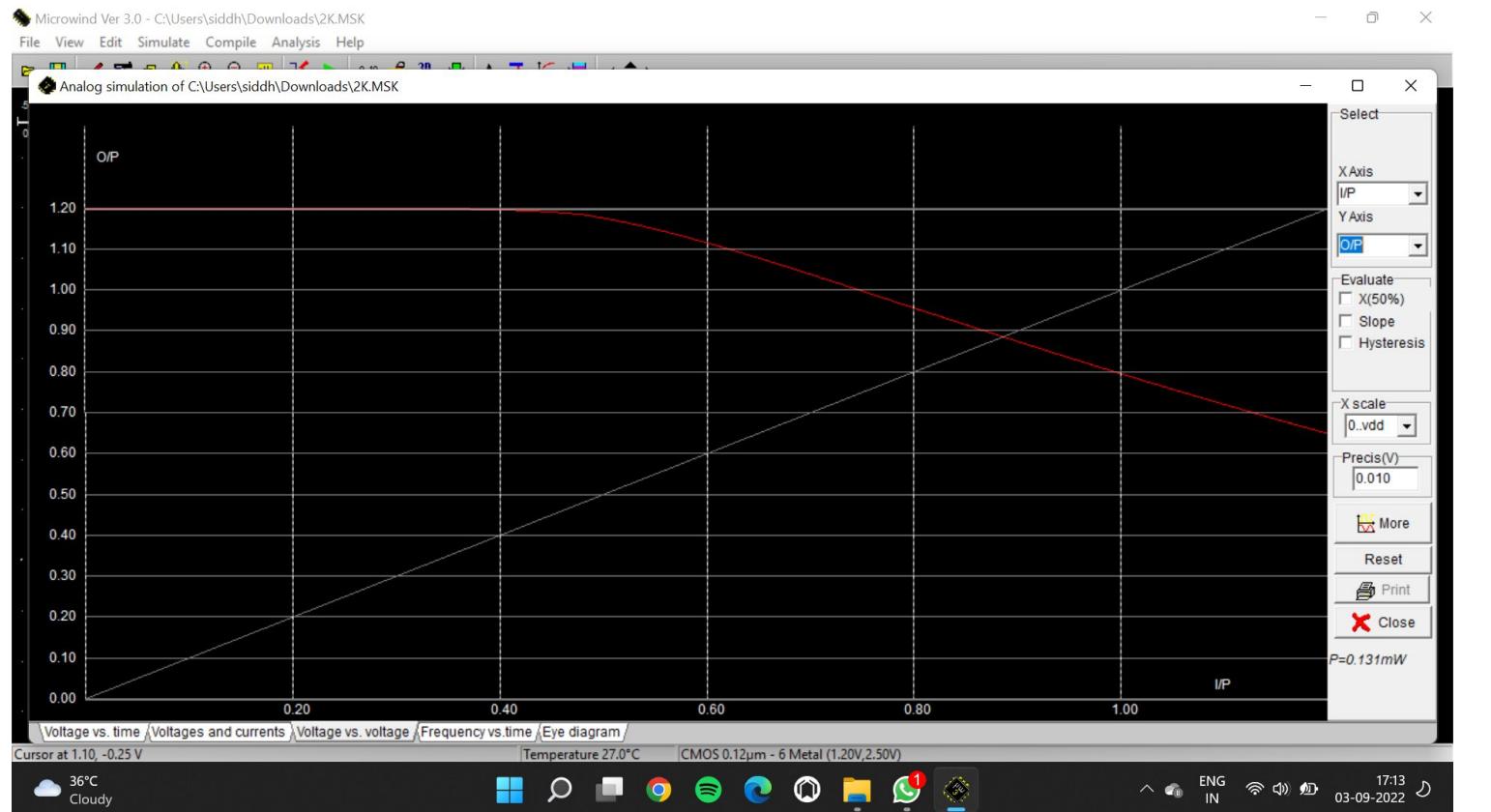


Vout v/s Vin

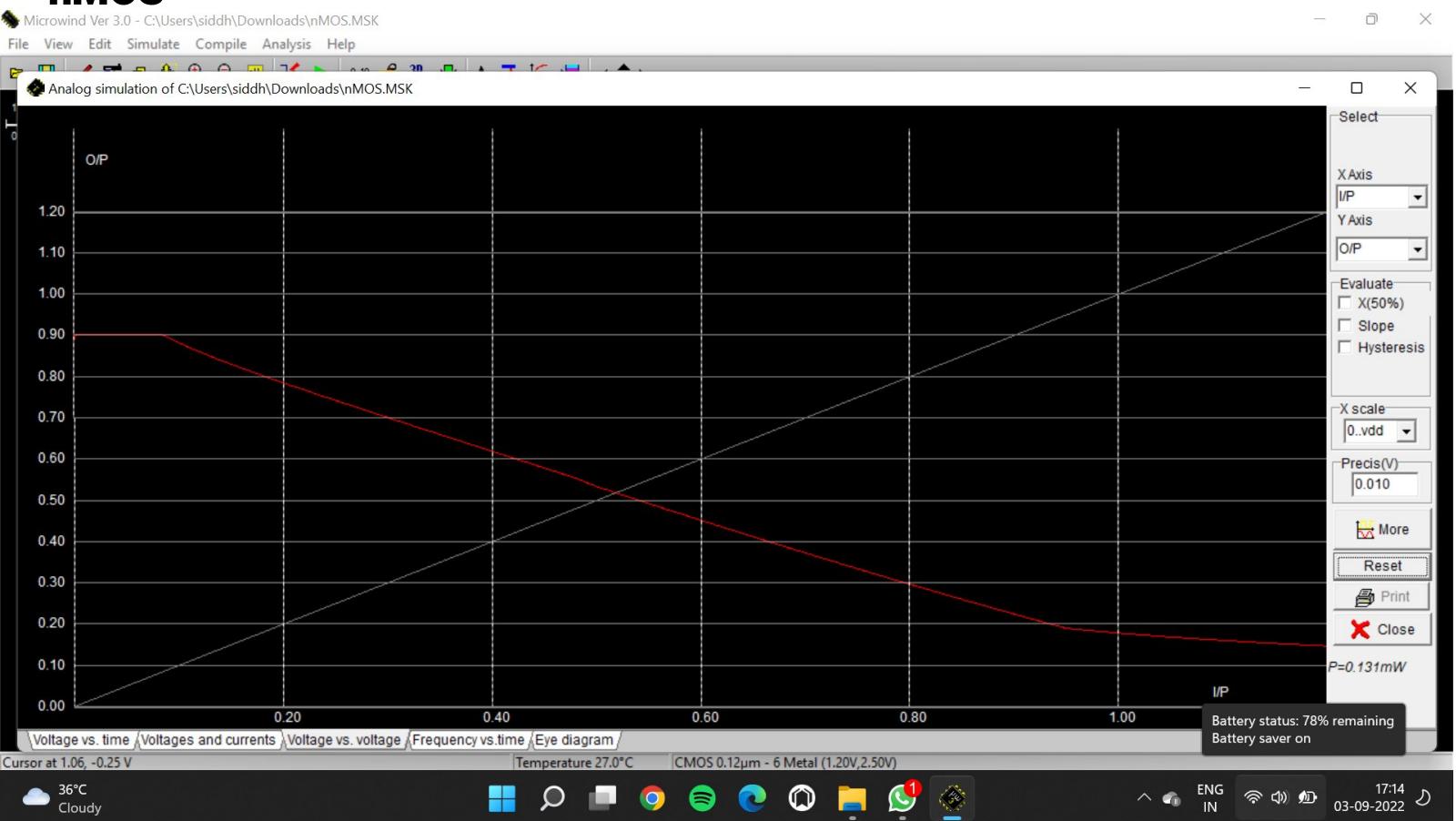
cMOS



RESISTIVE (2k)



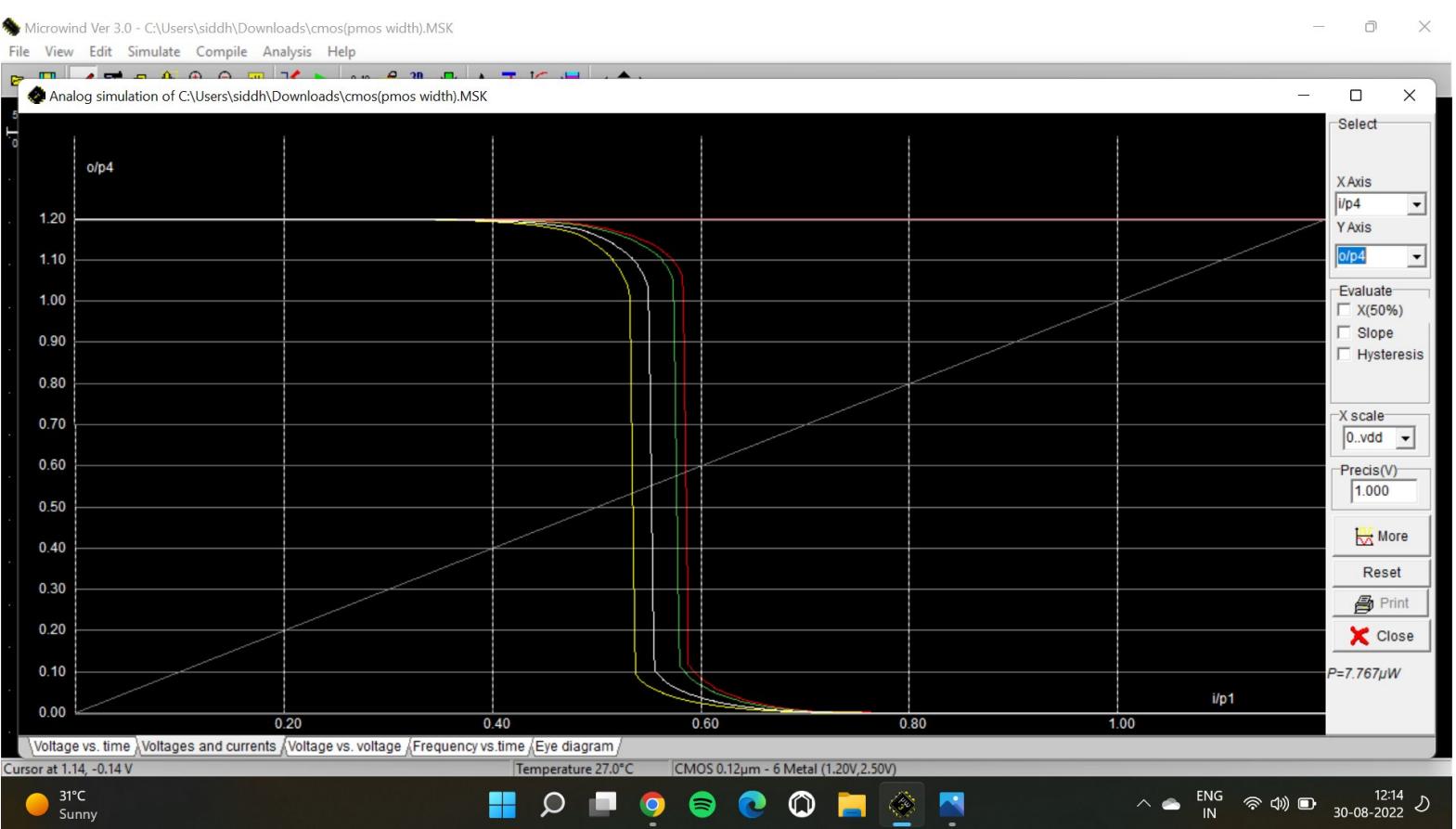
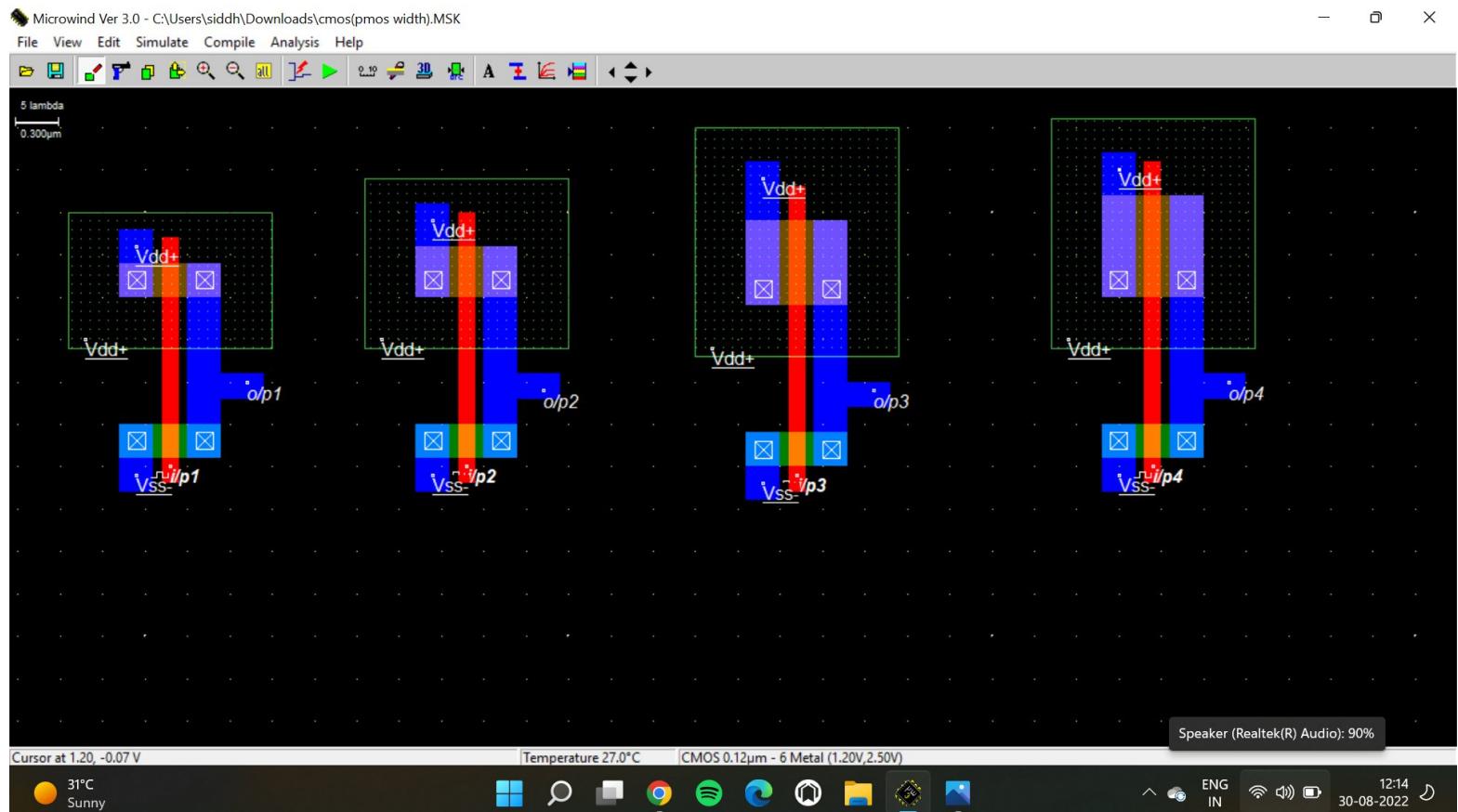
nMOS



Comparison between power and area

	comos	Resistive(2K)	nmos
POWER	0.642 mW	0.131 mW	96.352 mW
AREA	825	4536	280

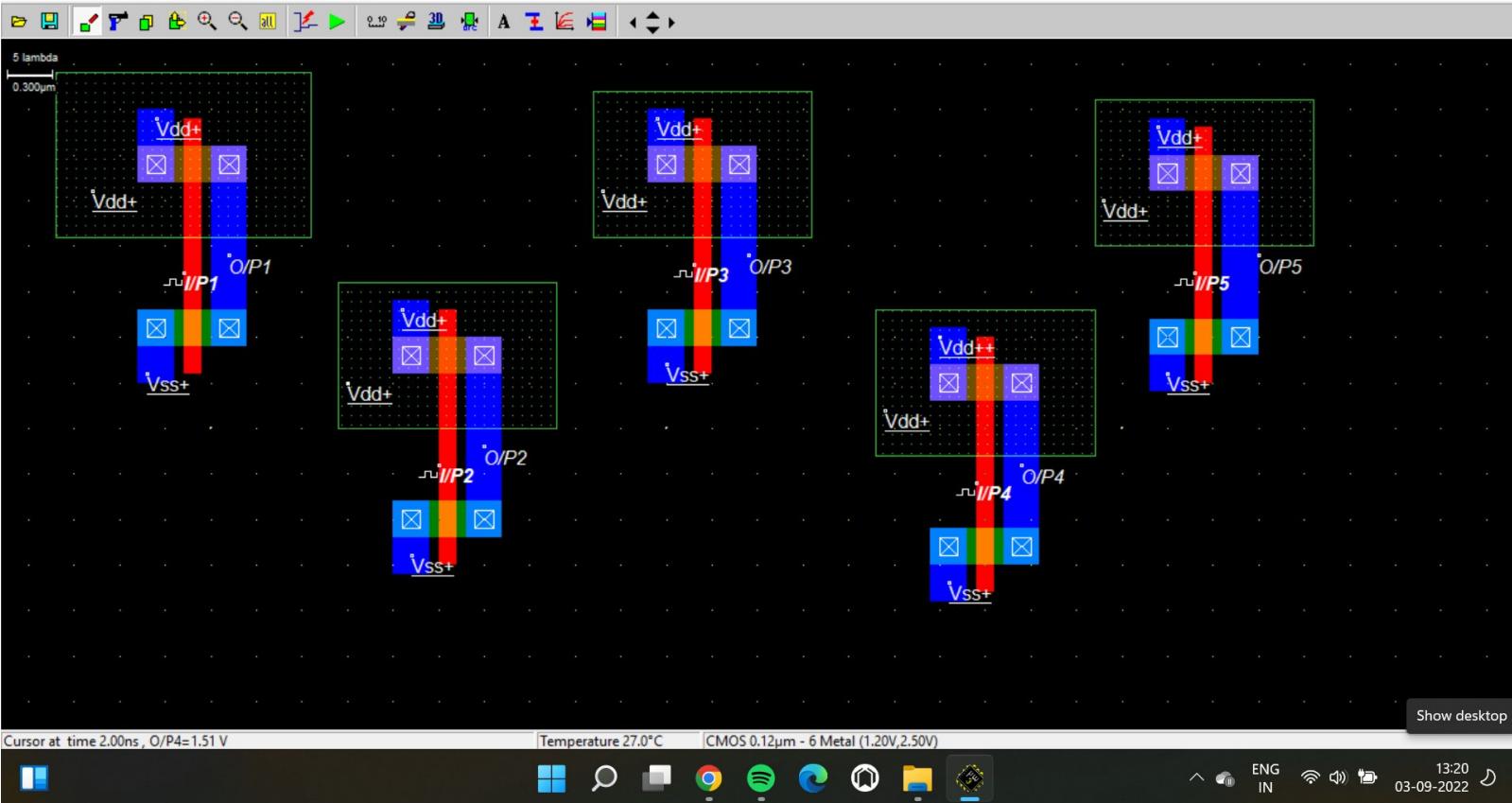
Experiment 10: DIFFERENT WIDTH OF PMOS



11: BODY BIAS

Microwind Ver 3.0 - C:\Users\siddh\Downloads\CMSOS.MSK

File View Edit Simulate Compile Analysis Help



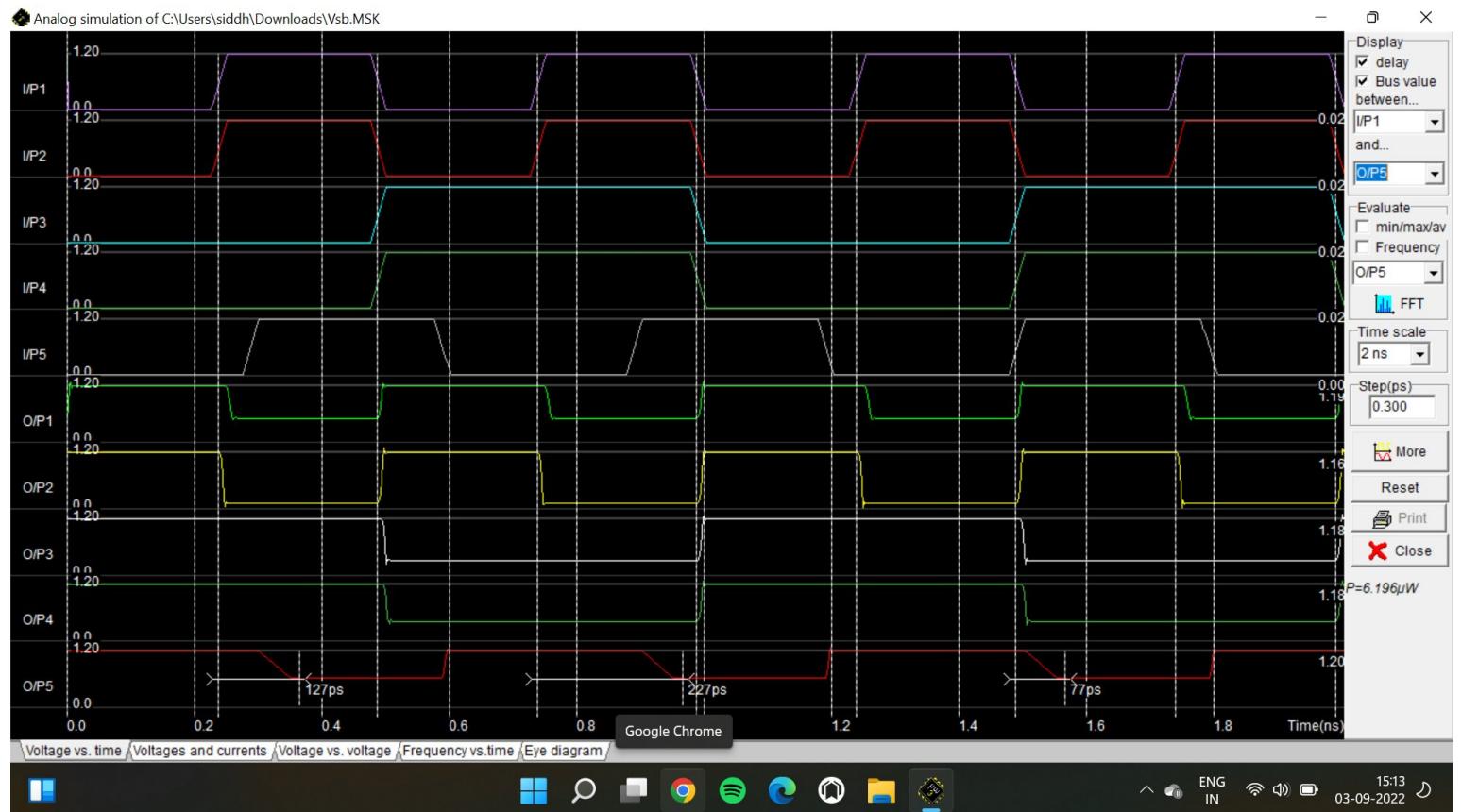
Vdd

- 1) 1.20v
- 2) 1.20v
- 3) 1.20v
- 4) 1.20v
- 5) 1.20v

Vss

- 1) 0.1V
- 2) 0.3V
- 3) 0.4V
- 4) 0.5V
- 5) 0.6V

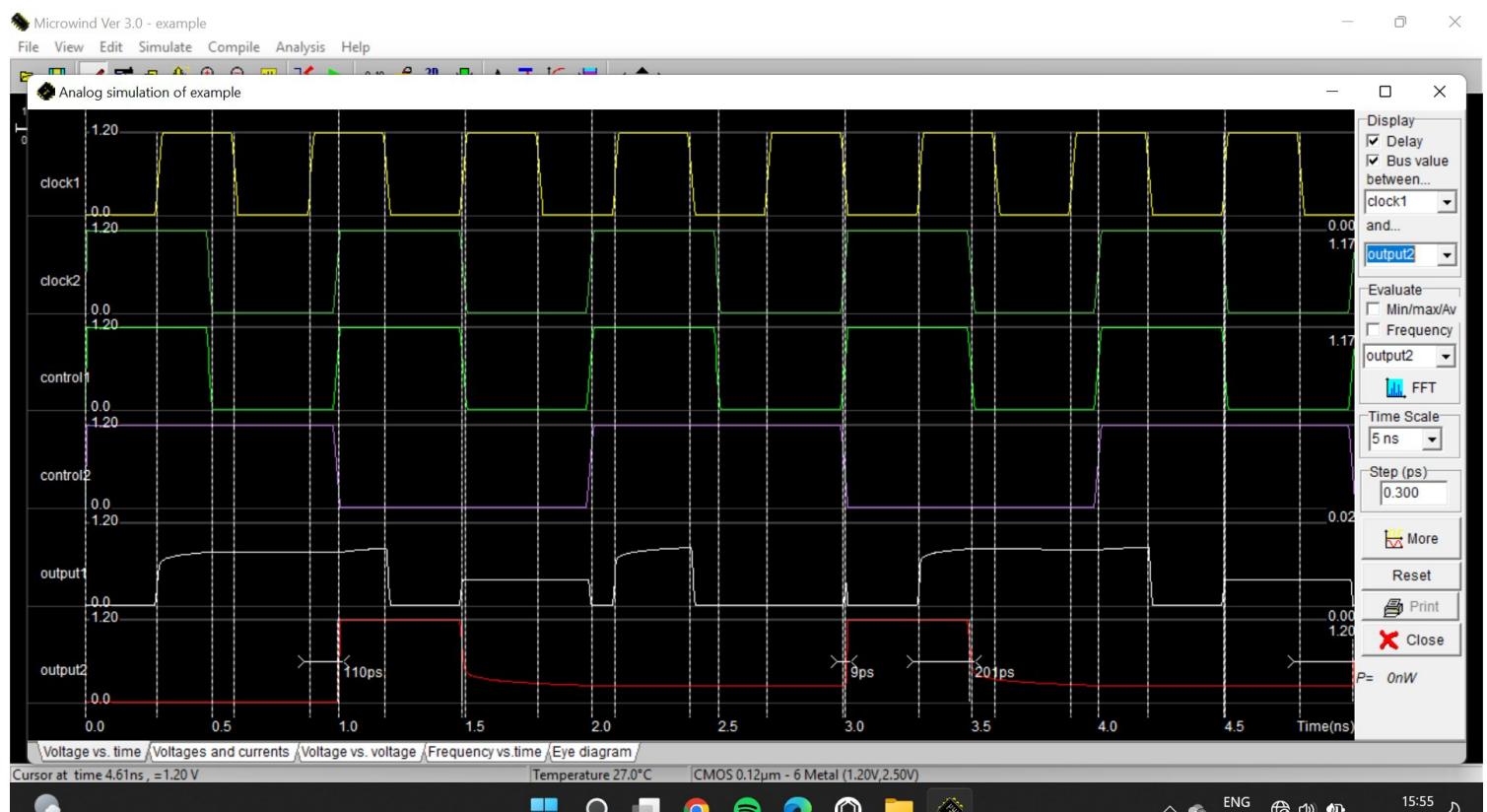
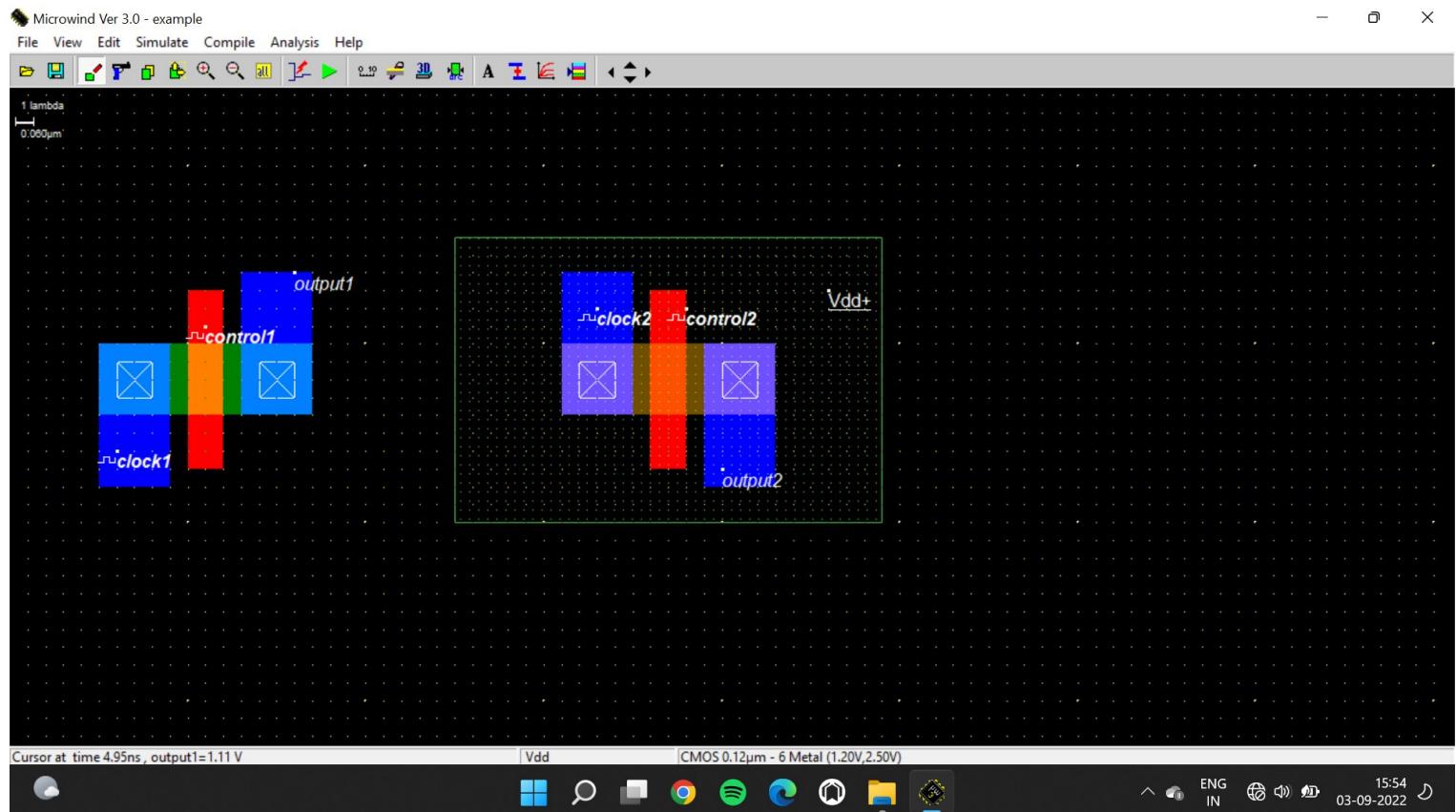
V->T



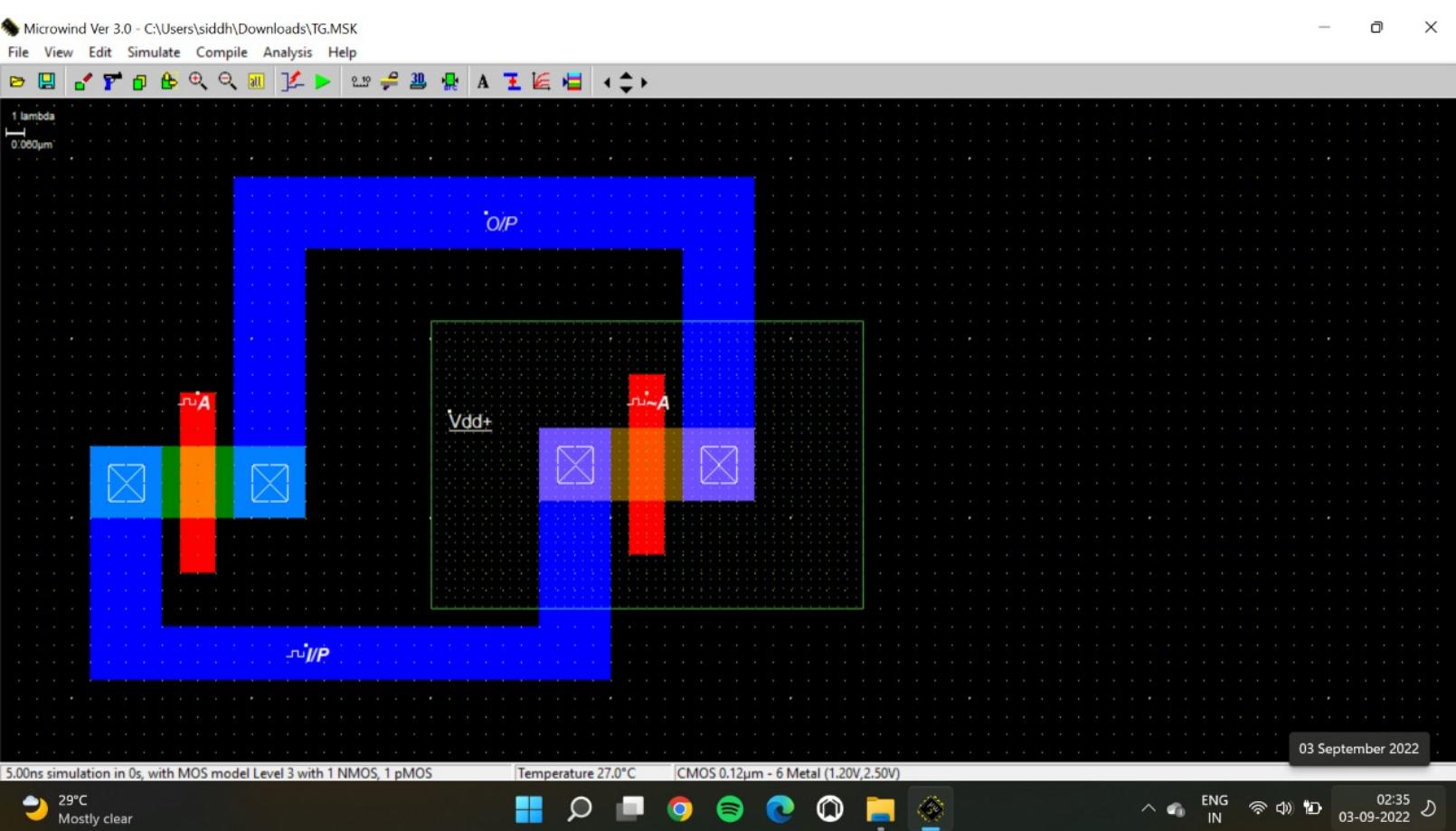
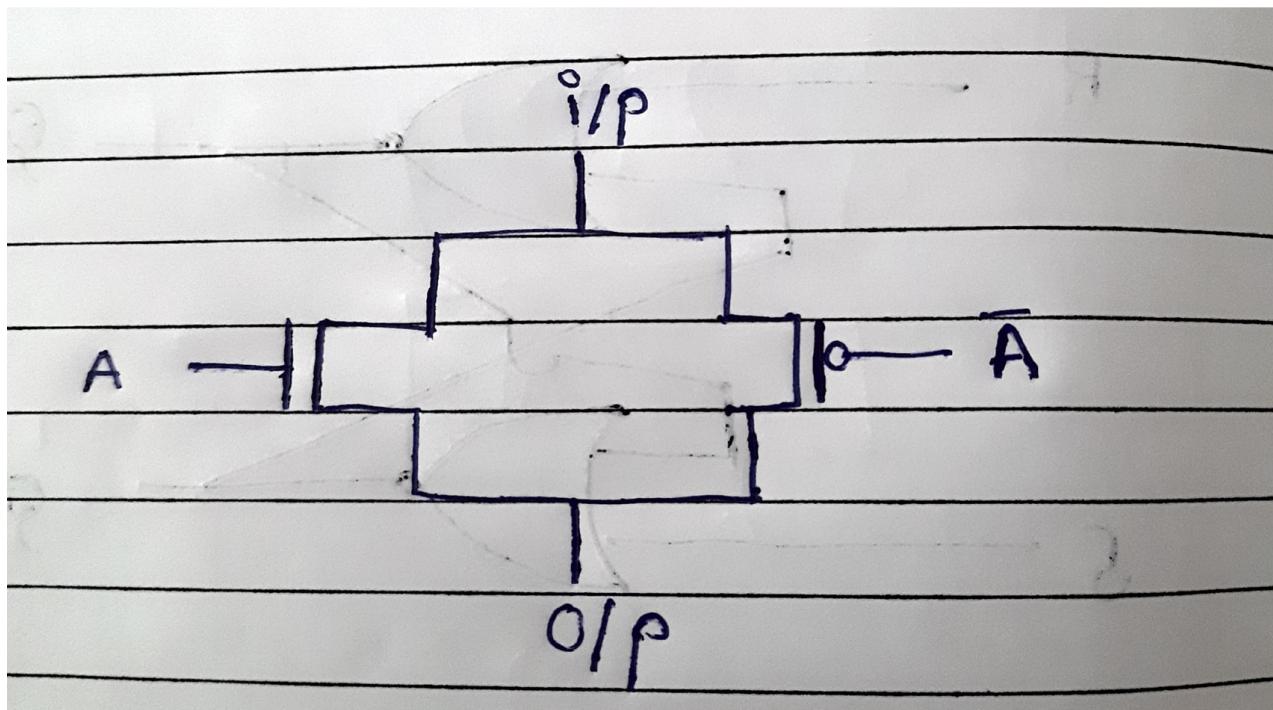
Vout->Vin

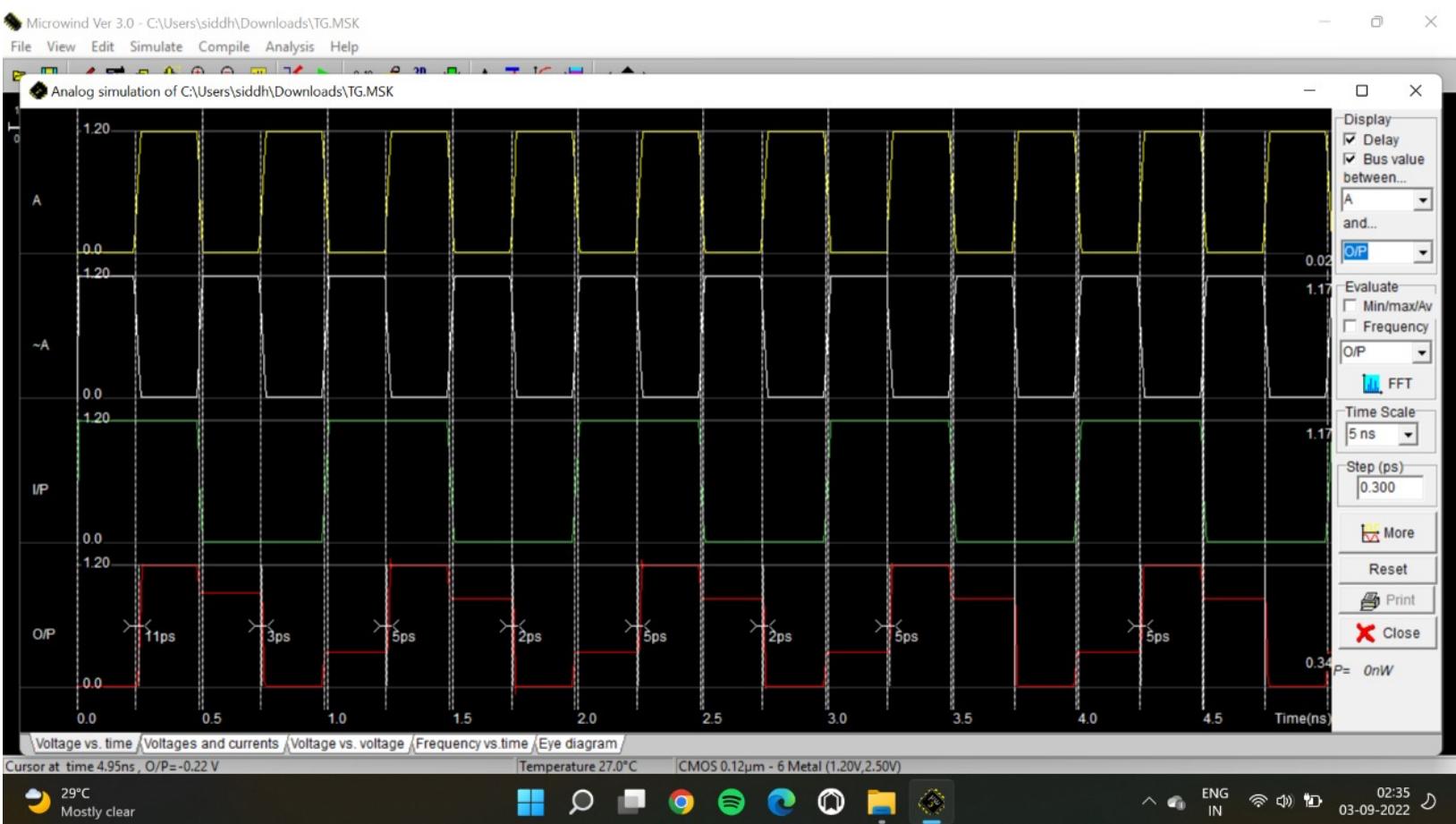


Experiment 12: pmos and nmos as pass transistor

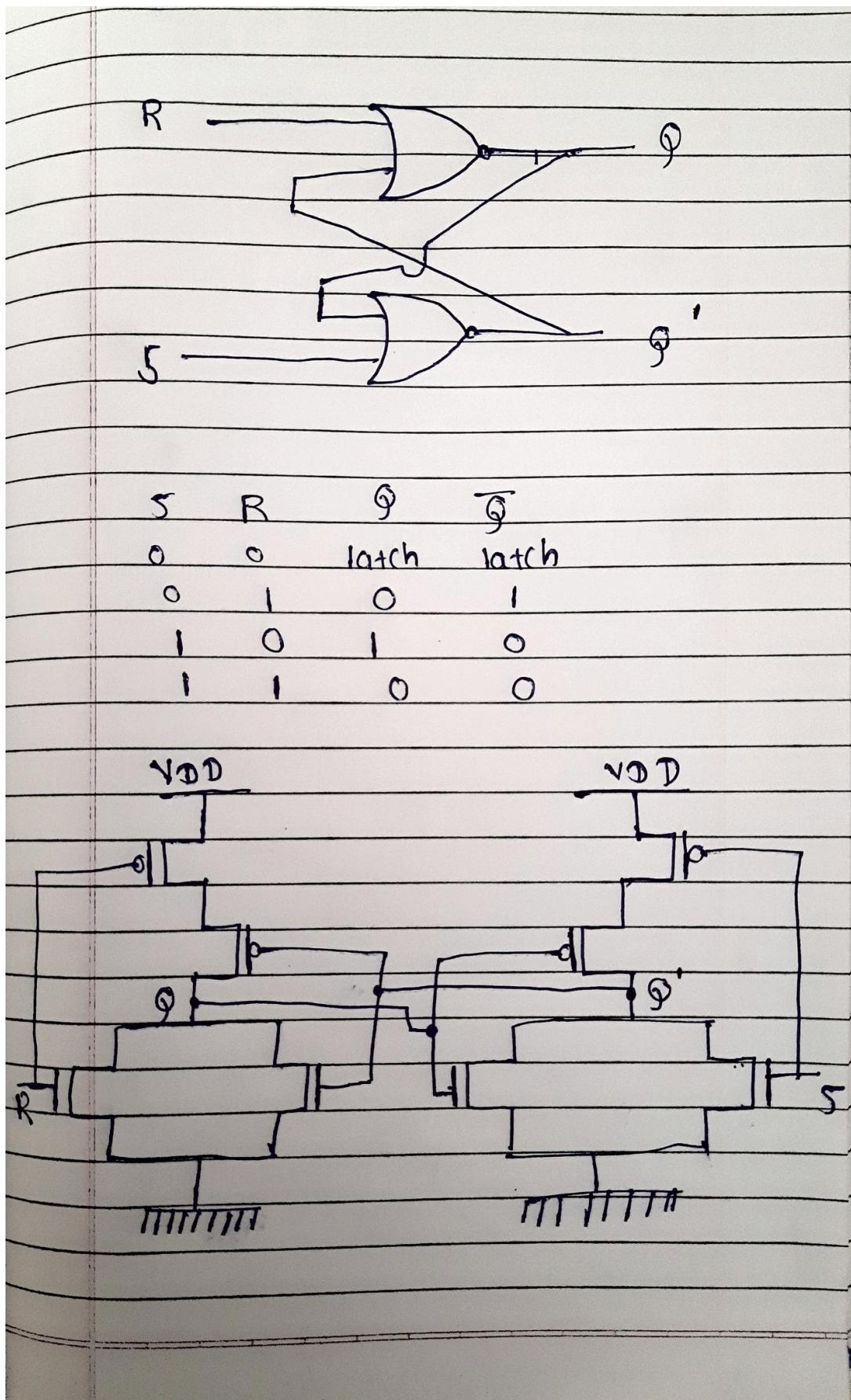


Experiment 13: TRANSMISSION GATE





Experiment 14: SR LATCH

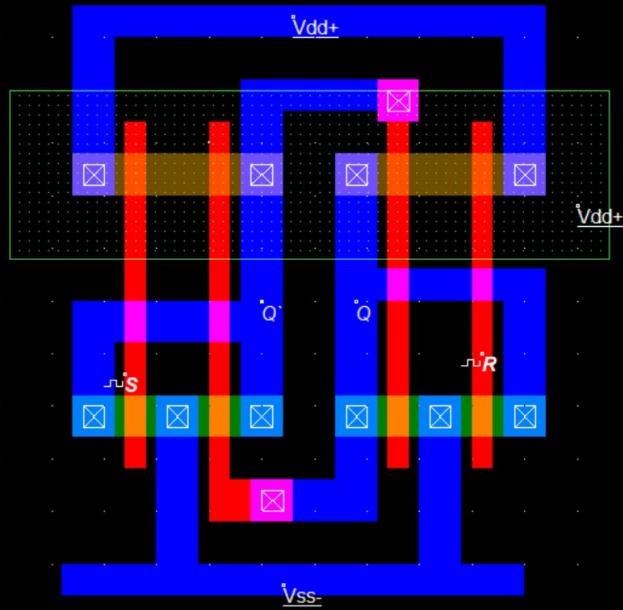


Microwind Ver 3.0 - C:\Users\siddh\Downloads\SR LATCH.MSK

File View Edit Simulate Compile Analysis Help



5 lambda
0.300 μ m

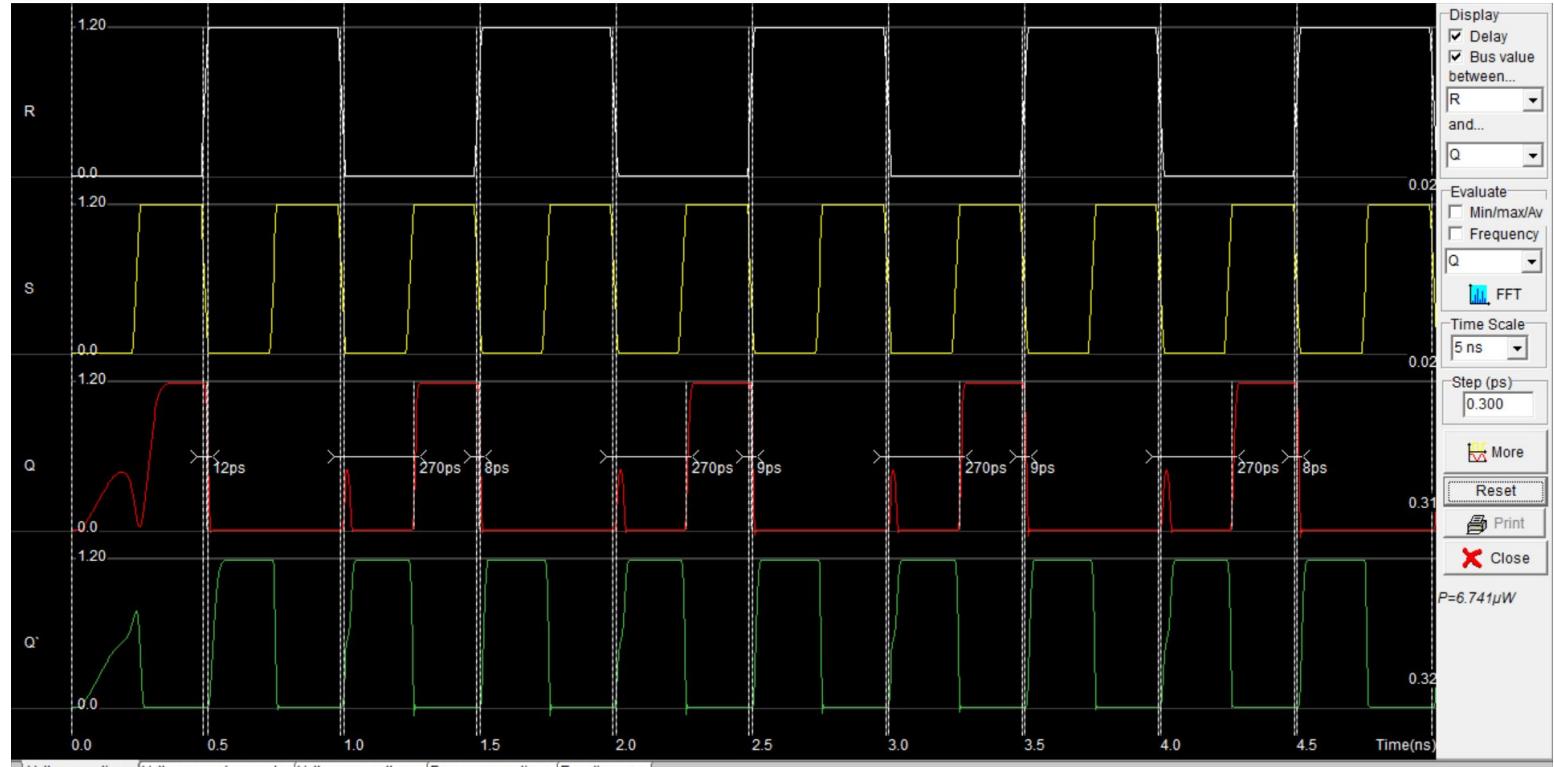


Saved 60 boxes in "C:\Users\siddh\Downloads\SR LATCH.MSK"

Vdd



Analog simulation of C:\Users\siddh\Downloads\SR LATCH.MSK



Voltage vs. time / Voltages and currents / Voltage vs. voltage / Frequency vs. time / Eye diagram /

