Design and Performance Analysis of SRAM Cells in CMOS nm Technologies

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Abstract:
Designing highly stable static random-access memory (SRAM) cells with low static noise margin (SNM) for various levels of cache memory is receiving a lot of attention as technology improves. In this project we propose to study different types of SRAM cells in various technologies and topologies. We have presented various SRAM cell topologies in CMOS technology, including the standard 6T and 8T SRAM cells and we have performed the simulation and characterization of these cells using industry standard EDA tools. Additionally, these cells have been created in 16nm, 50nm, and 180 nm technologies. Performance parameters of all these cells have been compared using the industry-standard tools e.g., Cadence Virtuoso and LTspice Tools. We have explored and thoroughly explained the SRAM Static Noise Margin (SNM) for Read Static Noise Margin (SNM_R) and Write Static Noise Margin (SNM_W) of all considered topologies. The above characteristics were evaluated using the butterfly curve techniques for static noise margin (SNM).
Keywords: SRAM cell; Cadence Virtuoso; LTspice; SNM (Static Noise Margin); CMOS Technology.

Introduction:

Many modern digital designs dedicate a significant amount of silicon/semiconductor space for storing of data values and programme instructions [1]. Boolean values can be stored via capacitive storage or positive feedback. Semiconductor memory are constructed using the same principle. Large arrays of memory cells are therefore created, reducing the overhead brought on by peripheral circuitry and boosting storage density. These array structures of extreme size and complexity bring a number of design issues. The resilience, performance, and power consumption of the memory unit are significantly influenced by the peripheral circuitry. Memories comes in different formats, the ideal type of memory unit for a given application is determined by the system requirements i.e., application, memory size, the time it takes to retrieve the stored data etc. The number of individual cells required to hold the data expressed in terms of bits, which is the size of the memory. The amount of time between the time a read request is made and the time the data is really available at the output is known as the read-access time. The write access time is the amount of time that passed between a write request and the memory's final writing of the input data. A charge on a capacitor or flip-flops are used to store data. These memory cells are referred to as dynamic and static, respectively. Dynamic memory cells require periodic refreshing to make up for the charge loss brought on by leakage, the static memory cell retain their data as long as the supply voltage is maintained [2]. On the basis of the sequence in which data can be accessed,

memory can be categorized. Memory locations in the random-access class can be read or written in any sequence. The fact that an SRAM cell has a latch means that it does not need to perform refresh operations; instead, the cell data is retained for as long as the power supply is available. SRAM is mostly utilized for the cache memory in microprocessors, mainframe computers, engineering workstations, and memory in handheld devices due to its high speed and low power consumption [3]. Four transistors, which together make up two cross coupled inverters, store one bit in an SRAM. In modern days, SRAM cells are gaining attention in the area of memory design therefore it is becoming important to study SRAM cell in various advanced technological nodes for improved performance [4].
In this paper we present the design and simulation of SRAM cell in various advanced technological nodes in various topologies and compare their performance.

I. SRAM Cell Topologies:

SRAM cell consists of two back-to-back or cross coupled inverters along with two access transistors. The objective of the pass transistor is to choose the cell that the word line activates and pass the data inputs to be read or written to the cross coupled inverters. The inverter stores the data that is being read or written [5]. SRAM consists of some peripheral circuitry also which is used for read and write operation.

- Pre-charge Circuit: During read operation bit lines are charged to vdd. Pre-charge circuit maintains the bit line voltage [6].
- Sense Amplifier: It sense value stored in an SRAM cell during read operation. It amplifies small differential voltage on bit lines which reduces read operation time [7].

Word Line controls the access transistors. This access transistors are responsible for "OFF" or "ON" states of the SRAM cell. Writing mode, reading mode, and hold mode are the three operational modes of SRAM cells. During hold operation, word line (WL) is kept low so we can't read or write data to the SRAM cell. During write operation word line is kept high so both access transistors are 'ON' and data can be loaded to bit line and bit line bar. During read operation, word line is kept high, both bit lines are charged, sense amplifier sense the data stored in a cell.

Design Parameters:

Cell Ratio: The aspect ratio of the pull-down NMOS transistors to the aspect ratio of the access transistors is known as the cell ratio or CR [8].

$$\text{C.R.} = \frac{(\text{W/L})\text{pull down}}{(\text{W/L})\text{access transistor}}$$

$$K_{PDN} > K_{access}$$

Pull Up Ratio: The aspect ratio of the pull-up PMOS transistors to the aspect ratio of the access transistors is known as the pull-up ratio or PR [8].

$$\text{P.R.} = \frac{(W/L)pull\ up}{(W/L)access\ transistor}$$

$$K_{access} > K_{PUN}$$

$$K_{PDN} > K_{access} > K_{PUN}$$

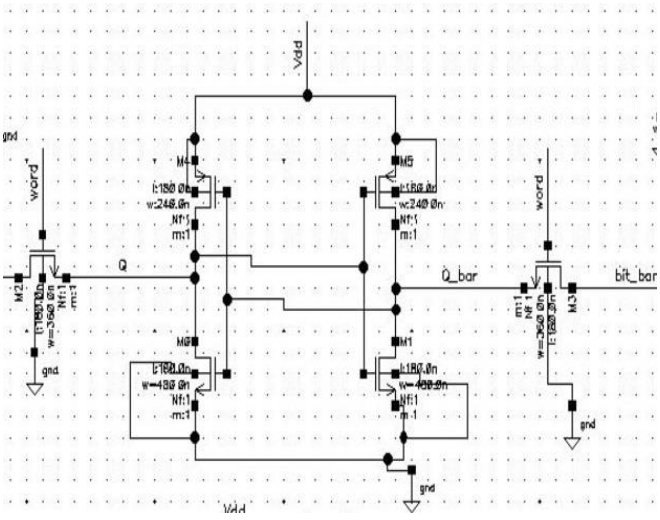

Figure 1: 6T SRAM

8T SRAM contains 8 transistors, additional two transistors are added to improve parameters. 8T SRAM uses separate word lines and bit lines for read and write cycles [9].

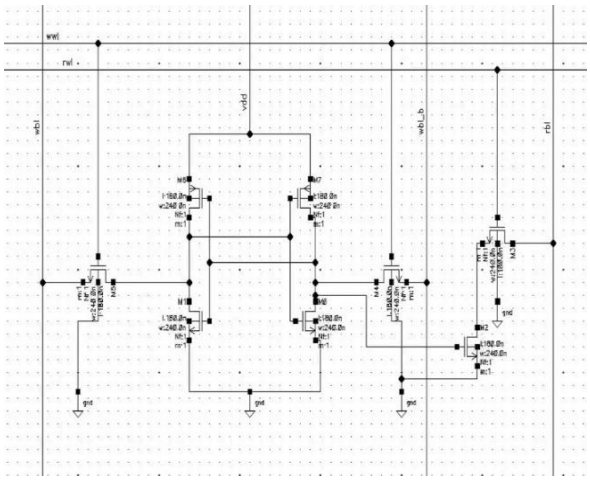

Figure 2: 8T SRAM

II. SIMULATION AND WAVEFORM:

The entire project is simulated using the 180nm Cadence Virtuoso Tool.

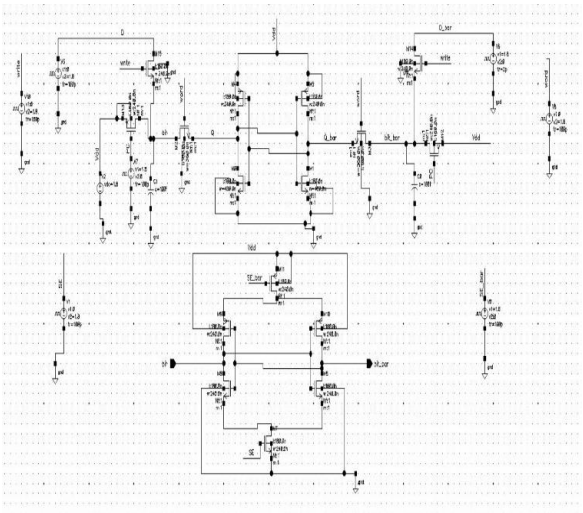

Figure 3: 6T Schematic

Write Operation:

Figure 4 contain the waveform of Data to be stored, Word Line (WL), Write Signal and data stored in Q and Q bar (QB). When the word line or write signal is low no data is stored in Q and QB. When WL and write signal is high data is written in Q. When WL or Write Signal varies from high to low, or then hold operation is performed by SRAM and data is stored in Q and QB.

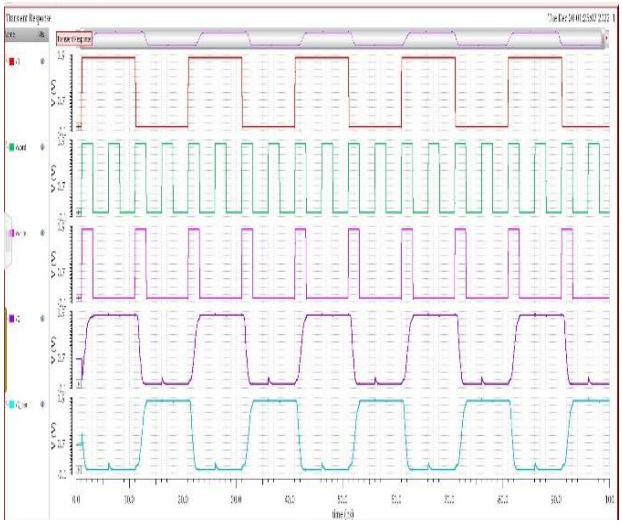

Figure 4: Simulation of write operation

Read Operation:

Figure 5 contain the waveform of, Word Line (WL), Sense Amplifier Enable Signal, Pre-charge signal, Bit Line and Data stored in Q. When the Sense amplifier enable is low stored data can't be read. When Sense amplifier enable is high data is read by bit lines.

In read operation access transistors are ON and both bit lines are charged at vdd, that is logic '1' [10].

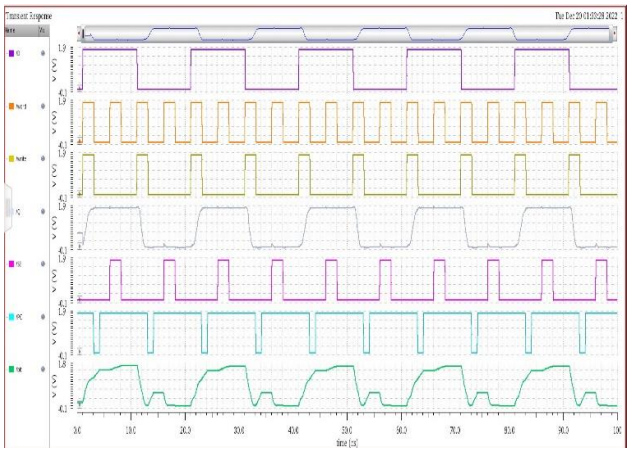

Figure 5: Simulation of read operation

III. SRAM Static Noise Margin Analysis

The SNM of SRAM is defined as the maximum value of the static noise that can be tolerated by SRAM cell without flipping the data [14]. The noise is generated by offsets and mismatches that come from variation in operation conditions. The SNM is the measure of stability of the SRAM cell that retains its data against noise. The SRAM cell read stability and write stability is major concerns in nm CMOS technologies. For error-less transmission high noise margin is required.

There are different approaches to obtain the SNM of the SRAM cell [12]. One of the methods is graphical measure in which SNM of SRAM cell is obtained from plotting the Voltage Transfer Characteristics (VTCs) of the two cross-coupled inverters, by flipping one of the VTC of the inverter with respect to the line y = x in order to form a Butterfly Curve [11][13].

Results and Discussions:

I. 180nm TECHNOLOGY NODE

A. SNM_R

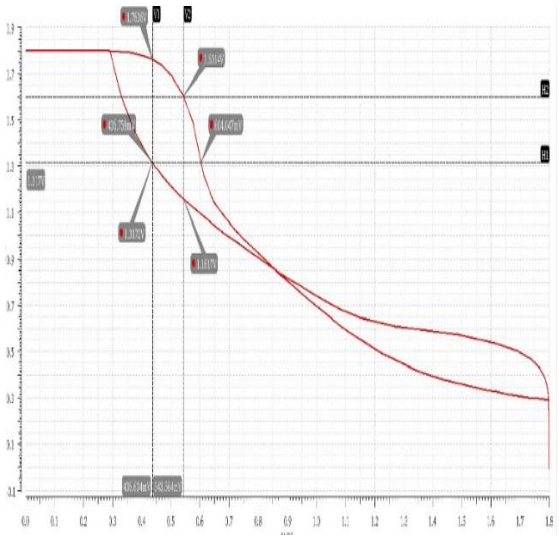

Figure 6: SNM_R for 180nm technology of 6T SRAM cell

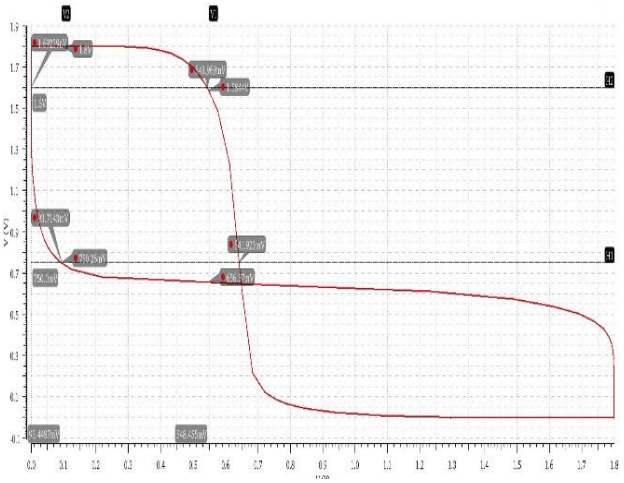

Figure 7: SNM_R for 180nm technology of 8T SRAM cell

B. SNM_W

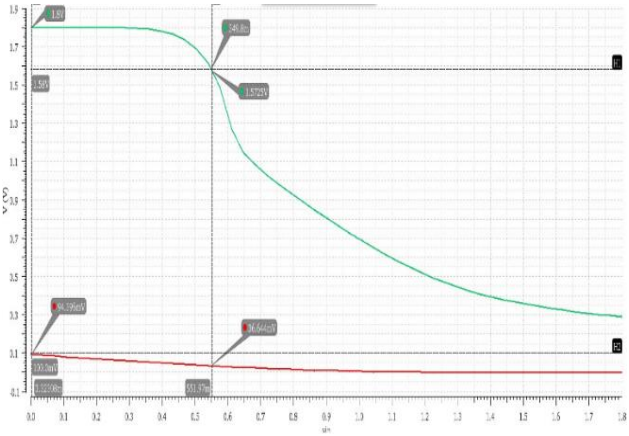

Figure 8: SNM_W for 180nm technology of 6T and 8T SRAM cell

II. 50nm TECHNOLOGY NODE

A. SNM_R

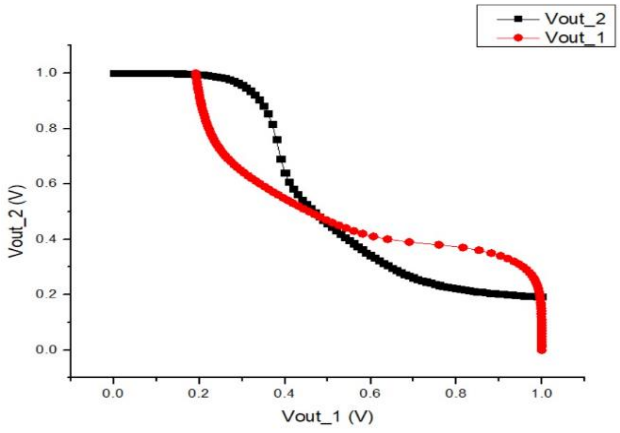

Figure 9: SNM_R for 50nm technology of 6T SRAM cell

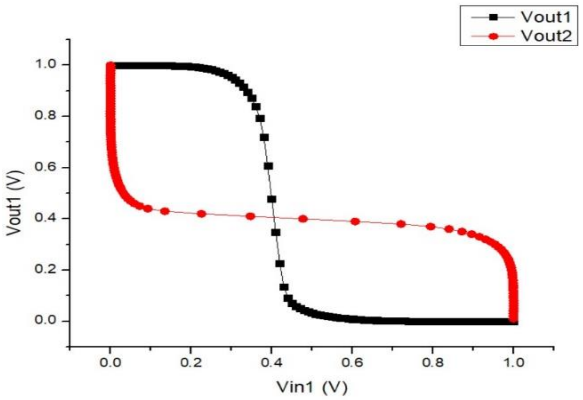

Figure 10: SNM_R for 50nm technology of 8T SRAM cell

B. SNM_W

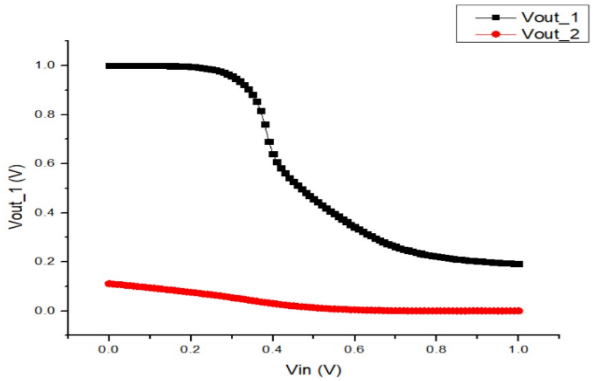

Figure 11: SNM_W for 50nm technology of 6T and 8T SRAM cell

III. 16nm TECHNOLOGY NODE

A. SNM_R

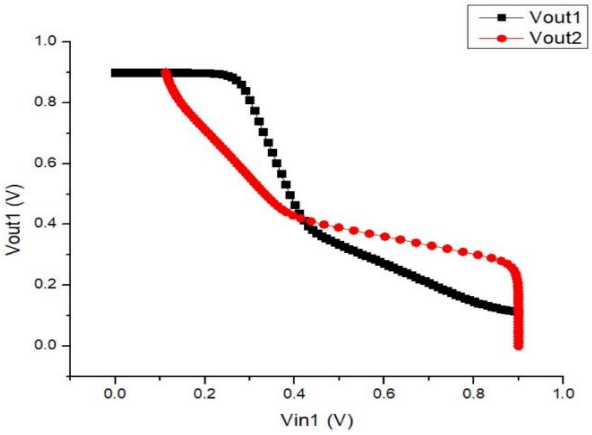

Figure 12: SNM_R for 16nm technology of 6T SRAM cell

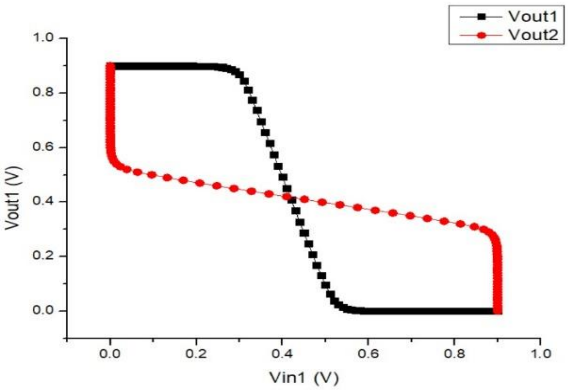

Figure 13: SNM_R for 16nm technology of 8T SRAM cell

B. SNM_W

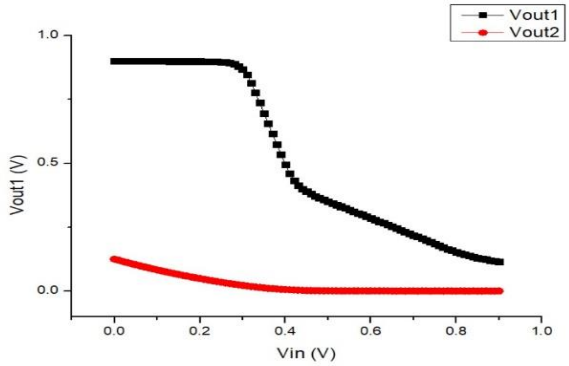

Figure 14: SNM_W for 16nm technology of 6T and 8T SRAM cell

Comparisons of performance parameter of different SRAM cells in various advanced technological nodes:

TECHNOLOGY NODE	TOPOLOGIES	SNM_R	SNM_W
180nm	6T	284mV	1.478V
	8T	942mV	1.478V
50nm	6T	138mV	465mV
	8T	381mV	465mV
16nm	6T	125mV	391mV
	8T	338mV	391mV

Table 1: Comparison of several parameters at various CMOS Technology

Conclusion:

In this paper we presented design, simulation and performance analysis of SRAM cells in CMOS nm technologies. We have designed simulated and compared the performance of 6T and 8T SRAM cells in different advanced technological nodes. We have simulated performance of the SRAM cells and obtained the waveforms for hold operation, read operation and write operation. Also, we have calculated static noise margin (SNM) for above mentioned cells for hold read and write compared the performance of SRAM cells in various technological nodes and various topologies. We observed that static noise margin for read of 8T cell is significantly improved in comparison to 6T cell. The static noise margin (SNM) for read of 180nm is greater than 50nm and 16nm. The static noise margin (SNM) for write operation in both cells of different nm technology node were almost same.

References:

[1]. Ishibashi, Koichiro and Kenichi Osada. “Low power and reliable SRAM memory cell and array design.” (2011).

[2]. K. Anami, M. Yoshimoto, H. Shinohara, Y. Hirata and T.Nakano, "Design considerations of a static memory cell", IEEE J.Solid-State Circuits, vol. SC-18, no. 4, pp. 414-418, Aug. 1983

[3]. A. Agal, Pardeep, B. Krishan, 6T SRAM Cell: Design And Analysis, Int. J. Eng. Res. Appl. 4 (2014) 574–577

[4]. S. Saun and H. Kumar, "Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization,"IOP Conference Series: Materials Science and Engineering, vol. 561, p.012093, 2019/11/12 2019.

[5]. S. Mutum and K. Mondal, "Comparative Performance Analysis of 6T SRAM cell in 180nm and 90nm Technologies," 2021 Asian Conference on Innovation in Technology (ASIANCON), PUNE, India, 2021, pp. 1-4, doi: 10.1109/ASIANCON51346.2021.9544733.

[6]. C. A. Kumar, B. K. Madhavi and K. Lalkishore, "Performance analysis of low power 6T SRAM cell in 180nm and 90nm," 2016 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), Chennai, India, 2016, pp. 351-357, doi: 10.1109/AEEICB.2016.7538307.10.1109/ICECA52323.2021.9676022.

[7]. Gul, W.; Shams, M.; Al-Khalili, D. SRAM Cell Design Challenges in Modern Deep Sub-Micron Technologies: An Overview. Micromachines 2022, 13, 1332. https://doi.org/10.3390/ mi13081332

[8]. R. Kolhal and V. Agarwal, "A Power and Static Noise Margin Analysis of different SRAM cells at 180nm Technology," 2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India, 2019, pp. 6-12, doi: 10.1109/ICECA.2019.8821868.

[9]. P. N. V. Kiran and N. Saxena, "Design and analysis of different types SRAM cell topologies," 2015 2nd International Conference on Electronics and Communication Systems (ICECS), Coimbatore, India, 2015, pp. 1060-1065, doi: 10.1109/ECS.2015.7124742.

[10]. Vijayan, Sarang & Kodavanti, Praneeth. (2014). Novel Design and Implementation Of 8 X 8 SRAM Cell Array for Low Power Applications. International Journal of Engineering

Research AND TECHNOLOGY. 3. 1355. 10.13140/2.1.1132.3520.

[11]. D. Suneja, N. Chaturvedi and S. Gurunarayanan, "A comparative analysis of read/write assist techniques on performance & margin in 6T SRAM cell design," 2017 International Conference on Computer, Communications and Electronics (Comptelix), Jaipur, India, 2017, pp. 659-664, doi: 10.1109/COMPTELIX.2017.8004051.

[12]. Kumar, Harekrishna & Tomar, Vinay. (2021). A Review on Performance Evaluation of Different Low Power SRAM Cells in Nano-Scale Era. Wireless Personal Communications. 11. 1-26. 10.1007/s11277-020-07953-4.

[13]. GANESH, MANEPALLY SATYA SAI, and SHYAM AKASHE. "Calculation of Static Noise Margin for 6T SRAM Cell." Journal of Active & Passive Electronic Devices 15 (2020).

[14]. V. Choudhary and D. S. Yadav, "Analysis of Power, Delay and SNM of 6T & 8T SRAM Cells," 2021 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India, 2021, pp. 78-82, doi: 10.1109/ICECA52323.2021.9676022.