Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous Institute Affiliated to University of Mumbai)

Course (Category) Code	Course Name	Teaching Scheme (Hrs/week)					Credits Assigned			
		L	T	P	O	E	L	T	P	Total
(PC)	Computer Architecture Organization	3	0	2	4	9	3	0	1	4
CS203		Examination Scheme								
		Component	ISE		MSE		ESE			Total
		Theory	20		20		60			100
		Laboratory	80		--		20			100

Pre-requisite Course Codes, if any.	Digital Systems
Course Objective: Imparting concepts of each component of computer architecture thoroughly with practical aspects including memory systems and I/O communications with interfacing	
Course Outcomes (CO): *At the End of the course students will be able to*	
CO.1	Conceptualize basic computer structure with its models and compute performance metrics.
CO.2	Design algorithms to solve ALU operations
CO.3	Comprehend processor organization with various design methods of CPU with comparative analysis
CO.4	Design memory systems with analysis of mapping techniques for cache and virtual memory
CO.5	Comprehend different types of I/O buses, compare and contrast different types of data transfer methods and arbitration techniques
CO.6	Analyze different parallel organizations that includes pipelined and parallel processors

CO-PO Correlation Matrix (3-Strong, 2-Moderate, 1-Weak Correlation)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO.1	3				2							
CO.2	3	3			2							
CO.3	3	2	2		2							
CO.4	3											
CO.5		2	2		2							
CO.6	3											

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CO-PEO/PSO Correlation Matrix (3-Strong, 2-Moderate, 1-Weak Correlation)

	PEO1	PEO2	PEO3	PEO4	PSO1	PSO2
CO.1	**2**	**2**	-	-	-	-
CO.2	**2**	**2**	-	-	-	-
CO.3	**2**	**2**	-	-	-	-
CO.4	**2**	**2**	-	-	-	-
CO.5	**2**	**2**	-	-	-	-
CO.6	**2**	**2**	-	-	-	-

BLOOM'S Levels Targeted (Pl. Tick appropriate)

Remember	Understand	Apply	Analyze ✓	Evaluate	Create

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Theory Component

Module No.	Unit No.	Topics	Ref.	Hrs.
1	Title	**Overview of Computer Architecture and Organization**		5
	1.1	Introduction of Computer Organization and Architecture, Basic organization of computer and block level description of the functional units, Evolution of x86 Computers, Von Neumann model, Harvard Model, Embedded system	1,2	
	1.2	Performance Issues: Designing for performance, Amdahl's Law, Multi-core, GPGPU	1,2	
2	Title	**ALU, Processor Organization and Control Unit Design**		10
	2.1	ALU: Integer and Floating Point Operation CPU Architecture, Register Organization , Instruction formats, basic instruction cycle. Instruction interpretation and sequencing, Case Study of 80386 architecture and Register Organization	2,3	
	2.2	Control Unit: Soft wired (Micro-programmed) and hardwired control unit design methods. Microinstruction sequencing and execution. Micro operations	2,3	
	2.3	RISC and CISC: Introduction to RISC and CISC architectures and design issues.	2,3	
3	Title	**Memory Systems Organization**		12
	3.1	Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics.	2	
	3.2	Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associative memory. Case study of Pentium Processor Cache Memory Model (MESI Protocol)	2,4	
	3.3	Virtual Memory: Concept, Segmentation and Paging, Page replacement policies. Case study of 80386 Virtual Memory Concepts	2,3	
4	Title	**I/O Organization**		5
	4.1	Buses: Types of Buses, Bus Arbitration, BUS standards	1,2	
	4.2	I/O Interface, I/O channels, I/O modules and IO processor, Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA.	1,2	
5	Title	**Parallel Processing**		11
	5.1	Advanced Processor Models: Real Model, Protected Model, Virtual Model (x86 Processors)	3	
	5.2	Superscalar Architecture: Case study of Pentium processor	4	
	5.3	Pipelined Architecture: Pipleine Stages, Pipeline Hazards, Mitigation of Hazards with branch prediction and data forwarding techniques	1,2,4	

	5.4	Introduction to parallel processing concepts, Flynn's classifications,	2	
6	**Self-Study**	Comparative Study of microprocessors and micro architectures with respect to their important features. Detailed analysis of Multicore and GPGPU Architectures. Vector and Array Processors with VLIW architecture. 8086 instructions set with assembler directives		
			Total	**42**

Laboratory Component, if any. (Minimum 10 Laboratory experiments are expected) [Only for CE/CSE]

Sr. No	Title of the Experiment
1	Installation and configure: DOS, MASM, Debug and X86 Mode
2	Implementation of various arithmetic operations through assembly language programming for 8086 using MASM and Debug.
3	Implement various String Operations in 8086 through the utilities provided by DOS and BIOS interrupts (MASM)
4	Block Transfer and Block Exchange using Index Registers
5	Drawing basic shapes like triangle, etc. using BIOS services [Use C/MASM]
6	Design Password Detection Application using BIOS and DOS interrupts along with 8086 instructions.
7	Implement file operations [DOS Interrupts in C/MASM]
8	Implement I/O interfacing using inbuilt speakers of IBM PC
9	Implement Booth's Multiplication Algorithm
10	Implement Division Algorithm (Non-Restoring and Restoring)
11	Implementation of Mapping techniques of Cache memory
12	Implementation of Page Replacement Policies

Text Books

Sr. No	Title	Edition	Authors	Publisher	Year
1	Computer Organization	**Fifth**	Carl Hamacher, Zvonko Vranesic and Safwat Zaky	**Tata McGraw-Hill**	**2002**
2	Computer Organization and Architecture: Designing for Performance	**Eighth**	William Stallings	**Pearson**	**2010**
3	The 80386, 80486, and Pentium Microprocessor: Hardware, Software, and	**Third**	Walter Triebel	**Pearson**	**1997**

	Interfacing				
4	Pentium Pro Processor System Architecture	**Third**	Tom Shanely	**Addison Wesley**	**1996**

Reference Books

Sr. No	Title	Edition	Authors	Publisher	Year
1	Structured Computer Organization	**Sixth**	Andrew S. Tanenbaum	**Pearson**	**2013**
2	Microprocessor and Interfacing: Programming & Hardware	**Third**	Douglas V Hall	**Tata-McGraw Hill**	**2012**
3	Computer Architecture and Organization: Design Principles and Applications	**Second**	B. Govindarajulu	**McGraw Hill**	**Paperback-2017**
4	Advance Computer Architecture: Parallelism, Scalability, Programmability	**Third**	Kai Hwang	**Tata-McGraw Hill**	**2017**
5	Programmer's reference Manual for IBM Personal Computers	**First**	Steven Armburst	**Tata-McGraw Hill**	**1986**